AMD Geode™ Solutions Integrated Processors, Companion Devices, and System Platforms

October 2003

NOTICE

Advanced Micro Devices, Inc. (“AMD”) has purchased the Information Appliance business unit of National Semiconductor Corporation (“National”), which consisted primarily of the Geode™ family of microprocessor products and related support products (GX1, GX2, CS5530A, CS5535, CS1301, CS1311, SC1100, SC1200, SC1201, SC2100, SC2200, SC3200, XpressROM™ and XpressLoader™ software, collectively, the “IA Products”). This business unit is now being operated by AMD’s PCS Division.

During a transitional period, AMD will continue to use and distribute IA Product technical and marketing documents originally produced by National in hard copy, pdf, html or other electronic format.

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SC3200 TEPBGA Reference Schematic Rev 1.0

-TFT and IDE supported.
-Parallel port not available from SC3200

Design Notes:

1) This design features the SC3200 in the TEPBGA package. Please read the SC3200 Data sheet, and Errata document for the particular revision of silicon to be used. Certain parts of this schematic may need to be changed to accommodate work-arounds for issues with a particular silicon revision.
2) PCB Layout notes are included with this schematic in various places. However, use the SC3200 Layout Guidelines for proper PCB layout.
3) No board has been built from this schematic.
4) Not all sections of this design may be appropriate for a particular application.
5) It is not recommended that both CompactFlash and IDE be used in the same design. CompactFlash, Dual IDE ports, and a Single IDE port are shown on separate sheets. The designer should choose one of the three sheets to use in a design.
6) It is not recommended that both a standard PCI slot and a Mini-PCI slot be used in the same design. These are shown on separate sheets. The designer should choose one or the other sheets to use in a design.
7) Please read the "Important Notice" below.
8) Be sure to check the IA Developers Web Site often to get updated schematics or a schematic errata document.
9) The pin properties on part symbols may need to be changed to support a particular application.

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Revision History:

Rev	Date	Change Log
1.0	04-25-03	Initial release

LAST USED REFERENCES

Z53
U29
R160
TP26
C307
Q7
Y4
FB22
JP3
BT1
BH1
SW1
D20
JLCD1
J20
JCF1
T2
PCI1
X1
L8
FS1
JS2
RP11
JDCIN1
F1

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Title: SC3200 REFERENCE SCHEMATICS
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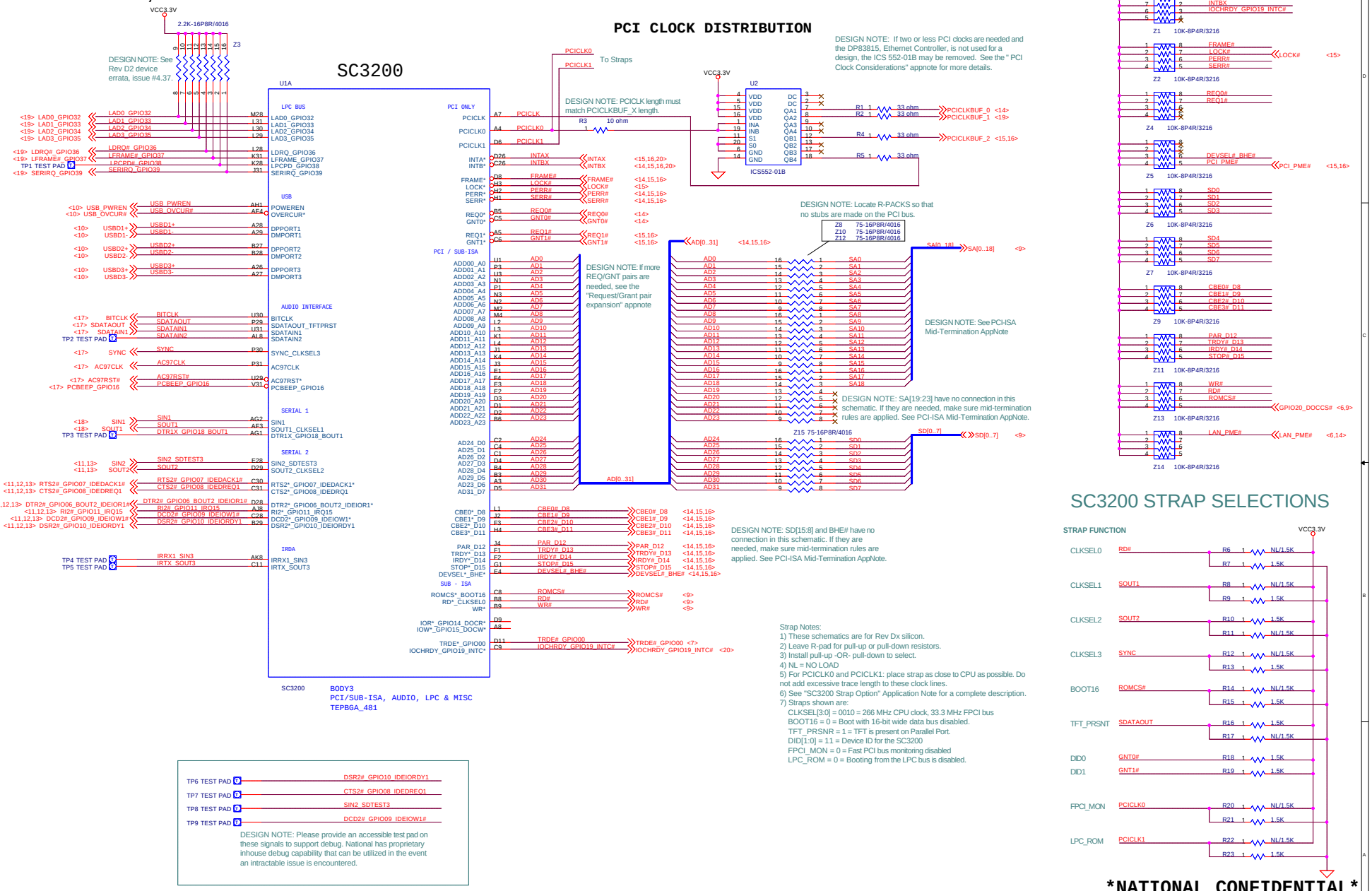
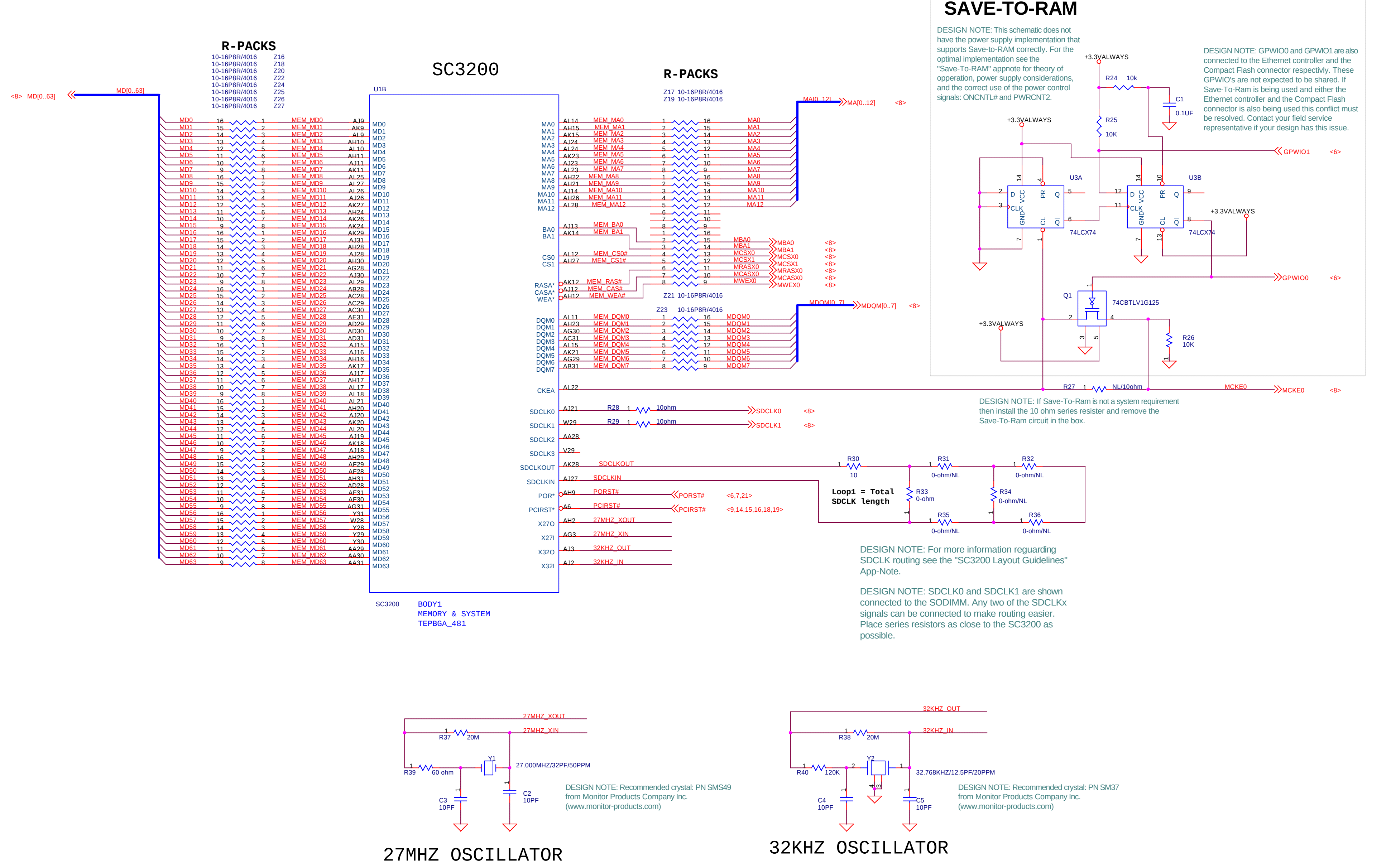
SC3200 INTERFACES: PCI/SUB-ISA, LPC, AUDIO, DOC, PCI CLOCKS; STRAP OPTIONS, PCI BUS PULL-UPS



SC3200 INTERFACES: MEMORY, 32KHZ AND 27MHZ OSCILLATORS



R-PACKS
SC3200
R-PACKS
SAVE-TO-RAM
DESIGN NOTE: This schematic does not have the power supply implementation that supports Save-to-RAM correctly. For the optimal implementation see the "Save-To-RAM" appnote for theory of opperation, power supply considerations, and the correct use of the power control signals: ONCNTL# and PWRCNT2.
DESIGN NOTE: GPWIO0 and GPWIO1 are also connected to the Ethernet controller and the Compact Flash connector respectivly. These GPWIO's are not expected to be shared. If Save-to-Ram is being used and either the Ethernet controller and the Compact Flash connector is also being used this conflict must be resolved. Contact your field service representative if your design has this issue.
DESIGN NOTE: If Save-To-Ram is not a system requirement then install the 10 ohm series resister and remove the Save-To-Ram circuit in the box.
Loop1 = Total SDCLK length
DESIGN NOTE: For more information reguarding SDCLK routing see the "SC3200 Layout Guidelines" App-Note.
DESIGN NOTE: SDCLK0 and SDCLK1 are shown connected to the SODIMM. Any two of the SDCLKx signals can be connected to make routing easier. Place series resistors as close to the SC3200 as possible.
SC3200
BODY1
MEMORY & SYSTEM
TEPBGA_481
DESIGN NOTE: Recommended crystal: PN SMS49 from Monitor Products Company Inc. (www.monitor-products.com)
DESIGN NOTE: Recommended crystal: PN SM37 from Monitor Products Company Inc. (www.monitor-products.com)
27MHZ OSCILLATOR
32KHZ OSCILLATOR

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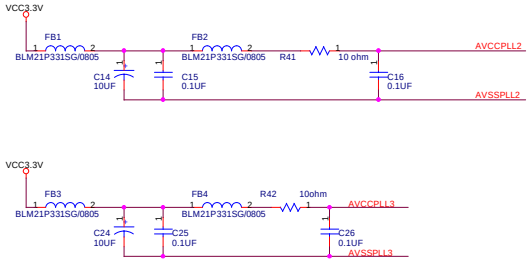
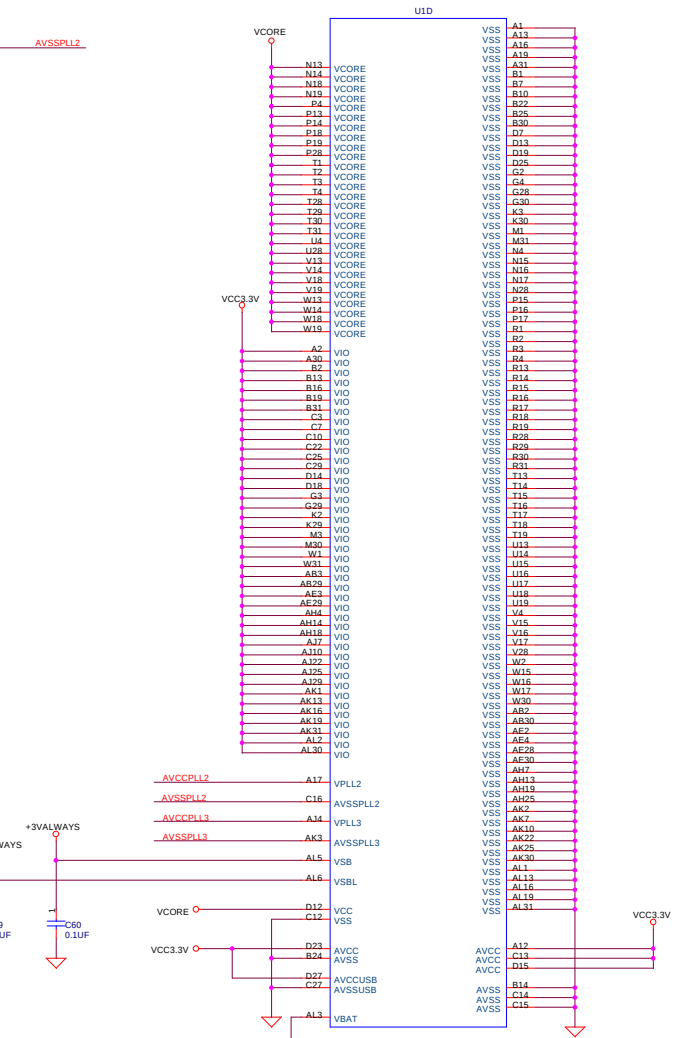
SC3200 INTERFACES: POWER; DECOUPLING CAPS, BATTERY HEADER

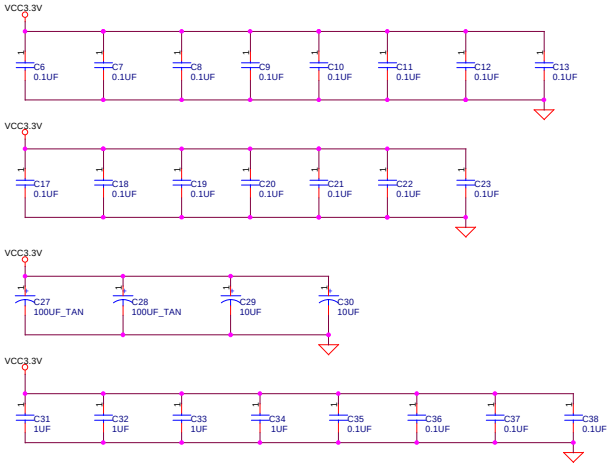


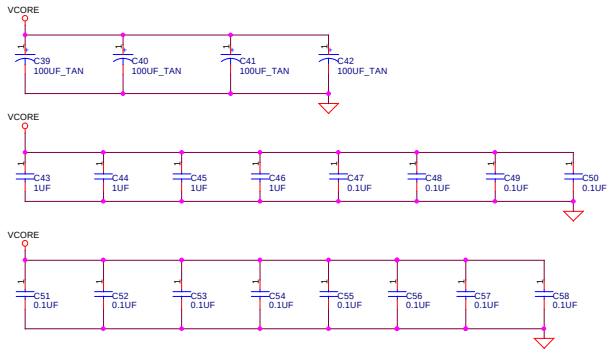
DESIGN NOTE: These filtered analog supplies should be laid out using separate power planes. See Layout Guidelines for details.

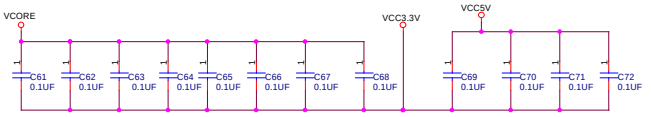
SC3200



DESIGN NOTE: Use low-ESR electrolytic capacitors. See Layout guidelines for placement.

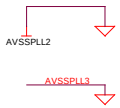




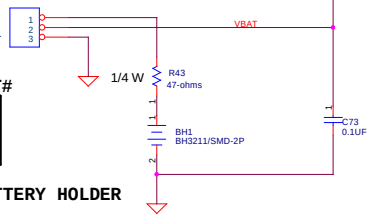


DESIGN NOTE: These Core-to-I/O caps as shown here, provide return current paths for signals which traverse the core plane split. Careful layout or a single power plane design with proper placement can eliminate these caps.

SINGLE POINT GROUND CONNECTIONS:

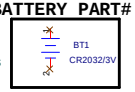


Jumper 1-2 for normal operation, 2-3 to clear CMOS memory.



DESIGN NOTE: To prevent damage to the battery, explosion, bursting, etc. it is recommended to include a current limiting resistor in case the battery is shorted by accidentally shorting pins 1-3 on the jumper.

BATTERY PART#



BATTERY HOLDER

DESIGN NOTE: This circuit allows the CMOS data to be cleared by momemtarily grounding the VBAT pin. It shows a battery holder. To reduce cost, batteries with pins may be soldered directly to the PCB. If no battery backup is required, ground the VBAT ball.

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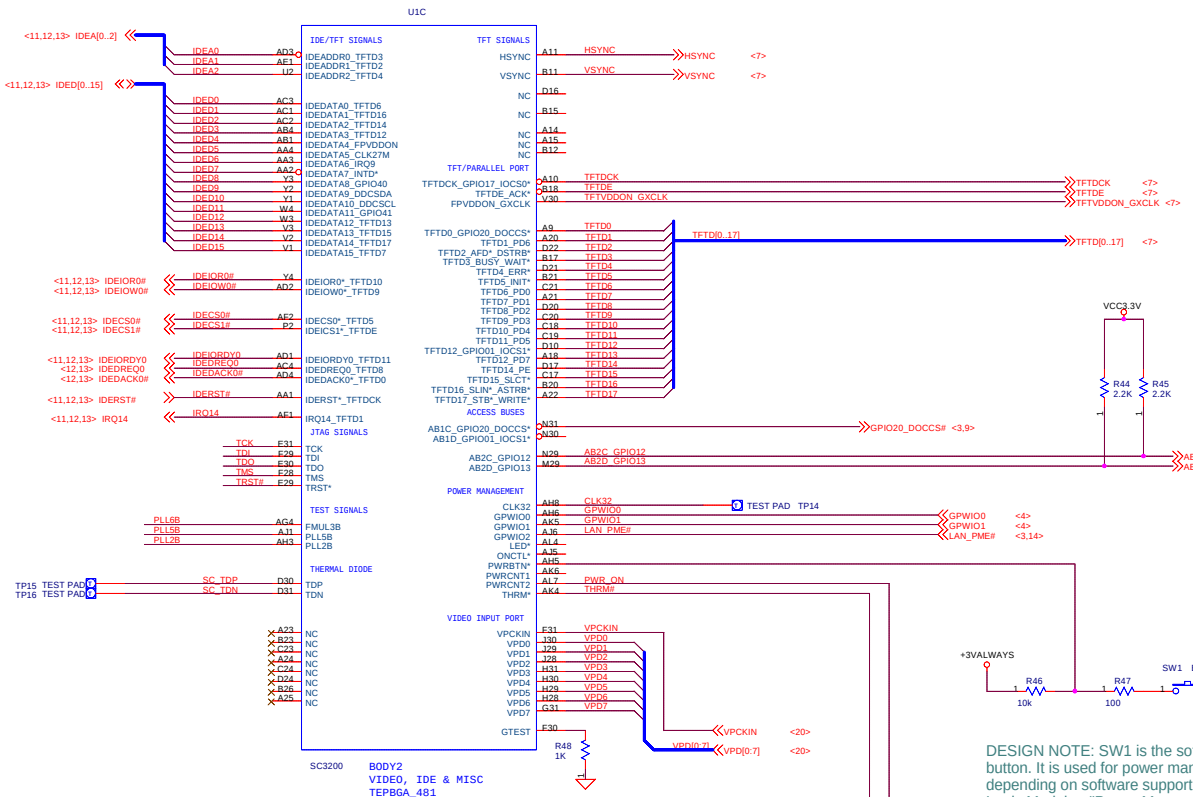
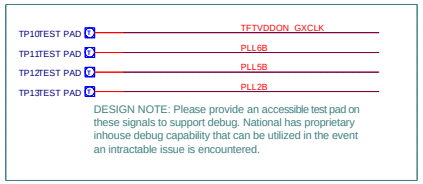
SC3200 INTERFACES: IDE, PARALLEL PORT, TFT, VIP, POWER MANAGEMENT, JTAG (WITH HEADER), ACCESS BUS 1&2, TEMP SENSOR

SC3200



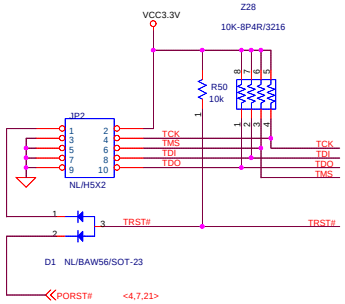


DESIGN NOTE: Please provide an accessible test pad on these signals to support debug. National has proprietary inhouse debug capability that can be utilized in the event an intractable issue is encountered.

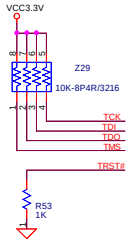
DESIGN NOTE: SW1 is the soft On/Off button. It is used for power management depending on software support. See the Core Logic Module - "Power Management Logic" section of the SC3200 databook.

DESIGN NOTE: Use one JTAG circuit or the other.

JTAG signals used.

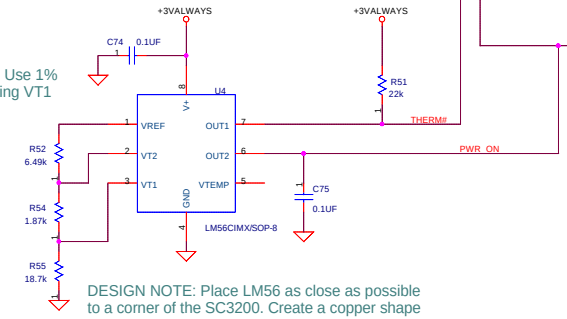


JTAG signals not used.



CPU TEMP SENSOR

DESIGN NOTE: Use 1% resistors for setting VT1 and VT2



DESIGN NOTE: With the resistors as shown, OUT1 goes low when the LM56 temp exceeds 75.6 degrees C. OUT2 goes low when the LM56 temp exceeds 89.5 degrees C. See the LM56 data sheet for details. Other devices such as the LM92 may also be used. The LM92 requires programming through the ACCESS.bus.

DESIGN NOTE: Place LM56 as close as possible to a corner of the SC3200. Create a copper shape or make sure the LM56 and SC3200 have a continuous ground plane to allow thermal coupling. This will ensure consistent and useful temperature readings for the SC3200.

DESIGN NOTE: OUT1 of the LM56 temp sensor is open collector, and if goes low if VT1 is exceeded. PWRCNT2 from the SC3200 is open drain, goes low to shut off power. Connecting these two together with a pull-up creates a WIred-OR circuit. If either goes low, PWR_ON will be low and shut off the VCORE and VCC3.3V supplies. For Save-to-RAM (Not shown in these schematics), the ONCTL# signal must be used.

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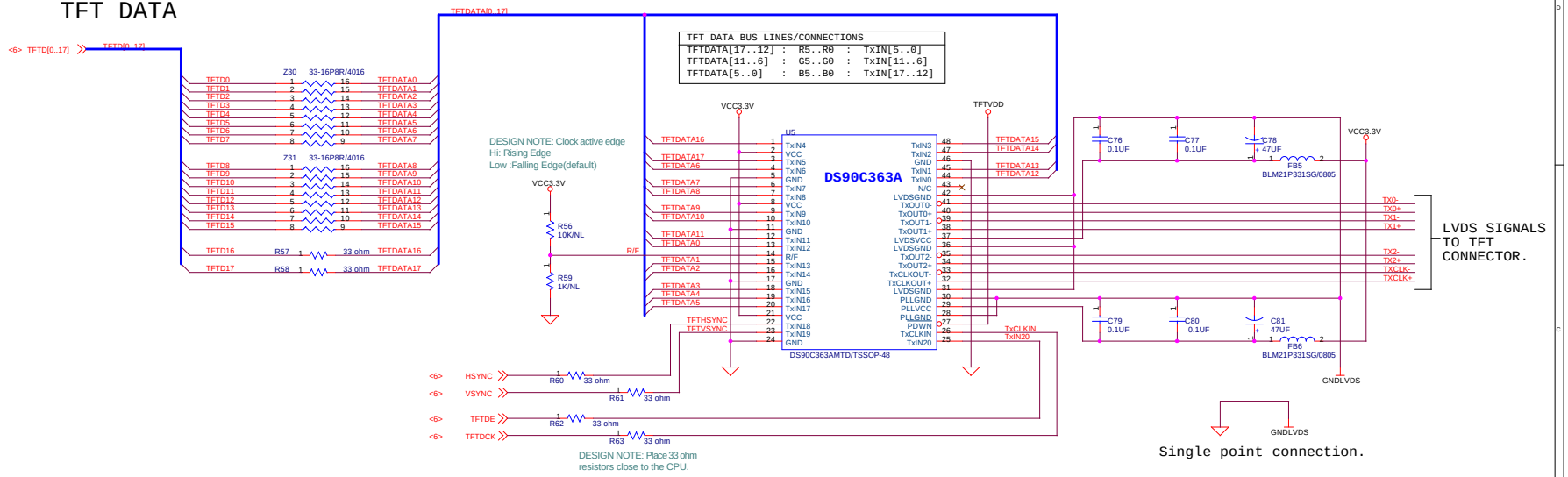
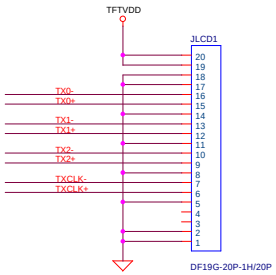
LVDS TFT: CONTROLLER, INVERTER, AND CONNECTOR.

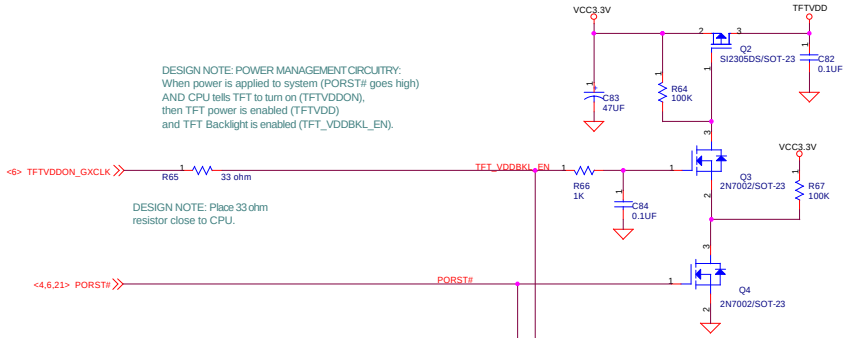
LVDS TFT CONVERTER/TRANSMITTER

TFT DATA

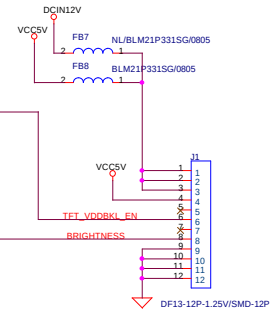


GENERIC TFT LVDS CONNECTOR





INVERTER CONNECTOR



BACKLIGHT INVERTER CIRCUIT

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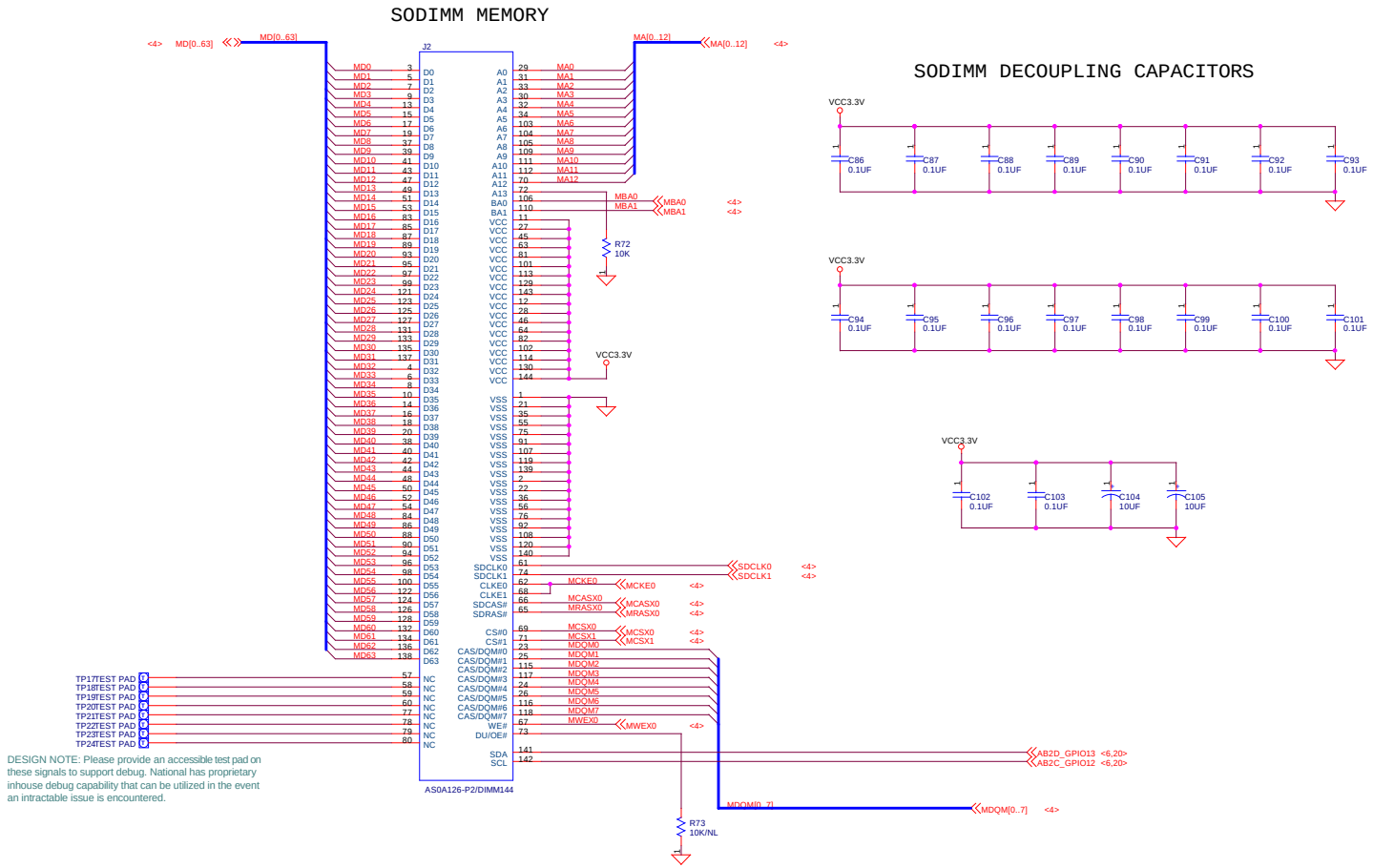
SODIMM: SODIMM CONNECTOR AND SODIMM DECOUPLING CAPACITORS



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Size: C	Document Number: SODIMM	Rev: 1.0
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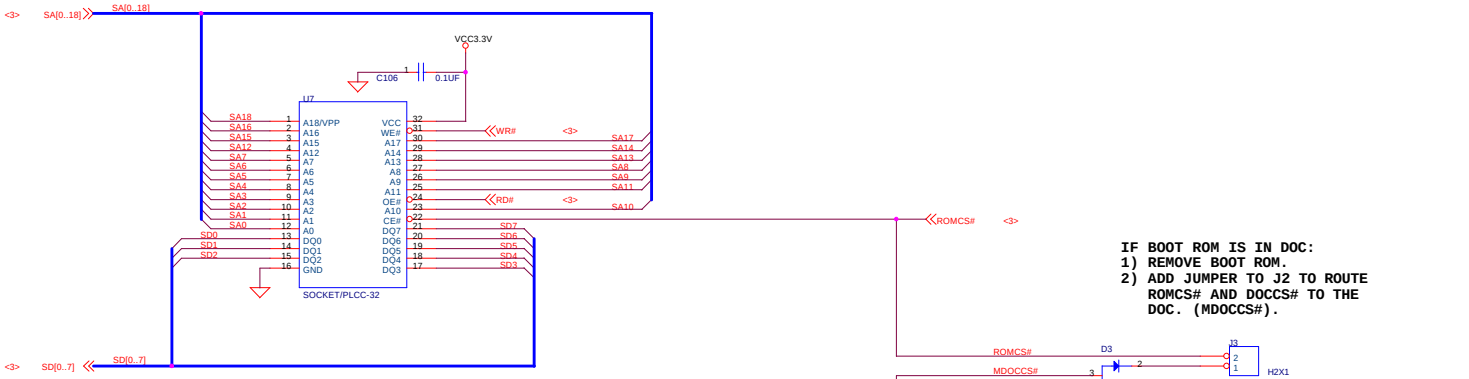
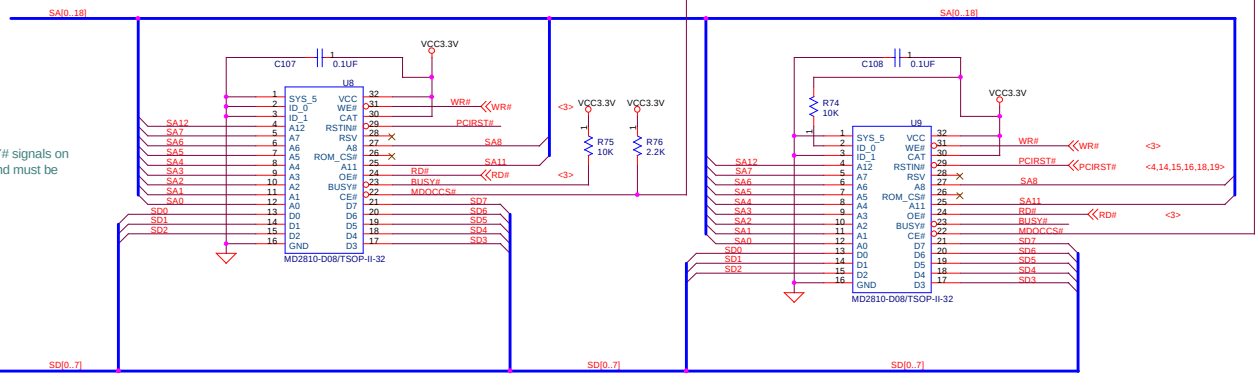
ISA BOOT ROM AND DOC DEVICES

BOOT ROM



IF BOOT ROM IS IN DOC:
1) REMOVE BOOT ROM.
2) ADD JUMPER TO J2 TO ROUTE ROMCS# AND DOCCS# TO THE DOC. (MDOCCS#).

DOC DEVICES



DESIGN NOTE: BUSY# signals on DOC are open drain and must be pulled up to VCC3.3V.

DESIGN NOTE: Two DOCs TSOP devices are shown in a cascade configuration to create a 16 MB storage space. The 8 MB DIP device cannot be cascaded. Cascading is done by setting the ID[1:0} pins to: First device: 00, second device: 01.

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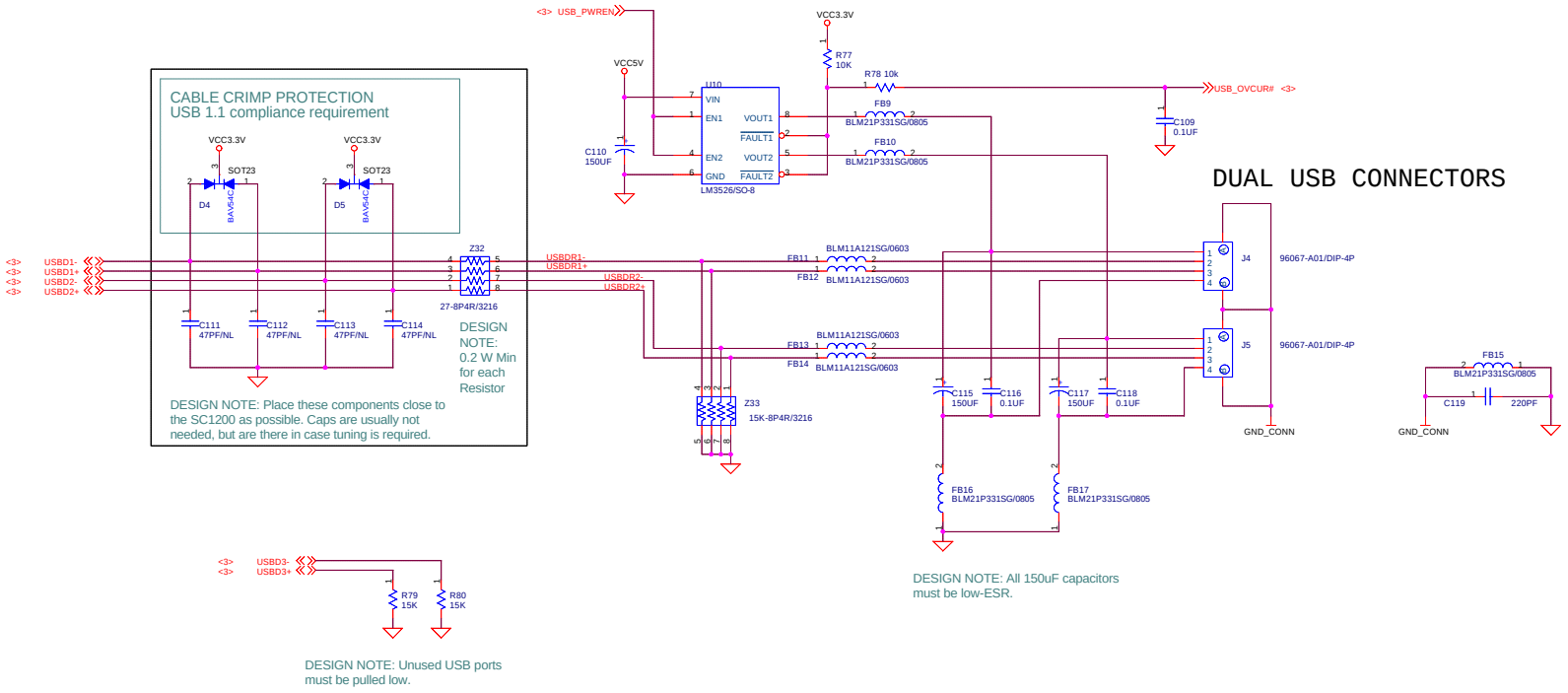
USB INTERFACE AND CONNECTOR



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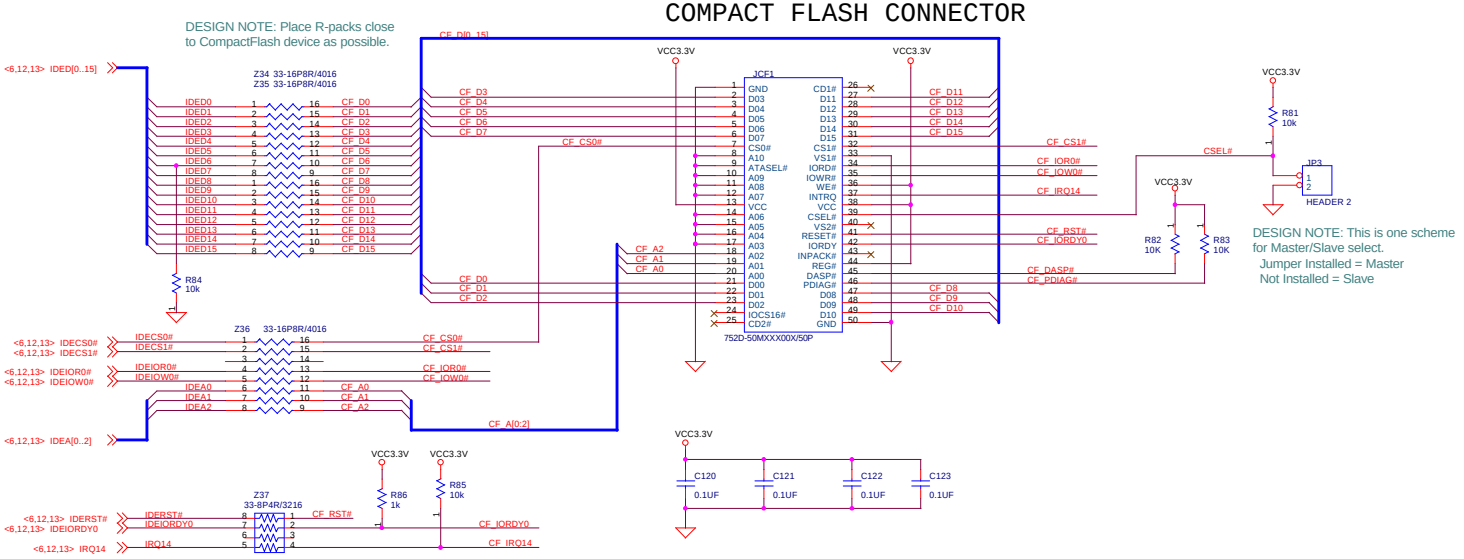
COMPACT FLASH, SERIAL PORT

DESIGN NOTE: These schematics intend for the Compact Flash -OR- IDE connector(s) to be included, but not both. The designer should choose between this sheet -OR- one of the IDE schematic pages.

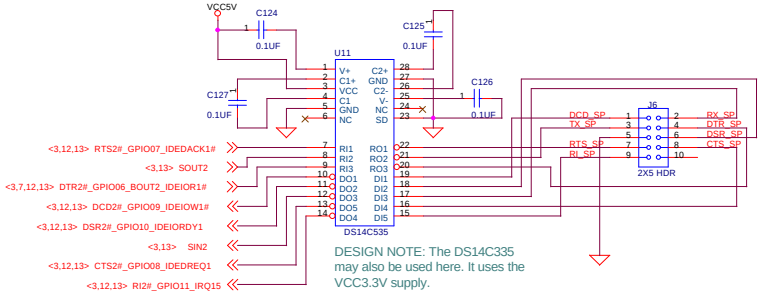
DESIGN NOTE: Using a Compact Flash device allows use of the Serial Port from the SC3200 as shown below.

COMPACT FLASH CONNECTOR



SC3200 SERIAL PORT

DESIGN NOTE: Do not use this page and the PRIMARY IDE INTERFACE AND CONNECTORS, SERIAL PORT page in a user design. This serial port exists on both pages. When the DRC is run on this schematic there are pin type and signal name conflicts due to the duplication.



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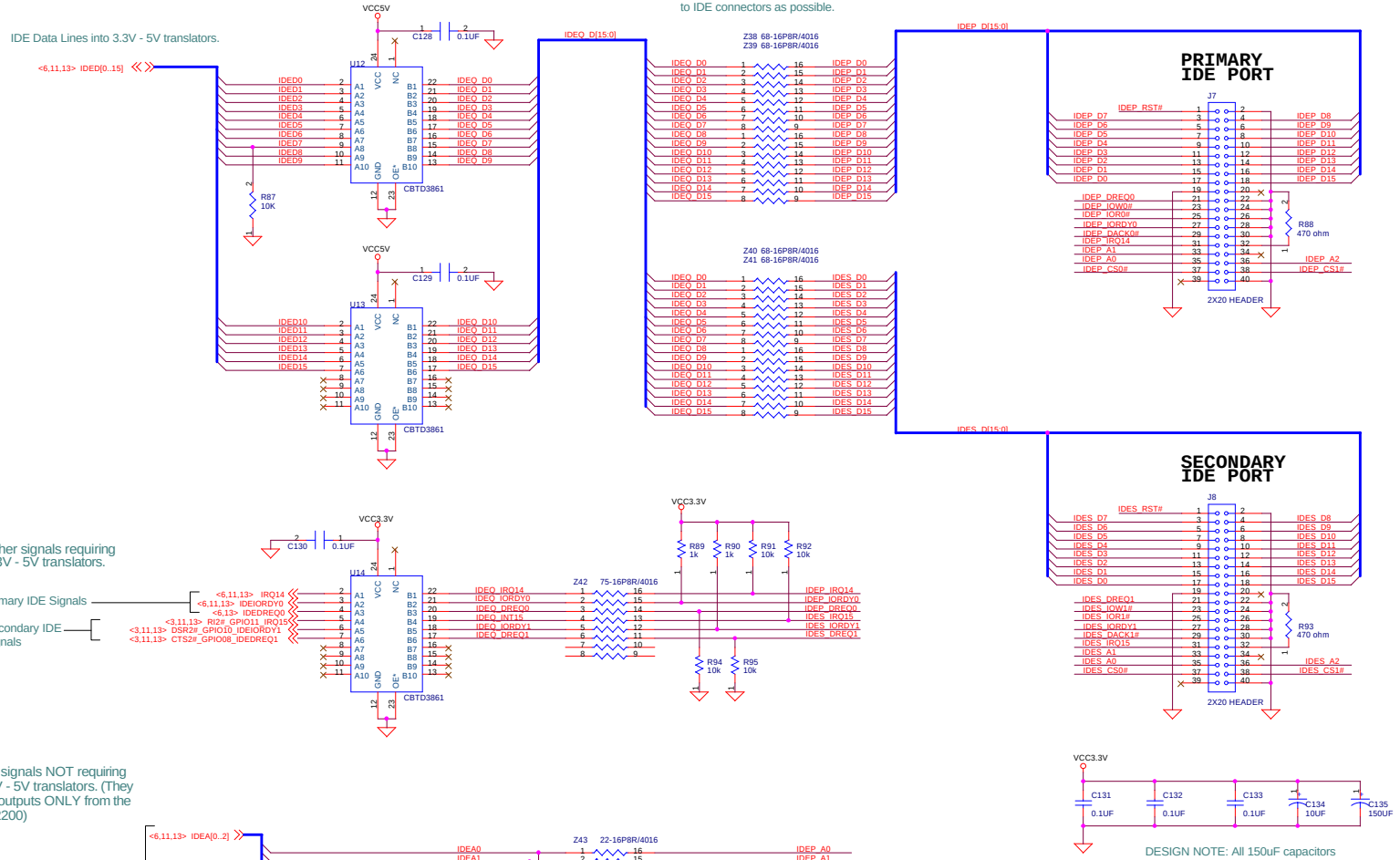
PRIMARY AND SECONDARY IDE INTERFACE AND CONNECTORS

DESIGN NOTE: Use this sheet for Primary and Secondary IDE Ports, no Serial Port

DESIGN NOTE: The 3.3V to 5V Translators shown below are not needed if a 3.3V compatible IDE drive is used such as an ATA100 hard drive.

IDEP_ designates Primary IDE Port signals.
IDES_ designates Secondary IDE Port signals.

DESIGN NOTE: Place R-packs close to IDE connectors as possible.



DESIGN NOTE: All 150uF capacitors must be low-ESR.

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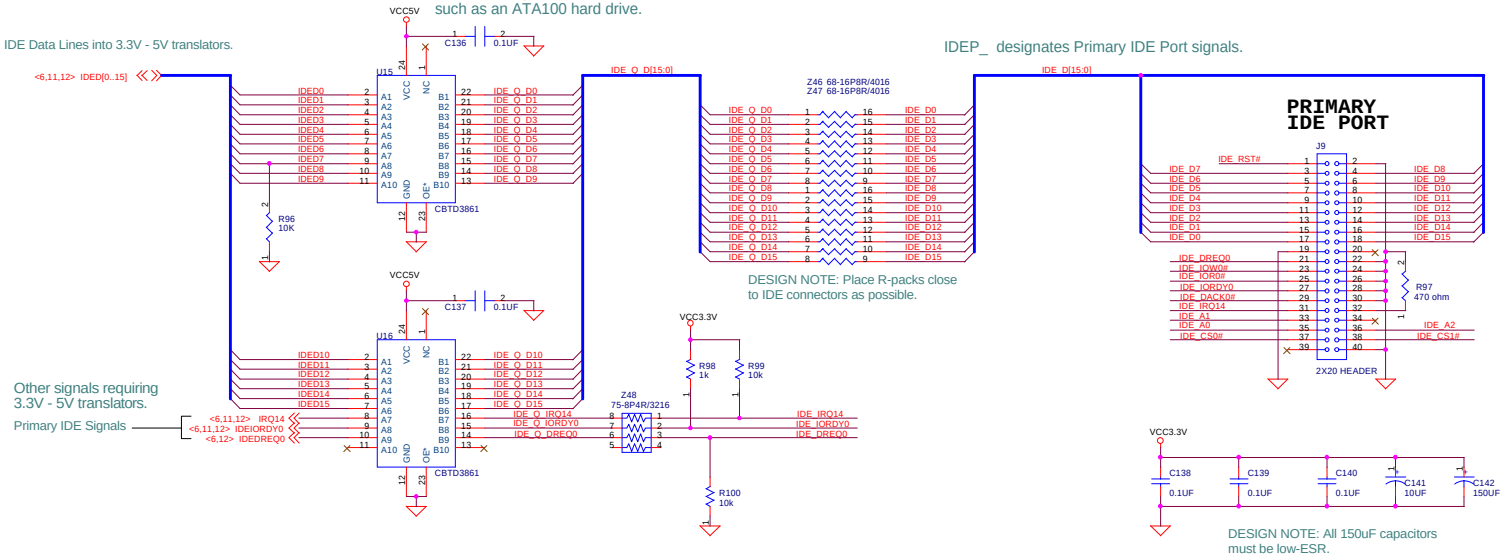
PRIMARY IDE INTERFACE AND CONNECTORS, SERIAL PORT

DESIGN NOTE: Use this sheet for Primary IDE Port only. Using one IDE port allows for SC3200 Serial port.

DESIGN NOTE: The 3.3V to 5V Translators shown below are not needed if a 3.3V compatible IDE drive is used such as an ATA100 hard drive.

IDE Data Lines into 3.3V - 5V translators.

IDEP_ designates Primary IDE Port signals.



DESIGN NOTE: Place R-packs close to IDE connectors as possible.

DESIGN NOTE: All 150uF capacitors must be low-ESR.

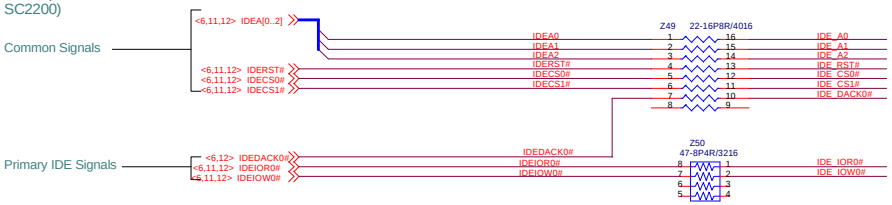
Other signals requiring 3.3V - 5V translators.

Primary IDE Signals

<6,11,12> IRQ14
<6,11,12> IDEIORDY0
<6,12> IDEDREQ0

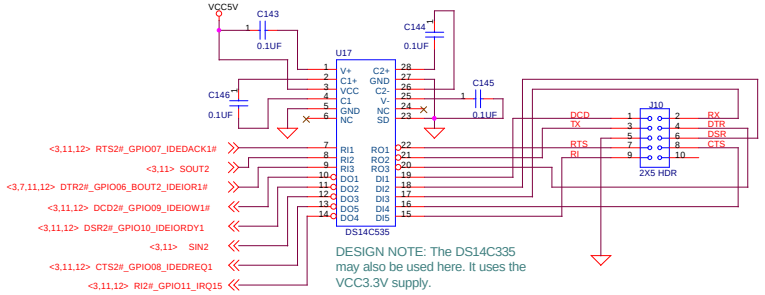
IDE signals NOT requiring 3.3V - 5V translators. (They are outputs ONLY from the SC2200)

Common Signals



SC3200 SERIAL PORT

DESIGN NOTE: Do not use this page and the COMPACT FLASH, SERIAL PORT page in a user design. This serial port exists on both pages. When the DRC is run on this schematic there are pin type and signal name conflicts due to the duplication.



DESIGN NOTE: The DS14C335 may also be used here. It uses the VCC3.3V supply.

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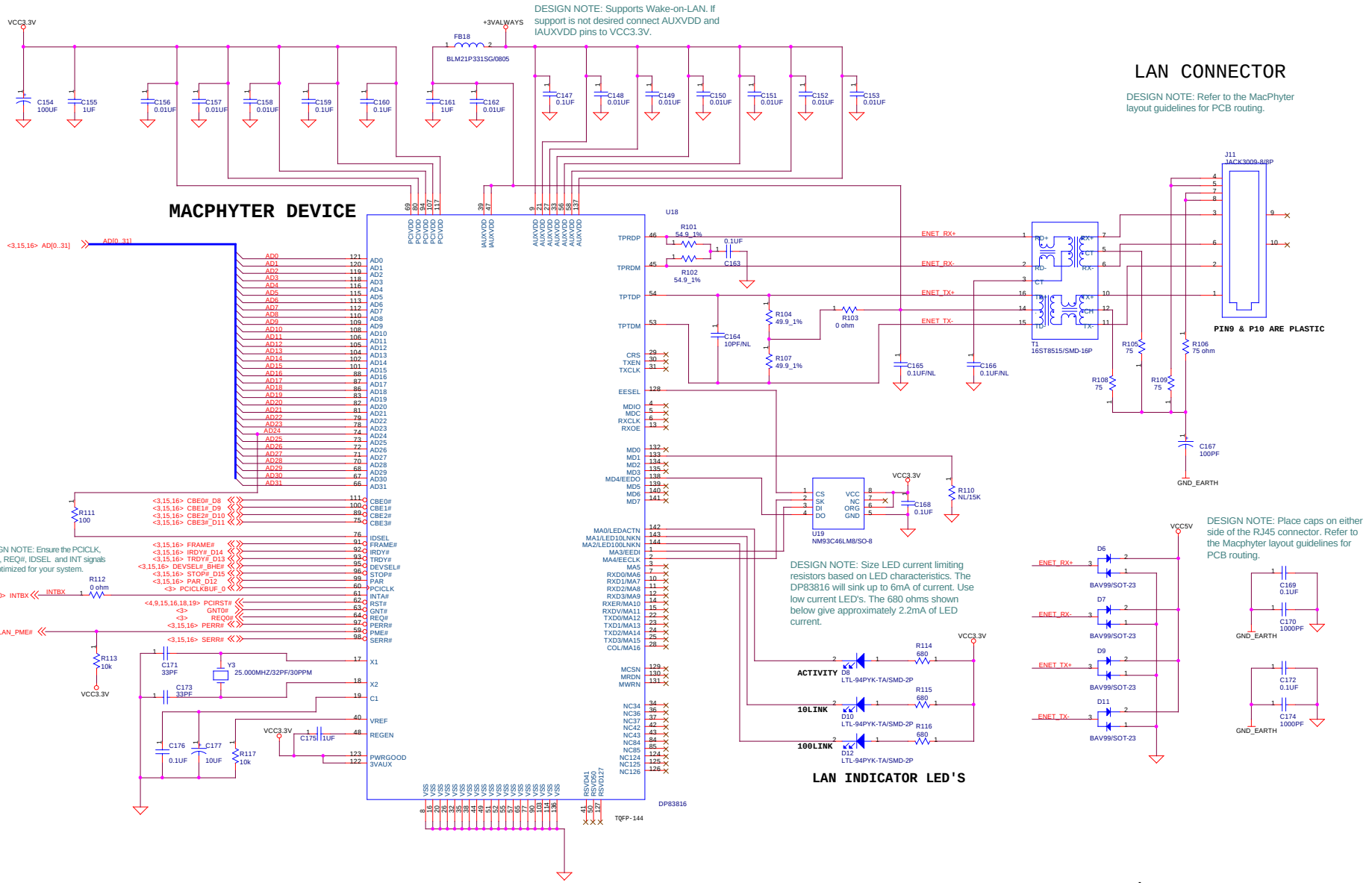
ETHERNET: DP83816 MACPHYTER DEVICE, LAN CONNECTOR



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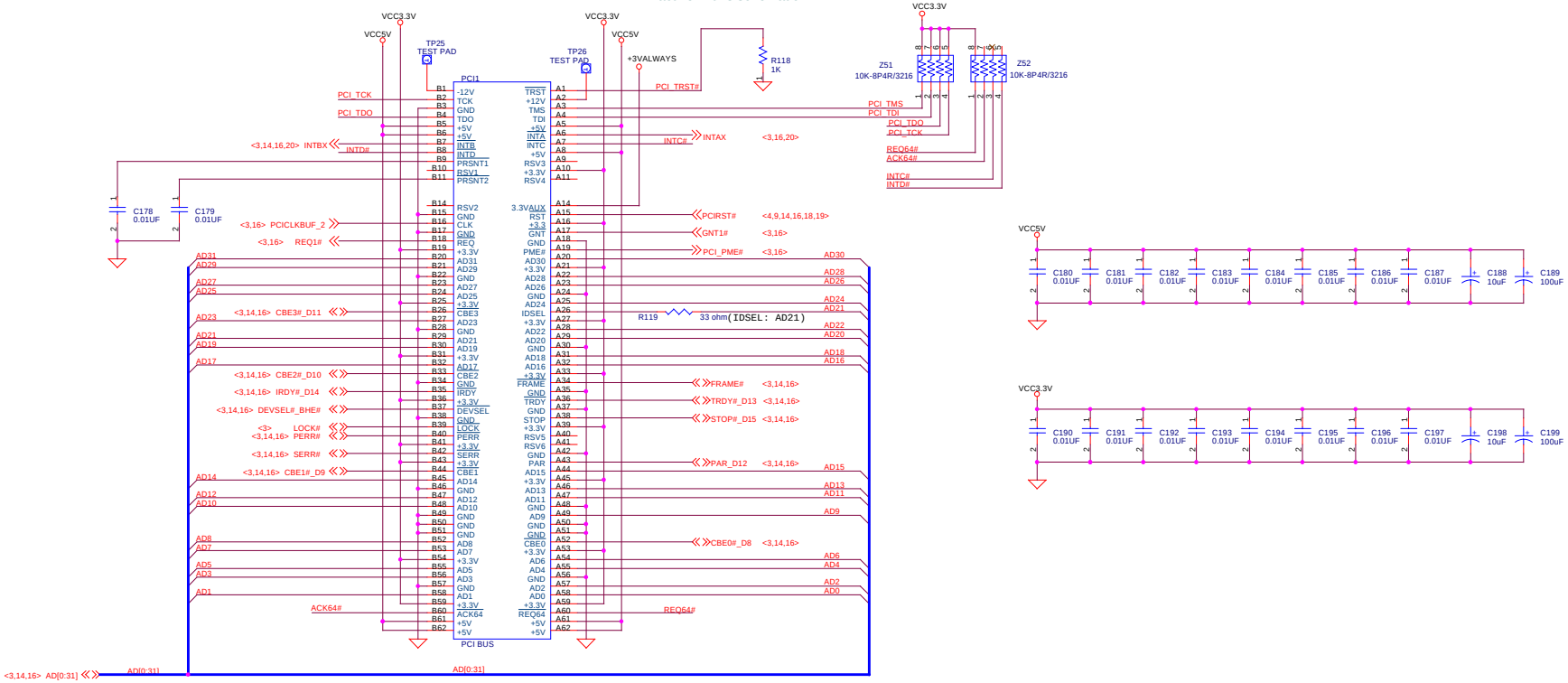
STANDARD PCI SLOT

DESIGN NOTE: Use standard PCI slot shown on this sheet -OR- Mini-PCI slot shown on next sheet, but NOT BOTH.

DESIGN NOTE: PCI bus supports only 3.3V devices and cards. Do not plug a 5V PCI card without using an adapter. +/- 12V power is not provided in this design.

DESIGN NOTE: The JTAG test signals, PCI_TCK, PCI_TDI, PCI_TDO, PCI_TMS, and PCI_TRST#, are tied inactive in this schematic.

3.3V PCI SLOT



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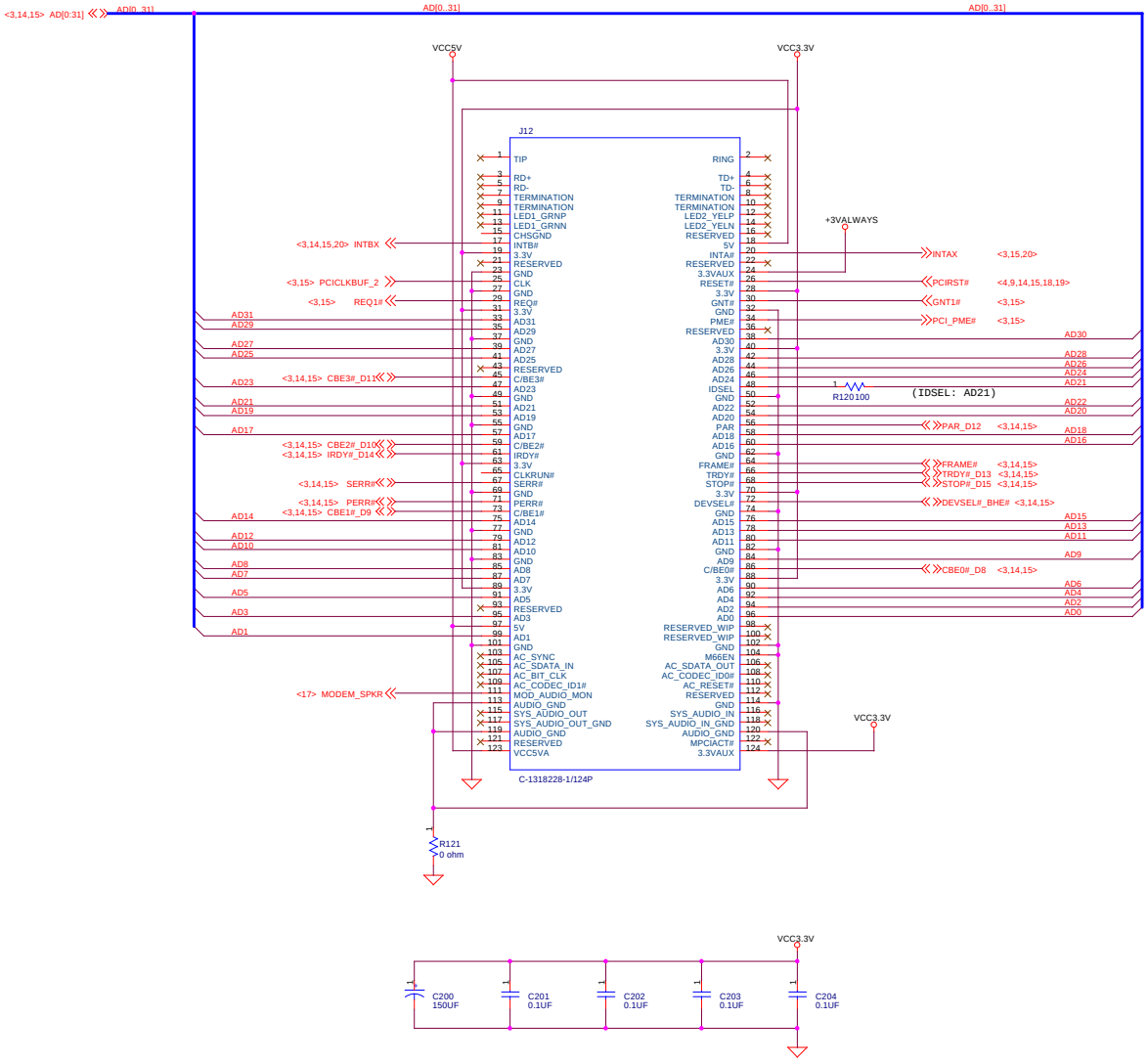
MINI PCI SLOT:

DESIGN NOTE: Use Mini-PCI slot shown on this sheet -OR- standard PCI slot shown on previous sheet, but NOT BOTH.

MiniPCI
TYPEIII
CONNECTOR



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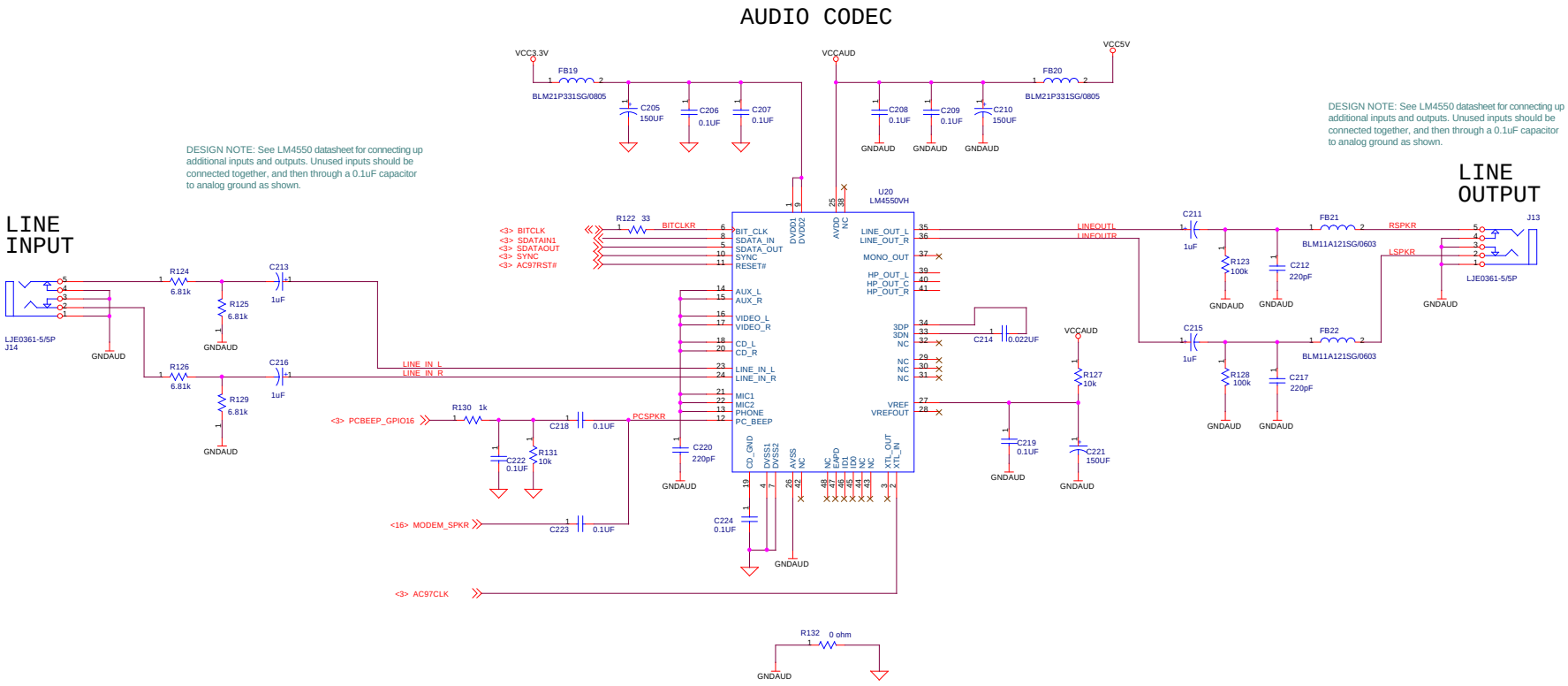
AUDIO: AC'97 CODEC, AUDIO AMPLIFIERS, LINE INPUT, LINE OUTPUT CONNECTORS



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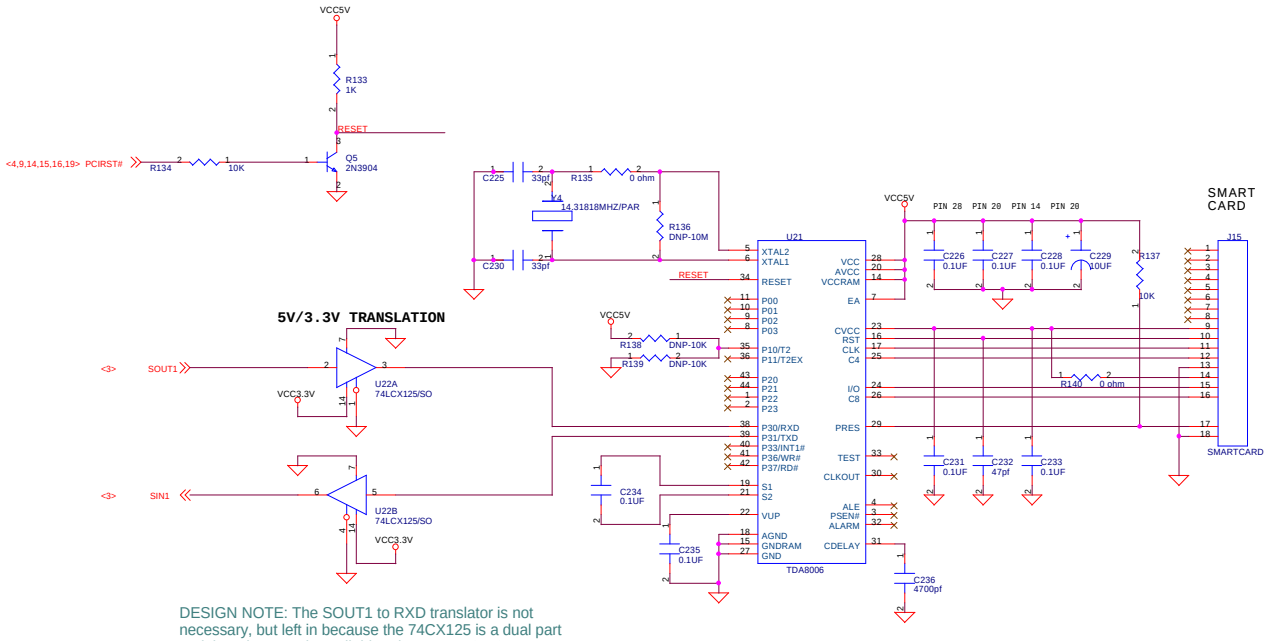
SMART CARD: SMART CARD INTERFACE AND CONNECTOR



DESIGN NOTE: The SOUT1 to RXD translator is not necessary, but left in because the 74CX125 is a dual part and the other gate is available. The TXD to SIN2 translator is required because the CPU is not 5V tolerant.

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LPC SUPERIO:

Floppy port, Serial ports 1 and 2, Parallel port, Keyboard and Mouse ports.

DESIGN NOTE: See the PC87364 datasheet for information on straps. The following pins function as straps. With no pull-up strap on these pins, they default to the functions listed below.

- Pin 101, BADDR: Sets the Index-Data pair to 2Eh, 2Fh.
- Pin 99, PSLDC0 and Pin 107, PSLDC1: Sets Pins 33-35 and 37 function as PWBTOUT#, PSON, PWBTIN#, and SLPS5# respectively.
- Pin 109, PSONPOL: Sets PSON to active low with open-drain output.

LPC Bus Signals

Parallel Port signals.

Serial port 1 and 2 signals.

MOUSE

KEYBOARD

FLOPPY DRIVE PORT

SERIAL PORT 1

Serial Port 1 signals from SuperI/O

SERIAL PORT 2

Serial Port 2 signals from SuperI/O

PARALLEL PORT

Parallel Port signals from SuperI/O

In order to minimize the crosstalk in ECP mode, the termination circuits shown above are recommended
Place all termination circuits close to the connector to avoid EMI

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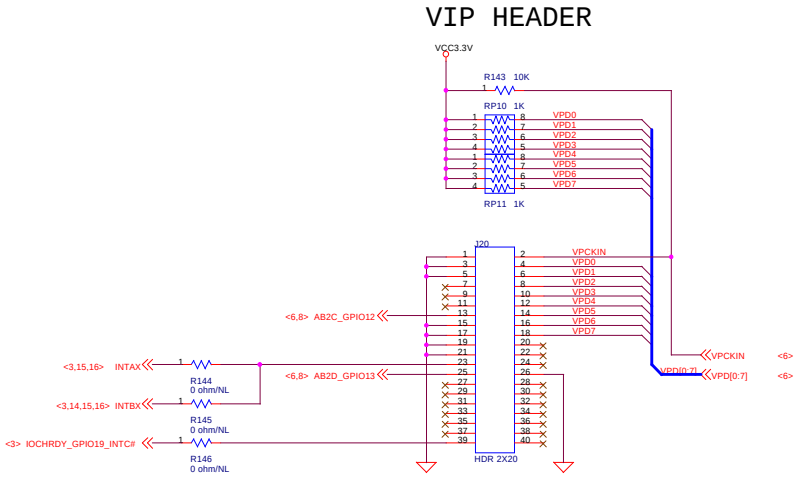
VIP HEADER



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Title: SC3200 Reference Schematics

Size: C | Document Number: VIDEO INPUT PORT | Rev: 1.0

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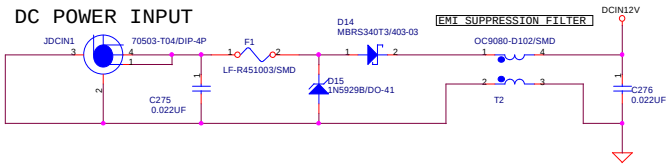
SYSTEM POWER: DC-DC CONVERTERS, POWER SEQUENCING, CORE VOLTAGE SETTING

DESIGN NOTE: This schematic shows power supply circuits based on a regulated +12V DC, +/-10% DC voltage input. Make sure the power requirements for the supply are adequate for the specified load currents. In the design shown, the power requirements are:
VCORE = 1.8V @ 2A Max = 3.6W max
VCC3.3V = 3.3V @ 1.5A Max = 5W max
VCC5V = 5.0V @ 1A max = 5W
Total 13.6W @ 80% efficiency typical = 17W supply
Therefore, the recommended power supply should be +12V @ 2A.

DC POWER INPUT

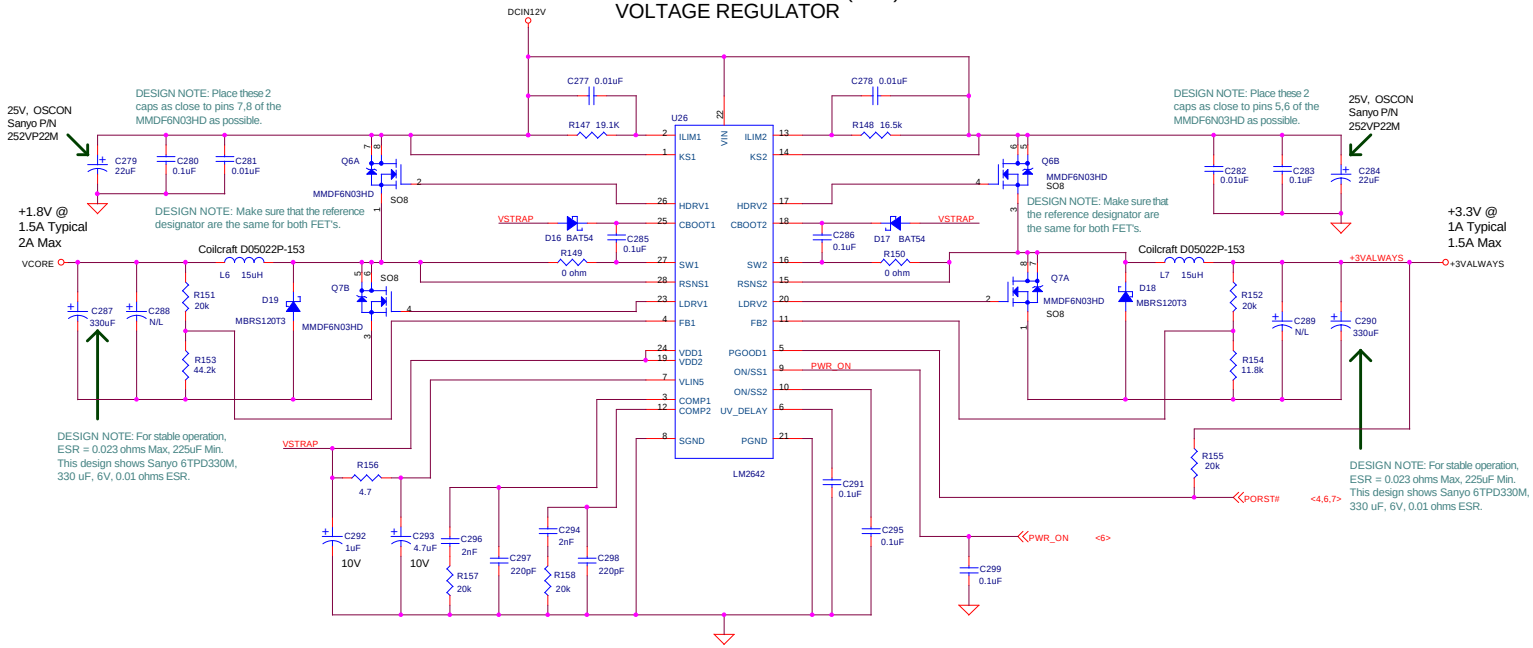


DESIGN NOTE: See the SC3200_03 Sheet for power supply connections to the SC3200. The relation to net names and SC3200 supply names are:

SC3200 Supply	Connects to (This Sheet)
VCORE	VCORE
VIO	VCC3.3V
VSB	+3VALWAYS
VSBL	VCOREALWAYS
VSS	GND SYMBOL

CAUTION! : VCOREALWAYS AND VCORE MUST BE SET TO THE SAME VOLTAGE.

VCORE & 3.3VALWAYS (VSB) VOLTAGE REGULATOR



DESIGN NOTES FOR THE LM2642:

DESIGN NOTE: For always on operation, the On/Off inputs to devices (currently shown connected to PWR_ON) should be connected to a Pull-up. Additionally, the VCOREALWYS regulator and VCC3.3V switch may be removed, and VCORE = VCOREALWAYS, and VCC3.3V = +3VALWAYS

DESIGN NOTE: When VCORE is shut off, there is 500 ohms between VCORE and ground.

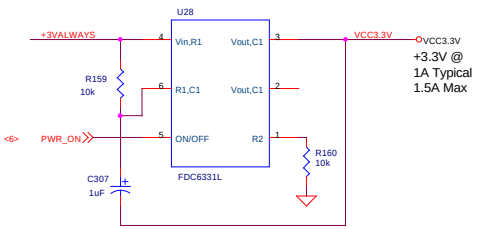
DESIGN NOTE: The values selected in this design are for the following conditions:
1) VCORE = 1.8V, 1.5A typical, 2.0A Max
2) +3VALWAYS = VCC3.3V = 3.3V, 1.0A typical, 1.5A Max

DESIGN NOTE: The time from PWR_ON asserted high, to VCORE and +3VALWAYS brought up is about 10 mSec. The start-up delay in the VCC3.3V switch (FDC6331L) attempts to match this delay.

DESIGN NOTE: LM2642 pins KS1, KS2, RSNS1, RSNS2 are sense lines. They should connect to the FETs using SEPARATE traces of minimal width.

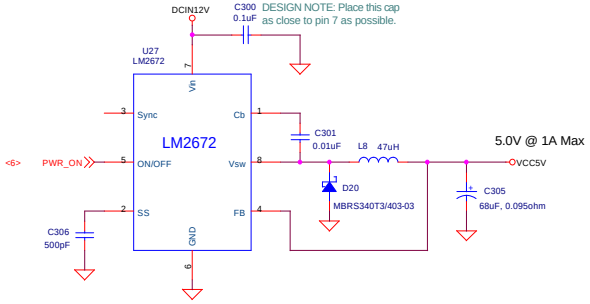
VCC3.3V (VIO) SWITCH

DESIGN NOTE: The Fairchild FDC6331L is a switch that controls the main VCC3.3V rail. The switch allows shutoff during power management events such as Save-to-RAM. The R's and C's in the circuit control a start-up delay so the VCC3.3V rail comes up at the same time as the VCORE rail. They also limit the start-up current spike. See the FDC6331L datasheet and application note AN1030 to set the values. The values shown below provide approximately 10 mSec delay bewteen the Input (VCC3VALWAYS) and the Output (VCC3.3V)



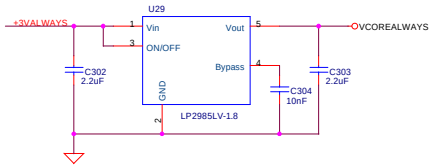
VCC5V REGULATOR

DESIGN NOTE: This example circuit can support up to 3 USB low-power devices plus audio. Another typical use is USB, one IDE drive, and audio. Use the LM2676 if >1A is required.



VCOREALWAYS (VSBL) REGULATOR

DESIGN NOTE: The LP2985LV-1.8 is a fixed 1.8V regulator. It is also available in 1.5V and 2.0V. There are a variety of other low-cost fixed output voltage regulators for VCOREALWAYS. The current requirement for VCOREALWAYS is 2mA max at 25 C. IMPORTANT: VCORE and VCOREALWAYS MUST be set to the same value.



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