AMD Geode™ GX1 Processor/ CS5530A Companion Device Schematic Checklist

1.0 Scope

AMD Geode™ Solutions offer custom products for the information appliance market. This schematic review checklist was developed to assist FAEs and OEMs in their schematic design and review process when using the AMD Geode™ GX1 processor and AMD Geode™ CS5530A companion device.

Note: This is revision 1.2 of this document. The difference from revision 1.1 (dated October 2000) is the addition of item 2 in Section 2.5 "MK1491 Clock Generator" on page 3 regarding spread spectrum support.

2.0 Discussion

The following subsections describe the critical device and interface connections for the GX1 processor and CS5530A companion device and National Semiconductor's PC97317 SuperI/O and DP83815 MacPHYTER devices.

2.1 GX1 Processor

1) Bypass and pull-up components on SDCLK lines at the DIMMs should be no-loads if they are there at all.
2) Verify that the SDCLK lines and SDCLK_OUT → SDCLK_IN loop adhere to the current layout guidelines for the processor being used.
3) Make sure SMI# is pulled up.
4) 10 ohm series termination resistors are required on the MA bus, MD bus, and memory control lines. The resistors should be placed close to the processor.
5) Make sure TEST is pulled down.
6) Make sure FLT# is pulled up with a 10 K-ohm resistor.
7) Make sure 10K pull-ups are on all the processor's REQ# and GNT# lines.
8) MICTOR connectors should be included in the design to provide access to the PCI bus for debug. Refer to the *AMD Geode™ Processor PCI Access Header* application note.
9) Be sure not to significantly imbalance the memory controller. An example of this situation would be a system with four pieces of SDRAM using CS0#, RAS0#, CAS0#, etc. and a DIMM socket using CS2# and CS3#, RAS1#, CAS1#, etc. Since a DIMM can have 16 or more pieces of SDRAM and the other half of the interface only has four, setup and hold times will vary significantly between the two halves and will likely cause one of them to fail.
10) Ensure the GX1 processor's core voltage is bulk decoupled with four 100 µF Tantalum or OsCon capacitors as close to the processor as possible.

2.2 CS5530A Companion Device

1) Ideally, PLLVAA should have its own regulator. Filtering V_{CC3}, however, is usually OK.
2) Verify that a separate ground plane for AV_{DD1} and AV_{DD3} exists. This ground plane should extend underneath the RGB runs from the CS5530A to the VGA port with one connection to digital ground at the VGA port. Termination components on the RGB lines should also connect to this ground plane.
3) Verify that a separate ground plane for PLLVAA exists and that it connects to digital ground at a single point.
4) Make sure there are 2.7K pull-ups on all the PCI bus control signals.
5) Make sure the CS5530A is placed in the correct ISA mode:
   – Strap pin P26 (INTR) low through a resistor: ISA Limited Mode.
   – Strap pin P26 (INTR) high through a resistor: ISA Master Mode.
6) If CLK_32K is provided to the CS5530A, it must be active when power is applied to the CS5530A. Otherwise, it should be pulled down.
7) SUSP_3V on the CS5530A must be pulled up or down at power-up to determine the inactive state of SUSP_3V.
8) HOLD_REQ# must be pulled up or down to determine CS5530A IDSEL (**IMPORTANT NOTE**: Many BIOSs, including the XpressROM, require this to be strapped low):
   – Strap pin H26 (HOLD_REQ#) low: IDSEL = AD28 (Chipset Register Space) and AD29 (USB Register Space).
   – Strap pin H26 (HOLD_REQ#) high: IDSEL = AD26 (Chipset Register Space) and AD27 (USB Register Space).
9) 10K pull-down required on IDE_DATA7 to prevent system BIOS from thinking a drive is connected and busy during IDE auto-detect routines.
10) A 220 µF cap across V_{CCDAC} at the CS5530A should be in place to eliminate switching power supply noise at the RGB output.
11) All IRQs to the CS5530A should be pulled up or down to prevent edge-triggered interrupts from occurring as a result of floating or momentarily non-driven IRQs.
12) IOCS16# and MEMCS16# must be pulled up.
13) If the CS5530A is in ISA slave mode, ISA_D[15:0] must be pulled up before the latches that convert these lines to ISA_A[15:0].
14) Pull up ISA_A[23:20] if these lines will not be used as GPIOs, especially if they go to a boot ROM.
15) If the CS5530A is in ISA slave mode driving a flat panel, series terminate FPDATA[17:0] with 33 ohm resistors at the CS5530A.
16) Make sure the 3.3V inputs to the CS5530A have enough high frequency decoupling and some bulk decoupling. Twelve 0.1 µF ceramic capacitors and three 10 µF Tantalum or OsCon capacitors are recommended as a minimum.

2.2.1 USB Interface

1) There should be ferrite beads on D+_PORT1, D–_PORT1, D+_PORT2, and D–_PORT2 at the USB connector.
2) There should be ferrite (90) between the USB port GND-1 and GND-2 signals and digital ground capable of carrying 1.5 amps minimum.
3) USB port pins 9, 10, 11, and 12 should connect to chassis ground, not to digital ground. Chassis ground should connect to digital ground through ferrite (600) and a 220 pF capacitor in parallel.

2.2.2 Mouse/Keyboard Interface

1) There should be ferrite (90) between MSGND and KBGND signals and digital ground, capable of carrying 1.5 amps minimum.

2.2.3 Audio Interface

1) Verify that a separate ground for audio exists and that the analog audio components tie to this ground. Digital ground should tie into this plane at a single point. **IMPORTANT NOTE**: This should be a wire connection - not a ferrite connection.
2) If a National Semiconductor LM454x codec is being used, make sure that the SDATA_OUT from the CS5530A goes to SDO on the codec and SDATA_IN from the CS5530A goes to SDI on the codec.

2.2.4 VGA Interface

1) There should be ferrite on the RGB lines at the VGA connector.

2.3 PC97317 SuperI/O

1) Many BIOSs, including XpressROM, expect this part to be clocked at 14.318 MHz.

2) CFG0/STXD1 should not be strapped. This allows the internal pull-down to strap the signal low, allowing the FDC, KBC, and RTC to wakeup inactive with the clock source set to 32.766 KHz with the on-chip clock multiplier disabled. **IMPORTANT NOTE:** Many BIOSs, including XpressROM, expect this configuration.

3) CFG1/SDTR2X should be pulled high with a 10K resistor if the SuperI/O's XD buffer is used for the system boot ROM. If the system boot ROM will exist on the CS5530A's ISA bus, this signal should not be strapped so that the internal pull-down will strap it low.

4) BADDR0/SDTR1X and BADDR1/SRTS1X should both be pulled high. This tells the SuperI/O to wake in config mode, that a PnP motherboard is present, and that the SuperI/O's index is 002Eh. **IMPORTANT NOTE:** Many BIOSs, including XpressROM, expect this configuration.

5) Pull up KBDAT, KBCLK, MSDAT, and MSCLK, even if the PS/2 mouse and/or keyboard ports are not being used.

2.4 DP83815 MacPHYTER

1) The National Semiconductor DP83815 MacPHYTER is very sensitive to its 25 MHz input crystal frequency. Make sure traces between the crystal and the MacPHYTER are at least 8 MILs wide to reduce inductance effects.

2) Make sure the output side of the ethernet transformer to the RJ45 connector is isolated with its own ground island and that no unrelated high-speed signals pass over this area.

3) Make sure the differential pairs to and from the MacPHYTER (TX+, TX-, RX+, and RX-) are identical in length.

2.5 MK1491 Clock Generator

1) Pull up PWRDWN#, SLOW#, and PCISTP# on the ICS Microclock MK1491 to be sure these input pins default to the inactive state. Even though the MK1491 data sheet indicates these signals are internally pulled up, these pull ups have occasionally failed. This situation can cause the chip to stop producing clocks.

2) Pull up 48M(LE#). This disables spread spectrum mode. If there is an option to pull this signal low, it must be removed. GX1 processors do not support spread spectrum clocking.

2.6 Power

1) Do not run switching regulators in series to produce any on-board voltages. This causes compound noise effects that can lead to system failures.

2) The system input voltage to all regulators should be relatively high compared to the regulated voltages. A 12V system input voltage works very well. However, it has been noted that systems with a 5V system input voltage are susceptible to intermittent failures due to input voltage fluctuations.

www.amd.com

One AMD Place
P.O. Box 3453,
Sunnyvale, CA 94088-3453 USA
Tel: 408-732-2400 or 800-538-8450
TWX: 910-339-9280
TELEX: 34-6306

TECHNICAL SUPPORT
USA & Canada: 800-222-9323 or 408-749-5703
USA & Canada: PC Microprocessor: 408-749-3060
USA & Canada Email: pcs.support@amd.com

Latin America Email: spanish.support@amd.com
Argentina: 001-800-200-1111, after tone 800-859-4478
Chile: 800-532-853
Mexico: 95-800-222-9323

Europe & UK: +44–0-1276-803299
Fax: +44–0-1276-803298
France: 0800-908-621
Germany: +49–89-450-53199
Italy: 800-877224
Europe Email: euro.tech@amd.com

Far East Fax: 852-2956-0588
Japan Fax: 81-3-3346-7848