AMD Geode[™] GX1 Processor/ CS5530A Companion Device Disabling Graphics/Video Hardware



1.0 Scope

In systems based on the AMD Geode[™] GX1 processor and CS5530A companion device the graphics/video functions are already integrated. However, if the system designer uses some type of external graphics controller, then the AMD Geode device's unused signals must be reconfigured. This document explains what to do with those unused signals.

- How to configure unused GX1 processor graphics/video I/O.
- How to configure unused CS5530A companion device graphics/video I/O.
- How to configure unused CS5530A companion device DCLK PLL I/O.

2.0 Discussion

Listed next are the areas of concern related to disabling the hardware graphics/video functions in the GX1 processor and CS5530A companion device:

2.1 Unused GX1 Processor Graphics/Video I/O Configuration

Table 2-1 details how to connect the unused GX1 processor graphics/video pins.

Signal Name	BGA Pin No.	SPGA Pin No.	Configuration	
PCLK	AC1	AJ1	No Connection	
VID_CLK	P1	V4	No Connection	
DCLK	AB1	AD4	Connect to Ground	
CRT_HSYNC	W2	AD2	No Connection	
CRT_VSYNC	AA3	AH2	No Connection	
FP_HSYNC	L2	R4	No Connection	
FP_VSYNC	J1	P2	No Connection	
ENA_DISP	AD5	AM6	No Connection	
VID_RDY	AD1	AK2	Connect to Ground	
VID_VAL	M2	S3	No Connection	
VID_DATA[7:0]	AB4, AB3, AD2, AC3, AD3, AE3, AF3, AD4			
PIXEL[17:0]	AB2, AA2, AA1, W3, W1, V3, V2, V1, T3, T2, T1, R3, R2, R1, P2, P3, N2, N3	AG3, AF4, AF2, AE1, AB4, AB2, AA3, Z4, X4, Y1, Y5, W1, W3, W5, V2, T4, T2, S5	No Connection	

Table 2-1. Unused GX1 Processor Graphics/Video IO Configuration

2.2 Unused CS5530A Companion Device Graphics/Video I/O Configuration

Table 2-2 details how to connect the unused CS5530A companion device graphics/video pins.

Signal Name	Pin No.	Configuration	
PCLK	A13	Connect to POR# (See CS5530A errata #18.)	
PIXEL[23:0]	C10, B11, C9, D9, A9, B9, C8, A8, B8, C7, D7, A7, C5, A5, D6, B6, A4, D5, B4, B3, C4, A3, A2, A1,	Connect to Ground	
ENA_DISP	B1	Connect to Ground	
HSYNC	C6	Connect to Ground	
HSYNC_OUT	N1	No Connection	
VSYNC	B5	Connect to Ground	
VSYNC_OUT	N2	No Connection	
DDC_SCL	M2	No Connection	
DDC_SDA	M4	Pull down with 1K resistor	
IREF	R3	No Connection	
EXTVREFIN	T2	No Connection	
AVDD[3:1]	U1, T3, N4	Connect to 3.3V	
AVSS[5:1]	R2, R4, T4, P1, P2	Connect to Ground	
IOUTR	P3	No Connection	
IOUTG	P4	No Connection	
IOUTB	R1	No Connection	
FP_DATA17	F3	No Connection if in ISA Slave Mode. Route as MASTER# if in ISA Master Mode.	
FP_DATA16	H3	No Connection if in ISA Slave Mode. Route as SA_OE# if in ISA master mode.	
FP_DATA[15:0]	H2, K1, K2, L1, D1, E2, F1, G1, G3, G4, G2, H1, J1, J3, J2, K3	No Connection if in ISA Slave Mode. Route as SA[15:0] if in ISA Master Mode.	
FP_CLK	M1	No Connection	
FP_CLK_EVEN	L3	No Connection	
FP_HSYNC	C2	Connect to Ground	
FP_HSYNC_OUT	E1	No Connection if in ISA Slave Mode. Route as SMEMW# if in ISA Master Mode.	
FP_VSYNC	C1	Connect to Ground	
FP_VSYNC_OUT	E3	No Connection if in ISA Slave Mode. Route as SMEMR# if in ISA Master Mode.	
FP_DISP_ENA_OUT	F2	No Connection	
FP_ENA_VDD	L2	No Connection	
FP_ENA_BKL	J4	No Connection	
VID_DATA[7:0]	C12, B12, A12, D11, C11, B13, C13, A11	Connect to Ground	
VID_CLK	A6	Connect to Ground	
VID_VAL	В7	Connect to Ground	
VID_RDY	B10	No Connection	
TVCLK	B2	Connect to Ground	

 Table 2-2. Unused CS5530A Companion Device Graphics/Video IO Configuration

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2.3 Unused CS5530A Companion Device PLL I/O Configuration

Table 2-3 details how to connect unused CS5530A companion device PLL pins. It is important to remember that this PLL can be used for functions other than video. It can generate frequencies of up to 157.5 MHz, and can be used as a clock source for other system functions. Table 2-3 shows what to do if the PLL is not being used for CS5530A graphics/video or any other system function.

Signal Name	Pin No.	Configuration
PLLLTEST	N23	No Connection - This pin is an internal test pin and should always be left disconnected for normal operation.
PLLVAA	M25	Connect to 3.3V
PLLAGD	N25	Connect to Ground
PLLDVD	M23	Connect to 3.3V
PLLDGN	N26	Connect to Ground
CLK_14MHZ	P24	This signal must be connected to a 14 MHz clock source. Even though it's primarily used to drive the PLL in the CS5530A, it is also used to properly configure reset to the GX-series processor.

Table 2-3. Unused CS5530A Companion Device PLL I/O Configuration

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