AMD Geode™ GX2 Processor/ CS5535 Companion Device Thin Client CRT Reference Schematic Specification

1.0 Scope

The reference schematic incorporates the AMD Geode™ GX2 x86 integrated processor and the AMD Geode™ CS5535 companion device into a design targeted at providing the basic features of a thin client CRT platform.

This document describes the features and options included in the reference schematic. Refer to Section A.1 "Related Documents" on page 13 for additional device information.

Figure 1-1 shows a high-level block diagram of the reference schematic.

Note: This is revision 1.3 of this document. The changes from revision 1.2 (dated February 2003) are the updates to reflect revision 1.6 of the reference schematic, specifically Section 3.1.1, updates to Table 3-1, added note and changed 0Ω NL to 10K NL for 66 MHz in Figure 3-1, edited Section 3.2.2.1 and Section 3.2.8, and changed 1.4V to 1.5V in the last sentence of Section 3.7.3.

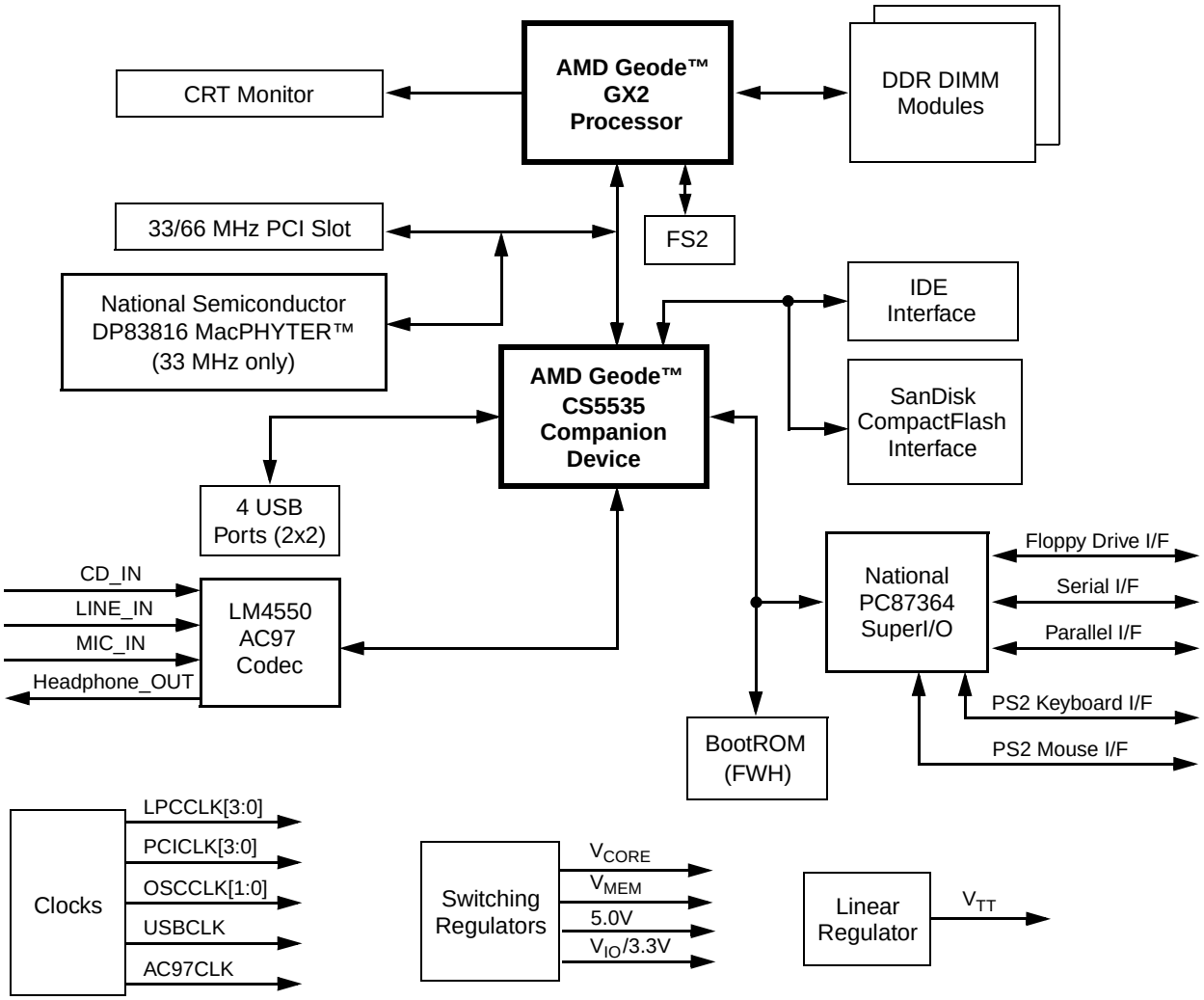


Figure 1-1. Thin Client CRT Block Diagram

2.0 System Overview

System Features

- AMD Geode™ GX2 integrated processor
- GX2 die temperature thermal sensor (National Semiconductor LM82)
- AMD Geode™ CS5535 companion device
- ACPI (Advanced Configuration Power Interface) control and RTC (Real-Time Clock)
- National Semiconductor LM4550 AC97 v2.1 codec:
  - MIC_IN
  - CD_IN
  - LINE _IN
  - Headphone_OUT
- One 3.3V PCI 2.2 slot (66 MHz is available if National Semiconductor MacPHYTER is not used in the design)
- LPC ROM
- CRT interface
- Four USB 1.1 ports supported by two independent USB controllers with overcurrent detection and protection
- DP83816 MacPHYTER ethernet device
- SanDisk Corporation's CompactFlash connector
- One ATA-5 (UltraDMA 66) IDE interface (supports two devices), 3.3V or 5.0V tolerant with buffering
- Two 184-pin unbuffered DDR (Double Data Rate) SDRAM DIMM modules
- National Semiconductor PC87364 SuperI/O LPC:
  - Serial port
  - Parallel port
  - Floppy interface
  - PS2 keyboard/mouse
- First Silicon Solutions, Inc. FS2 compatible JTAG interface
- Cost efficient voltage regulation from +12V power input

Future GX2/CS5535 Thin Client CRT System Options

- M-Systems DiskOnChip off the LPC bus
- DDR Memory (SODIMM)
- SDR (Single Data Rate) Memory (DIMM and SODIMM)
- MiniPCI connector
- National Semiconductor DP83861 GigPHYTER

3.0 Hardware Description

The following subsections describe the GX2/CS5535 reference schematic hardware components.

3.1 GX2 Integrated Processor

GX2 Integrated Processor Features

- 32-bit x86 compatible CPU core:
  - 16 KB instruction/16 KB data L1 caches
  - Fully pipelined FPU (Floating Point Unit) with AMD 3DNow!™ SIMD instruction set
- Intel MMX™ compatible instruction set extensions
- High performance and low power:
  - Target: 4W @366 MHz
  - Target: Core voltage of 1.4V
- UMA (Unified Memory Architecture) SDRAM memory controller:
  - 64 MB to 1 GB system memory
  - PC2100 DDR operation
    - Unbuffered DDR DIMM modules
  - 64-bit data path
- 2D graphics accelerator and display controller:
  - Hardware VGA display controller
  - Frame buffer compression
  - Three operand BitBLTs with 256 ROPs (Raster Operations)
  - Hardware cursor and Bresenham line drawing
- Display controller support logic:
  - 250 MHz DOTCLK PLL (Phase Lock Loop)
  - Color space conversion (YUV to RGB):
    - Supports YUV 4:2:20, YUV 4:2:0 support for PC98 and RGB 5:6:5 formats
  - Bi-linear video scaler with horizontal and vertical filters
  - 230 MHz VESA compliant triple video DAC
  - Directly supports VESA compliant CRT monitors
  - Directly supports VESA compliant active matrix TFT LCD panels
  - Directly supports DSTN passive matrix LCD panels
- PCI north bridge:
  - PCI 2.2 compliant with delayed transaction support
  - 32-bit with 3.3V signaling
  - 66 MHz operation
  - PCI arbiter:
    - Three external masters
    - Non-preemptable legacy master support
- AMD GeodeLink™ architecture
- IEEE 1149.1 JTAG interface:
  - GLCP (GeodeLink Control Processor) for software debug and performance analysis

- 368-terminal 5-row thermally enhanced BGA package:
  — CRT DAC or LCD interface (DSTN or TFT)
- 0.15µ Dual Gate Oxide (DGO) process

3.1.1 GX2 Clocking

The frequency selection is done at reset using the external strap options: GNT0#, GNT1#, and GNT2#. The strap options are soft, meaning the boot code reads the straps and then programs the appropriate registers. The meaning of the straps is determined by software and therefore can change. Specific implementations can chose to ignore them and program a fixed frequency. However, to maintain compatibility to existing boot code, it is strongly recommended that the hardware/software standard be maintained. There is a resistor pull-up/down pair connected to each of the GNTx# signals (shown on page 6 of the reference schematic). Table 3-1 shows the definition of the current strapping resistors.

Table 3-1. CPU Frequency Straps

Installed Resistors GNT[2:0]# Input Value	CPU MHz	GLIU MHz	Memory MHz
R16, R216, R217 GNT[2:0]# = 000b	200	133	66.5[1]
R16, R216, R15 GNT[2:0]# = 001b	266	177	88.5
R16, R14, R217 GNT[2:0]# = 010b	300	200	100[2]
R16, R14, R15 GNT[2:0]# = 011b	333	222	111
R215, R216, R217 GNT[2:0]# = 100b	366	244	122
R215, R216, R15 GNT[2:0]# = 101b	400	266	133[3]
R215, R14, R217 GNT[2:0]# = 110b[4]	433	289	144.5
R215, R14, R15 GNT[2:0]# = 111b	Reserved		

1. Mode not valid for DDR.
2. PC1600 compliant.
3. PC2100 compliant.
4. Not currently supported.

3.1.2 Graphics and Video

The graphics and video hardware are fully contained in the GX2 processor. The GX2 processor supports both CRT and TFT display panels, which are bond out options. This design is only compatible with the CRT version of the GX2.

3.1.2.1 CRT Output

The CRT output supports all display modes generated by the GX2. Refer to the *AMD Geode™ GX2 Processor Data Book* for a list of supported display modes.

3.1.3 System Memory

The GX2/CS5535 reference schematic supports up to two 184-pin, 512 MB unbuffered DDR DIMM modules. Bank interleaving can be automatically enabled by the boot firmware if both modules are populated with the same type.

DDR mode is fully supported per the *Double Data Rate (DDR) SDRAM Specification*. Memory interface features include:

- 2.5V DIMM module power supply voltage.
- 1.25V reference voltage to the GX2 and DDR SDRAM modules.
- 1.25V termination voltage (V_{TT}).
- SSTL_2 single terminated topology:
  — 22Ω series termination at the first DIMM module.
  — 51Ω parallel termination after the last DIMM module to V_{TT}.
- Matched trace lengths within a data byte lane, including the strobe (required in the layout; see the *AMD Geode™ GX2 Processor and CS5535 Companion Device Layout Recommendations* application note).

Memory Clocking

The GX2 memory controller derives the DRAM clocks from the GLIU clock. In DDR mode, the SDRAM clocks are one-half the GLIU clock frequency (the data rate is 2x the clock frequency). The DRAM clocks have a pre-programmed frequency range from 50 to 133 MHz, but can be adjusted by writing to the internal GLCP registers. DDR clock options from 83 to 100 MHz require the use of PC1600 compliant DIMM modules. DDR clock frequencies greater than 100 MHz require the use of PC2100 compliant DIMM modules.

Memory Sizing

The DIMM modules can be dynamically sized by the boot firmware during the POST (Power-On Self Test) routines by reading the SPD (Serial Presence Detect) EEPROM through the CS5535 SMB (System Management Bus) port. If the module does not support SPD, the boot firmware cannot determine the memory type (DDR or SDR), in which case, the system will be halted.

3.1.4 GX2 Packaging

The GX2 processor is packaged in a 5-row, thermally enhanced 368-terminal BGA (Ball Grid Array) with a 50 MIL ball pitch. There are two display packaging options: CRT DAC or TFT/DSTN LCD display. The LM82 thermal diode measurement sensor monitors the GX2 die temperature and is accessible through an industry standard two-wire interface on the board.

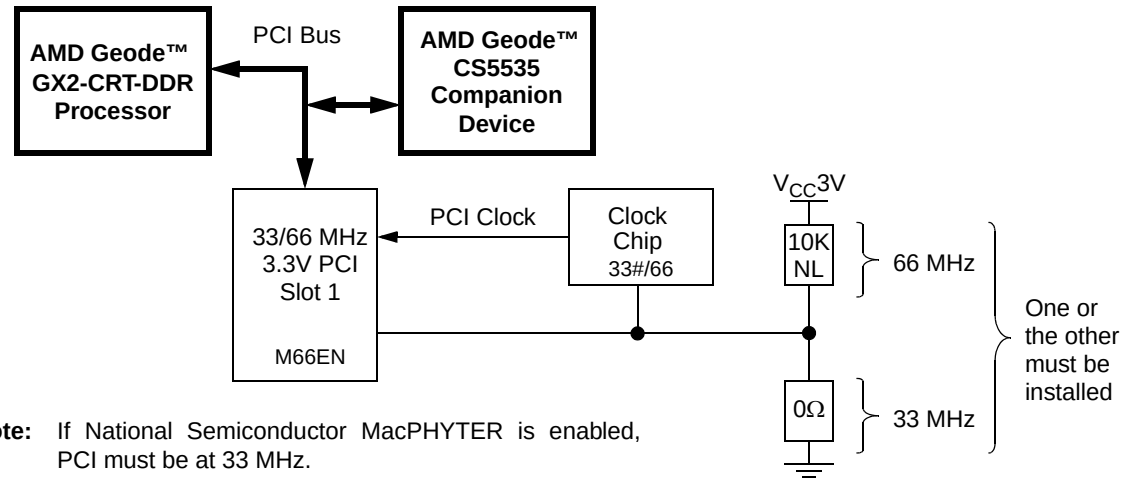
3.2 CS5535 Companion Device

CS5535 Companion Features

- PCI south bridge:
  - PCI version 2.2 compliance
  - 32-bit, 66 MHz operation, 3.3V signaling
- LPC bridge:
  - 3.3V signals
- PCI bus-mastering IDE controller:
  - 66 MB/s in ATA-5 mode
  - PIO (Programmed I/O) modes 0-4
  - Multiword DMA modes 0-2 and UltraDMA modes 0-4 (UltraDMA 33/66)
  - Two drive support with independent device timing across one channel
  - Read-ahead cache and posted write buffering
- Four USB 1.1 OHCI (OpenHost Controller Interface) ports:
  - Legacy device support
  - Two ports are allocated to two separate OHCI controllers to increase bandwidth
- Audio controller:
  - Native sound (only) support
  - AC97 rev 2.1 audio codec interface
- RTC (Real-Time Clock):
  - DS1287, MC146818 compatible with 242 bytes of battery backup CMOS RAM
- Flash interface:
  - Alternate use of IDE pins
  - Support bootROM interface
  - Connect to a variety of industry standards:
    - NAND or NOR Flash
- DDC (Display Data Channel) support:
  - Through GPIO with 5V tolerance and back-drive protection
  - Alternate use of serial port 2 pins
- Serial Port 1:
  - Alternatively infrared port
  - Software compatible with 16550A and the 16450 with at data rate of up to 115.2 Kbaud
- Serial Port 2:
  - Alternate use of DDC pins
  - Software compatible with 16550A and the 16450 with at data rate of up to 115.2 Kbaud
- IR communication port:
  - Alternatively serial port 1
  - Data rate of up to 115.2 Kbps (SIR)
- System Management Bus controller:
  - Compatible with Intel SMB, Philips' I^2C bus, and ACCESS.bus.
- On-chip ROM:
  - 1 to 4 KB
  - Optional boot source to eliminate boot device
- 208-terminal 4-row BGA package, socketed or soldered onto the board
- 0.15µ DGO (Dual Gate Oxide) process

3.2.1 PCI 66 MHz Support

Pin 49B on the PCI connector is M66EN. The GX2/CS5535 reference schematic provides a pull-up/down configuration to determine the PCI bus speed (see Figure 3-1). 33 MHz is the default due to the DP83816 MacPHYTER. The PCI clock speed select input is also connected to the M66EN to generate the appropriate clock for the system.



Note: If National Semiconductor MacPHYTER is enabled, PCI must be at 33 MHz.

Figure 3-1. PCI Bus Clocking Scheme

3.2.2 IDE Controller

The CS5535 contains an integrated PCI bus mastering IDE controller. The primary interface has a single 16-bit data path to the CS5535. The primary IDE channel interrupt lines are wired to IRQ14.

3.2.2.1 Cable Detection for UltraDMA 33/66

The CS5535 IDE controller supports PIO, Multiword DMA, and UltraDMA mode 0 through 4. The CS5535 must determine the type of cable present for proper configuration. UltraDMA 66 requires a 40-pin 80-conductor IDE cable. The system BIOS detects the type of cable. If the BIOS detects an 80-pin conductor cable, it can use any UltraDMA mode supported by both the CS5535 and the IDE device. If a 40-pin cable is detected, the system software must not enable modes faster than UltraDMA 33.

3.2.3 Audio Controller

The CS5535 contains an integrated PCI bus mastering audio controller. The audio controller supports an AC97 rev 2.1 compliant interface to an audio and modem codec using six bus mastering engines. See Section 3.5 "AC97 Audio Codec" on page 8 for more information.

3.2.4 PC Beep Transducer

The PC beep transducer is a mono audio output driven from the GPIO1/PC_BEEP signal. It drives an on-board audio transducer.

3.2.5 USB Ports

The CS5535 supports four OHCI USB host ports with enable/disable and overcurrent detection. The ports are rated for 500 mA each and are short circuit protected using a UL rated silicon switch. The USB power switch contains circuitry to prevent dynamic attach inrush currents from causing spurious overcurrent faults for 1 ms after the hot attach event.

Note: If only two USB ports are desired, then the suggested approach is to use one port from each OHCI controller along with its associated PWREN output to achieve maximum throughput.

3.2.6 LPC Bus Support

The CS5535 contains a PCI-to-LPC bridge for all unclaimed PCI transactions. Support for LPC bus mastering devices is included in this design. The CS5535 LPC bus interface uses 3.3V.

3.2.7 COM Port or DDC Header

2-Wire Debug Communication Port Features:

- Software configurable I/O port addresses: 3F8h-3FFh, 2F8h-2FFh or 2E8h-2EFh.
- Software configurable hardware interrupt: IRQ3 or IRQ4.
- 3-pin header.
- Default I/O address: 3F8h.

DDC Header Features:

- Software configurable I/O port address of 3F8h-3FFh, 2F8h-2FFh or 2E8h-2EFh.
- Software configurable hardware interrupt: IRQ3 or IRQ4.
- 3-pin header.
- Default I/O address: 2F8h.

3.2.8 Power Button (Optional - not on schematic)

If a power button is to be used, the following must be considered: Any power button change must be at least two 32 KHz clocks (approximately 62 µs) in duration to be accurately detected.

3.2.9 IRQ Map

Table 3-2 shows the IRQ mapping of the CS5535.

Table 3-2. CS5535 IRQ Mapping

IRQ #	CS5535	Source Location
0	Timer	CS5535
1	USB/KEL Keyboard	CS5535
	Legacy Keyboard	LPC SIO
2	Slave PIC	CS5535
3	UART/IR COM2	CS5535
	COM4	LPC SIO
4	UART/IR COM1	CS5535
	COM3	LPC SIO
5	Audio	CS5535 AC97
	Legacy Parallel Port 2	LPC SIO
6	GPIO	CS5535 GPIO
	Legacy Floppy Controller	LPC SIO
7	NAND Flash Ready	CS5535
	NAND Flash Distraction	CS5535
	Legacy Parallel Port 1	LPC SIO
8	RTC (RTC Alarm IRQ)[1]	CS5535
9	USB Controller #1 HC Registers	CS5535 USB #1
	USB Controller #2 HC Registers	CS5535 USB #2
10	Power Management	CS5535 GPIO
	SMB Controller	CS5535
	KEL Emulation IRQ[2]	CS5535 KEL
11	PCI Slot	PCI device
	SW Generated	CS5535
	MFGPT	CS5535
12	USB Mouse	CS5535
	Legacy Mouse	LPC SIO
13	Numeric Coprocessor	GX2
14	IDE Channel	CS5535 ATA-5
15	Reserved	Reserved

1. Y[3] is the RTC alarm IRQ source.
2. Y[13] is the KEL emulation IRQ source. KEL ASMI is used for emulation service but an IRQ can be used optionally.

3.3 JTAG Interface

The GX2/CS5535 reference schematic uses one JTAG interface to connect to the GX2, CS5535, and PCI slot (optional) in a serial scan chain.

The IEEE 1149.1 JTAG port supports software debugging. The IDC header is a 2-row, 14-position (0.1” x 0.1” center-line) vertical mount. Table 3-3 lists the IDC header pin assignments.

A ribbon cable connects the FS2 to the JTAG controller box. All signals are LVTTL compatible (JEDEC standard JESD8-B), and referenced between V_{IO} (3.3V nominal, except TMS @2.5V) and GND.

Table 3-3. IDC Header Pin Assignments

Pin #	Signal Name	Description
1	GND	Ground
2	V_{IO}	TAP Controller Reference Voltage
3	GND	Ground
4	TCK	Test Clock
5	GND	Ground
6	TMS	Test Mode Set
7	GND	Ground
8	TDI	Test Data Input
9	GND	Ground
10	TDO	Test Data Output
11	DGB IN	Debug In
12	POR#	Power-On Reset
13	DBG OUT	Debug Out
14	GND	Ground

3.4 PCI Bus

The GX2 processor contains an internal master/slave PCI bus controller. The GX2 PCI I/O buffers support 3.3V PCI devices only, and are not 5.0V tolerant. Table 3-5 shows the PCI device numbering scheme used and the wiring of the PCI interrupt lines.

3.4.1 PCI Arbitration

The GX2 processor contains an internal PCI bus arbiter, supporting up to two external masters in addition to the CS5535 companion. The default GX2 arbitration is distributed as follows:

Internal	GX2 processor
Master 0	PCI slot
Master 1	Ethernet controller
Master 2	CS5535 companion

3.4.2 PCI Interrupt Routing

Table 3-4 shows the PCI INTx# to IRQ routing.

Table 3-4. PCI INTx# IRQ Mapping

Device	INTx#	IRQ
USB Controller 1	INTC#	9
USB Controller 2	INTD#	10
PCI Slot	INTB#	11
MacPHYTER	INTA#	15
Primary IDE	N/A	14

3.4.3 PCI Clocking

The PCI bus clock is selectable between 33 and 66 MHz. The ICS MK1491-09F clock generator guarantees a pin-to-pin skew between PCI clock outputs of no more than 500 ps (the cycle-to-cycle jitter is typically 250 ps). This leaves a PCI clock budget of 1.5 ns for all external effects (flight time skew, manufacturing tolerances, receiver threshold variation, jitter, and crosstalk). All clocks from the clock chip can be stopped by asserting the MK1491-09F PD# pin low.

Table 3-5. PCI Device Numbering Scheme and Interrupt Line Wiring

PCI Device Name	Vendor ID[1]	Device ID	Device Number	IDSEL Line	Function Number	IRQ Number	PCI Device or Function Type	Interrupt Line	
								Device	Bus
GX2	100Bh	0028h	01h	AD11[2]	0	---	Host PCI Bridge[3]	---	---
		0030h	16h		1	---	Graphics Controller[3]	---	---
PCI Slot	---	---	0Dh	AD23	---	11	---	INTA#	INTB#
								INTB#	INTC#
								INTC#	INTD#
								INTD#	INTA#
MacPHYTER (optional)	---	---	0Dh	AD24	---	11	Ethernet Controller	INTA#	INTA#
CS5535	100Bh	002Bh	0Fh	AD25	0	---	ISA Bridge[3]	---	---
		002Ch			1	---	Flash Controller[3]	---	---
		002Dh			2	14	IDE Controller[3]	---	---
		002Eh			3	---	Audio Controller[3]	---	---
		002Fh			4	9	USB Controller 1[3]	INTC#	N/A[4]
		002Fh			5	10	USB Controller 2[3]	INTD#	N/A

1. The PCI vendor ID for AMD is defined as 100Bh.
2. The GX2 PCI device number is internally fixed and cannot be changed.
3. The CS5535 PCI header is virtualized by VSA (Virtual System Architecture™) technology code in system memory.
4. The CS5535 USB interrupt is internally routed to PCI INTC# and INTD#.

3.5 AC97 Audio Codec

The LM4550 AC97 audio codec is a 16-bit stereo ΣΔ codec with full duplex capability, a hardware mixer, 2D spatial enhancement algorithm (SRS-like), and a stereo headphone amplifier (40 mW). The codec is driven by a 24.576 MHz clock source.

The master volume register is controlled by 32 steps of 1.5 dB each (0 dB to -46.5 dB).

Note: The PCM (Pulse Code Modulation) DACs must receive samples in left/right pairs to function correctly with the audio controller. In addition, the A/D converters must deliver samples in left/right pairs to function correctly with the audio controller.

The GX2/CS5535 reference schematic was modified to account for the following errata item for the CS5535 silicon revision A2:

After PCI$RESET is de-asserted, the AC97 software expects AUD$SDATA_OUT to be low to drive AUD$BITCLK to the CS5535, but the CS5535 drives this high. This is an intermittent problem. If AUD$SYNC is low and AUD$SDATA_OUT is high, the code assumes “ATE In-Circuit Test Mode”. Under this mode, all pins TRI-STATE and the codec output CLK$AUDBIT is not driven.

A multiplexor was added between the AUD$SDATA_OUT and AUD$SYNC outputs on the CS5535 and the LM4550 audio codec to allow the inputs to be driven low during reset. Allowances are made on the schematic (option resistors) for silicon revision A3 of the CS5535.

3.5.1 Line Input

The line input provides an externally accessible miniature 1/8” (3.5 mm) stereo jack to the AC97 codec. The line input level is 1 Vrms and the frequency response is 20 Hz to 20 KHz (-3 dB).

3.5.2 Microphone Input

The microphone input provides an externally accessible miniature 1/8” (3.5 mm) jack to a preamplifier circuit that provides 18 dB of gain. The AC97 codec microphone input has a selectable -34.5 to +12 dB gain stage. An additional internal 20 dB gain block is also available for lower output dynamic microphones. The microphone input features are:

- Supports three conductor electret microphones.
- Supports two conductor dynamic microphones.
- Provides bias power on the ring connection for electret microphones.
- Minimum bias of 2.0V at 0.8 mA load.
- Minimum bias impedance between bias voltage source and ring: 2 KΩ.
- Minimum input impedance between AC coupled tip and sleeve: 10 KΩ.
- Preamplifier with a typical gain of 18 dB.
- Frequency response of 60 Hz to 15 KHz (-3 dB).

3.5.3 CD Audio Input

The CD audio input provides an internally accessible 4-pin 100 MIL pitch vertical connector, compatible with the Sony standard. It has a differential input and a maximum input level of 2 Vrms.

3.5.4 Headphone Output

The headphone output provides an externally accessible miniature 1/8” (3.5 mm) stereo jack from an audio amplifier output for low impedance loads such as headphones. The headphone output is controlled by the master volume register (32 steps of 1.5 dB) and has shutdown and mute capability. The amplifier is enabled when both an external load is connected and the AC97 codec EAPD (External Amplifier Power Down) register is set to a logic 1.

The headphone output can also be used as a line output to line level devices. The major difference between the headphone output and a true line level output is that the line level output volume remains fixed at 1 Vrms while the headphone output volume can be adjusted. The headphone output features are:

- Maximum output power: 70 mWrms/channel (32Ω load).
- Power amplifier with a typical gain of 2.18 dB.
- Frequency response of 24 Hz to 20 kHz (-3 dB).
- Total harmonic distortion + noise (THD+N): < 0.02% (70 mWrms, 32Ω load, f = 1 KHz).
- Automatic shutdown when no load is attached (<100 µA).
- AC97 2.1 codec EAPD support.

3.6 Non-Volatile Memory

The GX2/CS5535 design supports bootROM and CompactFlash.

3.6.1 BootROM

The GX2/CS5535 design uses a 3.3V, 4-Mbit sector-erase SST FWH (Firmware Hub) from the LPC interface or CS5535 on-chip ROM. The GX2/CS5535 reference schematic provides a jumper option to select the bootROM, as shown in Table 3-6.

Off = V_{CC} /Jumper is not installed

On = GND/Jumper is installed

Table 3-6. BootROM Jumper Settings

Pins 1-2	Pins 3-4	Boot Device
On	On	LPC ROM on LPC Bus
Off	On	Reserved
On	Off	NOR Flash; Not supported in this design
Off	Off	Boot from FWH off LPC Bus

3.6.2 CompactFlash Interface

The GX2/CS5535 design supports CompactFlash connection to the IDE bus. However, only an IDE drive or CompactFlash interface can be used, not both simultaneously.

3.7 Power Management

An external 12V power supply provides input power to the GX2/CS5535 design. Secondary regulators provide the GX2 core and I/O voltages. Figure 3-2 depicts a block diagram of the GX2/CS5535 reference schematic power distribution.

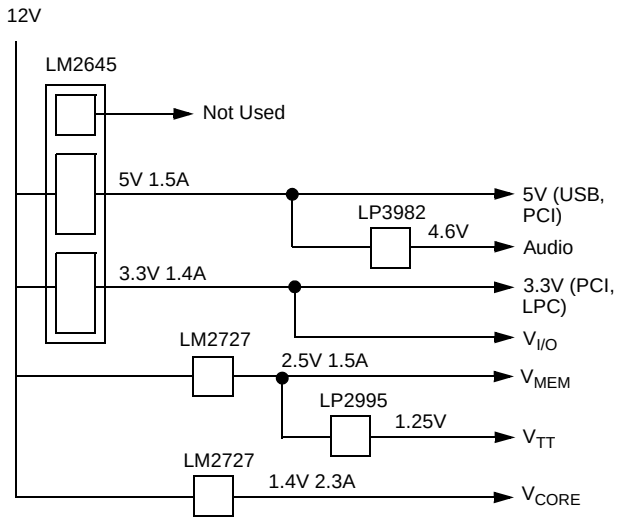


Figure 3-2. GX2/CS5535 Power Distribution

3.7.1 5.0V and 3.3V Generation

The National Semiconductor LM2645 advanced two-phase switching controller with two linear outputs generates 5.0V and 3.3V from a single input voltage.

3.7.2 GX2 and CS5535 Power Supply Specifications

The GX2/CS5535 design contains individual regulators for the GX2 and CS5535 core and I/O pins. Table 3-7 provides the V_{CORE} and $V_{I/O}$ power supply specifications.

- V_{CORE}: DC output of the V_{CORE} (1.4V) regulator. Used for GX2 and CS5535 core voltages.
- $V_{I/O}$: DC output of the I/O (3.3V) regulator. Used for GX2 and CS5535 I/O voltages.

Table 3-7. V_{CORE} and V_{IO} Specifications

Nominal Output Voltage	V_{CORE} (1.4V)	$V_{I/O}$ (3.3V)	Unit
Minimum Load	0	0	A
Maximum Load	2.3	1.4	A
Efficiency	Efficiency at full load is more than 85%.		

3.7.3 GX2 and CS5535 Power Supply

The National Semiconductor LM2727 current mode synchronous buck regulator generates the GX2 and CS5535 core voltage. The LM2727 is a voltage-mode, high-speed N-channel synchronous buck regulator controller that provides a power good flag, under/over-voltage protection, and an output-enable feature. The LM2727 can set the regulator output voltage down to 0.6V using a voltage divider on the feedback circuit. The nominal core voltage for the 0.15 process is 1.5V.

3.7.4 Memory I/O Power Supply Specifications

- The GX2/CS5535 design contains individual regulators for the memory I/O and termination voltage supplies. In accordance with the *Double Data Rate (DDR) SDRAM Specification*, memory I/O comes into regulation before V_{TT} begins to turn on.
- V_{MEM}: DC output of the V_{MEM} (2.5V) regulator. Used for GX2 and DDR memory voltage.
- V_{TT}: DC output of the V_{TT} (1.25V) regulator. Used for DDR memory termination voltage. It tracks one-half of V_{MEM}.

Table 3-8 provides the specifications for the memory power supplies.

Table 3-8. Memory I/O Power Supply Specs

Nominal Output Voltage	V_{MEM} (2.5V)	V_{TT} (1.25V)	Unit
Minimum Load	0	0	A
Maximum Load	1.5A	1.5A	A
Efficiency	Efficiency at full load is more than 85%.		

3.7.4.1 Memory I/O Power Supply

The LM2727 generates the GX2 and DDR DIMM memory voltage. The LM2727 can set the regulator output voltage down to 0.6V using a voltage divider on the feedback circuit. The nominal voltage is 2.5V when operating with DDR.

3.7.5 Memory Termination Voltage Supply

The National Semiconductor LP2995 DDR termination regulator meets the *Double Data Rate (DDR) SDRAM Specification* for termination of DDR SDRAM. It contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot-through while delivering a continuous 1.5A and transient peaks of up to 3A, as required for DDR SDRAM termination. The LP2995 also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output for the chipset and DDR DIMMS.

3.7.6 GX2 Thermal Management

The National Semiconductor LM82 thermal sensor is accessed by software through the ACCESS.bus port. If the GX2 gets warm, pin 11 of the LM82 generates an interrupt.

3.7.7 Reset Logic

The hard reset logic contains a reset switch and a JTAG port reset input.

3.7.8 Power Sequence

The GX2 reset input, LPC and PCI buses are driven by the CS5535 PCIRST# output. The power sequence is:

1) +12V from the wall jack supply
2) +5V
3) 3.3V (V_{IO}), V_{CORE}
4) V_{MEM}
5) V_{TT}/V_{REF}

3.8 Connectors and Switches

Tables in this subsection discuss the connectors, headers, switches, indicators, and no-load/option resistors and capacitors in the GX2/CS5535 design.

Table 3-9. Standard Connectors

Jumper #	Function
J2	VGA Analog Monitor
J3	Memory DDR DIMM 0
J4	Memory DDR DIMM 1
J7	5V IDE
J8	33 or 66 MHz 3.3V PCI Slot
J10	First Two USB Ports
J11	Second Two USB Ports
J12	AUX_IN
J13	CD_IN
J14	Headphone_OUT
J15	LINE_IN
J16	MIC_IN
JDCIN1	+12V Input Jack
JCF1	CompactFlash
J17	Ethernet
J18	PS2 Keyboard
J19	Parallel Port
J20	PS2 Mouse
J21	LPC Serial Port
J22	Floppy
J23	LPC Serial Port

Table 3-10. Headers

Header #	Function
J1	FS2 JTAG Header
J5	Battery Header
J6	Serial Debug Header
J9	Bootstrap Option Header

Table 3-11. Switches and Indicators

Switches/ Indicators	Function
CR1	IDE DMA Indicator
CR2	IDE Active Indicator
SP1	PC Beep Speaker
SW1	Sleep Button
SW2	Reset Button
D27	Ethernet Activity Indicator
D29	10 Mb/s Ethernet Indicator
D30	100 Mb/s Ethernet Indicator

Table 3-12. No-Load/Option Resistors and Capacitors

Component	Function
R5	Isolates the LM82 from CS5535.
R43, R52	Adds PCI header to JTAG chain. R42 must be removed.
R54, R55	Required if PCI slot is added to SMBus.
R79, R87	Used for SST/Intel FWH differences.
R64	Used for 66 MHz PCI bus operation. R70 must be removed.
R60, R61	Enables Spread Spectrum (EMI reduction).
R177, R178	Pull-up/down VS1 on the CompactFlash connector.
R180	Pull-up IRQ14 for CompactFlash.
R199	Pull-down on MD1 DP83816.
R208, R209	Three-mode floppy support.
R210, R211	For use with CS5535 silicon revision A3.
R215, R216, R217	For support of additional future speed SKUs.
R218	Not required after the CS5535 achieves UL approval.
C278, C292	Additional 12V inrush capacitance, if needed.
C361	Between TPTDP and TPTDM on DP83816.
C362	On IAUXVDD on DP83816.
C363	On CT of Ethernet Transformer (T2).

4.0 Software Components

The following subsections discuss the software components necessary for platform development.

4.1 ACCESS.bus Devices

Several ACCESS.bus devices, accessed by ‘bit banging’ CS5535 GPIO pins 14 (SCL) and 15 (SDA), are listed below:

- DDR DIMM module 1 SPD EEPROM:
  — ACCESS.bus address A0h-A1h
- DDR DIMM module 2 SPD EEPROM:
  — ACCESS.bus address A2h-A3h
- Thermal sensor:
  — ACCESS.bus address 98h-99h

4.2 GPIO List

Table 4-1 describes the GPIO usage in the GX2/CS5535 design.

Table 4-1. GPIO Signal Descriptions

CS5535	Function	Signal Name	Description
GPIO0	PCI_INTA#	PCI$INTA*	**PCI Interrupt A#.**
GPIO1	PC_BEEP	AUD$PCBEEP	**Audio Beep.**
GPIO2	IRQ14	IDE$IRQ14R	**IDE Channel IRQ14.**
GPIO3	DDC_SCL	VGA$DDC_SCL	**DDC Channel Clock to External Monitor.** Option to use as UART2_RX.
GPIO4	DDC_SDA	VGA$DDC_SDA	**DDC Channel Data to External Monitor.** Option to use as UART2_TX.
GPIO5	MFGPT0	CF$PRESENT	**CompactFlash Presence Indicator.** Option to use as GPIO, if CompactFlash is not required.
GPIO6	MFGPT1	NC	**Available GPIO.**
GPIO7	INTB#	PCI$INTB*	**PCI Interrupt B#.**
GPIO8	UART1_TX	5535$UART_TX	**UART Transmit.** Option to use as UART1_TX for FIR/MIR IP development.
GPIO9	UART1_RX	5535$UART_RX	**UART Receive.** Option to use as UART1_TX for FIR/MIR IP development.
GPIO10	THRM_ALRM#	LM82$INT*	**Thermal Alarm.** This pin defaults to the input state. This signal is driven low by the LM82 thermal sensor when either the CPU or ambient temperature has exceeded its critical set point. This signal releases after the status has been read and the temperature has fallen below the programmed set point. Option to use as GPIO if LM82 is not required.
GPIO11	SLP_CLK#	5535$CLK_DISP*	**Sleep Clock Output.** This signal is connected to the PD# pin on the clock source, and is used to turn off the output clocks.
GPIO12	INTR_OUT	PCI$INTC*	**PCI Interrupt C#.**
GPIO13	SMI#	PCI$INTD*	**PCI Interrupt D#.**
GPIO14	SM_SCL	SMB$SCL	**System Management Clock.**
GPIO15	SM_SDA	SMB$SDA	**System Management Data.**
GPIO16	LAD0	LPC$AD[0]	**LPC Multiplexed Address and Data[0].**
GPIO17	LAD1	LPC$AD[1]	**LPC Multiplexed Address and Data[1].**
GPIO18	LAD2	LPC$AD[2]	**LPC Multiplexed Address and Data[2].**
GPIO19	LAD3	LPC$AD[3]	**LPC Multiplexed Address and Data[3].**
GPIO20	LDRQ#	LPC$DRQ*	**LPC DMA/Bus Master Request.**
GPIO21	SERIRQ#	LPC$SERIRQ	**LPC Serialized IRQ.**
GPIO22	LFRAME#	LPC$FRAMEN*	**LPC Frame.** Start a New LPC Cycle.
GPIO23	None	None	**Does Not Exist.**
GPIO24	WORK_AUX	Pulled High	**Not Used; Pulled high.**
GPIO25	LOW_BAT#	FP$SLPBUT*	**Low Battery Input.** This signal should be configured as an input and set up to create an SMI# upon detection of a falling edge. This signal is driven low upon assertion of a front panel SMI request, at which time the CS5535 pulls the 5535$SMI* low, causing the system to go into SMI mode.
GPIO26	PME#	PCI$PME*	**Power Management Event Input.** This pin defaults to the input state and is set up to create an SMI# upon detection of a falling edge. This signal is pulled low by a PCI device to indicate a pending power management event.
GPIO27	MFGPT7	No Connect	**Not Used; Pulled high.**
GPIO28	PWR_BUT	Tied Low	**Not Used; Tied low.**

Appendix A Support Documentation

A.1 Related Documents

Additional device information can be found in the following documents (revision numbers are as of this printing):

- *Double Data Rate (DDR) SDRAM Specification*, Release 1, June 2000, JEDEC Solid State Technology Association
- *PC SDRAM Serial Presence Detect (SPD) Specification*, Revision 1.2B, November 1999, Intel Corporation
- *PCI Local Bus Specification*, Revision 2.2, December 1998, PCI Special Interest Group
- *PCI LPC Bus Specification, LPC Interface Specification*, Revision 1.01 February 1999, PCI Special Interest Group
- *AMD Geode™ GX2 Processor Data Book*
- *AMD Geode™ GX2 Processor/CS5535 Companion Device Layout Recommendations*

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