AMD Geode™ GX1 Processor Memory Timings for Maximum Performance

1.0 Scope

There are many variables and trade-offs that the system designer must consider to achieve maximum memory performance in a design. This document provides memory timings and the factors affecting them for systems based on the AMD Geode™ GX1 processor.

In addition to this document, the system designer should also refer to the application note *AMD Geode™ GX1 Processor PC133 Layout Recommendations* for recommended layout methodologies and guidelines. Following those guidelines is of utmost importance for designs supporting processor core and memory speeds of 300/100 MHz and 333/111 MHz. Designers who do not follow those recommendations are at high risk of producing an unstable motherboard, with the only corrective action being a redesign.

Note: This is revision 4.0 of this document. The change made from revision 3.0 (dated September 2000) is the additional timings and data to support a GX1 333 MHz based system with a memory speed of 111 MHz.

2.0 Discussion

The GX1 processor has a very flexible memory architecture in that it can be configured to support many different SDRAM clock frequencies and timing parameters. Timing parameters can vary between memory devices, even within the PC100 and PC133 specifications. Consequently, there are several variables to consider in order to achieve maximum memory performance. For any given core speed, it is important for the BIOS to set the optimum memory settings based upon the memory devices being used.

2.1 Validation Testing

The AMD Geode™ SP4GX10 (GX1/CS5530A-based) system platform was used to validate the memory subsystem. Proper power supply design and sufficient decoupling of the GX1 processor is of extreme importance in the system design. That is why the SP4GX10 was used for validation. It is designed with proportionate power and decoupling margin.

2.2 SDRAM Clock Considerations

The SDRAM clocks generated by the GX1 processor are not perfectly periodic; some clock periods can be slightly longer and others slightly shorter. The memory settings must account for these shorter periods. This jitter is the reason for requiring PC133 memory devices for speeds of 90 MHz and higher.

2.2.1 Loading Restrictions Between 78 and 100 MHz

To support speeds between 78 and 100 MHz, loading must be restricted to a maximum of 16 devices. There are four SDRAM clocks generated by the GX1, each of which must be restricted to a maximum of four loads each, to support speeds over 78 MHz. These 16 loads can take the form of one DIMM, two SODIMMs, or discrete memory. Total memory achieved by 16 devices is a function of the SDRAM technology used.

2.2.2 Loading Restrictions at 111 MHz

To support the 111 MHz speed, loading must be further restricted to a maximum of eight devices. These eight loads can take the form of one SODIMM, or discrete memory. Total memory achieved by eight devices is a function of the SDRAM technology used. The four SDRAM clocks generated by the GX1 should be restricted to a maximum of two loads. For the SODIMM, this requirement can be met by connecting SDCLK0 to SDCLK1 and SDCLK2 to SDCLK3 as close to the processor as possible. It should be noted that the SP4GX10 platform (used to validate this configuration) did not meet the clock loading requirement.

2.2.3 SDCLK_OUT to SDCLK_IN Length

The application note titled *AMD Geode™ GX1 Processor PC 133 Layout Recommendations* describes the SDCLK_OUT to SDCLK_IN length to have three selectable loop lengths. Testing on the SP4GX10 platform indicates the shortest loop to be the best setting for the 333 MHz memory configuration. All other configurations should use the large loop.

2.3 Memory Speed and Timing

Three registers are used for programming memory speed and timing (see Table A-2 on page 7 for bit definitions):

- MC_MEM_CNTRL1: Sets the appropriate clock divisor and buffer strength settings for the associated speeds.
- MC_MEM_CNTRL2: Sets the appropriate values for Shift Clock and Read Data Phase. (Shift Clock is the setting used to maximize setup and hold margins and is discussed in detail in Section 2.5 on page 6.)
- MC_SYNC_TIM1: Sets the memory timing: CL, tRC, tRAS, tRP, tRCD, tRRD, tDPL

2.3.1 Memory Speed Parameters

MC_MEM_CNTRL1 and MC_MEM_CNTL2 are used for programming memory speed. Table 2-1 shows the settings for these registers based upon the memory device used and core speed.

2.3.2 Memory Timing Parameters

The MC_SYNC_TIM1 register is used for programming the memory timing. The timing parameters are programmed in the first five nibbles of MC_SYNC_TIM1 and significantly affect memory performance; in particular CL and tRCD:

- CL – CAS Latency
- tRC – RAS Cycle Time
- tRAS – RAS Active Time
- tRP – RAS Precharge Time
- tRCD – RAS to CAS Delay

For the purpose of this application note, the memory timings have been divided into two categories: Validated (Table 2-2 on page 3) and Aggressive (Table 2-3 on page 3). The CL, tRC, tRAS, tRP, and tRCD parameters for the aggressive timings are set according to Table 2-4 on page 3, plus a 12% clock period margin to account for clock jitter. This SDCLK jitter has been observed on actual systems. To keep the jitter within this 12%; the incrementor bit in the configuration register PCR1 must be enabled (i.e., (Index F0h[1] = 1). The correct incrementor margin must also be set for the processor speed in PCR0 (i.e., Index 20h[2,0] = 1,0 for 200-266 MHz and 1,1 for 300-333 MHz). It should be noted that the minimum clock period for SDCLK, specified in the GX1 data book, is a conservative 15% clock period margin. This means that the validated memory timings between 85 and 88 MHz are technically out of spec when using PC100 SDRAMS. Designers that are uncomfortable with that aspect should use faster SDRAMs for those configurations. The aggressive timings have not been thoroughly tested. If stability problems are encountered, it is recommended that the validated timings be used in order to debug and evaluate the individual parameters.

Table 2-1. Supported Memory Speeds

CPU Core Speed (MHz)	SDCLK Divisor	SDCLK Speed (MHz)	GX_BASE+Memory Offset xxh		Memory Speed Required	Max Load (Devices)
			Offset 8400h: MC_MEM_CNTRL1	Offset 8404h: MC_MEM_CNTRL2		
200	3.0	66.7	B68E310Ch	00000018h	PC100	32
233	3.0	77.7	B68E390Ch	00000018h	PC100	32
233	3.5	66.7	B692390Ch	0000001Ah	PC100	32
266	3.0	88.7	B68E3F0Ch	0000001Ah	PC100	16
266	3.5	76.0	B6923F0Ch	0000001Ah	PC100	32
266	4.0	66.7	B6963F0Ch	0000001Ah	PC100	32
300	3.0	100.0	B68E470Ch	00000012h	PC133	16
300	3.5	85.7	B692470Ch	0000001Ah	PC100	16
300	4.0	75.0	B696470Ch	0000001Ah	PC100	32
300	4.5	66.7	B69A470Ch	00000022h	PC100	32
333	3.0	111	B68E4F0C	00000018	PC133	8
333	4.0	83.3	B696470C	00000018	PC100	16

Table 2-2. Validated Memory Timings

CPU Core Speed (MHz)	SDCLK Divisor	SDCLK Speed (MHz)	GX_BASE+Memory Offset 840Ch: MC_SYNC_TIM1	Memory Speed Required	Max Load (Devices)	(CLKs)				
						CL	tRC	tRAS	tRP	tRCD
200	3.0	66.7	26422125h	PC100	32	2	7	5	2	2
233	3.0	77.7	37533125h	PC100	32	3	8	6	3	3
233	3.5	66.7	26422125h	PC100	32	2	7	5	2	2
266	3.0	88.7	37533125h	PC100	16	3	8	6	3	3
266	3.5	76.0	37533125h	PC100	32	3	8	6	3	3
266	4.0	66.7	26422125h	PC100	32	2	7	5	2	2
300	3.0	100.0	38633125h	PC133	16	3	9	7	3	3
300	3.5	85.7	38633125h	PC100	16	3	9	7	3	3
300	4.0	75.0	37533125h	PC100	32	3	8	6	3	3
300	4.5	66.7	26422125h	PC100	32	2	7	5	2	2
333	3.0	111	38633125	PC133	8	3	9	7	3	3
333	4.0	83.3	38633125	PC100	16	3	9	7	3	3

Table 2-3. Aggressive Memory Timings

CPU Core Speed (MHz)	SDCLK Divisor	SDCLK Speed (MHz)	GX_BASE+Memory Offset 840Ch: MC_SYNC_TIM1	Memory Speed Required	Max Load (Devices)	(CLKs)				
						CL	tRC	tRAS	tRP	tRCD
200	3.0	66.7	25322125	PC100	32	2	5	4	2	2
233	3.0	77.7	35422125	PC100	32	3	6	5	2	2
233	3.5	66.7	34322125	PC100	32	3	5	4	2	2
266	3.0	88.7	36433125	PC100	16	3	7	5	3	3
266	3.5	76.0	25422125	PC100	32	2	6	5	2	2
266	4.0	66.7	24322125	PC100	32	2	5	4	2	2
300	3.0	100.0	36433125	PC133	16	3	7	5	3	3
300	3.5	85.7	26422125	PC100	16	2	7	5	2	2
300	4.0	75.0	25322125	PC100	32	2	6	4	2	2
300	4.5	66.7	24322125	PC100	32	2	5	4	2	2
333	3.0	111	36433125	PC133	8	3	7	5	3	3
333	4.0	83.3	26422125	PC100	16	2	7	5	2	2

Table 2-4. PC100/PC133 Specification Assumptions

Specification	CL (CLKs)	tRC (ns)	tRAS (ns)	tRP (ns)	tRCD (ns)
PC100	2 or 3	70.0	50	20	20
PC133	2 or 3	67.5	45	20	20

2.3.3 Factors Affecting Memory Timings

Note that within the PC100 and PC133 specifications, the timing values can vary and be vendor specific. In order to verify these parameters, the BIOS should read them directly from the Serial Presence Detect (SPD) of the DIMM/SODIMM, if applicable, or from the SDRAM data specifications.

It is common for CL2 and CL3 to have different specifications including minimum clock period, tCLK. A PC133 DIMM might support CL2 at tCLK = 10 ns, and CL3 at tCLK = 7.5 ns. Therefore, at 111 MHz the memory should not be configured for CL2 because of the clock jitter. In the case of 111 MHz, tCLK must be 8 ns or less to remain in spec.

As noted in Section 2.4 on page 5, CL has an important impact on performance. A designer looking to maximize system performance by running at 333/111 MHz should design with memory that supports CL2, which requires a minimum tCLK of 7.5 ns at CL2. tCLK is specified in the SPD separately for all supported CAS Latencies.

The PC133 specification has an aggressive set of timing goals for CL, tRC, tRP, and tRCD that provide increased performance if supported by the memory. The values in Table 2-5 are the fastest supported timing goals for PC133. For memory that meets these faster timings, tighter settings can be used that previously only supported CL = 3 CLKs (see Table 2-6).

Table 2-5. Fastest Supported Goal for PC133

Specification	CL (CLKs)	tRC (ns)	tRAS (ns)	tRP (ns)	tRCD (ns)
PC133	2	60	45	15	15

Table 2-6. Fast PC133 Settings

CPU Core Speed (MHz)	SDCLK Divisor	SDCLK Speed (MHz)	GX_BASE+Memory Offset 840Ch: MC_SYNC_TIM1	Max Load (Devices)	(CLKs)				
					CL	tRC	tRAS	tRP	tRCD
233	2.5	93.2	25422125	16	2	6	5	2	2
266	3.0	88.7	25422125	16	2	6	5	2	2
300	3.0	100.0	25422125	16	2	6	5	2	2
333	3.0	111	25422125	8	2	6	5	2	2

2.4 Timing Parameter Impact on Performance

CAS Latency (CL) significantly impacts memory performance. Faster SDRAM clock speed does not always correlate to faster memory performance if CL is increased to three clocks. Table 2-7 through Table 2-9 highlight the impact of CL on performance. The performance values in Table 2-7 indicate memory accesses per time, but do not have specific units. The higher the number, the better the performance. These results indicate that a 300/85.7 MHz system with CL2 out-performs 300/100 MHz with CL3 for certain memory accesses. Therefore, it is important to understand the impact of the speed ratings of the memory that is used in order to maximize system performance.

The results of the system benchmark in Table 2-8 further demonstrate the importance of CL on performance. Higher scores indicate better performance. Timing parameters are in SDRAM clocks.

Table 2-9 shows the effect that the individual parameters have on performance with core, divisor, and SDRAM held constant. Although CL has the greatest impact, optimizing the other values is also important, especially tRCD.

Table 2-7. Impact of CL on Performance

CPU Core Speed (MHz)	SDCLK Divisor	SDCLK Speed (MHz)	Performance
CAS Latency = 3			
300	3.0	100.0	483
300	3.5	85.7	469
CAS Latency = 2			
300	3.0	100.0	586
300	3.5	85.7	549

Table 2-8. WinTach Results

CPU Core Speed (MHz)	SDCLK Divisor	SDCLK Speed (MHz)	(CLKs)					Score
			CL	tRC	tRAS	tRP	tRCD	
300	3.0	100.0	3	6	4	3	3	194
300	3.5	85.7	2	5	4	2	2	190
266	3.0	88.7	2	5	4	2	2	175

Table 2-9. WinTach Results

CPU Core Speed (MHz)	SDCLK Divisor	SDCLK Speed (MHz)	(CLKs)					Score
			CL	tRC	tRAS	tRP	tRCD	
300	3.0	100.0	3	7	5	3	3	188
300	3.0	100.0	3	6	4	3	3	194
300	3.0	100.0	3	6	4	2	2	201
300	3.0	100.0	2	6	4	3	3	204
300	3.0	100.0	2	6	4	2	2	211

2.5 Shift Clock Tuning

In order to maximize timing margin, the SDRAM clock can be tuned per design to provide the optimum setup and hold timings at the SDRAM. The shift value timings in this application note are optimized for the SP4GX10 development platform.

The shift clock values in this note should not need modification, however, it would be prudent to verify the timing for any given design and loading, especially at higher speeds. A simple way to do this is to measure the setup and hold time of a memory address line on the SDRAM in relation to SDCLK and if they are in spec, do not change them. Input setup and hold times are shown in Table 2-10 for PC66, PC100, and PC133 ratings.

Table 2-10. Input Setup and Hold Times

Parameter	PC66 (ns)	PC100 (ns)	PC133 (ns)
Input Setup Min	3.0	2.0	1.5
Input Hold Min	1.5	1.0	0.8

3.0 Summary

Guidelines to adhere to when designing for maximum memory performance are summarized below.

1) Memory must be rated 10% higher than the speed of the SDRAM clock to account for clock jitter. For example, 300/100 MHz must use PC133 rated memory to meet timings.

2) The loading, or amount of devices, that can be supported affects the speed at which the SDRAMs operate reliably in the system. Lightly loaded systems can be tuned to run faster. For speeds between 78 and 100 MHz, clock loading must be restricted to four or less loads per clock, for a maximum of 16 devices. For the 111 MHz speed, loading is restricted to eight devices.

3) SDRAM clock lengths must all have the same length ±0.25 inches and be matched to the distance of the SDCLK_IN trace. The memory bus should be as short as possible and placed as close to the GX1 processor as possible.

4) Choosing optimum timing parameters is important for maximizing memory performance. Memory that can support a CAS Latency of 2 impacts performance as much as a notch up in SDRAM clock speed.

Appendix A Support Documentation

The bit formats for registers referenced in this document pertaining to programming incrementor margin and memory speed/timing are provided in the tables that follow.

Table A-1. Incrementor Related Register Bits

Bit	Name	Description
Index 20h		**PCR0: Performance Control 0 Register (R/W)** **Default Value = 07h**
2	INC_MGN1	**Incrementor Margin 1:** 00 = Least margin 01 to 10 = Increasing margin 11 = Most margin The first bit is represented by Index 20h bit 2 and the second bit is represented by Index 20h bit 0.
0	INC_MGN0	**Incrementor Margin 0:** 00 - Least margin 01 to 10 - Increasing margin 11 - Most margin The first bit is represented by Index 20h bit 2 and the second bit is represented by Index 20h bit 0.
Note: MAPEN (CCR3[4]) must = 1 to read or write this register.		
Index F0h		**PCR1: Performance Control 1 Register** **Default Value = 01h**
1	INC	**Incrementor:** 0 = Disable; 1 = Enable.

Table A-2. Memory Controller Speed and Timing Related Registers

Bit	Name	Description
GX_BASE+ 8400h-8403h		**MC_MEM_CNTRL1 (R/W)** **Default Value = 248C0040h**
31:29	RSVD	**Reserved**
28:26	RSVD	**Reserved**
25:23	RSVD	**Reserved**
22	RSVD	**Reserved:** Set to 0.
21	RSVD	**Reserved:** Must be set to 0. Wait state on the X-Bus x_data during read cycles - for debug only.
20:18	SDCLKRATE	**SDRAM Clock Ratio:** Selects SDRAM clock ratio: 000 = Reserved 001 = ÷ 2 010 = ÷ 2.5 011 = ÷ 3 (Default) 100 = ÷ 3.5 101 = ÷ 4 110 = ÷ 4.5 111 = ÷ 5 Ratio does not take effect until the SDCLKSTRT bit (bit 17 of this register) transitions from 0 to 1.
17	SDCLKSTRT	**Start SDCLK:** Start operating SDCLK using the new ratio and shift value (selected in bits [20:18] of this register): 0 = Clear; 1 = Enable. This bit must transition from 0 (written to zero) to 1 (written to one) in order to start SDCLK or to change the shift value.
16:8	RFSHRATE	**Refresh Interval:** This field determines the number of processor core clocks multiplied by 64 between refresh cycles to the DRAM. By default, the refresh interval is 00h. Refresh is turned off by default.
7:6	RFSHSTAG	**Refresh Staggering:** This field determines number of clocks between the RFSH commands to each of the four banks during refresh cycles: 00 = 0 SDRAM clocks 01 = 1 SDRAM clocks (Default) 10 = 2 SDRAM clocks 11 = 4 SDRAM clocks Staggering is used to help reduce power spikes during refresh by refreshing one bank at a time. If only one bank is installed, this field must be set to 00.

Table A-2. Memory Controller Speed and Timing Related Registers (Continued)

Bit	Name	Description
5	2CLKADDR	**Two Clock Address Setup:** Assert memory address for one extra clock before CS# is asserted: 0 = Disable; 1 = Enable. This can be used to compensate for address setup at high frequencies and/or high loads.
4	RFSHTST	**Test Refresh:** This bit, when set high, generates a refresh request. This bit is only used for testing purposes.
3	XBUSARB	**X-Bus Round Robin:** When enabled, processor, graphics pipeline and non-critical display controller requests are arbitrated at the same priority level. When disabled, processor requests are arbitrated at a higher priority level. High priority display controller requests always have the highest arbitration priority: 0 = Enable; 1 = Disable.
2	SMM_MAP	**SMM Region Mapping:** Map the SMM memory region at GX_BASE+400000 to physical address A0000 to BFFFF in SDRAM: 0 = Disable; 1 = Enable.
1	RSVD	**Reserved:** Set to 0.
0	SDRAMPRG	**Program SDRAM:** When this bit is set, the memory controller will program the SDRAM MRS register using LTMODE in MC_SYNC_TIM1. This bit must transition from zero (written to zero) to one (written to one) in order to program the SDRAM devices.
GX_BASE+8404h-8407h		**MC_MEM_CNTRL2 (R/W)** **Default Value = 00000801h**
31:14	RSVD	**Reserved:** Set to 0.
13:11	RSVD	**Reserved**
10	SDCLKOMSK#	**Enable SDCLK_OUT:** Turn on the output. 0 = Enable; 1 = Disable.
9	SDCLK3MSK#	**Enable SDCLK3:** Turn on the output. 0 = Enable; 1 = Disable.
8	SDCLK2MSK#	**Enable SDCLK2:** Turn on the output. 0 = Enable; 1 = Disable.
7	SDCLK1MSK#	**Enable SDCLK1:** Turn on the output. 0 = Enable; 1 = Disable.
6	SDCLK0MSK#	**Enable SDCLK0:** Turn on the output. 0 = Enable; 1 = Disable.
5:3	SHFTSDCLK	**Shift SDCLK:** This function allows shifting SDCLK to meet SDRAM setup and hold time requirements. The shift function will not take effect until the SDCLKSTRT bit (bit 17 of MC_MEM_CNTRL1) transitions from 0 to 1: 000 = No shift 001 = Shift 0.5 core clock 010 = Shift 1 core clock 011 = Shift 1.5 core clock 100 = Shift 2 core clocks 101 = Shift 2.5 core clocks 110 = Shift 3 core clocks 111 = Reserved
2	RSVD	**Reserved:** Set to 0.
1	RD	**Read Data Phase:** Selects if read data is latched one or two core clock after the rising edge of SDCLK: 0 = 1 core clock; 1 = 2 core clocks.
0	FSTRDMSK	**Fast Read Mask:** Do not allow core reads to bypass the request FIFO: 0 = Disable; 1 = Enable.

Table A-2. Memory Controller Speed and Timing Related Registers (Continued)

Bit	Name	Description
GX_BASE+840Ch-840Fh		**MC_SYNC_TIM1 (R/W)** **Default Value = 2A733225h**
31	RSVD	**Reserved:** Set to 0.
30:28	LTMODE	**CAS Latency (LTMODE):** CAS latency is the delay, in SDRAM clock cycles, between the registration of a read command and the availability of the first piece of output data. This parameter significantly affects system performance. Optimal setting should be used. If DIMMs are used BIOS can interrogate EEPROM across the I2C interface to determine this value: 000 = Reserved 010 = 2 CLKs 100 = 4 CLKs 110 = 6 CLKs 001 = Reserved 011 = 3 CLKs 101 = 5 CLKs 111 = 7 CLKs This field will not take effect until SDRAMPRG (bit 0 of MC_MEM_CNTRL1) transitions from 0 to 1.
27:24	RC	**RFSH to RFSH/ACT Command Period (tRC):** Minimum number of SDRAM clocks between RFSH and RFSH/ACT commands: 0000 = Reserved 0100 = 5 CLKs 1000 = 9 CLKs 1100 = 13 CLKs 0001 = 2 CLKs 0101 = 6 CLKs 1001 = 10 CLKs 1101 = 14 CLKs 0010 = 3 CLKs 0110 = 7 CLKs 1010 = 11 CLKs 1110 = 15 CLKs 0011 = 4 CLKs 0111 = 8 CLKs 1011 = 12 CLKs 1111 = 16 CLKs
23:20	RAS	**ACT to PRE Command Period (tRAS):** Minimum number of SDRAM clocks between ACT and PRE commands: 0000 = Reserved 0100 = 5 CLKs 1000 = 9 CLKs 1100 = 13 CLKs 0001 = 2 CLKs 0101 = 6 CLKs 1001 = 10 CLKs 1101 = 14 CLKs 0010 = 3 CLKs 0110 = 7 CLKs 1010 = 11 CLKs 1110 = 15 CLKs 0011 = 4 CLKs 0111 = 8 CLKs 1011 = 12 CLKs 1111 = 16 CLKs
19	RSVD	**Reserved:** Set to 0.
18:16	RP	**PRE to ACT Command Period (tRP):** Minimum number of SDRAM clocks between PRE and ACT commands: 000 = Reserved 010 = 2 CLKs 100 = 4 CLKs 110 = 6 CLKs 001 = 1 CLK 011 = 3 CLKs 101 = 5 CLKs 111 = 7 CLKs
15	RSVD	**Reserved:** Set to 0.
14:12	RCD	**Delay Time ACT to READ/WRITE Command (tRCD):** Minimum number of SDRAM clocks between ACT and READ/WRITE commands. This parameter significantly affects system performance. Optimal setting should be used: 000 = Reserved 010 = 2 CLKs 100 = 4 CLKs 110 = 6 CLKs 001 = 1 CLK 011 = 3 CLKs 101 = 5 CLKs 111 = 7 CLKs
11	RSVD	**Reserved:** Set to 0.
10:8	RRD	**ACT(0) to ACT(1) Command Period (tRRD):** Minimum number of SDRAM clocks between ACT and ACT command to two different component banks within the same module bank. The memory controller does not perform back-to-back Activate commands to two different component banks without a READ or WRITE command between them. Hence, this field should be set to 001.
7	RSVD	**Reserved:** Set to 0.
6:4	DPL	**Data-in to PRE Command Period (tDPL):** Minimum number of SDRAM clocks from the time the last write datum is sampled till the bank is precharged: 000 = Reserved 010 = 2 CLKs 100 = 4 CLKs 110 = 6 CLKs 001 = 1 CLK 011 = 3 CLKs 101 = 5 CLKs 111 = 7 CLKs
3:0	RSVD	**Reserved:** Leave unchanged. Always returns a 101h.
Note: Refer to the SDRAM manufacturer's specification for more information on component banks.		

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