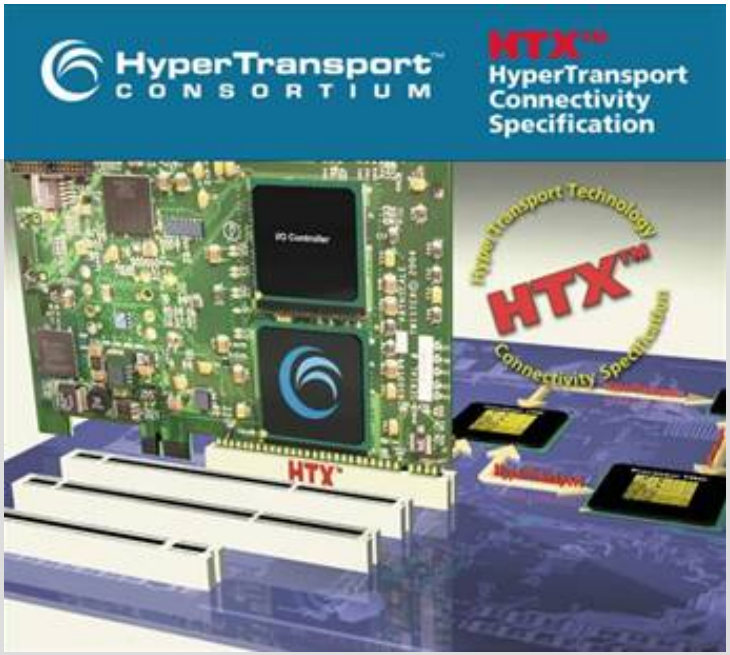
HTX™ - PCI Express Compared



How and Why HyperTransport HTX Proves Best Choice for Compute-Intensive Applications

HTX™ Delivers the Extra Performance that PCI-Class Interconnects Cannot Deliver

Compute-Intensive Applications Expect Best Architectural and Transactional Efficiency from Interconnect Technologies

HTX™

Best-in-Class Slot Connector Interfaces such as HTX and HTX3 are Designed for Lowest Latency, Highest Bandwidth. They are Best Choice for Compute-Intensive Processing and Coprocessing Applications

PCI EXPRESS®

General Purpose Slot Connector Interfaces such as PCI Express are Designed for Wide End-User Configurability and are Best Choice for Latency-Insensitive Peripheral and I/O Applications

Latency is The HPC Market Driver

Peak computing power is no longer the metric to consider

Feeding processing units with data is the real concern, and flow control dependencies in applications make latency the key performance metric

Prof. Jose Duato
Polytechnic Univ. of Valencia, Spain (*)

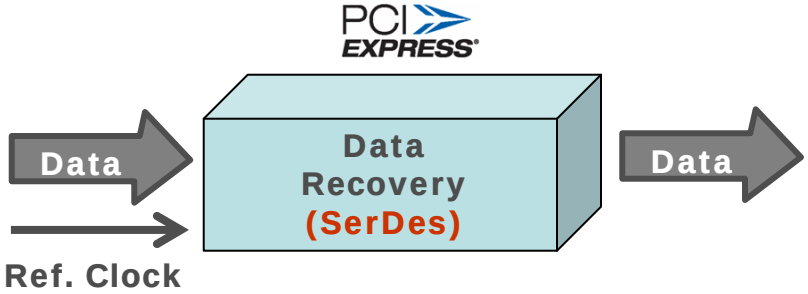
HTX Has Been and Continues to Be The Lowest Latency Slot Interface in Industry

(*) Jose Duato is Professor of Computer Science at the Polytechnic University of Valencia, Spain and a world authority in high performance computing (HPC). Prof. Duato has directly contributed to some of the computer industry's most advanced HPC product developments by companies like Compaq, Cray, IBM and Sun Microsystems. In 2006 Prof. Duato received Spain's most prestigious technology achievement award from Queen Sophia of Spain. Dr. Duato is an active contributor to Hypertransport technology and the HyperTransport Consortium.

Multiple Latency Advantages

Advantage 1: Physical Layer Efficiency

- 1 Clock Lane per x8 Link
- 3 Sideband Lanes (x2 through x32)
- No 8B / 10B Conversion Overhead
  (No SerDes)
- Lower Power Consumption
  (No SerDes)



- 1 Reference Clock Lane
- 4 Sideband Lanes (x1 through x32)
- 8B / 10B Conversion Overhead
  (SerDes)
- Higher Power Consumption
  (SerDes)

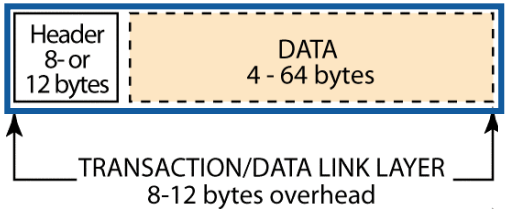
HTX Offers 20% Better Physical Layer Bandwith and Latency

Multiple Latency Advantages
Advantage 2: Leaner Protocol

HTX™

High-Performance Protocol

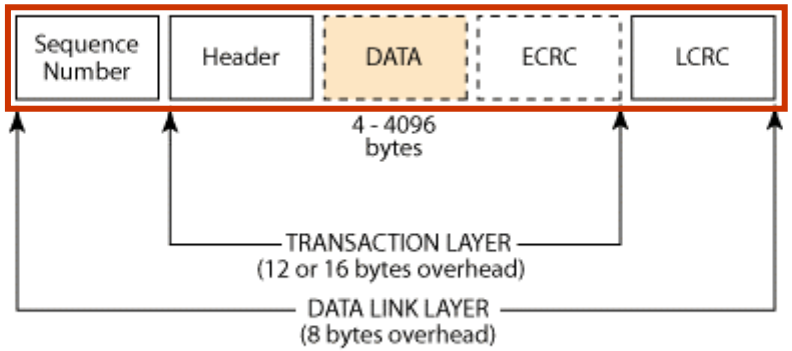
- **Minimized Packet Overhead**
  - 8/12 bytes (Min/Max)
- **Ideal for HPC Applications**



PCI EXPRESS®

General Purpose Protocol

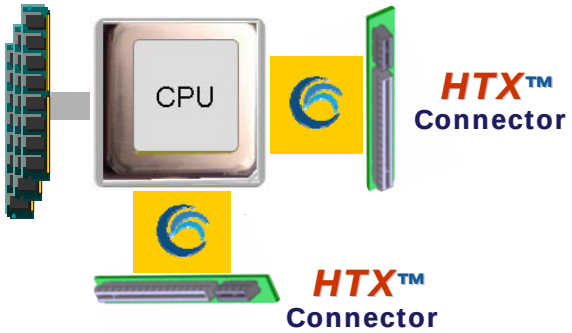
- **Considerable Packet Overhead**
  - 20/24 bytes (Min/Max)
- **Non-Optimal for HPC Applications**



HTX's Vastly Leaner Packet Payload Yields Latency Advantage that Scales Linearly with Applications and Job Transactions

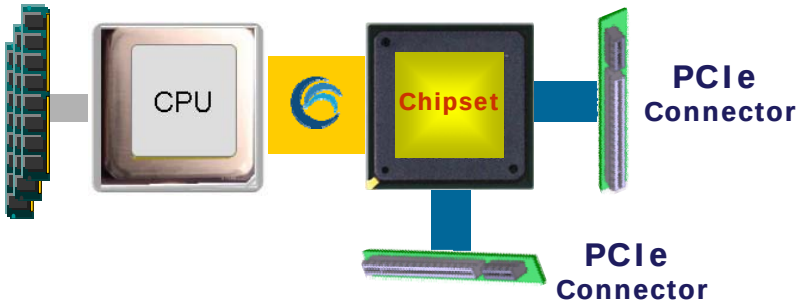
Multiple Latency Advantages

Advantage 3: No Intermediate Logic Overhead



HTX™

- Direct CPU-to-Subsystem Connection
- No Latency Penalty from Intermediate Control Logic



PCI EXPRESS

- Peripheral Slot Connector Interface
- Intermediate Control Logic
- Chipset Processing Time Penalty
  - Estimated at 95 nS Round-Trip Penalty out of 170 nS Total on Short, Open-Page DRAM Reads (*)

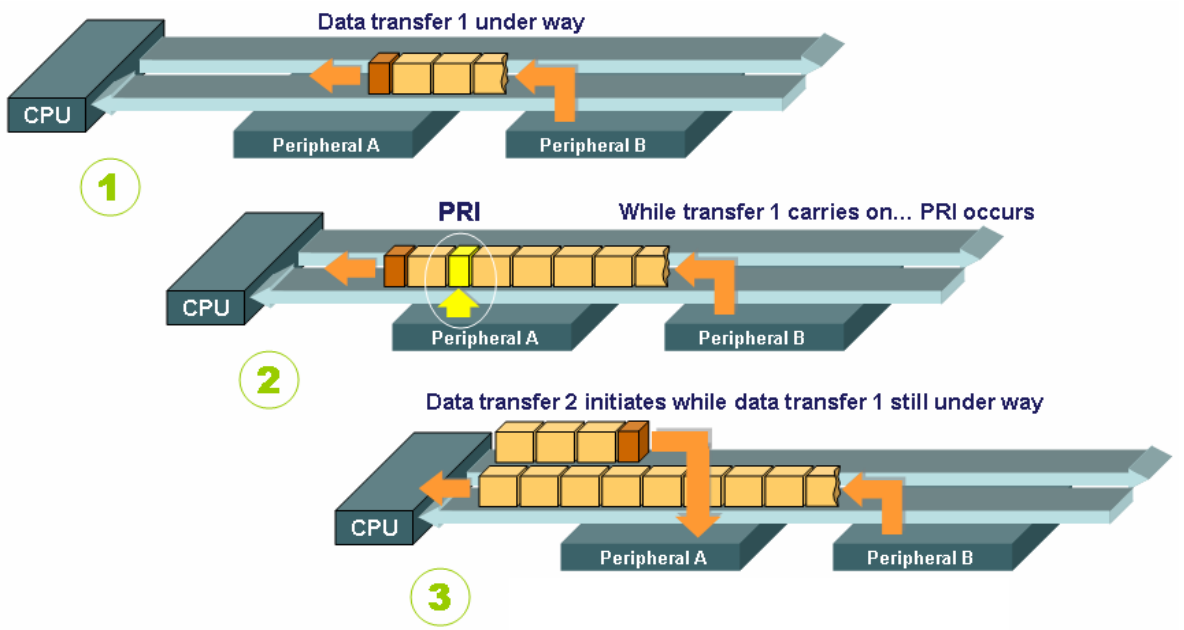
HTX Delivers 55% Lower Latency per Transaction Due to Absence of Intermediate Control Logic and Multiplexing

(*) PCIe Gen2

Multiple Latency Advantages

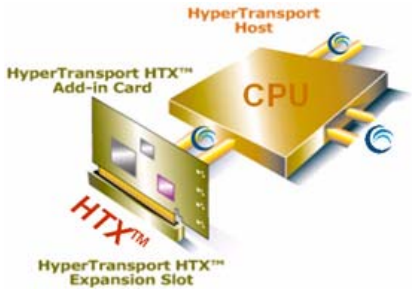
Advantage 4: Peripheral Processing Efficiency

HyperTransport is the Only Interconnect that Can Dynamically Insert Peripheral Read Requests in the Middle of Data Packets (Priority Request Interleaving™)



- PRI's Delivers an Average of 20nS Less Per-Transaction Latency in Heavily Loaded Environments
- High Priority Packets Not Penalized by Low Priority Packets
- Lowest Peripheral Processing Latency

HTX™ & PCI Express Bandwidth Comparison

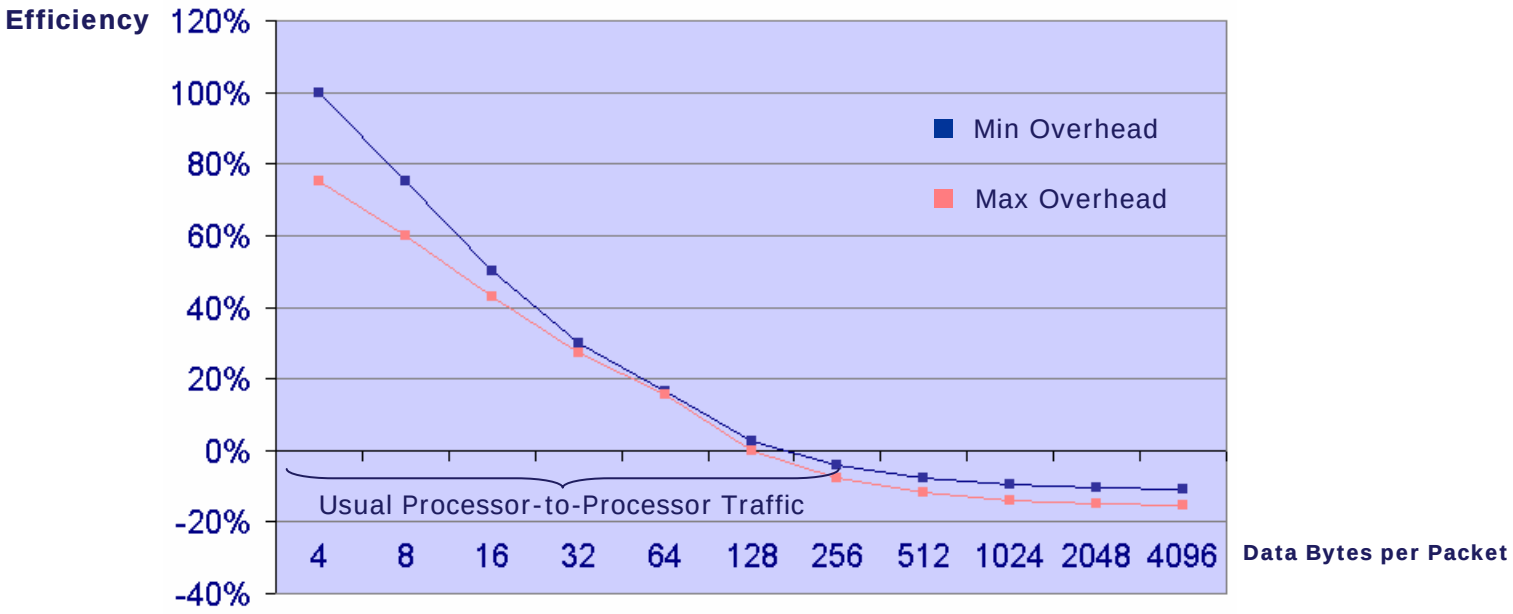


Feature	PCIe Gen1	PCIe Gen2	HTX	HTX3
Max Clock Rate	2.5 GHz	5.0 GHz	800 MHz	2.6 GHz
Double Data Rate	NO	NO	YES	YES
Max Bandwidth x Lane	2.5 Gbps	5.0 Gbps	1.6 GT/s (*)	5.2 GT/s (*)
8B/10B Penalty	-20%	-20%	No Penalty	No Penalty
Net Bandwidth x Lane	2.0 Gbps	4.0 Gbps	1.6 GT/s (*)	5.2 GT/s (*)
Net Bandwidth 16-Bit - Aggregate	8 Gbytes/s	16 Gbytes/s	6.4 GBytes/s	20.8 GBytes/s

(*) HyperTransport supports Double Data Rate (DDR), transferring data on both the leading and trailing edge of the clock. Therefore HyperTransport's bandwidth is more appropriately represented by the term "Transfers/second" than the term "Bits/second"

HTX™ Packet Efficiency in Figures

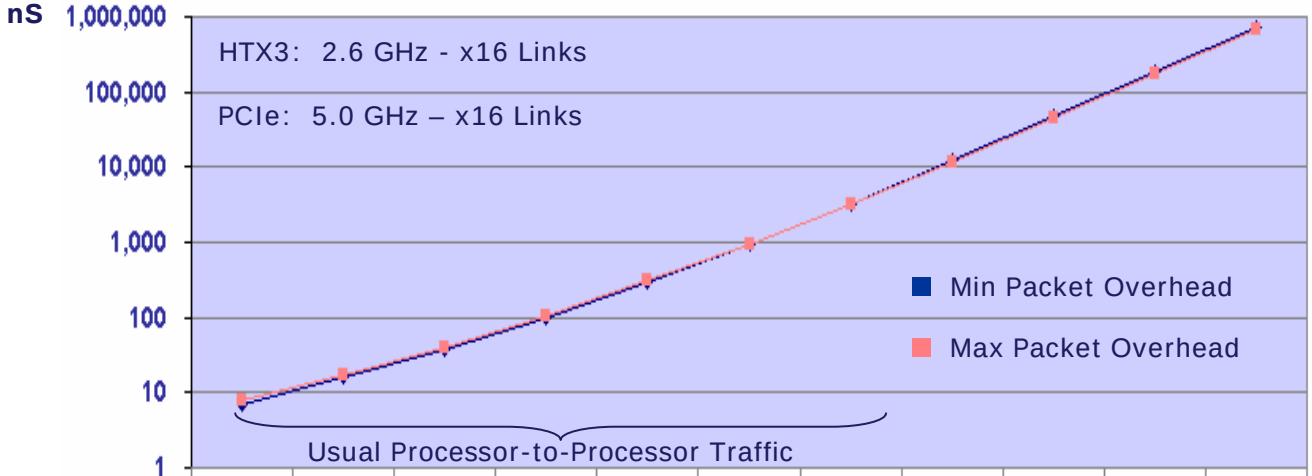
HTX™ Packet Overhead Efficiency Margins over PCIe



HTX Delivers up to Twice the Packet Efficiency of PCIe with Proportional Latency Advantages

HTX™ Per-Packet Latency Advantage

HTX3™ Per-Packet Latency Advantage over PCIe Gen2



Data Bytes Per Packet	4	8	16	32	64	128	256	512	1024	2048	4096	
Latency Advantage	7	16	37	100	299	949	3,300	12,209	46,851	183,436	725,807	nS
Latency Advantage	8	17	40	106	312	949	3,202	11,619	44,097	171,626	676,982	nS

The results take into account PCIe's 20% clock recovery, packet payload and 55% chipset overhead penalties. HTX's Priority Request Interleaving, if applicable, will add to HTX's total latency advantage

HTX™ Real World Time-to-Result Savings

Combined Bandwidth, Pysical Layer and Protocol Latency Advantages

Compute-Intensive Tasks Require Hundreds of Thousand to Billions of Packet Transactions

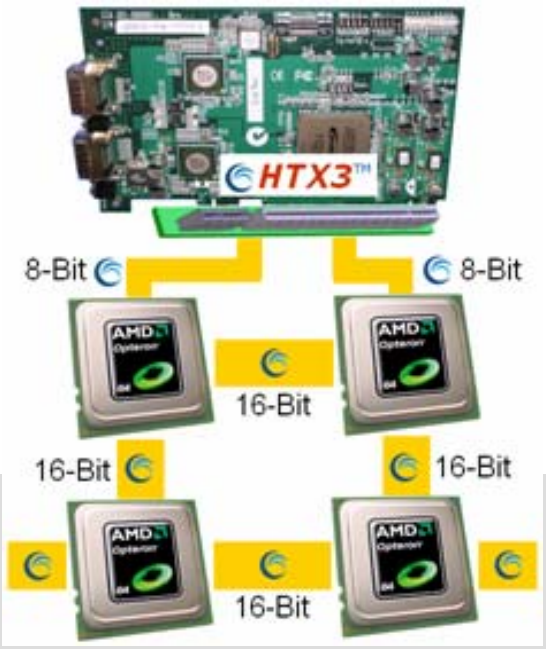
HTX3™ Time-to-Result Saving vs. PCIe Gen2

Number of Packets Trasferred / Bytes per Packet Transferred	100,000 Per Task	1 Million Per Task	1 Billion Per Task
4	0.78 mS	7.8 mS	7.8 Sec
16	4 mS	40 mS	40 Sec
256	0.32 Sec	3.20 Sec	53 Min
512	1.16 Sec	11.62 Sec	3.23 Hrs

The results take into account PCIe's 20% clock recovery, packet payload and 55% chipset overhead penalties. HTX's Priority Request Interleaving™, if applicable, will add to HTX's total time-to-result latency advantage

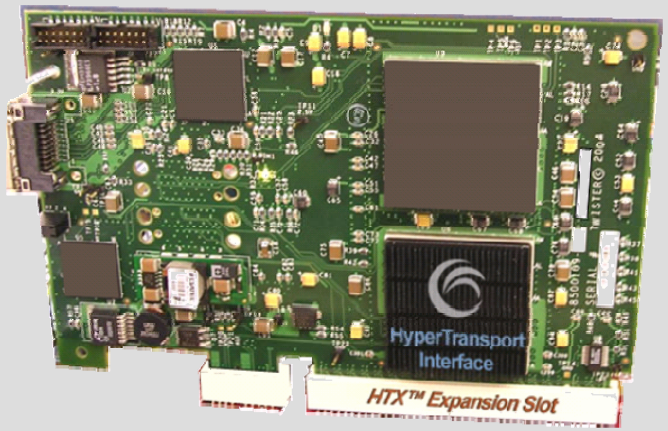
HTX3™ Link Splitting Capability

The 16-Bit HyperTransport Link in an HTX3 Connector Can Split into Two Independent 8-Bit Links



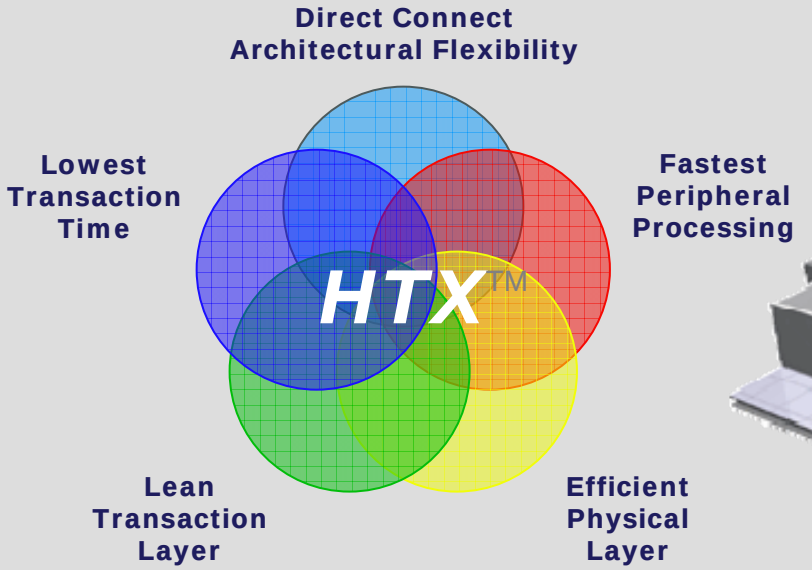
Allows HTX Subsystem to Connect Directly to 2 CPUs
Supports New-Generation System Functionality

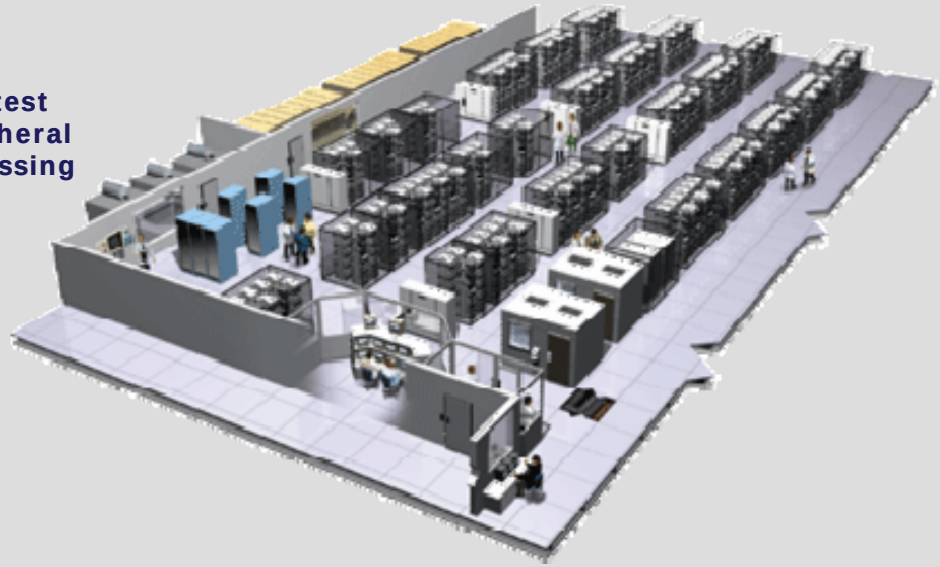
HTX™ in Summary



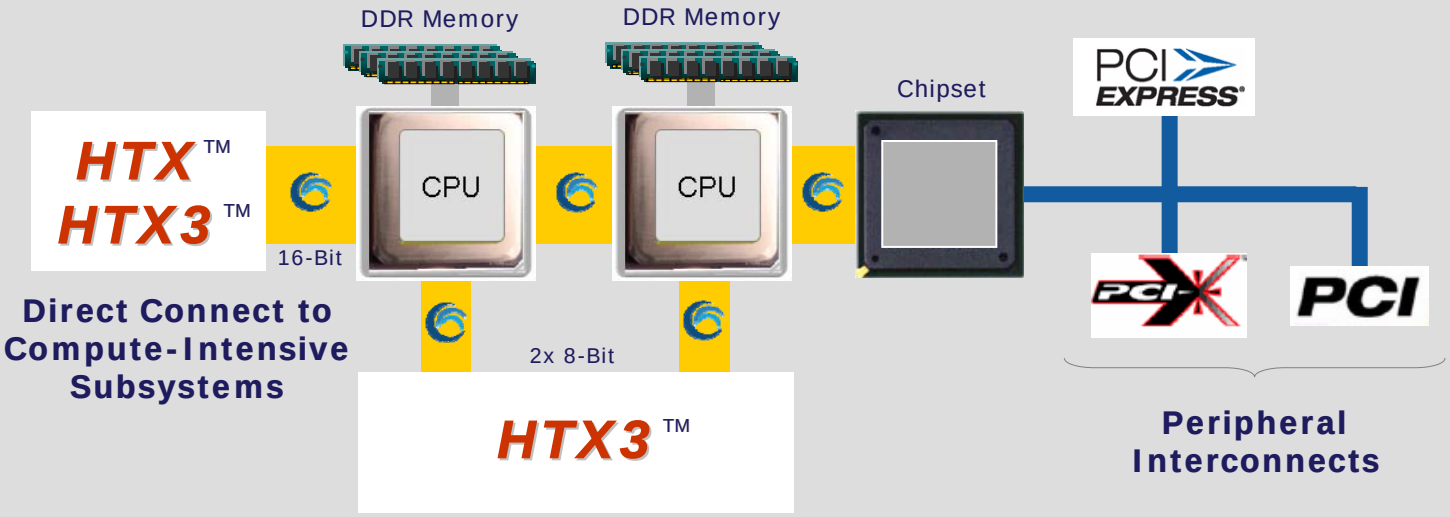
Unique Technical Values

HTX™ Provides Superior Performance and Architectural Capabilities In Line with HPC Market Expectations





HTX™ Complements PCI Express

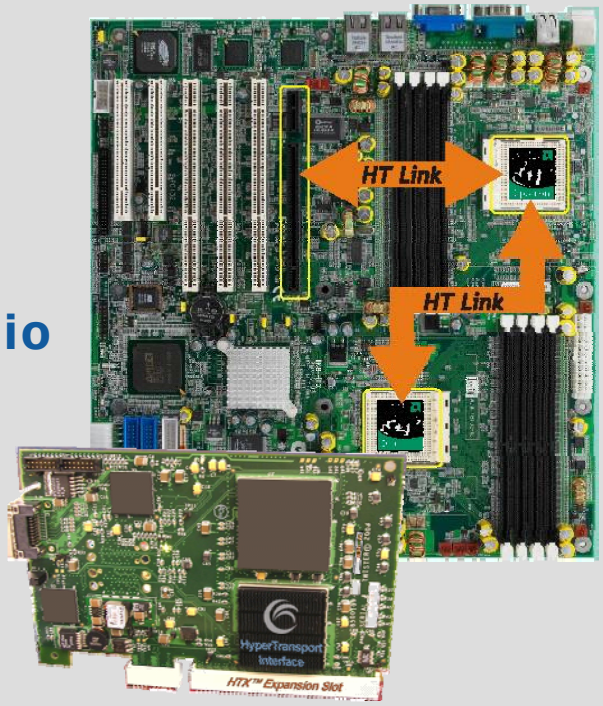


With its Unique Architectural and Performance Edge over General Purpose Interconnects, HTX is an Ideal Complement to PCI-Class Slot Connector Interfaces

HTX™ Business Values

HTX™ is a Competitive Differentiator for High-Performance Total Solution Vendors

- **Negligible BOM Cost**
  - Leverages PCIe Economy of Scale
- **System Flexibility**
  - Single MB Serves Multiple Markets
- **Growing HTX Subsystem Portfolio**
  - Coprocessors, Accelerated 10GE, ccNUMA Cluster Controllers, Content Processors, Others Released Soon
- **Up-Selling Enabler**
  - Delivers Greater End-User Value



HyperTransport™ CONSORTIUM