AMD Product Brief - Preliminary Information

AMD-8132[™] HyperTransport[™] PCI-X[®] 2.0 Tunnel

Product Overview

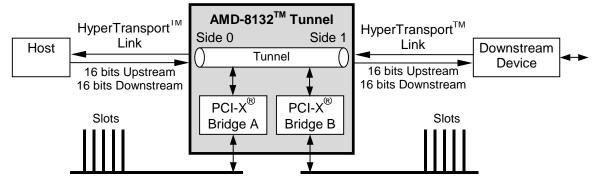
The AMD-8132TM HyperTransportTM PCI-X[®] 2.0 tunnel developed by AMD provides two PCI-X bridges designed to support PCI-X 266 transfer rates¹. The AMD-8132 tunnel is compliant with *HyperTransportTM I/O Link Specification, Rev 2.0* including errata up to specification Rev 1.05c. The package is a 31 x 31 millimeter, 829 ball, flip-chip organic BGA. The core is 1.2 volts. Power dissipation is 7 watts.

HyperTransport TM Features:

- HyperTransport tunnel with side 0, 16-bit input/ 16-bit output; and side 1, 16-bit input/16-bit output.
- Either side can connect to the host or to a downstream HyperTransport technology compliant device.
- Each side supports HyperTransport technologydefined reduced bit widths: 8-bit, 4-bit, and 2-bit.
- Each side supports transfer rates of 2000, 1600, 1200, 1000, 800, and 400 mega-bits per second per wire.
- Maximum bandwidth is 8 gigabytes per second across each side (half upstream and half downstream).
- Independent transfer rate for each side and each direction.
- Independent bit width selection for each side and each direction.
- Link disconnect protocol supported.
- HyperTransport interrupt control support.
- 64-bit address support.

PCI-X[®] Features:

- Two PCI-X bridges: bridge A and bridge B.
 - Each bridge supports a 64-bit data bus.
 - Each bridge supports Mode 1 PCI-X and Conventional PCI protocol. Each bridge is designed to support Mode 2 operation.¹
 - In PCI-X Mode 2, bridges are designed to support transfer rates of 266 and 200 MHz.¹
 - In PCI-X Mode 1, bridges support transfer rates of 133, 100, 66, and 50 MHz.
 - In PCI mode, bridges support transfer rates of 66, 50, 33, and 25 MHz.
 - Independent transfer rates and operational modes for each bridge.
 - Each bridge includes support for up to 5 PCI masters with clock, request, and grant signals.
 - Each bridge includes a HyperTransportTM technology compliant interrupt controller. Legacy interrupt controller and IOAPIC modes are also supported.
 - Each bridge can receive PCI device interrupts via INTA/B/C/D pins or via MSI/MSI-X transactions.
 - SHPC-compliant hot-plug controller and support.
- PCI-X Mode 2, 1.5 V link signaling. PCI-X Mode 1, 3.3 V link signaling. PCI, 3.3 V link signaling.



AMD-8132[™] HyperTransport[™] PCI-X[®] 2.0 Tunnel

1. Mode 2 operation is being evaluated.

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Licensed Technology

PCI-X and PCI Hot Plug technology developed by Compaq/Hewlett Packard Corporation.

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