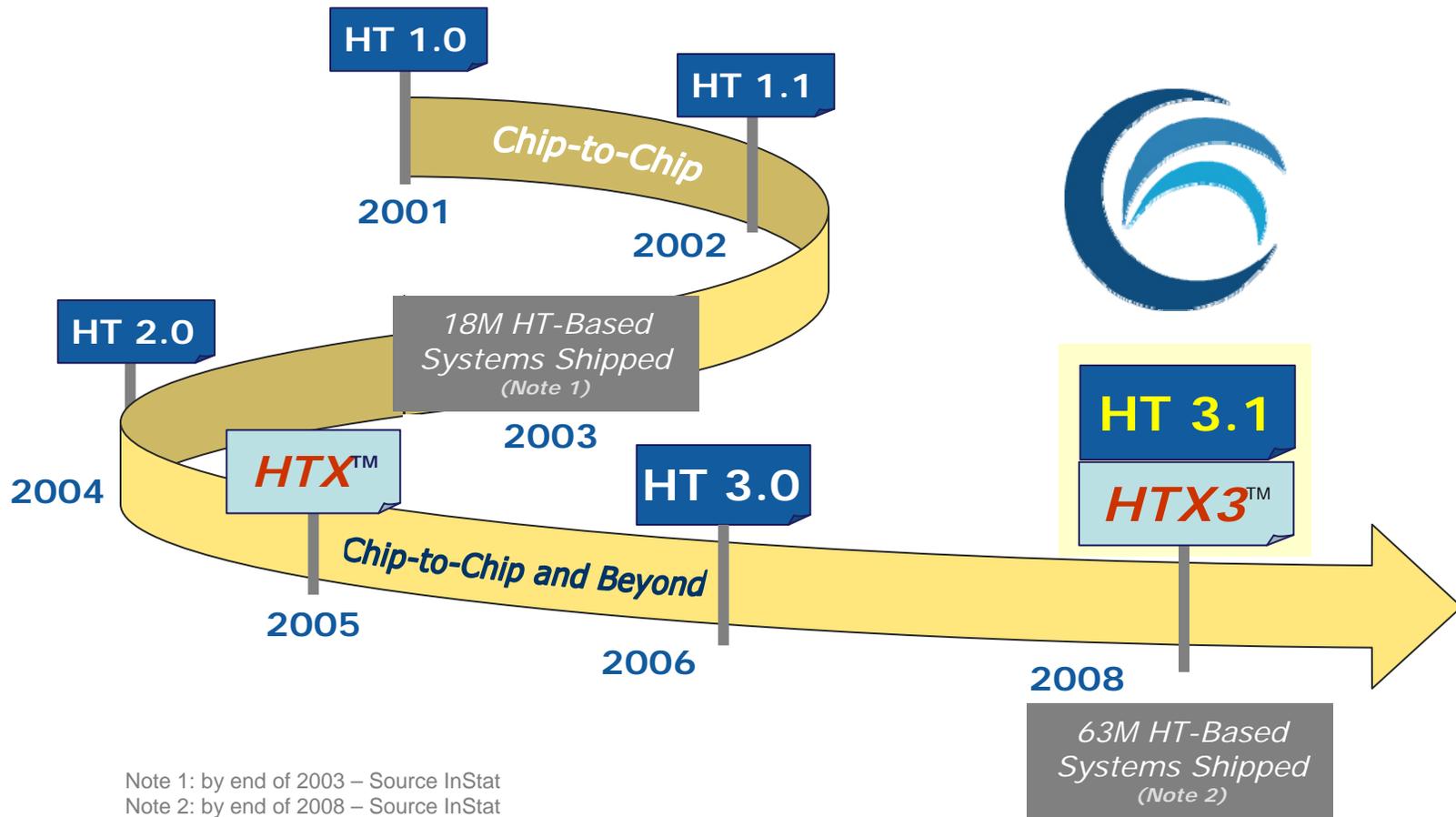




HyperTransport™ HTX™ Snapshot

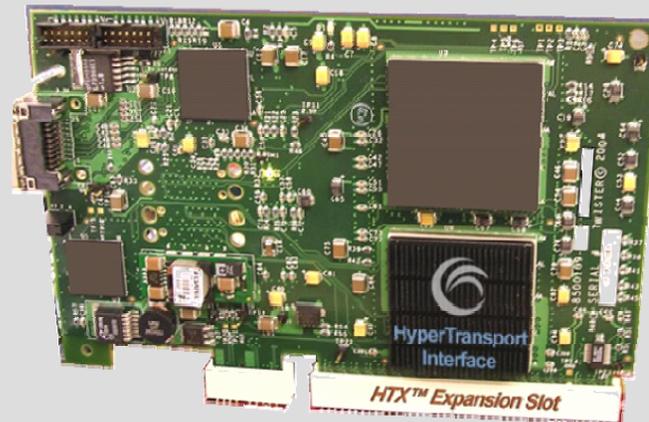


HTX™ Leaps Forward to HTX3™



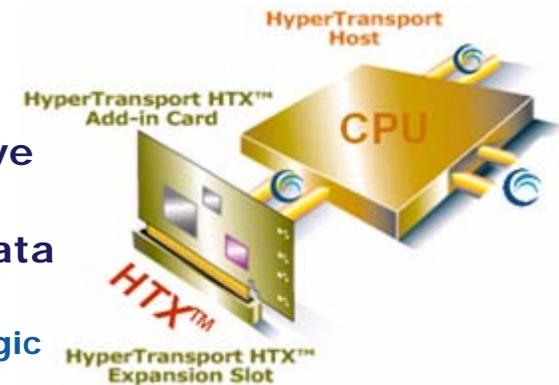
Note 1: by end of 2003 – Source InStat
Note 2: by end of 2008 – Source InStat

Technology Overview



HTX™ Interface = Performance Edge That PCI-Class Interconnects Cannot Deliver

- Lowest Latency, Highest Bandwidth Direct Connect Between CPU and Compute-Intensive Subsystems
- Removes Performance Bottlenecks in HPC Data Processing and Coprocessing Functions
 - No Intermediate CPU-to-Subsystem Control Logic
- Reduces Overall Power Consumption
- Complements PCI-Class Interconnects
 - Typically Co-Exist with PCI-X and PCI Express Connectors in Same MB Design



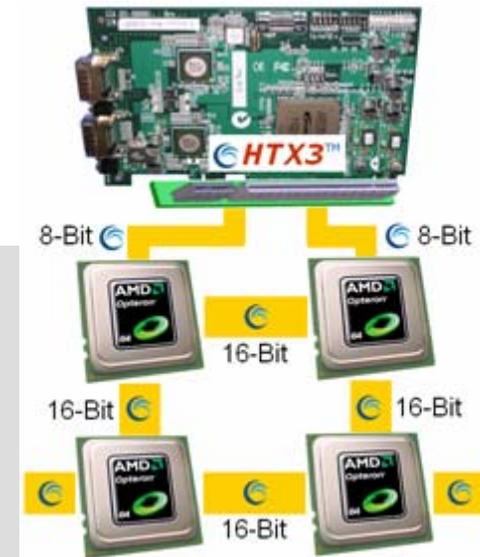
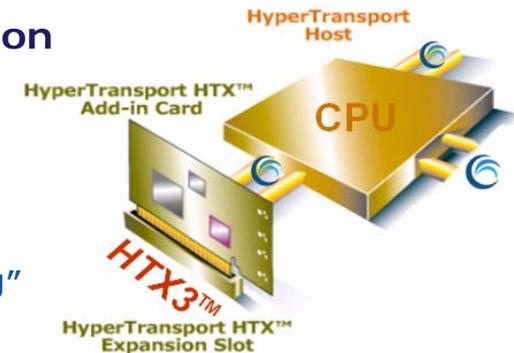
Features

8-Bit and 16-Bit HyperTransport Link Support
800 MHz Max Clock Rate
6.4 GB/s Bandwidth (16-bit, Aggregate)

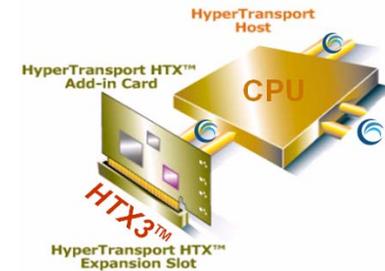


Introducing HyperTransport™ HTX3™

- >3x Bandwidth of Standard HTX Specification
- Brings HT 3.0 Performance and Architectural Latitude to HTX Connector
- Triples HT Clock Rate While Preserving Signal Integrity
 - Leverages HT 3.0 Clock Recovery “Scrambling” and “Training” Features
- Adds Power Management Features
- Adds Link-Splitting Capability
 - Allows Subsystem Connection to 2 CPUs



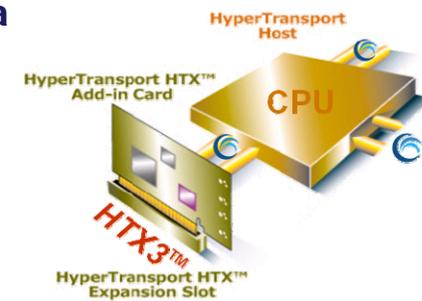
HTX3™ Features Summary



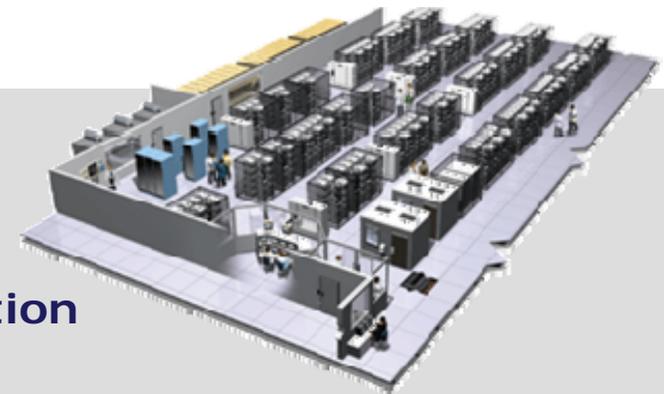
Feature	<i>HTX</i>	<i>HTX3</i>	Notes
Max Clock Rate	800 MHz	2.6 GHz	12" Trace length
Max Bandwidth x Lane	1.6 GT/s	5.2 GT/s	Bi-directional
Max Bandwidth Aggregate	6.4 GB/s	20.8 GB/s	Bi-directional 16-Bit HT link
HT3 Link Splitting Support	NO	YES	HT link can be 1x 16-Bit or 2x 8-Bit for mutli-CPU support
HT3 Extended Power Management	NO	YES	LDTREQ# Signal Added to participate in x86 power states
Extended FPGA Guidelines	NO	YES	Incorporated field-proven recommendations
Full Backward Compatibility	--	YES	Level shifters and signal allocation

Why HyperTransport™ **HTX3™** ?

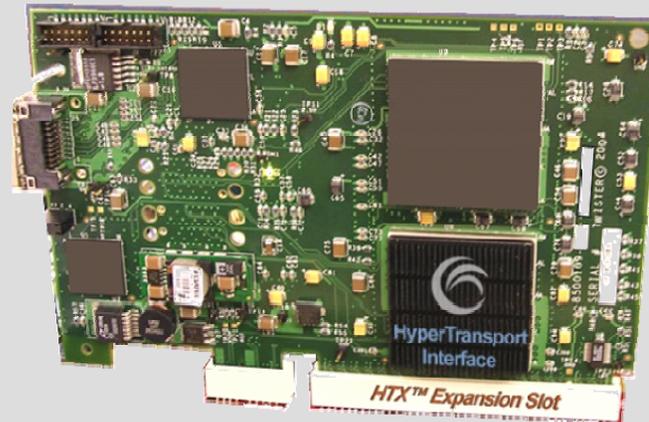
- FPGAs Play Key Role in Compute-Intensive Designs
- HTX3 Well Aligns with Expected FPGA Technology Progress
- FPGA Cores Expected to Support HT3.0-Class Clock Rates
 - From Bandwidth Bottlenecks to Drivers
- Power Optimization Ranks High in HPC Agenda
- HT 3.0 Has Reached Maturity and Stability
 - Design Learning Curve
 - Product Implementations
 - Market Feedback
- HT 3.0 Capability Now Safely and Stably “Connectorized”



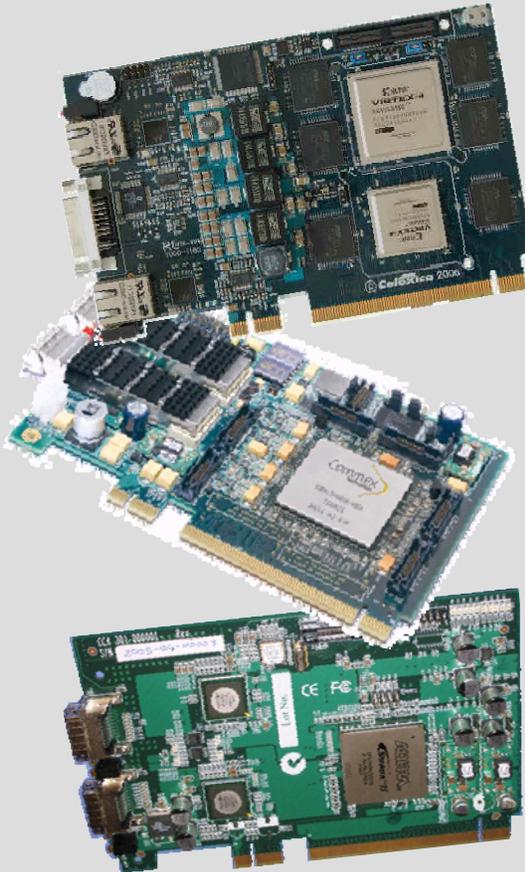
With its State-of-the-Art Features Set
HTX3™ Empowers Future HPC Innovation



Main Applications



HTX™ Applications



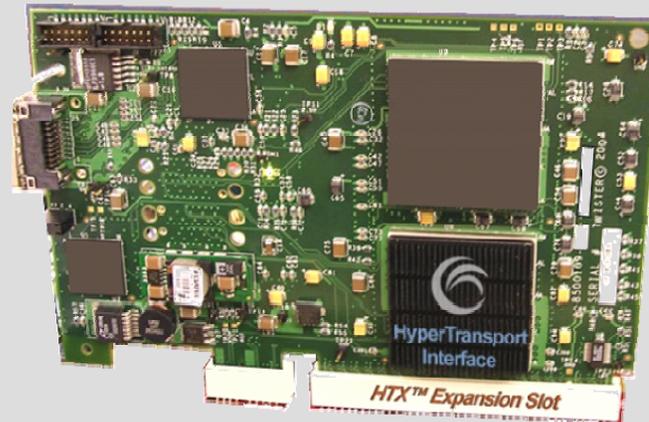
Compute-Intensive Board Level Subsystems Requiring:

- High Bandwidth + Low Latency
- Multi-CPU Connections (HTX3)
- Advanced Power Management (HTX3)

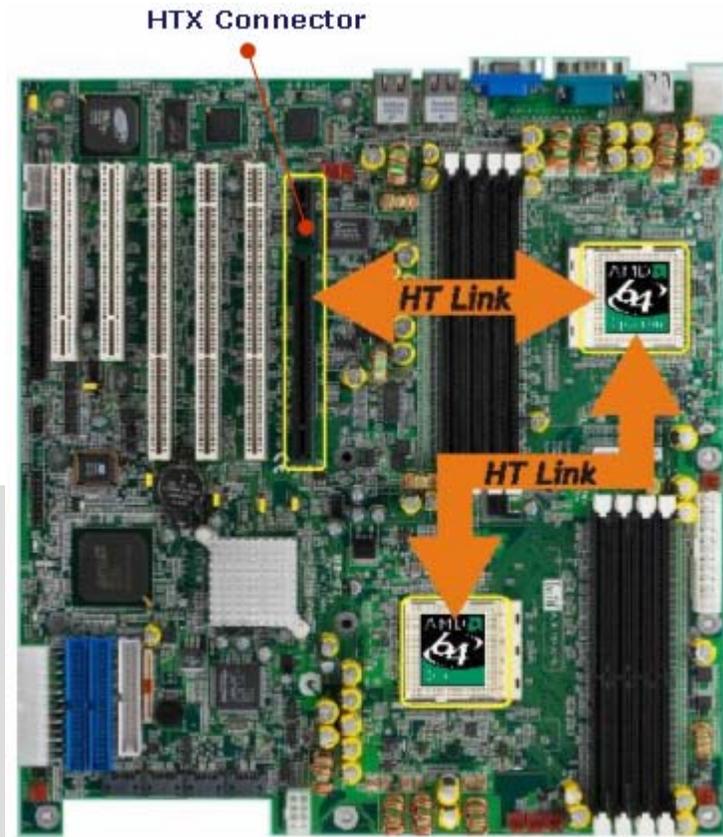
Targeting:

- Database Analytics
- Stock Trading Acceleration
- High-Traffic Web-Based Applications
- Transaction Servers
- Streaming Media Servers
- Storage Servers
- Server Clustering and SMP
- Financial Modeling
- Communications
- Content Processing
- Security Processing
- High-Perf Real World Rendering

Core Values

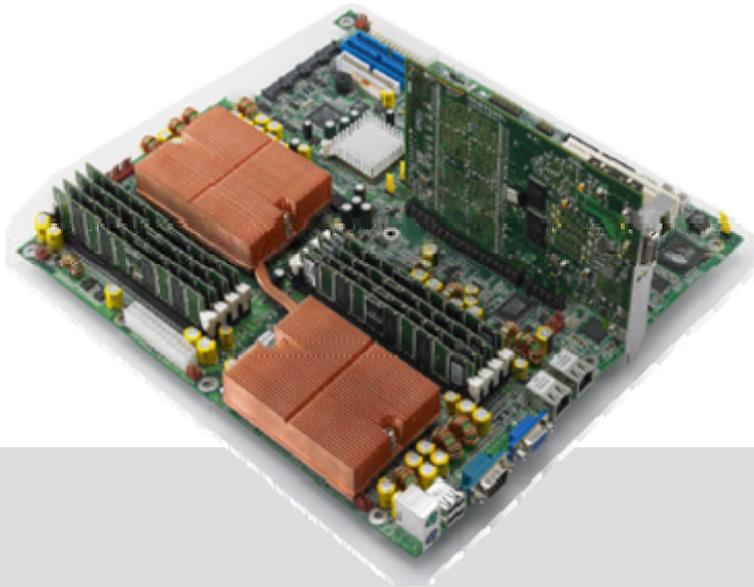


HTX™ and HTX3™ Connector

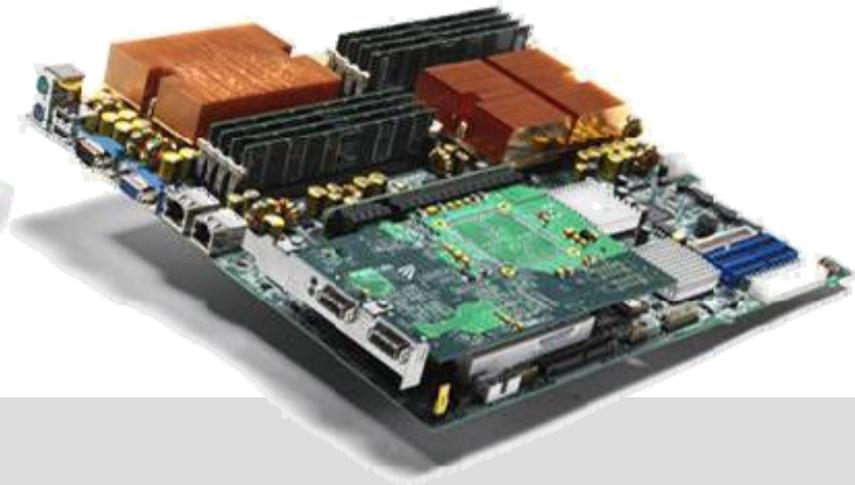


- **Uses popular PCIe Connector**
 - High-volume part, Low cost
- **HT-defined signals**
- **Reverse-Installed vs. PCIe Slots**
 - Prevents Wrong Card Insertion

HTX™ and *HTX3™* Connector Mounting



- **Vertical Mount**

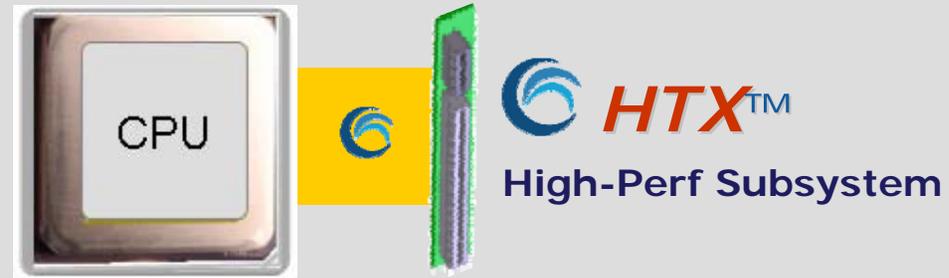


- **Horizontal Mount
via HTX Riser**

Lowest Achievable Latency



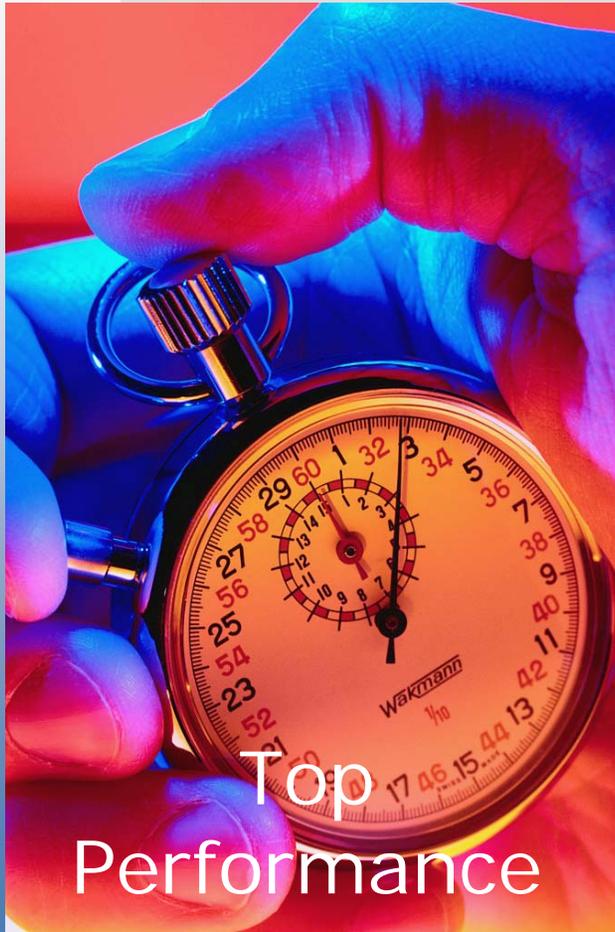
No Control Logic Penalty



Control Logic Penalty



Lowest Achievable Latency (cont.)



No 8B/10B Overhead Penalty



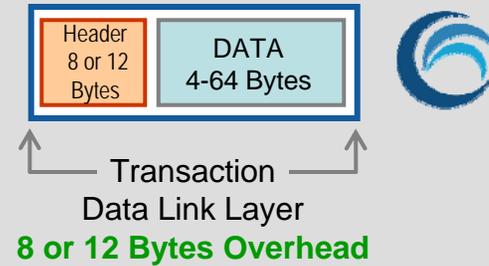
20% 8B/10B Fixed Overhead Penalty



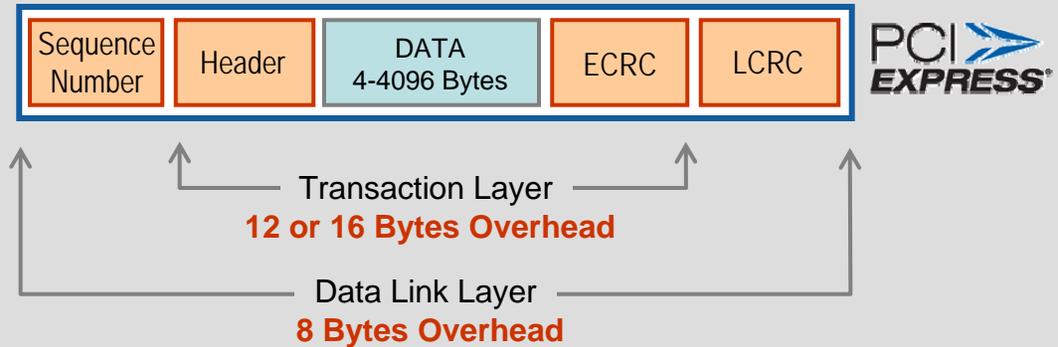
Lowest Achievable Latency (cont.)



Minimized Packet Overhead



12 Byte Overhead Penalty vs. HT



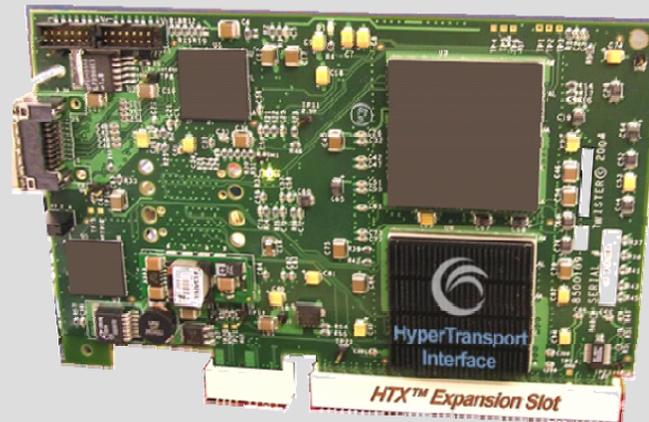
HTX™ Delivers the Extra Performance that PCI-Class Interfaces Cannot Deliver

Complements
PCIe and PCI-X

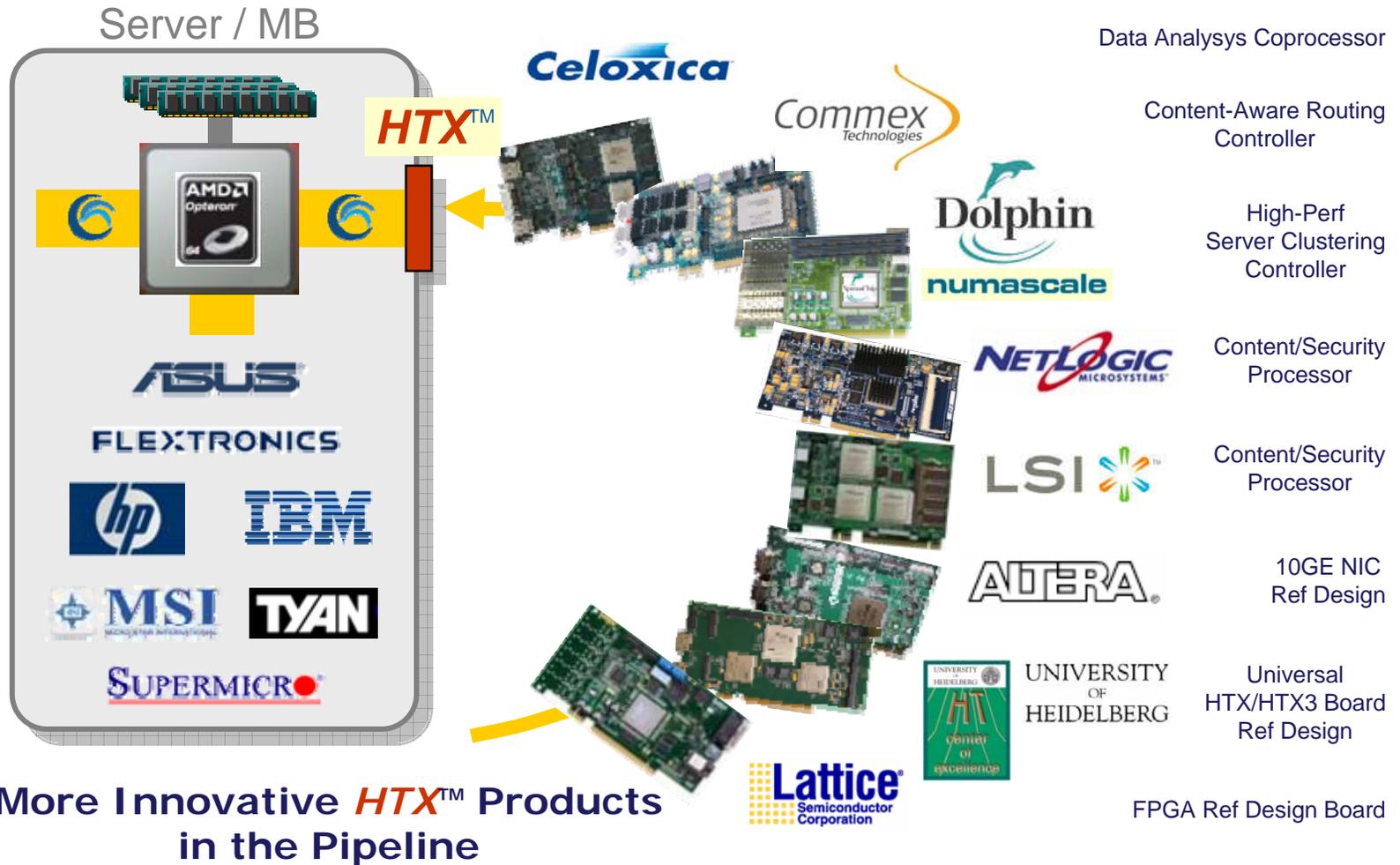


Cohexists within
Same System

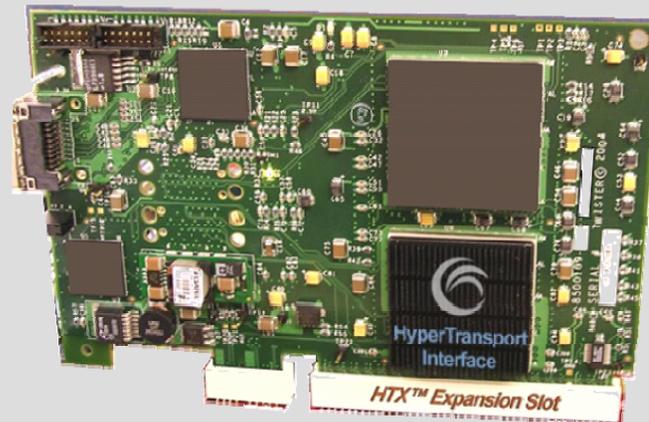
Product Ecosystem

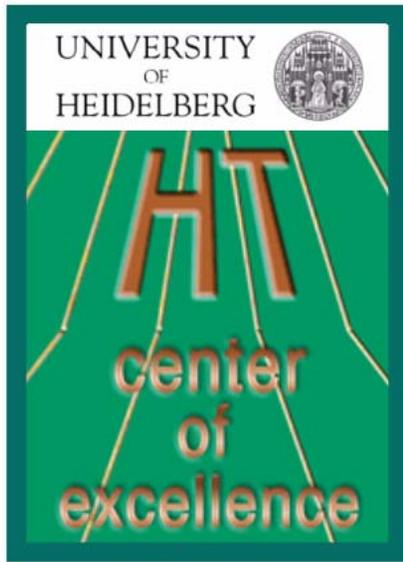


Expanding HTX™ Products Ecosystem



Development Support





HyperTransport Center of Excellence Design Support and Services

Universal Board Reference Designs



HTX™



HTX3™

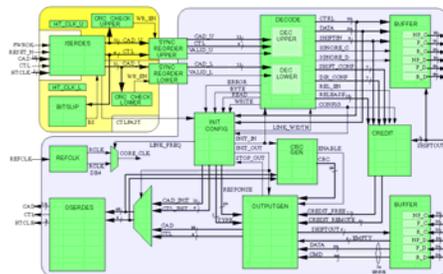
Test Tools



Design Support Product Validation



HT and cHT Cores



ALTERA

HTX™ 10GE NIC Design Kit

- Validated and Tested 10 Gigabit Ethernet Solution
- Downloadable Free-of-Charge from HTC Web Site



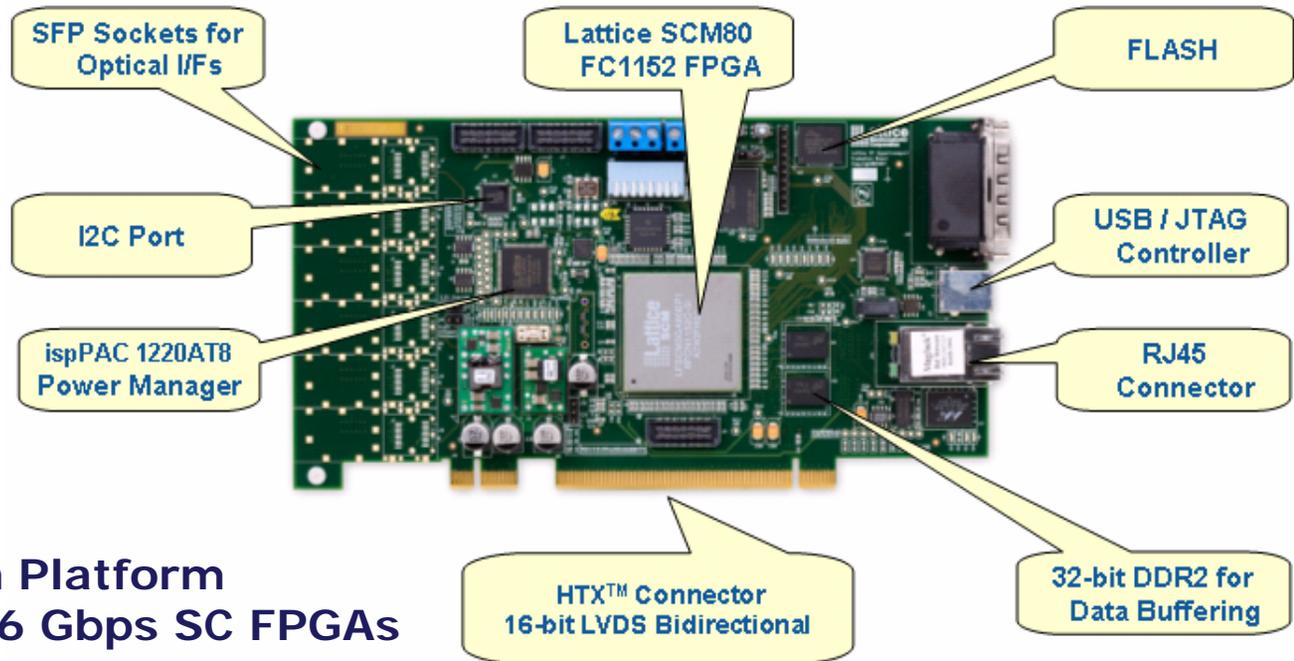
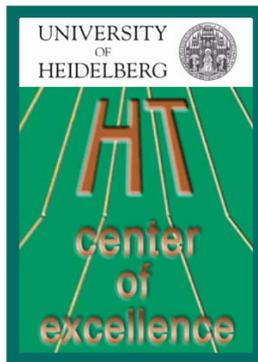
- 2x 10GE Ports
- Stratix II FPGA

Fast Time-to-Market

 **HTX™ Connector**



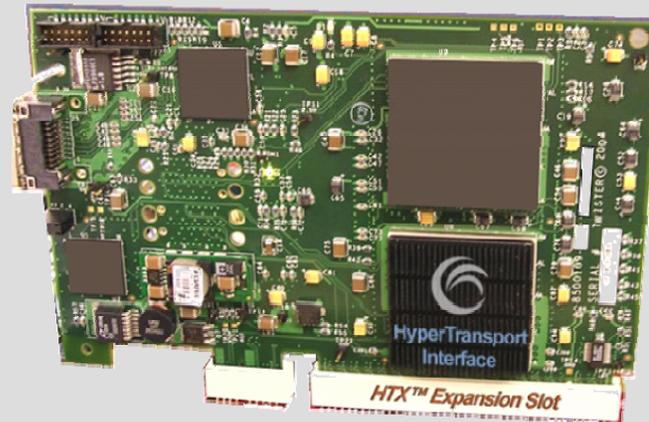
HTX™ FPGA Development Board



**Rapid Design Platform
for Lattice 1.6 Gbps SC FPGAs**



BIOS Support



HTX™ BIOS Support

Consortium-Defined and Standardized
HTX™ BIOS Specifications

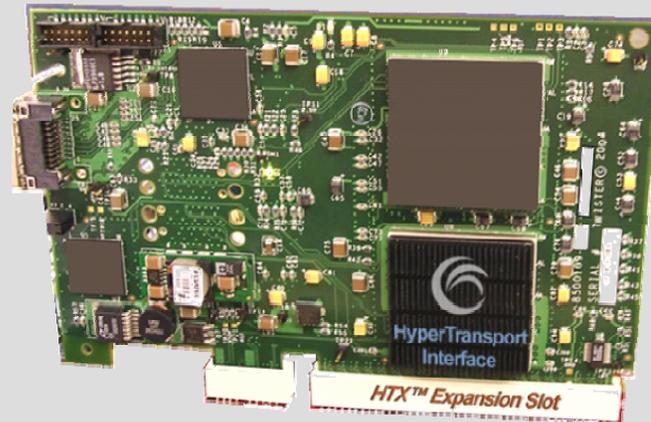


Aptio.

Cross-Compatibility

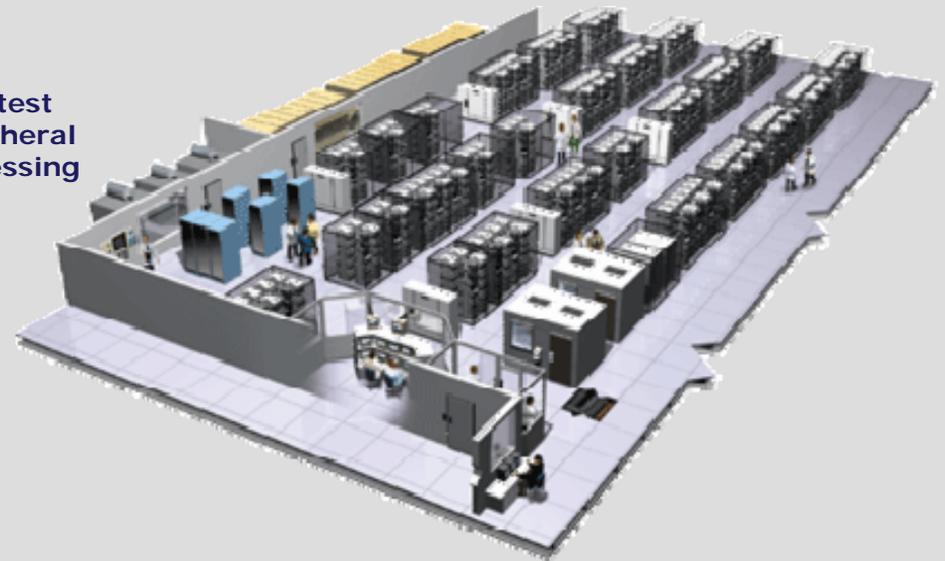
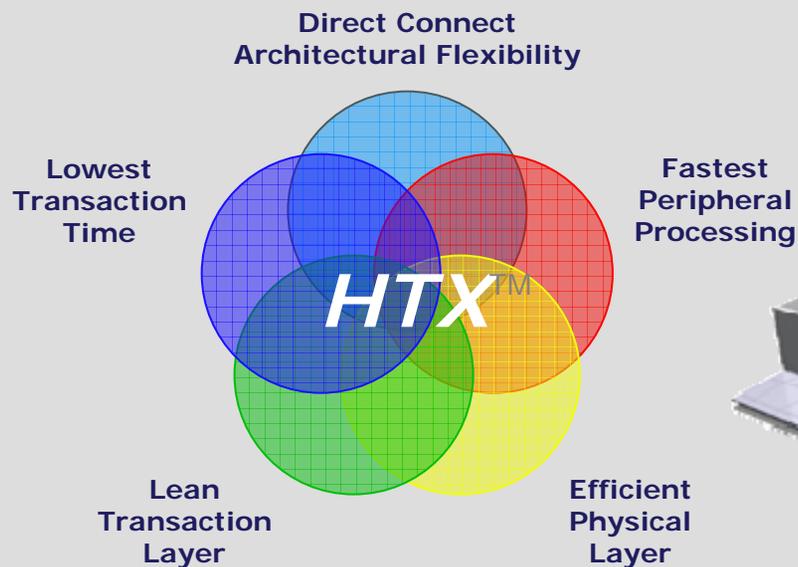
Fast Time-to-Market

Why HTX?

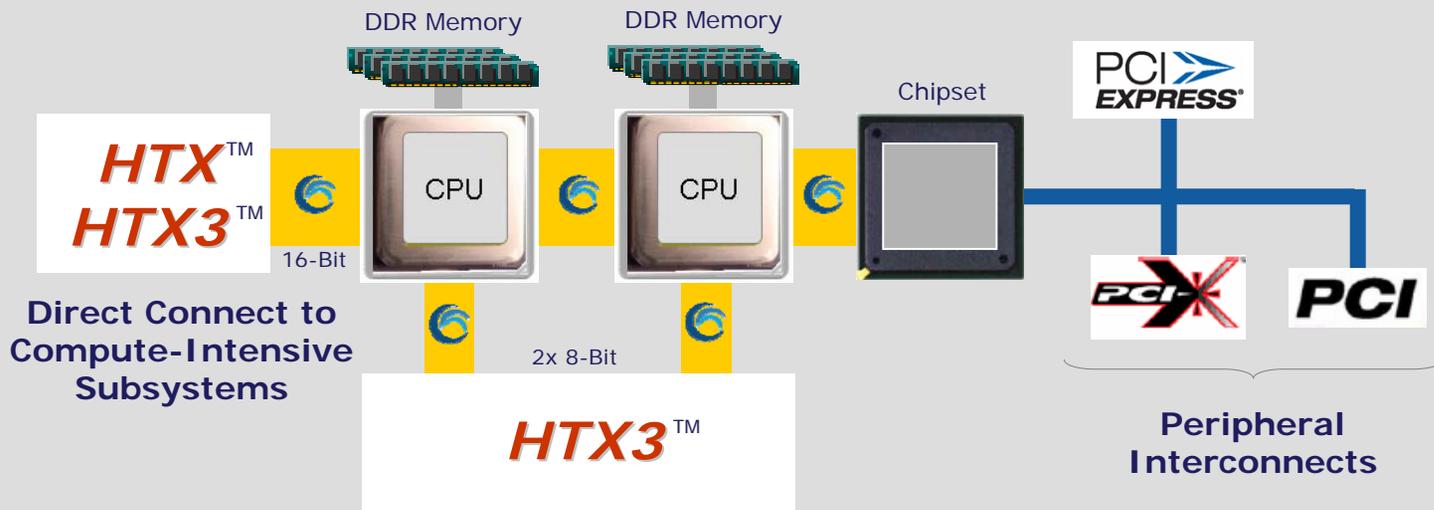


Unique Technical Values

HTX™ Provides Superior Performance and Architectural Capabilities In Line with HPC Market Expectations



HTX™ Complements PCI Express

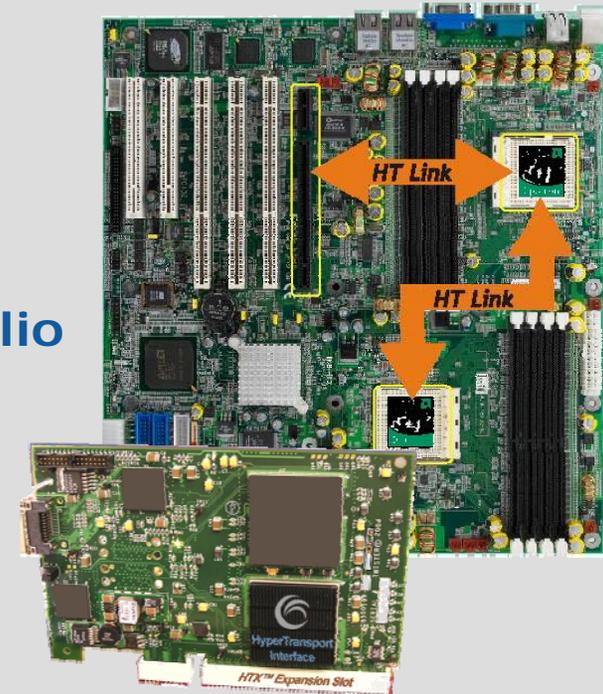


With its Unique Architectural and Performance Edge over General Purpose Interconnects, HTX is an Ideal Complement to PCI-Class Slot Connector Interfaces

HTX™ Business Values

HTX™ is a Competitive Differentiator for High-Performance Total Solution Vendors

- **Negligible BOM Cost**
 - Leverages PCIe Economy of Scale
- **System Flexibility**
 - Single MB Serves Multiple Markets
- **Growing HTX Subsystem Portfolio**
 - Coprocessors, Accelerated 10GE, ccNUMA Cluster Controllers, Content Processors, Others Released Soon
- **Up-Selling Enabler**
 - Delivers Greater End-User Value





HTX™

The
HPC Interconnector™

With HyperTransport™ The Technology Industry Wins

