

# AMD Geode™ GX Processors

## Intermittent Screen Tearing

### Issue Resolution



## 1.0 Scope

This document provides a programming resolution for an Intermittent graphics issue observed with the AMD Geode™ GX processor (i.e., Geode GX 533@1.1W processor\*, Geode GX 500@1.0W processor\*, and Geode GX 466@0.9W processor\*).

## 2.0 Discussion

During testing of the Geode GX processors, some devices exhibited a tearing in the rendered display. The programmed value in the RAM Control MSR (MSR Address 80002012h) bits [26:24] and [18:16] were found to be the cause of this issue. (See Table 2-1 for bit descriptions.)

The default BIOS value of 4h (100b) is incorrect and needs to be changed to 6h (110b). The full value of this register should be changed in the BIOS from 04040202h to 06060202h. Additional testing with the new value corrected the observed problem.

**Table 2-1. MSR\_RAM\_CTL Bit Descriptions**

Bit	Name	Description
63:27	RSVD	<b>Reserved.</b> Write as read.
26:24	DFIFO_CTL1	<b>DFIFO RAM 1 Delay Control.</b> This bit determines the precharge delay for the DFIFO1 DFIFO0, CFIFO, or DVJ RAM cell. (Recommended setting: 110.)
23:19	RSVD	<b>Reserved.</b> Write as read.
18:16	DFIFO_CTL0	<b>DFIFO RAM 0 Delay Control.</b> This bit determines the precharge delay for the DFIFO0 RAM cell. (Recommended setting: 110.)
15:11	RSVD	<b>Reserved.</b> Write as read.
10:8	CFIFO_CTL	<b>CFIFO RAM Delay Control.</b> This bit determines the precharge delay for the CFIFO RAM cell.
7:3	RSVD	<b>Reserved.</b> Write as read.
2:0	DV_RAM_CTL	<b>DV RAM Delay Control.</b> This bit determines the precharge delay for the DV RAM cell.

\*The AMD Geode GX 533@1.1W processor operates at 400 MHz, the AMD Geode GX 500@1.0W operates at 366 MHz, and the AMD Geode GX 466@0.9W processor operates at 333 MHz. Model numbers reflect performance as described here: <http://www.amd.com/connectivitysolutions/geodegxbenchmark>.

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