AMD Geode™ GX Thin Client RDK Hardware Developer's Guide and Schematic Checklist

1.0 Scope

The AMD Geode™ GX thin client reference design kit (RDK) provides a complete system solution, including schematics, layout and full documentation. The intent of this document is to describe the overall hardware design of the board, provide insight on key design constraints and where appropriate, provide design alternatives.

Note: This is revision B of this document. The changes from revision A (dated August 2004) include rewrites and enhancements of several sections. It is recommended that the user review the entire document.

2.0 Overview

The AMD Geode™ GX thin client RDK is a compact, low-power and high-performance system designed to help facilitate the next generation of thin client networked computing appliances. Building on AMD's philosophy of delivering low total cost of ownership, the thin client reference design kit is optimized to provide value through all phases of the design and development cycle (device choices, schematics, layout, and software). It was designed to provide an extensible solution for both hardware and software while serving as a powerful, near manufacture-ready reference design tool.

It is intended to provide a complete solution for both hardware and software, or can be used as a powerful beginning for a differentiated design. As a complete solution, utilizing AMD's Geode solutions and design flexibility, the thin client RDK dramatically reduces the costly time-to-market concerns; while at the same time creating an effective, efficient thin client design.

The Geode GX thin client RDK is based on proven, third generation Geode RDK technology providing a complete system design package that gives designers flexibility, versatility and enhanced capabilities – all in a small package (approximately 27.5 square inches). The AMD Geode™ GX 533@1.1W processor* provides the flexibility of the x86 instruction set with the power to run current popular operating systems.

The Geode GX thin client RDK and other advanced development tools represent AMD's commitment to low-power customer-centric solutions for the x86 thin client marketplace by providing an integrated suite of support and development capabilities. The thin client RDK contains materials needed to quickly and efficiently move networked computing appliance solutions to market.

Application Markets

The Geode GX thin client RDK features a flexible design that can address a broad range of embedded devices:

- Corporate Thin Client
- Terminal in Blade PC
- Point-of-Sale
- Education
- Information Appliance
- Kiosk

3.0 Board Devices

This section describes the hardware devices found on the board.

3.1 AMD Geode™ GX Processor

The AMD Geode™ GX 533@1.1W processor provides the foundation of the design. This component integrates the CPU core, memory controller, and graphics subsystem from traditional designs into a single chip reducing system cost and complexity.

If an application does not require the full performance level of the Geode GX 533@1.1W, then two other, lower cost and power options are available: the AMD Geode GX 500@1.0W processor* and AMD Geode GX 466@0.9W processor*.

*The AMD Geode GX 533@1.1W processor operates at 400 MHz, the AMD Geode GX 500@1.0W processor operates at 366 MHz, and the AMD Geode GX 466@0.9W processor operates at 333 MHz. Model numbers reflect performance as described here: http://www.amd.com/connectivitysolutions/geodegxbenchmark.

3.1.1 GX BGU396

The thin client RDK was built using the Geode GX BGD368 (368-terminal Ball Grid Array Cavity Down) CRT version of the processor, however, another package option is available, the BGU396 (396-terminal Ball Grid Array Cavity Up). The BGU396 is a lower cost version of the processor and has the ball assignments for both CRT and digital RGB in the same package. The output option is selectable at boot time. The option schematic (publication #32211) is available on the Developer Support web site.

3.1.2 CPU Core

The x86 core of the Geode GX processor is transparent in the hardware design of the system. No special measures are taken with respect to this module other than to provide an adequate cost-effective power supply and appropriate configuration software.

3.1.3 Memory Controller

The Geode GX processor provides an integrated DDR SDRAM memory controller with a 64-bit wide access path. The platform design utilizes standard 4x16-bit DRAM devices soldered on-board.

In this design, soldered down DRAM provides the advantage of allowing the system to operate without V_{TT} termination rail prescribed for JEDEC standard DDR SDRAM without compromising signal integrity. Removal of this voltage rail reduces both system cost and power consumption significantly. Additional cost reductions are also obtained by the absence of the memory connector, memory module printed circuit board (PCB) and serial presence detect (SPD) EEPROM.

The memory clock is tied to the core clock in a 3:2 ratio. Latencies are configurable over the full range allowed in the JEDEC standards. This allows CAS latency down to 1.5.

An SPD ROM device is usually implemented so that memory can be properly configured (memory configuration, size, and timings) by the BIOS or loader. The RDK has soldered down memory and no SPD so the configuration is hard coded into the platform BIOS or loader. Soldered down memory has the performance advantage that CAS latency of 1.5 is supportable. Memory device selection is important in order to utilize the fast CAS latency.

If a custom design requires more flexibility in the memory subsystem, either an SODIMM or DIMM may be used. In both cases, SPD will need to be supported.

When designing in one or two DDR SODIMM slots, or one DDR DIMM slot, the design can either supply V_{TT} termination or proceed without. However, if no V_{TT} termination is provided then the layout guidelines are much stricter. Consult the *AMD Geode™ GX Processors/CS5535 Companion Device Layout Recommendations* application note (publication #31535) for more information.

There is currently a timing limitation on the DDR memory interface that prevents support of a two DIMM solution. Limited testing has shown that most DIMM combinations will work, but exhaustive stress and stability has not been performed to guarantee results. Customers wanting to use two DIMMs in their design should read and understand the issue (#1.41) as described in the *AMD Geode™ GX Processors Silicon Revision 2.1 Specification Update* document (publication #31533A) and then contact their field service representative for the latest information on this issue.

3.1.4 Graphics Subsystem

The Geode GX processor includes an integrated 2D graphics accelerator, display controller, and CRT DACs and utilizes system DDR SDRAM in unified memory architecture. The GeodeLink bus structure on the Geode GX processor enables this to be a high performance solution in a cost-effective manner. The Geode GX processor also contains proprietary compression hardware that reduces the overall load on the memory bus.

The frame buffer can be up to 16 MB in size, however, for systems using 1280x1024x16 or smaller graphics resolution, 8 MB of frame buffer may be used. For higher graphics resolutions and graphics intensive applications, 12 MB or 16 MB is recommended, however, this reduces the overall available system RAM.

3.2 AMD Geode™ CS5535 Companion Device

3.2.1 GPIO Usage

The Geode CS5535 companion device has up to 28 GPIOs, with most having alternate functions. BIOS and bootloaders developed for this RDK generally expect the functionality to be selected on the GPIOs. It is strongly recommended that system developers do not arbitrarily change the usage model because of the effect on BIOS and/or bootloader development. On the thin client RDK, very few GPIOs are used, however, if additional features are added then more may be required. Care must be taken when adding features as a GPIO/feature conflict may occur.

3.2.2 Boot Options

Booting from the LPC or Flash ports is selected via a strap option. If a pull-down resistor is connected to SDATA_OUT (pin L2 of the CS5535) the system boots from the LPC port. If there is a pull-up resistor on the signal, the system boots from the Flash port. The system can be configured either way. Option cards can be created to support booting from DiskOnChip or NOR Flash. Schematics are available on the Developer Support web site (publication #32555 and #32732).

3.2.2.1 Bootstrap options

Three boot options for the CS5535 are available.

BOS1 (Ball L2)	BOS0 (Ball L3)	Description
L	L	LPC ROM off LPC
H	L	NOR FLASH off IDE
L	H	Reserved
H	H	SST FWH off LPC

3.2.3 LPC Bus

The Low Pin Count (LPC) bus is an industry standard interface utilized for connecting with legacy device interfaces. There are numerous devices in production that support this interface. These include, but are not limited to:

- Super and Advanced I/O devices
- ROM devices
- System controllers

3.2.3.1 LPC BootROM

Initial boot code for the Geode GX thin client RDK may be stored in a 256 KB LPC NOR Flash bootROM. The design utilizes a PLCC (Plastic Leaded Chip Carrier) package of this device connected to the LPC port on the Geode CS5535 companion device via a socket. This socket is not compatible with an LPC firmware hub device due to the configuration of the CS5535. Other bootROM sizes are supported as well.

3.2.3.2 LPC Expansion Header

The LPC expansion header (JLPC1) is designed to allow extension of the design through targeted mezzanine cards. To this end, the header provides connectivity to both the LPC interface, a UART receive/transmit pair from the CS5535 and 5 volt power. In addition, the signals from the CS5535 companion device may be used as general purpose input/output (GPIOs) or interrupt inputs. Hardware signal conditioning may be employed for the GPIOs. In a custom design, desired features could be implemented on the main system board to reduce cost.

The LPC bus is a relatively slow interface. Devices placed on this bus are usually bootROMs or SuperI/O (SIO) devices. These SIO devices provide legacy functions that do not have significant performance requirements such as UARTs, parallel printer port, floppy port, PS2 mouse and keyboard.

3.2.3.3 LPC Interface Design Considerations

1) For heavily loaded systems LPC_AD[3:0], LPC_DRQ#, LPC_SERIRQ, LPC_FRAME# require a 100K pull-up.
2) For low cost designs, all LPC devices should be soldered down to the board. For applications requiring flexibility, a header similar to the one on thin client RDK can be used, however, this reduces the number of available GPIOs.

3.2.4 IDE and Flash Port

One of the unique features of the Geode CS5535 companion device is the pin-multiplexed interface that can be configured as either a standard IDE port or a Flash port. The Flash port allows for direct connection to a NAND Flash device or (with proper latching) connection to a parallel address/data interface. The IDE port supports ATA standard devices such as DiskOnModule and hard disk drive, for mass storage.

DiskOnModule is a standard that uses an IDE controller front end connected to NAND Flash device(s). It can plug directly into the 44-pin IDE header. An LPC bootROM is required with a DiskOnModule. M-Systems offers an iDiskOnChip that has the added advantage of supporting multiword DMA Mode 2 for considerably better performance than programmed I/O.

3.2.4.1 IDE Design Considerations

1) The IDE interface is not 5V tolerant. Use level translators if necessary.
2) 80-wire cable detection components: 10K and 0.01 µF in parallel to GND on pin 34 of the IDE connector.
3) 10K pull-down required on D7 to prevent system BIOS from thinking that a drive is connected and busy during IDE auto-detect routines.
4) Dynamic switching of port between IDE and Flash port is not supported. The Flash port may be used for system initialization, the switched to IDE made. However, additional circuitry is required to so support DMA under this circumstance.

3.2.5 USB

The Geode CS5535 companion device provides a total of four USB 1.1 compliant ports into the RDK. Utilizing two separate host controllers, the total possible USB throughput is 24 megabits per second.

Design optimization of the RDK limits the total amount of power available to the USB ports in the system. The design power for this interface is a maximum of 12 USB loads or 1.2 amps. Software is responsible for imposing the aggregate power limitations for the system. Loads may be distributed across the four USB ports in any combination.

While the RDK has these USB power limitations, a custom design could remove them. It is important to note that the CS5535 has two USB controllers. If only two ports are implemented, maximum data throughput can be achieved by using one port from each controller.

There is one additional design optimization associated with the USB ports. The design utilizes a reset-able fuse to limit the current to the ports.

3.2.5.1 USB Design Considerations

1) 15K pull-down resistors required on each signal (positive and negative) of each of the four ports even if not used.
2) There should be ferrite (100) between the USB port digital ground and system digital ground capable of carrying 1.5 amps minimum.
3) USB shell ground should connect to chassis ground, not to digital ground. Chassis ground should connect to digital ground through an appropriate EMI filter.
4) Ferrite beads or appropriate chokes on D+, and D– for each port (if used) is recommended for EMI reduction. Component should be placed close to the connector.

3.2.6 RTC and CMOS

The system uses a CR1220/3V battery to supply the RTC (Real-Time Clock) circuit inside the CS5535. This battery has a 35 mAh capacity. The CS5535 companion device's input current from the battery is 5 µA maximum. The battery should last at least 7000 "system off" hours worst case, but typically lasts much longer.

3.2.7 Universally Unique ID

A 24LC02 EEPROM device is connected on the ACCESS.bus interface providing 256 bytes of non-volatile memory and is intended to provide the system manufacture a unique identification number called Universally Unique Identification (UUID). The device is not write protected so the ID can be in-system erased.

- Connected to ACCESS.bus interface
- Size: 256 Bytes
- 7-bit ACCESS.bus Address: 1010000b

The EEPROM does not have to be used for the UUID. The memory device can be used for whatever the system manufacture wants to use it for. The Realtek Ethernet controller subsystem also has an EEPROM. This device can also hold a unique ID.

3.2.8 SMB Interface

1) Connect to PCI device if SMBus required
2) Pull-up with 2.2K

3.3 Memory Interface

1) Follow *AMD Geode™ GX Processor/CS5535 Companion Device Layout Guidelines* application note (publication #31535).
2) Termination:
   — Series:
     – 43 ohm on all Address and Control signals (near DRAM)
     – 68 ohm on all Data, DQM, and DQS signals (near DRAM)
   — Clocks:
     – No series resistors
     – 120 ohm resistor between differential pair (near DRAM)
3) S3 CKE gate control not required if power sequence is followed.

3.4 JTAG Interface

The JTAG port is connected in a daisy chain mode between the Geode GX processor and the CS5535 companion device. If additional JTAG devices are added to the design, they can also be added to the JTAG daisy chain.

3.5 PCI Interface

The Geode GX processor and CS5535 companion device meet PCI Specification v2.1 criteria.

3.6 Ethernet Controller

For the RDK, an RTL8139D(L) from Realtek was chosen. It is a cost-effective solution and has been proven to be the right fit for the RDK.

The RTL8139D(L) is a highly integrated single-chip fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that are capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management possible. For more information about this device see www.realtek.com.tw.

The board also supports the boot SEEP (serial EEPROM) enabling the RTL8139D Ethernet controller to upload PCI header and other register programming information.

For a custom solution, other Ethernet controllers can be implemented. In general, drivers are supplied by the vendor removing that obstacle. Additional or different system requirements require different solutions. Gig Ethernet, 66 MHz PCI, security, etc. can lead to different choices. Realtek has more ethernet solutions as well as do other vendors.

3.7 Audio Codec

For the GX thin client RDK, an ALC203 audio codec from Realtek was chosen. It is a cost-effective solution and has been proven to be the right fit for the RDK. It is connected to the Geode CS5535 companion device via the AC97 interface. The AC97 interface is fully AC97 compliant, so a host of other audio codecs are also supported.

The ALC203 is a 20-bit DAC and 18-bit ADC full-duplex AC97 v2.3 compatible stereo audio codec designed for multimedia systems, including host/soft audio, and AMR/CNR based designs.

The ALC203 incorporates proprietary converter technology to achieve a high SNR (Signal to Noise Ratio), greater than 100 dB, sensing logics for device reporting, and a universal audio jack for improved user convenience. The ALC203 supports multiple codec extensions with independent variable sampling rates and built-in 3D effects. The ALC203 codec provides two pairs of stereo outputs with independent volume controls, a mono output, multiple stereo and mono inputs, along with flexible mixing, gain, and mute functions to provide a complete integrated audio solution.

The circuitry of the ALC203 codec operates from a 3.3V digital and 3.3V/5V analog power supply with EAPD (External Amplifier Power Down) control. The ALC203 integrates a 50 mW/20 ohm headset audio amplifier into the codec, saving BOM (Bill Of Material) costs. For more information about this device see www.realtek.com.tw.

Note: The CS5535 only supports 16-bit audio.

3.7.1 Microphone

The system has a microphone jack that is internally biased; thus, only an passive microphone should be connected to this jack. A passive microphone does not require a separate power source, whereas a biased microphone does (to provide the bias voltage).

The ALC203 has an analog boost between 6 db and 30 db and an 18-bit ADC on the MIC input.

3.7.2 Headphone and Line Out

Audio out is supported directly using a standard headphone jack. The audio signals to this connector are boosted with a 50 mW amplifier internal to the ALC203 audio codec. The ALC203 utilizes a 20-bit DAC to convert the digital data to analog.

The audio signals pass through the headphone jack to a 4-pin header when headphones are not attached. This connector can be used with a cable to create a LINE OUT connection. The RDK does not use the LINE OUT provided on the ALC203.

The universal audio jack function is not implemented.

3.7.3 Additional Codec Features for a Custom Solution

The ALC203 supports more features than the RDK implements. Some of the additional features are:

- CD and AUX IN - Provides for more analog input to be mixed or played.
- PCBEEP - The CS5535 can output the legacy sound output from the 8254 device, which can be input on this pin.
- SPDIF IN and OUT - Provides support for this standard encoded audio format.
- LINE OUT - Non-amplified audio out.
- Phone - Support for hands free phone. A biased microphone is expected on this input.

3.7.4 Audio Options

For a custom solution, other devices from other vendors can be used. However, not all audio codecs are identical in their programming. Therefore, selecting a different audio codec will likely result is some custom work to the audio driver. The additional features of the ALC203 could also result in additional audio driver custom work.

Wolfson has an audio codec, the WM9712L, that supports touchscreen. This is a unique low cost feature to support a touchscreen requirement.

3.7.5 Audio Design Considerations

1) Verify that a separate ground for audio exists and that the analog audio components tie to this ground. Digital ground should tie into this plane at a single point. **IMPORTANT NOTE**: This should be a wire connection, not a ferrite connection.
2) V_{CC} digital must reach 2.5V before V_{CC} analog. V_{CC} analog can be connected to V_{CC} digital through a 4.7 ohm resistor to achieve this requirement.

3.8 Clocking

3.8.1 Clock Generator

The ICS MK1491-09 is a low cost, low jitter, high performance clock synthesizer for the Geode GX processor. Using patented analog Phase-Locked Loop (PLL) techniques, the device accepts a 14.318 MHz crystal input to produce multiple output clocks. It provides selectable PCI local bus clocks, 48 MHz clocks for SuperI/O and USB, as well as multiple reference outputs. Low EMI Enable reduces EMI radiation on PCI clocks, LCLKs, and the 66 MHz clock by producing a spread spectrum clock. The device also has a power down mode to reduce power consumption. See www.icst.com for details on the clock synthesizer.

Other clock generators could also be used, however, the MK1491-09 is specifically designed to be used with the Geode GX processor/CS5535 companion device. It is unlikely that a more compact and cost-effective solution could be found.

3.8.2 CS5535

The Geode CS5535 requires 32 KHz for proper operation: 32KHZ_XCI (ball A4) and 32KHZ_XCO (ball B3). For the XTAL circuit, a 20M ohm resistor is required. Two 10M ohm resistors in series may be used if a 20M ohm resistor is not available. If driven by an oscillator, the output signal must not be present when there is no VBAT or VIO_VSB or ESD protection diodes could be damaged. 32KHZ_XCO must be a NC (No Connect). in the case of an oscillator.

3.8.3 DRAM Clocks

Unused DRAM clocks will be toggling, therefore they should not have traces as this could impact EMI.

3.9 Keyboard and Mouse

To meet the overall design goals of low cost, the keyboard and mouse are supported via the USB interface. However, if a customer is required to support a PS/2 mouse and keyboard then a LPC SuperI/O device is required. The following companies provide these devices:

- Winbond
- SMSC
- National Semiconductor

3.9.1 PS/2 Keyboard and Mouse Considerations

1) There should be ferrite (90) between MSGND and KBGND signals and digital ground, capable of carrying 1.5 amps minimum.
2) Pull up KBDAT, KBCLK, MSDAT, and MSCLK, even if the PS/2 mouse and/or keyboard ports are not being used.

4.0 Power

The system has been shown to be exceptionally power efficient while performing as a thin client. When running WinBench99® Business Graphics over ICA6.30.1050 in Windows® CE.NET 4.2, the maximum power consumed is less than 5W for the complete system. Overall, both the system's performance and power scored very well. For more information on performance/power contact you local AMD sales office or representative.

4.1 External Power Supply

The system is powered from an external 1.2A, 12V, single output AC-to-DC power brick. If a different supply is used, it must be able to supply at least 1.1A with a voltage between 9V and 16V.

4.2 Internal Voltages

Internally there are four voltages produced: 1.5V, 2.5V, 3.3V, and 5.0V. 1.5V powers the core logic in the Geode GX processor and CS5535 companion device. 2.5V powers the DDR SDRAM interface and the on-board DDR SDRAMs. 3.3V powers most of the remaining devices and interfaces. 5.0V is used to provide USB and VGA power.

4.3 Other Power Considerations

1) CS5535 VSB1: Must be able to supply 5 mA
2) Required power sequence:
   – 3.3V/V_{IO}/V_{CORE} -> V_{MEM}.
3) V_{BAT}: The CS5535 companion device's internal battery circuit is UL approved and therefore does not require a protection resistor. UL file E146664, project 02SC15345.
4) Minimum button push time of 64 µs (this includes power button) is required. Rise time on power button input, must be less than 60 ns.

4.4 Power Button and LED

A power button is located on the front panel. Pressing this button powers on the system. While running, the system Suspends when the power button is pressed for less then four seconds. If pressed for more then four seconds, the system will be held in reset (soft off). The LED will be on.

There are no other power states supported in this system.

A custom solution could support other power states as well as additional LEDs or indicators. For mobile solutions, Low Battery or Sleep indicators might be desired. A separate Sleep button could be implemented along with the power button. These additional features will likely require custom work in drivers or BIOS to be properly supported.

5.0 Debug

While the Geode GX thin client RDK is designed to be a complete solution, some level of debug support is required. Three levels of debug tools are available which have trade-offs between features and cost.

5.1 FS2

The Geode GX processor design team worked with a company, First Silicon Solutions (http://www.fs2.com), to create a very high feature JTAG debugger called the ISA-GEODE.

Special silicon hooks for software debug and system testing have been jointly developed with AMD and are integrated into the processor. These On-Chip Instrumentation (OCI) extensions allow FS2 to provide a powerful debug tool with advanced features at a competitive price. The ISA-GEODE System Analyzer is used for hardware testing and integration, BIOS development, and other firmware/software testing. In addition to hardware and software breakpoints, processor run control, and access to all the CPU registers and coprocessor registers, the FS2 system analyzer has on-chip and off-chip trace features. Trace information is decoded and displayed as executed instructions. Trace can be captured either in on-chip memory (128 x 64-bit frames) or streamed off-chip (64K x 64-bit frames) for collection in the FS2 probe. The trace window displays disassembled instructions interspersed with special messages such as interrupts and exceptions.

The ISA-GEODE System Analyzer is contained in a compact chassis that connects to the target system using a 14-pin debug connector and optional off-chip trace connector. The system runs on a Windows 98/NT/2000/XP PC over an IEEE-1284 EPP/ECP high-speed parallel port or USB port. A graphical, source debugger program provides the user with an intuitive, easy-to-use interface.

5.1.1 Key Features

- Utilizes On-Chip Instrumentation (OCI) debug extensions in the Geode GX processor
- Read/write all CPU registers, Model Specific Registers (MSRs), memory, and I/O
- Go/halt processor run control
- Single step by assembly instruction
- Unlimited software breakpoints
- Real-time on-chip trace standard and optional off-chip trace
- On-chip trace depth 128 x 64-bit frames
- Off-chip trace depth 64K x 64-bit frames
- Support for System Management Mode (SMM), including single stepping through the transition to SMM
- Single step through real mode to protected mode transition while monitoring all register updates
- Flash programming support
- Hardware execution breakpoints using debug registers
- Trigger window for setting complex triggers
- Complex triggers can monitor address and cycle type
- Low-level access to JTAG functions
- Single line assembler and disassembler
- Trace window with full trace decode into instruction mnemonics
- Source window provides execution control: go; halt; goto cursor; step over/into call
- Source window can set or clear software or hardware breakpoints
- Interface driver for kernel level debug with Windows CE Platform Builder and WinDbg with Windows XP/XPe debugging
- Command-line interface with Tcl/tk scripting language standard

5.2 Ethernet

Another option for debugging is via the built-in Ethernet port. This option is supported by OS development tools such as Eboot.

5.3 RS232

The Geode CS5535 companion device has two TX/RX serial ports that can be used for serial debugging. BIOS setup is required.

- Serial port on VGA
- Serial port on JLPC1

6.0 Optional Hardware

This section describes other hardware devices that could be designed into a Geode GX processor/CS5535 companion device-based system.

6.1 Gig Ethernet Controller

To achieve the low cost goals of this design the Realtek RTL8139D(L) was chosen. However, as Gigabit Ethernet solutions become more prevalent, solutions from Realtek (RTL8110SB(L)) and others become viable options. Because the Geode GX processor supports 66 MHz PCI operation, it is able to take full advantage of Gigabit solutions. In fact, many of these solutions are being designed into our next generation solutions today.

6.2 SIO

In order to minimize size and cost, the GX thin client RDK took advantage of available connectivity on the CS5535 to support I/O devices. However, this is a limited set and if a solution requires PS/2 mouse or keyboard, floppy, or parallel port interfaces, then a SuperI/O (SIO) device is required. If this is the case, it is recommended to use an LPC SuperI/O device from Winbond (W83627HF). These devices have already been validated internally on other solutions.

6.3 USB 2.0 Controller

USB 2.0 is becoming a pretty common requirement for thin clients and other products. While the CS5535 does not support USB 2.0 natively, there are a number of PCI based USB 2.0 solutions on the market. The following is a list of ones that we have identified as potential solutions:

- NEC:
  - uPD720101 (see option schematic on Developer Support web site, publication #32731)
- ULi:
  - M5273

6.4 Mass Storage Options

As a Flash port, AMD Spansion™ memory devices and M-Systems DiskOnChip are Flash solutions that can be implemented. While the RDK does not support these options, the CS5535 does. (Schematics are available on the Developer Support web site: publication #32555 and #32732.)

The DiskOnChip device could be used in a custom solution with the device mounted directly on the main board. With a DiskOnChip solution, an LPC boot Flash device is not required. The initial program loader (IPL) code resides in the DiskOnChip device, and this code starts the boot sequence. With the IPL code in the DiskOnChip, there is a considerable cost advantage. However, this interface is slower and less flexible than Flash on the IDE port.

CompactFlash offers the most flexibility at the lowest cost. The CS5535 IDE port supports standard NAND Flash.

Another option is hard drive storage. The Geode GX thin client RDK was designed to operate with laptop hard drives at the cost of two USB ports. If a hard drive and four USB devices are required for an application, then the 5.0V power regulators will need to be redesigned to provide more current.

6.5 Memory Options

For cost, heat, performance and space constraints, the Geode GX thin client RDK uses soldered down DDR SDRAM devices. However, this creates a flexibility and configuration problem. For solutions that require more flexibility but still require a small form factor, it is suggested that DDR SODIMMS be used. For systems that do not require small size, but want memory flexibility, then DDR DIMMS are recommended. In all cases, the Geode GX processor supports unterminated operation which is recommended for the low power and space savings.

7.0 Other

7.1 Thermal Management

Due to its smart design, the thin client RDK does not have any thermal issues. However, the Geode GX processor has been designed to support thermal management devices such as the LM82. For systems that will be operating in extreme temperatures or require even a smaller form factor than the thin client RDK, use of thermal management device should be considered.

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