AMD

# Mobile AMD Athlon™ and Mobile AMD Duron™

# Processor System Requirements

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# Contents

# List of Figures

# List of Tables

# Revision History

| Date | Rev | Description |
|---|---|---|
| August 2000 | A | Initial Release |

# *Application Note*

# Mobile AMD Athlon™ and AMD Duron™ Processor System Requirements

Unless otherwise noted, the information in this application note pertains to all processors in the Mobile AMD Athlon™ and Mobile AMD Duron™ families, which include the Mobile AMD Athlon processor (Model 6) and the Mobile AMD Duron processor (Models 3 and 7).

## Purpose

The purpose of this document is to specify system level power management requirements for Mobile AMD Athlon™ and AMD Duron™ Processor-based notebooks. The scope includes motherboard implementation details and BIOS/Software usage of chipset features.

Because of the critical time to market pressure for Mobile AMD Athlon and Mobile AMD Duron processor-based systems, prototype systems have not been developed to test out the requirements in this document: these required features will be tested as part of the development cycle of the first Mobile AMD Athlon and Mobile AMD Duron processor-based notebooks.

# References

This document specifies mobile system requirements which are in addition to the general requirements. For more details on the general requirements, see the *Motherboard PGA Design Guide*, order #90009

For more information about the Mobile AMD Athlon™ and AMD Duron™ Processor families, refer to the following:

- *Mobile AMD Duron™ Processor Model 3 Data Sheet*, order # 23979
- *Mobile AMD Duron™ Processor Model 7 Data Sheet*, order # 24068
- *Socket A Mobile AMD Athlon™ Processor Data Sheet*, order # 90050
- *Mobile AMD Athlon™ and AMD Duron™ Processors Thermal Design Application Note*, order # TBD
- The ACPI specification, *Advanced Configuration and Interface Specification* Revision 1.0b February 2, 1999

# Critical Differences

There are several key differences between Mobile AMD Athlon and Mobile AMD Duron processors and Mobile AMD-K6® processors that system designers must be aware of. A direct comparison between different Mobile AMD Athlon and Mobile AMD Duron processors can be found in Table 1, "Summary of Critical Features/Differences Between Mobile AMD Processors," on page 5.

1. Processor RESET# and RESET# (PCI RESET#) to the Northbridge are always asserted together. If a RESET# signal to Mobile AMD Athlon and Mobile AMD Duron processors is asserted without asserting RESET# to the Northbridge, the AMD system bus will not connect, and the system will hang. Port 92h and KBC initiated resets must be routed to INIT#.
2. Mobile AMD Athlon and Mobile AMD Duron processor's 100 MHz input clock and the Northbridge's input clock for the AMD system bus interface can NEVER be stopped while in the working state (S0/C [0-3]) or the S1 sleep state. This CPUCLK to Mobile AMD Athlon and Mobile AMD Duron processor and the Northbridge is stopped (powered off) during S3 and deeper sleep states.
3. Mobile AMD Athlon and Mobile AMD Duron processors do not achieve significant power savings when they execute a Halt instruction, or issue a stop grant special cycle in response to STPCLK# assertion.
4. Mobile AMD Athlon and Mobile AMD Duron processors do achieve significant power savings after the AMD system bus is disconnected in response to a Halt special cycle or Stop Grant special cycle. The BIOS must enable halt and stop grant disconnect features in the Northbridge.
5. When the AMD system bus is disconnected, Mobile AMD Athlon and Mobile AMD Duron processor's caches cannot be snooped. AMD system bus must be temporarily reconnected to allow bus master accesses to memory that require cache snoops during C1, C2, and throttling.
6. For the Mobile AMD Athlon and Mobile AMD Duron processors, it is required that all of the VID[4:0] outputs of the processor be used to select the processor's core voltage.

The VID[4:0] codes defined for the Mobile AMD Athlon and Mobile AMD Duron processors must be used. This is discussed later in this document.

7. The Mobile AMD Athlon and Mobile AMD Duron processors dictates its startup frequency. The Mobile AMD Duron processor Model 3's operational Frequency Identification (FID) code dictates the frequency of the Mobile AMD Duron processor core clock grid. The motherboard does not dictate the frequency at which the processor will startup or run (as was the case for the AMD-K6 processor).
8. The Mobile AMD Athlon and Mobile AMD Duron processor core voltage (K7VCC) also powers the AMD system bus and the I/O driver cells for the AMD system bus in the Northbridge. Therefore, the Northbridge current consumption must be taken into account when sizing the K7VCC DC to DC power converter.

## Performance States and AMD PowerNow!™ Technology

Processor performance states are combinations of processor core voltage and core frequency that allow the processor's power consumption to be dynamically reduced when its full computing power (performance) is not required by the applications being run. Performance states can be changed dynamically to allow processor performance to match the demand of the applications being run. Performance states can also be used as part of the thermal management strategy for the system, and to allow the user to specify a preference for silence, or runtime versus performance.

AMD PowerNow! technology is supported by the Mobile AMD Athlon processor Model 6 and the Mobile AMD Duron processor Model 7. AMD PowerNow! technology software enables the most optimal usage of processor performance states.

AMD PowerNow! technology can also be adapted to optimize battery life and performance of Mobile AMD Duron processors with a Model 3 core and/or chipsets that do not support dynamic processor performance state transitions. For these systems, clock throttling can be used to allow performance on demand for optimal user experience. For these systems,

AMD PowerNow! technology may have a different name since voltage and frequency changes are not used.

**Table 1. Summary of Critical Features/Differences Between Mobile AMD Processors**

| | Mobile AMD Duron™ Processor Model 3 | Mobile AMD Duron™ Processor Model 7 | Mobile AMD Athlon™ Processor Model 6 |
|---|---|---|---|
| Integrated L2 | 64 Kbytes | 64 Kbytes | 256 Kbytes |
| On-die Thermal Diode | No | Yes | Yes |
| Supports AMD system bus FID Change protocol for dynamic voltage and frequency changes. | No | Yes | Yes |
| AMD System Bus Data Rate 200 MHz (100 MHz reference clock) | Yes | Yes | Yes |
| Power-up/C3/S1 sleep processor core and AMD System Bus voltage when disconnected **+/- 100 mV**. This is enforced by the motherboard with a VID MUX. Refer to section 2.1 | 1.4 V (investigating lower voltages) | 1.1 V (investigating voltages down to 1.0) | 1.1 V (investigating voltages down to 1.0) |
| Start-up Voltage (Dictated by the processor's VID[4:0] outputs.) | Operational voltage | 1.2 V +/- 100 mV | 1.2 V +/- 100 mV |

***Notes:***

1) *For maximum processor current consumption, and thermal design power targets for Mobile AMD Duron processors refer to the appropriate Mobile AMD Duron processor data sheet.*
2) *The operational voltages listed for Mobile AMD Athlon processor Model 6 and Mobile AMD Duron processor Model 7 are nominal. With AMD PowerNow! technology, the actual voltage that these processors run at will be determined by software based on processor utilization and user preference.*
3) *For Mobile AMD Athlon processor Model 6and Mobile AMD Duron processor Model 7, the start-up voltage and frequency are changed to operational voltage and frequency under software control.*
4) *Below 1.300 V, the Mobile AMD Athlon and Mobile AMD Duron processor's DC to DC converter output can be incremented/decremented in 25 mV steps.*
5) *Power-up and Sleep voltages for Mobile AMD Athlon and Mobile AMD Duron processors are contingent on the chipset also supporting AMD system bus voltages at these levels when the AMD system bus interface is disconnected. Processor data sheets will specify exact operating and sleep voltages supported by the processor.*
6) *CPUID extended function 8000_0007h - Advanced Power Management Feature Flags indicate the presence of mobile features: Thermal Diode, frequency, and voltage control mechanisms as indicated in the table above. These features are present in Mobile AMD Athlon processor Model 6 and Mobile AMD Duron processor Model 7.*
7) *The VID[4:0] codes for all versions of Mobile AMD processors (Mobile AMD Duron processor Model 3, Mobile AMD Duron processor Model 7 and Mobile AMD Athlon processor Model 6) are the same.*
8) *The FID codes for all versions of Mobile AMD Athlon and Mobile AMD Duron processors are the same.*

**Table 1. Summary of Critical Features/Differences Between Mobile AMD Processors (continued)**

| | Mobile AMD Duron™ Processor Model 3 | Mobile AMD Duron™ Processor Model 7 | Mobile AMD Athlon™ Processor Model 6 |
|---|---|---|---|
| Operational processor core and AMD system bus voltage **+/- 100 mV.** *Refer to the processor data sheet for exact operating voltages.* | 1.5 V to 1.3 V (under investigation) | 1.2 V (committed) (investigating voltages down to 1.0) Note voltages above 1.2 volts are also likely. | 1.2 V (committed) (investigating voltages down to 1.0) Note voltages above 1.2 volts are also likely. |
| Start-up Frequency (Dictated by the processor.) | Maximum frequency | 500 MHz | 500 MHz |
| CPUID | 630 | 670 (tentative) | 660 |
| Stop Grant Divisor | 128 | 512 | 512 |

***Notes:***

1) *For maximum processor current consumption, and thermal design power targets for Mobile AMD Duron processors refer to the appropriate Mobile AMD Duron processor data sheet.*
2) *The operational voltages listed for Mobile AMD Athlon processor Model 6 and Mobile AMD Duron processor Model 7 are nominal. With AMD PowerNow! technology, the actual voltage that these processors run at will be determined by software based on processor utilization and user preference.*
3) *For Mobile AMD Athlon processor Model 6and Mobile AMD Duron processor Model 7, the start-up voltage and frequency are changed to operational voltage and frequency under software control.*
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5) *Power-up and Sleep voltages for Mobile AMD Athlon and Mobile AMD Duron processors are contingent on the chipset also supporting AMD system bus voltages at these levels when the AMD system bus interface is disconnected. Processor data sheets will specify exact operating and sleep voltages supported by the processor.*
6) *CPUID extended function 8000_0007h - Advanced Power Management Feature Flags indicate the presence of mobile features: Thermal Diode, frequency, and voltage control mechanisms as indicated in the table above. These features are present in Mobile AMD Athlon processor Model 6 and Mobile AMD Duron processor Model 7.*
7) *The VID[4:0] codes for all versions of Mobile AMD processors (Mobile AMD Duron processor Model 3, Mobile AMD Duron processor Model 7 and Mobile AMD Athlon processor Model 6) are the same.*
8) *The FID codes for all versions of Mobile AMD Athlon and Mobile AMD Duron processors are the same.*

# Mobile AMD Athlon™ and AMD Duron™ Processor Notebook System Hardware Requirements

## Voltage ID (VID) Mux

Mobile AMD Duron processor Model 3 notebooks require a Voltage ID (VID) Mux to be implemented at the motherboard level.

The purposes of the VID Mux are:

1. Provide a deterministic (power-up) core voltage to the Mobile AMD Duron processor Model 3 before it is capable of driving its VID[4:0] outputs to select its startup voltage.
2. Reduce the core voltage of Mobile AMD Duron processor Model 3 during the C3 processor state and the S1 sleep state. This is required because the Mobile AMD Duron processor Model 3 has significant static power dissipation, which can be significantly reduced during the C3 and S1 states by reducing Mobile AMD Duron processor Model 3's core voltage.
3. Allow the processor to control its core voltage during the C0, C1, and C2 processor states. This is required to enable AMD PowerNow! technology / processor driver / operating system control of processor power states.
4. To isolate Mobile AMD Duron processor Model 3's VID[4:0] outputs from voltages above 2.5 volts.

### Deterministic Power Up of K7VCC and Sleep Voltages

K7VCC is the name used throughout this document for the main voltage rail that power Mobile AMD Athlon and Mobile AMD Duron processors. K7VCC powers both the core and I/O of Mobile AMD Athlon and Mobile AMD Duron processors. The following block diagram and timing diagram show conceptually how a notebook PC will be implemented to use Mobile AMD Duron processor's VID[4:0] outputs to control K7VCC during C0, C1 and C2, and how the VID Mux drives a "sleep VID" to the processor DC to DC power converter so that K7VCC is at a deterministic power-up and sleep voltage level at power on and during C3 and S1.

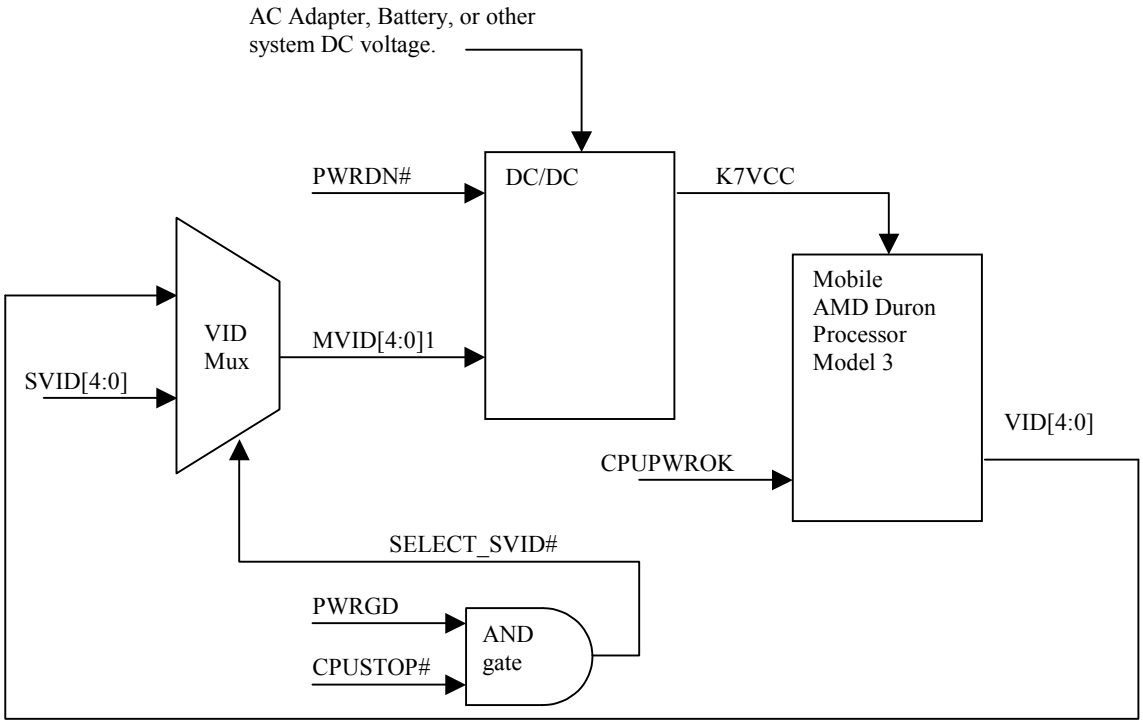


**Figure 1. VID[4:0] Control of K7VCC Block Diagram**

## Mobile AMD Athlon™ Processor Model 5 (K7VCC) DC to DC Control for Notebook PCs

**CPUPWROK** This is driven high to K7VCC after the core voltage is stable at the power-up voltage. Mobile AMD Athlon and Mobile AMD Duron processors use CPUPWROK to set various power-up defaults including the start-up VID[4:0] value.

**VID[4:0]** is the operational VID driven by Mobile AMD Athlon processor Model 5 to control the level of K7VCC. Mobile AMD Athlon processor Model 5 only drives VID[4:0] to the startup voltage after CPUPWROK to Mobile AMD Athlon processor Model 5 is asserted. VID[4:0] are controlled as specified in the Mobile AMD Athlon processor Model 5 specification. Note: that since the VID[4:0] outputs of Mobile AMD Athlon processor Model 5 are 2.5 volt tolerant open drain outputs, external pullups to +2.5 volts are needed, and voltage level shifting may be needed if the VID MUX or equivalent requires greater than 2.5 volts for VIH.

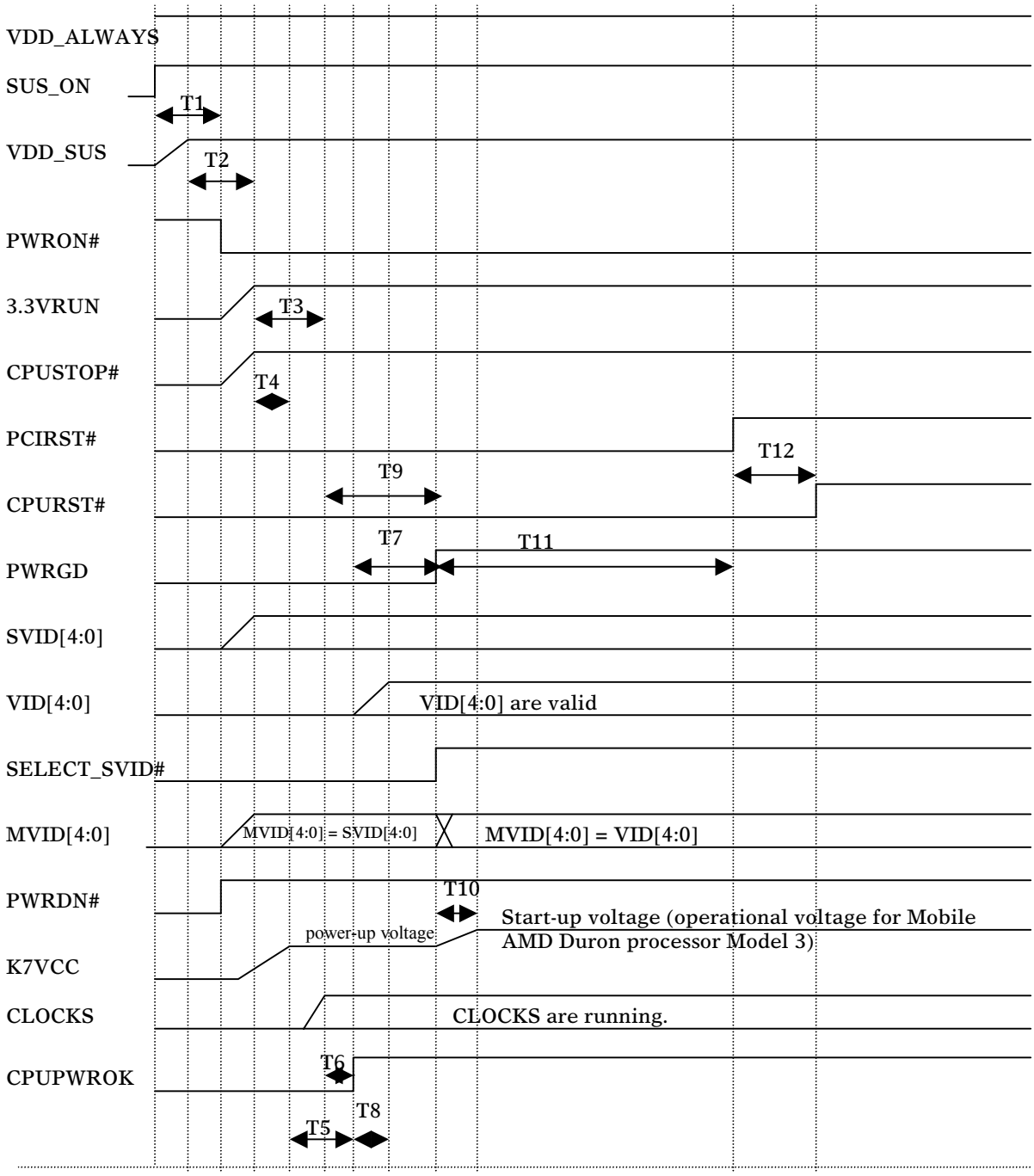


**Figure 2. Deterministic Power-up Sequence for K7VCC Timing Diagram**

**SVID[4:0]** is the Sleep VID set with resistors on the motherboard to dictate the level of K7VCC during:

1. Power on before CPUPWRGD (CPU Power Good) is asserted.
2. The C3 processor state and
3. The S1 sleep state

**MVID[4:0]** is the Multiplexed VID outputs of the VID Mux that are driven as inputs to the DC to DC.

**SELECT_SVID#** acts as the select control input for the VID Mux.

0= MVID[4:0] = SVID[4:0]

1= MVID[4:0} = VID[4:0]

**CPUSTOP#** is a signal from the Southbridge that is driven low during the C3 and S1 sleep states so that SVID[4:0] will be driven to the DC to DC converter on the MVID[4:0] inputs to the DC to DC power converter.

**PWRGD** is the combination of all of the power good indications for the power rails in the system that are powered when the system is operational. This signal ensures that the SVID[4:0] drives the DC to DC power converter before K7VCC is at a level where Mobile AMD Athlon and Mobile AMD Duron processors can deterministically drive their VID[4:0] outputs. This signal also goes to the Southbridge. When asserted, the Southbridge begins its power on reset count for CPURESET# and PCI RESET#.

**PWRDN#** is a control input that when asserted causes the DC to DC power converter to shut off its outputs, and enter a low power sleep state. PWRDN# ensures that the processor is only powered during the S0 and S1 states.

**Table 2. Power-up Timing Requirements**

| | | Minimum | Maximum |
|---|---|---|---|
| T1 | Delay between turning on the "Suspend" planes (SUS_ON high) to turning on "Run" planes (PWRON# low). | 0 ns | |
| T2 | Suspend Voltage Planes are within specification before "Run" voltage planes are within specification. | 0 µs | |
| T3 | 3.3VRUN within specification to all clocks from the clock synthesis chip running within specification. This is based on the spec for existing Mobile AMD Athlon and Mobile AMD Duron processor clock synthesis chips. | | 3.0 ms |
| T4 | 3.3VRUN within spec to K7VCC within spec of the power-up voltage specified by SVID[4:0] as strapped on the motherboard. | 0 µs | |
| T5 | K7VCC within specification at power-up voltage level before CPUPWROK is asserted. This applies to VDDA as well. | 100 µs | |
| T6 | Mobile AMD Athlon and Mobile AMD Duron processor 100 MHz processor clock input must be at 100 MHz and within specification prior to CPUPWROK assertion. | 100 µs | |
| T7 | CPUPWROK assertion to PWRGD assertion. | 20 ns | |
| T8 | CPUPWROK assertion to VID[4:0] being driven to the startup-VID by Mobile AMD Athlon and Mobile AMD Duron processors. Note: since VID[4:0] are 2.5 V tolerant open drain outputs of Mobile AMD Athlon and Mobile AMD Duron processors, transitioning to the startup VID may take longer than 20ns depending on the implementation of the 2.5 V isolation and VID MUX circuitry. | | 20 ns |

***Notes:***

1) *The delay between PWRGD going active and PCIRST# deassertion is 1.8 milliseconds for current AMD chipsets.*
2) *The delay between PCIRST# deassertion and CPURST# deassertion is 1.5 microseconds for current AMD chipsets. This delay could be 0ns.*
3) *CPURST# is never asserted without PCIRST# also being asserted. Therefore the CPURST# duration is always greater than 1.5 milliseconds, and the Northbridge is always reset when the processor is reset.*
4) *The names and polarity of the signals used to turn on the power supplies will vary by chipset and system. What is important here is the general timing relationship between signals.*
5) *Mobile AMD Athlon and Mobile AMD Duron processors have a "ring" oscillator that runs from a fixed 2.5volt supply (VDDA). This VDDA input to the Mobile AMD Athlon and Mobile AMD Duron processors have the same timing requirements as K7VCC.*
6) *CPURST# is required to be asserted before CPUPWROK is asserted. In practice CPURST# should be held low by the Southbridge before the "RUN" planes are turned on.*
7) *DC to DC converters may take several microseconds to significantly change their output voltage in response to changes in their VID[4:0] inputs. Therefore, if it takes several nanoseconds (even 100) to transition between the power-up VID and the startup VID, the voltage output of the DC to DC converter will not change quickly enough to bring K7VCC out of spec.*
8) *Timing for resume from S3 (Suspend to RAM) is the same as power-up timing except that the "Suspend Voltage" planes remain powered throughout S3. PCI RESET# and CPU RESET# are asserted throughout S3.*
9) *Refer to "Appendix C: Standard Power Sequencing Guidelines" on page 47 for definition and description of ALWAYS, RUN, and SUS power planes.*
10) *PWRDN# is functionally the inverse of PWRON#.*

**Table 2. Power-up Timing Requirements (continued)**

| | | Minimum | Maximum |
|---|---|---|---|
| T9 | All system clocks must be running within spec before PWRGD is asserted. | 100 µs | |
| T10 | K7VCC transition time from power-up voltage to start-up voltage. | | 100 µs |
| T11 | PWRGD assertion to PCIRST# de-assertion. | 1.0 ms | |
| T12 | PCIRST# deassertion to CPURST# de-assertion. | 0 ns | |

***Notes:***

1) *The delay between PWRGD going active and PCIRST# deassertion is 1.8 milliseconds for current AMD chipsets.*
2) *The delay between PCIRST# deassertion and CPURST# deassertion is 1.5 microseconds for current AMD chipsets. This delay could be 0ns.*
3) *CPURST# is never asserted without PCIRST# also being asserted. Therefore the CPURST# duration is always greater than 1.5 milliseconds, and the Northbridge is always reset when the processor is reset.*
4) *The names and polarity of the signals used to turn on the power supplies will vary by chipset and system. What is important here is the general timing relationship between signals.*
5) *Mobile AMD Athlon and Mobile AMD Duron processors have a "ring" oscillator that runs from a fixed 2.5volt supply (VDDA). This VDDA input to the Mobile AMD Athlon and Mobile AMD Duron processors have the same timing requirements as K7VCC.*
6) *CPURST# is required to be asserted before CPUPWROK is asserted. In practice CPURST# should be held low by the Southbridge before the "RUN" planes are turned on.*
7) *DC to DC converters may take several microseconds to significantly change their output voltage in response to changes in their VID[4:0] inputs. Therefore, if it takes several nanoseconds (even 100) to transition between the power-up VID and the startup VID, the voltage output of the DC to DC converter will not change quickly enough to bring K7VCC out of spec.*
8) *Timing for resume from S3 (Suspend to RAM) is the same as power-up timing except that the "Suspend Voltage" planes remain powered throughout S3. PCI RESET# and CPU RESET# are asserted throughout S3.*
9) *Refer to "Appendix C: Standard Power Sequencing Guidelines" on page 47 for definition and description of ALWAYS, RUN, and SUS power planes.*
10) *PWRDN# is functionally the inverse of PWRON#.*

### VID[4:0] Control Requirements During C0, C1 and C2

It is required that the Mobile AMD Athlon and Mobile AMD Duron processor's VID[4:0] Outputs control the Mobile AMD Athlon and Mobile AMD Duron processor core voltage during C0, C1 and C2.

As described in the previous section, the VID MUX on the motherboard passes the VID[4:0] outputs of the Mobile AMD Athlon and Mobile AMD Duron processor to the Mobile AMD Athlon and Mobile AMD Duron processor core voltage DC to DC during the C0, C1, and C2 states. It is required that all of the VID[4:0] outputs of Mobile AMD Athlon and Mobile AMD Duron processors are used for Mobile AMD Athlon and Mobile AMD Duron processor-based notebooks. This is required for compatibility with future processor drivers or operating systems that will control Processor Performance States (processor voltage and frequency) in a processor-specific manner that does not vary from system to system. This is also

required for optimal power management of Mobile AMD Athlon and Mobile AMD Duron processor-based notebooks.

## Power-up and Sleep Voltages

The motherboard must be capable of configuring the power-up and sleep voltages from 1.3 V to 1.0 V +/- 100 mV. Note: 1.0 V is in support of the Mobile AMD Duron processor Model 7 and the Mobile AMD Athlon processor Model 6. Because the Mobile AMD Athlon and Mobile AMD Duron processor's DC to DC power converter is capable of selecting voltages in increments of 25 mV, and because the sleep voltage for future Mobile AMD Athlon and Mobile AMD Duron processors is not currently known, the most optimized motherboards will allow for configuring the power-up/sleep voltages in 25 mV increments.

**Mobile AMD Duron™ Processor Model 3**

The Power-up and sleep voltage for Mobile AMD Duron processor Model 3 versions is determined by the processor and the chipset.

The Mobile AMD Duron processor Model 3 power up and sleep voltage is 1.3V +/- 100 mV.

**Mobile AMD Athlon™ Processor Model 6 and Mobile AMD Duron™ Processor Model 7**

The power-up and sleep voltages for Mobile AMD Athlon processor Model 6 and Mobile AMD Duron processor Model 7 are 1.0 V +/- 100 mV. Note: this is the goal and has not yet been proven; therefore, the motherboard must have stuffing options to select higher voltages.

## VID[4:0] Output Voltage Tolerance

The motherboard is required to prevent Mobile AMD Athlon and Mobile AMD Duron processor's VID[4:0] outputs from being pulled to voltages above 2.5 volts. Refer to the Socket A Mobile AMD Athlon™ Processor Data Sheet for the voltage tolerance of all Mobile AMD Athlon and Mobile AMD Duron processor I/O. There are many ways to implement voltage translation; some logic families support this directly. One potential implementation can be found in the AMD Athlon processor PGA design guide, this was implemented for desktop PCs; it is up to the OEM/ODM to determine if this solution is optimal for notebook PCs.

## DC to DC Power Converters

DC to DC power converters must support dynamic voltage transition requirements to enable AMD PowerNow! technology processor performance state transitions in Mobile AMD Athlon and Mobile AMD Duron processor notebooks, and to enable transitions between sleep and operating voltages as controlled by the system using the VID Mux. AMD has a recommended DC to DC design and specification for Mobile AMD Duron processors. Refer to the *Mobile AMD Athlon™ Processor Power Module Design Guide*, publication #24125.

Some of the requirements for this Mobile AMD Athlon and Mobile AMD Duron processor's DC to DC power converters which are met by AMD's recommended solution include:

1. It must be capable of generating all of the voltages that Mobile AMD Athlon and Mobile AMD Duron processors can operate at.
2. It must be capable of continuously supplying Mobile AMD Athlon and Mobile AMD Duron processor maximum current load PLUS the maximum current drawn by the AMD system bus interface on the Northbridge that is also powered by voltage rail that powers Mobile AMD Athlon and Mobile AMD Duron processors (K7VCC). The DC to DC power converters supplying K7VCC in systems capable of supporting the highest frequency Mobile AMD Athlon and Mobile AMD Duron processors are required to be capable of continuously supplying 22 Amps of K7VCC.

3. It should be high efficiency (greater than 90%) when the AMD system bus is connected (the processor is consuming 5Watts or more).
4. The DC to DC power converter is required to transition between the lowest and highest voltage selectable by VID[4:0] within 100 microseconds.
   Note: the Mobile AMD Athlon processor Model 6 and the Mobile AMD Duron processors Model 3 and Model 7 is in the equivalent of a Stop Grant state when VID[4:0] changes occur. See the processor data sheet for Stop Grant current.
   Also note: transitions from higher voltages to lower voltages are not required to complete in 100 microseconds because operation at lower frequencies can occur at higher than the minimum required voltage.
5. A power good indication signal is required for K7VCC (CPU core voltage) which:
   a. Is required not to de-assert based on VID[4:0] dictated voltage transitions. De-assertation of this K7VCC power good will cause the system to reset and is therefore not allowed in response to VID[4:0] dictated transitions.
   b. Has a threshold for assertion and de-assertion lower than the minimum voltage that will ever be selected for Mobile AMD Athlon and Mobile AMD Duron processors. A voltage threshold of 0.9 Volts is therefore recommended.
   c. During initial power-on, this power good signal must not assert until after K7VCC has reached the level specified by the VID[4:0]. This requirement must be verified by system characterization. A delay of 10 milliseconds from K7VCC reaching 0.9 volts to assertion of the K7VCC power good indication signal is recommended and will satisfy this requirement.
   d. This power good indication signal is open collector, and active high (pulled up on the motherboard). This signal is actively driven low when K7VCC is below 0.9 volts.
   e. The *AMD Athlon PGA Design Guide* has a circuit which is recommended for K7VCC power good.

## VID[4:0] Codes Used

It is a requirement that the DC to DC power converter used for K7VCC in Mobile AMD Athlon and Mobile AMD Duron processor-based notebook uses the following VID codes. This is required for compatibility with future Microsoft processor drivers and operating systems that will support processor performance states (voltage and frequency combinations) in a processor specific manner. Supporting these VID codes is also required to enable optimal power management for Mobile AMD Athlon and Mobile AMD Duron processors. These VID codes are used by all versions of Mobile AMD Duron processors, Model 3 and Model 7, and Mobile AMD Athlon processors, Model 5 and Model 6.

The VID codes used by Mobile AMD Athlon and Mobile AMD Duron processor and associated DC to DC power converters for K7VCC core voltage are:

**Table 3. VID Codes used by Mobile AMD Athlon™ and AMD Duron™ Processors**

| VID[4:0] | Voltage selected | VID[4:0] | Voltage selected |
|---|---|---|---|
| 00000 | 2.000 V | 10000 | 1.275 V |
| 00001 | 1.950 V | 10001 | 1.250 V |
| 00010 | 1.900 V | 10010 | 1.225 V |
| 00011 | 1.850 V | 10011 | 1.200 V |
| 00100 | 1.800 V | 10100 | 1.175 V |
| 00101 | 1.750 V | 10101 | 1.150 V |
| 00110 | 1.700 V | 10110 | 1.125 V |
| 00111 | 1.650 V | 10111 | 1.100 V |
| 01000 | 1.600 V | 11000 | 1.075 V |
| 01001 | 1.550 V | 11001 | 1.050 V |
| 01010 | 1.500 V | 11010 | 1.025 V |
| 01011 | 1.450 V | 11011 | 1.000 V |
| 01100 | 1.400 V | 11100 | 0.975 V |
| 01101 | 1.350 V | 11101 | 0.950 V |

**Table 3. VID Codes used by Mobile AMD Athlon™ and AMD Duron™ Processors (continued)**

| VID[4:0] | Voltage selected | VID[4:0] | Voltage selected |
|---|---|---|---|
| 01110 | 1.300 V | 11110 | 0.925 V |
| 01111 | Shutdown | 11111 | Shutdown |

## Processor Temperature Sensor

Using the Maxim 1617 (or similar/equivalent) temperature sensor, a notebook can be designed to support processors that have an on-die thermal diode and processors that do not have an on-die thermal diode. Refer to the Maxim 1617 data sheet for details of the 1617.

### Mobile AMD Athlon™ Processor Model 6 and the Mobile AMD Duron™ Processor Model 7

The Mobile AMD Athlon processor Model 6 and the Mobile AMD Duron processor Model 7 both have an on-die diode for measuring the processor's temperature. Motherboards should use the Maxim 1617 "Remote/Local Temperature Sensor with SMBus Serial Interface" (or equivalent/similar temperature sensor) to read the processor's on-die diode. The Maxim 1617 can read the processor's thermal diode and its own local temperature.

### Mobile AMD Duron™ Processor Model 3

The Mobile AMD Duron processor Model 3 does not have an on-die diode for measuring the processor's temperature. A discrete SOT23 packaged transistor should be used with the MAXIM 1617 temperature sensor (or equivalent), and should be placed in the design such that it can be thermally coupled to the processor and used to measure the processor's temperature. Per the Maxim 1617 data sheet:

> "Temperature accuracy depends on having a good-quality, diode-connected small-signal transistor."

Per the 1617 data sheet, Maxim has tested the following transistors for this purpose:

**Table 4. Recommended Transistors for Accurate Temperature Control**

| Manufacturer | Model Number |
|---|---|
| Central Semiconductor (USA) | CMPT3904 |
| Motorola (USA) | MMBT3904 |

**Table 4. Recommended Transistors for Accurate Temperature Control**

| Manufacturer | Model Number |
|---|---|
| National Semiconductor (USA) | MMBT3904 |
| Rohm Semiconductor (Japan) | SST3904 |
| Samsung (Korea) | KST3904-TF |
| Siemens (Germany) | SMBT3904 |
| Zetex (England) | FMMT3904CT-ND |

This approach leads to the possibility of using the on-die diode with the Mobile AMD Athlon processor Model 6 and the Mobile AMD Duron processor Model 7 versions. The OEM/ODM can choose to implement an alternate solution for monitoring the temperature of a Mobile AMD Duron processor Model 3, but should consider the migration path to using the on-die thermal diode that will be present on the Mobile AMD Athlon processor Model 6 and the Mobile AMD Duron processor Model 7 versions.

## Performance States for Mobile AMD Duron™ Processor Model 3

The Mobile AMD Duron processor Model 3 does not support dynamic core voltage and frequency changes. The AMD system bus FID Change protocol mechanism that allows dynamic processor core voltage and frequency changes is supported only by the Mobile AMD Athlon processor Model 6 and the Mobile AMD Duron processor Model 7.

Not all Mobile AMD Athlon and Mobile AMD Duron processor Northbridges support the AMD system bus FID Change protocol mechanism, for example, some Mobile AMD Duron processor Northbridges intended for use in Desktop PCs.

Notebooks that use Mobile AMD Duron processor Model 3 or chipsets that do not support the AMD system bus FID_Change protocol should implement the following alternate method for enabling the "power on demand" functionality of AMD PowerNow! technology automatic mode. The alternate method for enabling power on demand utilizes throttling of the processor with STPCLK#. Without such a mechanism, battery powered run time of a Mobile AMD Duron processor Model 3

based notebook will be significantly reduced under many operating scenarios.

### Power on Demand Enabled with THERM#

Conceptual Block Diagram of implementation that allows AMD PowerNow! technology power on demand automatic mode functionality by throttling the processor with STPCLK# instead of dynamic voltage and frequency changes (for Mobile AMD Duron processor Model 3).

The AMD PowerNow! technology or similar driver can use a Southbridge GPIO to assert the THERM# input to the Southbridge. Processor performance states can be implemented as follows with throttling. The number of performance states implemented is system specific:

**Table 5. STPCLK# Processor Throttling Performance States**

| Performance State | Performance | Performance State GPO |
|---|---|---|
| 0 | Highest: (no throttling) | Driven high |
| 1 | Throttle 1/8$^{th}$ of the time | Low |
| 2 | Throttle 1/4th of the time | Low |
| 3 | Throttle 3/8ths of the time | Low |
| 4 | Throttle 1/2 of the time | Low |
| 5 | Throttle 5/8ths of the time | Low |
| 6 | Throttle 3/4ths of the time | Low |
| 7 | Lowest: Throttle 7/8ths of the time | Low |

***Notes:***
*A Southbridge-specific register programs throttling duty cycle.*

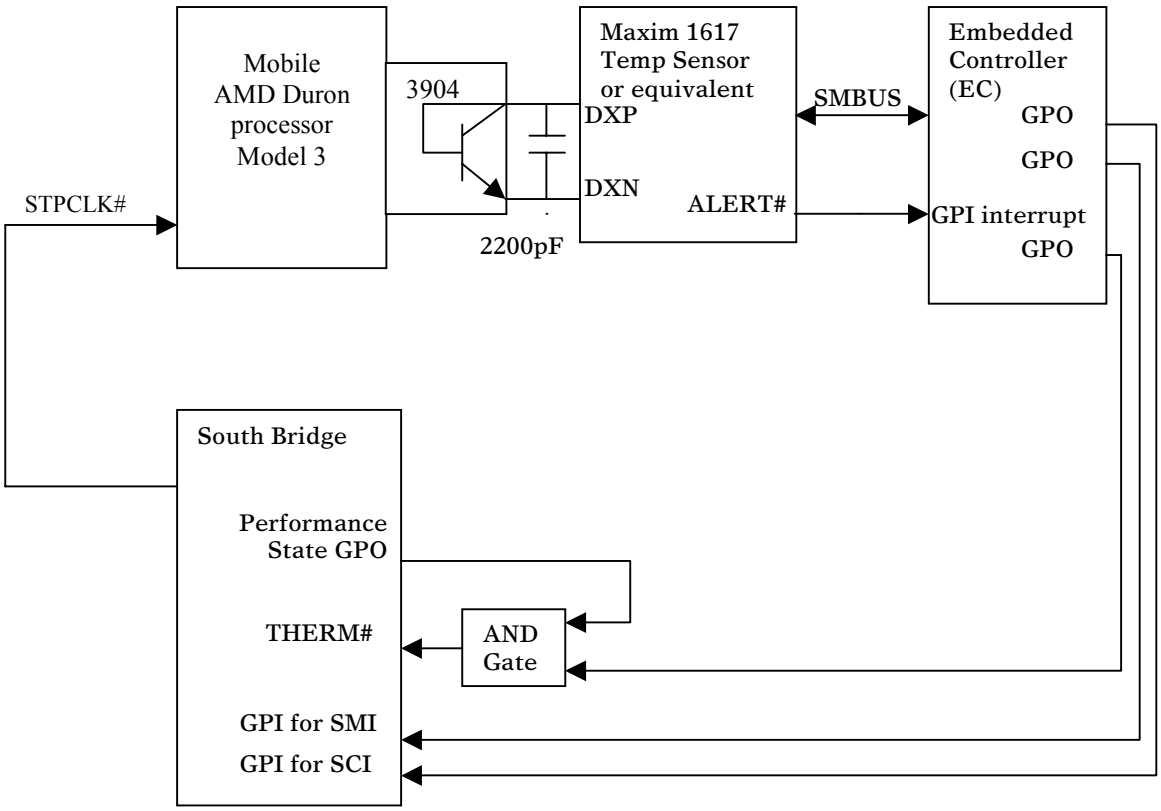


**Figure 3. AMD PowerNow!™ Technology Conceptual Block Diagram**

***Notes:***

1) *AMD PowerNow! technology software would program the THERM# clock throttling duty cycle and then drive the GPO low to force AMD PowerNow! technology throttling.*
2) *THERM# throttling is not the same as clock throttling used by the operating system for ACPI thermal zone throttling. ACPI thermal zone throttling is controlled by the operating system when the BIOS indicates (with _PSV) that the processor has reached a temperature at that the operating system should use throttling to control the processor's temperature. ACPI uses the ACPI defined Processor Control (P_CNT) for throttling the processor. An entirely different non-operating system owned register is used for AMD PowerNow! technology throttling with the Mobile AMD Duron processor Model 3 version.*

## FID[3:0] Output Pins

1. The FID[3:0] outputs are driven to the Northbridge and must be isolated from voltages above 2.5 volts.
2. Refer to the Northbridge data sheet to determine which Northbridge pins the processor FID[3:0] outputs will be muxed onto.
3. The Northbridge only samples its FID[3:0] inputs on the deassertion of RESET#. (RESET# to the Northbridge is functionally the same as the PCI RESET# signal).
4. The Northbridge uses the FID[3:0] sampled on the deassertion of RESET# to determine what the AMD system bus SIP (Serial Initialization Protocol) stream should be for the processor's reported frequency.
5. For dynamic voltage and frequency changes, the FID[3:0] pins do not transmit new information to the Northbridge. The AMD system bus FID Change Special cycle is used for this purpose. Refer to the S*ocket A Mobile AMD Athlon processor Data Sheet* for more details on the AMD system bus FID Change special cycle.
6. Refer to the Mobile AMD Athlon and Mobile AMD Duron processor data sheets for the FID code definitions.

## Thermal Requirements

Mobile AMD Athlon and Mobile AMD Duron processor-based systems are required to have thermal solutions which can keep the processor and all other system components within their specified operating temperatures given a processor power of 24W for thermal design purposes. For more details refer to the *Mobile AMD Athlon™ and AMD Duron™ Processor Thermal Design Application Note*, document #TBD.

# BIOS Requirements

This section is limited to Mobile AMD Athlon™ and AMD Duron™ Processor Power Management requirements for Mobile AMD Athlon and Mobile AMD Duron processor BIOS.

## VID[4:0] codes

These codes are specified in the section entitled *VID[4:0] Codes Used on page 16.*

## Chipset, Processor, and ACPI Table Entry Configuration

In an ACPI controlled system, transitions between ACPI defined power states are controlled by the operating system. Table 6, "Chipset, Processor, and ACPI Table Configuration by the BIOS to Enable ACPI State Support," on page 24 defines:

a. which registers the BIOS must configure in the processor and in the chipset

b. which ACPI defined table entries must be provided by the BIOS to enable the use of the ACPI states listed.

The specific intent is to enable optimal power savings based on the use of the ACPI defined processor power states C1, C2, and C3. Additionally, this table identifies which registers are used by the operating system to force transitions between the ACPI working state and the rest of the ACPI states that are supported by the system.

It is intended that there will be a chipset specific document to accompany the document that provides all of the chipset specific register programming information that is not included in the far-right column of Table 6, "Chipset, Processor, and ACPI Table Configuration by the BIOS to Enable ACPI State Support," on page 24

**Table 6. Chipset, Processor, and ACPI Table Configuration by the BIOS to Enable ACPI State Support**

| ACPI State Name/ Properties / Operating System name | Item # | Function and BIOS Responsibility | BIOS supplied ACPI Table entry/object/control method | Chipset-specific register info |
|---|---|---|---|---|
| C1 / Halt caches snoopable.<br>ACPI places the processor into the C1 state by executing the HLT (halt instruction). | 1 | Enable AMD system bus disconnect on Halt | – | |
| | 2 | **Mobile AMD Duron processor Model 3: BIOS** must program the ClkCtL MSR (C001_001Bh) as follows to select a halt disconnect divisor of 128 and stop grant divisor of 128.<br>Program ClkCtL MSR to 32'h2006_9223<br>**Mobile AMD Athlon processor Model 6 and Mobile AMD Duron processor Model 7: BIOS** must program the ClkCtL MSR (C001_001Bh) to 32'h6007_9263 that selects a Hlt divisor of 128 and a stop grant divisor of 512. | – | – |
| | 3 | **Fixed ACPI Description Table Fixed Feature Flag: PROC_C1** | BIOS builds the Fixed ACPI Description Table before loading the operating system. The PROC_C1 fixed feature flag in this table is set to a 1 by BIOS. | – |

***Notes:***

*1) The Item # field is used to correlate a chipset specific file to this table. VIA, ALI, etc., specific information is in a separate file to accompany this document as appropriate.*

*2) Unless otherwise specified BIOS configures the registers/tables during the POST routine and these settings are not changed during system operation.*

*3) Enabling the C3 processor state requires that the Mobile AMD Athlon and Mobile AMD Duron processor's Northbridge properly implements the ACPI defined PM2_CNT register bit 0 of that is the ARB_DIS (arbiter disable) bit. When the ACPI driver sets the ARB_DIS bit, the Northbridge must stop granting bus masters access to system memory (as the processor caches cannot be snooped during C3. Once the Northbridge has disconnected the AMD system bus in response to a stop grant special cycle when the ARB_DIS bit is set, the Northbridge is not allowed to initiate AMD system bus re-connect, the processor will initiate AMD system bus re-connect once a resume event occurs and STPCLK# has been de-asserted.*

*4) Reducing the Mobile AMD Athlon and Mobile AMD Duron processor's core voltage during C3 is strongly recommended as it significantly reduces the Mobile AMD Athlon and Mobile AMD Duron processor's static power consumption and therefore contributes to system cooling and extended battery powered run-time.*

**Table 6. Chipset, Processor, and ACPI Table Configuration by the BIOS to Enable ACPI State Support (continued)**

| ACPI State Name/ Properties / Operating System name | Item # | Function and BIOS Responsibility | BIOS supplied ACPI Table entry/object/control method | Chipset-specific register info |
|---|---|---|---|---|
| **C2 / Stop Grant caches snoopable.**<br>ACPI places the processor into the C2 state by reading the ACPI defined P_LVL2 register. | 4 | Enable the operating system use of the C2 processor power state. | BIOS specifies a P_LVL2_LAT of<br>5µs for Mobile AMD Duron processor Model 3<br>15µs for Mobile AMD Athlon processor Model 6 and Mobile AMD Duron processor Model 7 in the Fixed ACPI Description Table. | – |
| | 5 | Enable AMD system bus disconnect on Stop Grant | – | |
| | 6 | Enable SDRAM/DDR power-down mode when memory is idle/ Enable self refresh when memory is idle. | – | |
| | 7 | Mobile AMD Duron processor Model 3/ Mobile AMD Athlon processor Model 6/ Mobile AMD Duron processor Model 7 ClkCtL MSR was already configured by BIOS in item 2 above. | – | – |

***Notes:***

1) *The Item # field is used to correlate a chipset specific file to this table. VIA, ALI, etc., specific information is in a separate file to accompany this document as appropriate.*
2) *Unless otherwise specified BIOS configures the registers/tables during the POST routine and these settings are not changed during system operation.*
3) *Enabling the C3 processor state requires that the Mobile AMD Athlon and Mobile AMD Duron processor's Northbridge properly implements the ACPI defined PM2_CNT register bit 0 of that is the ARB_DIS (arbiter disable) bit. When the ACPI driver sets the ARB_DIS bit, the Northbridge must stop granting bus masters access to system memory (as the processor caches cannot be snooped during C3. Once the Northbridge has disconnected the AMD system bus in response to a stop grant special cycle when the ARB_DIS bit is set, the Northbridge is not allowed to initiate AMD system bus re-connect, the processor will initiate AMD system bus re-connect once a resume event occurs and STPCLK# has been de-asserted.*
4) *Reducing the Mobile AMD Athlon and Mobile AMD Duron processor's core voltage during C3 is strongly recommended as it significantly reduces the Mobile AMD Athlon and Mobile AMD Duron processor's static power consumption and therefore contributes to system cooling and extended battery powered run-time.*

**Table 6. Chipset, Processor, and ACPI Table Configuration by the BIOS to Enable ACPI State Support (continued)**

| ACPI State Name/ Properties / Operating System name | Item # | Function and BIOS Responsibility | BIOS supplied ACPI Table entry/object/control method | Chipset-specific register info |
|---|---|---|---|---|
| **C3 / Stop Grant caches not snoopable**<br>ACPI:<br>1) writes a 1 to the PM2_CNT register bit 0 (ARB_DIS) in the Northbridge before entry into C3. (The operating system does this for C3 only.)<br>2) Places the processor into the C3 state by reading the ACPI defined P_LVL3 register.<br>3) Writes a 0 to the PM2_CNT register bit 0 in IGD4 upon exit from C3.<br>*(Continued on the next page)* | 8 | Mobile AMD Duron processor Model 3/ Mobile AMD Athlon processor Model 6/ Mobile AMD Duron processor Model 7 ClkCtL MSR was already configured by BIOS in item 2 above. | – | – |
| | 9 | Enable the operating system use of the C3 processor power state. | BIOS specifies a P_LVL3_LAT of<br>a) 200µs to 900µs in the Fixed ACPI Description Table. If the chipset and system supports C3 and the processor voltage will be reduced during C3.<br>b) 15µs if the chipset/system does not support reducing the processor voltage during C3.<br>c) Greater than 1000µs if the chipset does not support the C3 state. | – |
| | 10 | AMD system bus disconnect on Stop Grant by the Northbridge was already enabled by the BIOS in item 5 above. | – | – |

***Notes:***

1) *The Item # field is used to correlate a chipset specific file to this table. VIA, ALI, etc., specific information is in a separate file to accompany this document as appropriate.*
2) *Unless otherwise specified BIOS configures the registers/tables during the POST routine and these settings are not changed during system operation.*
3) *Enabling the C3 processor state requires that the Mobile AMD Athlon and Mobile AMD Duron processor's Northbridge properly implements the ACPI defined PM2_CNT register bit 0 of that is the ARB_DIS (arbiter disable) bit. When the ACPI driver sets the ARB_DIS bit, the Northbridge must stop granting bus masters access to system memory (as the processor caches cannot be snooped during C3. Once the Northbridge has disconnected the AMD system bus in response to a stop grant special cycle when the ARB_DIS bit is set, the Northbridge is not allowed to initiate AMD system bus re-connect, the processor will initiate AMD system bus re-connect once a resume event occurs and STPCLK# has been de-asserted.*
4) *Reducing the Mobile AMD Athlon and Mobile AMD Duron processor's core voltage during C3 is strongly recommended as it significantly reduces the Mobile AMD Athlon and Mobile AMD Duron processor's static power consumption and therefore contributes to system cooling and extended battery powered run-time.*

**Table 6. Chipset, Processor, and ACPI Table Configuration by the BIOS to Enable ACPI State Support (continued)**

| ACPI State Name/ Properties / Operating System name | Item # | Function and BIOS Responsibility | BIOS supplied ACPI Table entry/object/control method | Chipset-specific register info |
|---|---|---|---|---|
| *(Continued from previous page)*<br><br>**C3 / Stop Grant caches not snoopable**<br><br>**ACPI**:<br>1) writes a 1 to the PM2_CNT register bit 0 (ARB_DIS) in the Northbridge before entry into C3. (The operating system does this for C3 only.)<br>2) Places the processor into the C3 state by reading the ACPI defined P_LVL3 register.<br>3) Writes a 0 to the PM2_CNT register bit 0 in IGD4 upon exit from C3. | 11 | BIOS configures Northbridge registers to enable maximum Northbridge power savings during C3. | – | |
| | 12 | BIOS configures Southbridge registers to enable reduction in processor voltage during the C3 state. | – | |

***Notes:***

1) *The Item # field is used to correlate a chipset specific file to this table. VIA, ALI, etc., specific information is in a separate file to accompany this document as appropriate.*
2) *Unless otherwise specified BIOS configures the registers/tables during the POST routine and these settings are not changed during system operation.*
3) *Enabling the C3 processor state requires that the Mobile AMD Athlon and Mobile AMD Duron processor's Northbridge properly implements the ACPI defined PM2_CNT register bit 0 of that is the ARB_DIS (arbiter disable) bit. When the ACPI driver sets the ARB_DIS bit, the Northbridge must stop granting bus masters access to system memory (as the processor caches cannot be snooped during C3. Once the Northbridge has disconnected the AMD system bus in response to a stop grant special cycle when the ARB_DIS bit is set, the Northbridge is not allowed to initiate AMD system bus re-connect, the processor will initiate AMD system bus re-connect once a resume event occurs and STPCLK# has been de-asserted.*
4) *Reducing the Mobile AMD Athlon and Mobile AMD Duron processor's core voltage during C3 is strongly recommended as it significantly reduces the Mobile AMD Athlon and Mobile AMD Duron processor's static power consumption and therefore contributes to system cooling and extended battery powered run-time.*

**Table 6. Chipset, Processor, and ACPI Table Configuration by the BIOS to Enable ACPI State Support (continued)**

| ACPI State Name/ Properties / Operating System name | Item # | Function and BIOS Responsibility | BIOS supplied ACPI Table entry/object/control method | Chipset-specific register info |
|---|---|---|---|---|
| **S1 / Power On Suspend / Standby**<br>**ACPI** places the system into the S1 state by writing the value specified in the _S1object to the SLP_TYP field and writing the SLP_EN bit to a one. The 3 bit SLP_TYP field and SLP_EN bit are in the ACPI defined PM1 control register. | 13 | | **BIOS** provides a _S1 object to the operating system that specifies a SLP_TYP[2:0] value that is chipset specific. | |
| | 14 | AMD system bus disconnect on Stop Grant by the Northbridge was already enabled by the BIOS in item 5 above. | – | |
| | 15 | BIOS configures the Southbridge to enable processor voltage to be reduced during S1. | – | |
| | 16 | BIOS configures the Northbridge registers to enable maximum power savings during S1. | – | |
| **S2: ABSOLUTELY NOT SUPPORTED**<br>Mobile AMD Athlon and Mobile AMD Duron processors cannot be reset independently of the Northbridge | – | – | – | – |

***Notes:***

1) *The Item # field is used to correlate a chipset specific file to this table. VIA, ALI, etc., specific information is in a separate file to accompany this document as appropriate.*
2) *Unless otherwise specified BIOS configures the registers/tables during the POST routine and these settings are not changed during system operation.*
3) *Enabling the C3 processor state requires that the Mobile AMD Athlon and Mobile AMD Duron processor's Northbridge properly implements the ACPI defined PM2_CNT register bit 0 of that is the ARB_DIS (arbiter disable) bit. When the ACPI driver sets the ARB_DIS bit, the Northbridge must stop granting bus masters access to system memory (as the processor caches cannot be snooped during C3. Once the Northbridge has disconnected the AMD system bus in response to a stop grant special cycle when the ARB_DIS bit is set, the Northbridge is not allowed to initiate AMD system bus re-connect, the processor will initiate AMD system bus re-connect once a resume event occurs and STPCLK# has been de-asserted.*
4) *Reducing the Mobile AMD Athlon and Mobile AMD Duron processor's core voltage during C3 is strongly recommended as it significantly reduces the Mobile AMD Athlon and Mobile AMD Duron processor's static power consumption and therefore contributes to system cooling and extended battery powered run-time.*

**Table 6. Chipset, Processor, and ACPI Table Configuration by the BIOS to Enable ACPI State Support (continued)**

| ACPI State Name/ Properties / Operating System name | Item # | Function and BIOS Responsibility | BIOS supplied ACPI Table entry/object/control method | Chipset-specific register info |
|---|---|---|---|---|
| **S3 / Suspend to RAM / Stand by**<br>**ACPI** places the system into the S3 state by writing the value specified by the _S3 object into the SLP_TYP field and writing the SLP_EN bit to a one. | 17 | | **BIOS** provides a _S3 ACPI object to the operating system that specifies a SLP_TYP[2:0] value that is chipset specific. | |

***Notes:***

1) *The Item # field is used to correlate a chipset specific file to this table. VIA, ALI, etc., specific information is in a separate file to accompany this document as appropriate.*
2) *Unless otherwise specified BIOS configures the registers/tables during the POST routine and these settings are not changed during system operation.*
3) *Enabling the C3 processor state requires that the Mobile AMD Athlon and Mobile AMD Duron processor's Northbridge properly implements the ACPI defined PM2_CNT register bit 0 of that is the ARB_DIS (arbiter disable) bit. When the ACPI driver sets the ARB_DIS bit, the Northbridge must stop granting bus masters access to system memory (as the processor caches cannot be snooped during C3. Once the Northbridge has disconnected the AMD system bus in response to a stop grant special cycle when the ARB_DIS bit is set, the Northbridge is not allowed to initiate AMD system bus re-connect, the processor will initiate AMD system bus re-connect once a resume event occurs and STPCLK# has been de-asserted.*
4) *Reducing the Mobile AMD Athlon and Mobile AMD Duron processor's core voltage during C3 is strongly recommended as it significantly reduces the Mobile AMD Athlon and Mobile AMD Duron processor's static power consumption and therefore contributes to system cooling and extended battery powered run-time.*

**Table 6. Chipset, Processor, and ACPI Table Configuration by the BIOS to Enable ACPI State Support (continued)**

| ACPI State Name/ Properties / Operating System name | Item # | Function and BIOS Responsibility | BIOS supplied ACPI Table entry/object/control method | Chipset-specific register info |
|---|---|---|---|---|
| | 18 | | **BIOS** provides a _S4 ACPI object to the operating system that specifies a SLP_TYP[2:0] value that is chipset specific. | |
| **S4 / Suspend to Disk / Hibernate**<br>**ACPI** places the system into the S4 state by writing the value specified by the _S4 object into the SLP_TYP field and writing the SLP_EN bit to a one. | 19 | To support S4 under BIOS control with Windows® 95 and Windows® 98 the BIOS specifies the S4BIOS_F flag = 1, and S4BIOS_REQ value in the Fixed ACPI description table.<br>In this case, BIOS in SMM mode is responsible for saving and restoring the system memory image to and from disk. | **BIOS** provides S4BIOS_REQ that is the value to write to SMI_CMD to enter the S4BIOS state. The S4BIOS state provides an alternate way to enter the S4 state where the firmware saves and restores the memory context. A value of zero in S4BIOS_F indicates S4BIOS_REQ is not supported. | |
| | 20 | S4 is supported under operating system control for Windows®2000 and subsequent operating system releases. | **BIOS** returns control to the operating system upon resume from S4, and the operating system restores the system memory image from disk. | – |

***Notes:***

1) *The Item # field is used to correlate a chipset specific file to this table. VIA, ALI, etc., specific information is in a separate file to accompany this document as appropriate.*
2) *Unless otherwise specified BIOS configures the registers/tables during the POST routine and these settings are not changed during system operation.*
3) *Enabling the C3 processor state requires that the Mobile AMD Athlon and Mobile AMD Duron processor's Northbridge properly implements the ACPI defined PM2_CNT register bit 0 of that is the ARB_DIS (arbiter disable) bit. When the ACPI driver sets the ARB_DIS bit, the Northbridge must stop granting bus masters access to system memory (as the processor caches cannot be snooped during C3. Once the Northbridge has disconnected the AMD system bus in response to a stop grant special cycle when the ARB_DIS bit is set, the Northbridge is not allowed to initiate AMD system bus re-connect, the processor will initiate AMD system bus re-connect once a resume event occurs and STPCLK# has been de-asserted.*
4) *Reducing the Mobile AMD Athlon and Mobile AMD Duron processor's core voltage during C3 is strongly recommended as it significantly reduces the Mobile AMD Athlon and Mobile AMD Duron processor's static power consumption and therefore contributes to system cooling and extended battery powered run-time.*

**Table 6. Chipset, Processor, and ACPI Table Configuration by the BIOS to Enable ACPI State Support (continued)**

| ACPI State Name/ Properties / Operating System name | Item # | Function and BIOS Responsibility | BIOS supplied ACPI Table entry/object/control method | Chipset-specific register info |
|---|---|---|---|---|
| **S5 / Soft Off / Shut down**<br>**ACPI** places the system into the S5 state by writing the value specified by the _S5 object into the SLP_TYP field and writing the SLP_EN bit to a one. | 21 | | **BIOS** provides a _S5 ACPI object to the operating system that specifies a SLP_TYP[2:0] value that is chipset specific. | |

***Notes:***

1) *The Item # field is used to correlate a chipset specific file to this table. VIA, ALI, etc., specific information is in a separate file to accompany this document as appropriate.*
2) *Unless otherwise specified BIOS configures the registers/tables during the POST routine and these settings are not changed during system operation.*
3) *Enabling the C3 processor state requires that the Mobile AMD Athlon and Mobile AMD Duron processor's Northbridge properly implements the ACPI defined PM2_CNT register bit 0 of that is the ARB_DIS (arbiter disable) bit. When the ACPI driver sets the ARB_DIS bit, the Northbridge must stop granting bus masters access to system memory (as the processor caches cannot be snooped during C3. Once the Northbridge has disconnected the AMD system bus in response to a stop grant special cycle when the ARB_DIS bit is set, the Northbridge is not allowed to initiate AMD system bus re-connect, the processor will initiate AMD system bus re-connect once a resume event occurs and STPCLK# has been de-asserted.*
4) *Reducing the Mobile AMD Athlon and Mobile AMD Duron processor's core voltage during C3 is strongly recommended as it significantly reduces the Mobile AMD Athlon and Mobile AMD Duron processor's static power consumption and therefore contributes to system cooling and extended battery powered run-time.*

## BIOS Requirements for Mobile AMD Duron™ Processor Model 3

For the chipset–specific registers for control of THERM# initiated throttling for enabling STPCLK# based performance states, refer to the chipset–specific document that compliments this document for VIA, ALI, etc. for chipset–specific register programming information.

## BIOS Requirements for Mobile AMD Athlon™ Processor Model 6 and Mobile AMD Duron™ Processor Model 7

Refer to See “Chipset, Processor, and ACPI Table Entry Configuration” on page 23 and the chipset specific documentation.

## ACPI Thermal Zone Implementation for Mobile AMD Athlon™ and AMD Duron™ Processor

This section will be written in a later revision of this document.

# Appendix A: ACPI state transitions

Note: In this document signals named DCSTOP#, CPUSTOP#, RUNON, and PWRON#, etc., will have different names but similar functionality and slightly different timing in various chipsets.

Also, note that the S2 state is not supported by Mobile AMD Athlon and Mobile AMD Duron processor systems, because it is not possible to reset Mobile AMD Athlon and Mobile AMD Duron processors without also resetting the Northbridge. The industry as a whole does not use the S2 state because it does not provide significant power savings over the S1 sleep state.

## C1 Processor Halted: Caches Snoopable

When the processor is idle, ACPI will place the processor into the C1 state (halt).

**The sequence is as follows:**

1. The operating system determines that processor is idle.
2. The operating system reads ACPI defined PM_TMR in the Southbridge.
3. The operating system executes a HLT instruction.
4. Processor halts.
5. Processor issues a Halt special cycle on the AMD system bus.
6. Northbridge passes the halt special cycle to the PCI bus although no other device in the system uses the PCI halt special cycle.
7. When no probe activity (snoops of the processor cache etc.) is required of the processor, the Northbridge will disconnect the AMD system bus.
8. The Northbridge will continue to grant the PCI bus and AGP bus to PCI and AGP masters, and will retry any PCI cycles that require a snoop of the processor's caches. If bus master activity requires a snoop of the processor caches, the

Northbridge must reconnect the AMD system bus to service the bus master activity, and will retry the PCI bus cycle while the AMD system bus is reconnecting.

9. When probe activity ceases again, the Northbridge will disconnect the AMD system bus again.
10. When the processor receives an interrupt, it will initiate an AMD system bus connect (if currently disconnected) and then issue a connect special cycle.
11. The processor will service the interrupt, and continue execution.

## C2 Processor Power State: Stop Grant, Caches Snoopable.

**The following sequence is associated with the C2 state:**

1. The operating system determines that the processor is idle.
2. The operating system reads the ACPI defined PM_TMR in the Southbridge.
3. The operating system reads the ACPI defined P_LVL2 register in the Southbridge.
4. The Southbridge asserts STPCLK# to the processor.
5. The processor enters the stop grant state.
6. The processor issues a Stop Grant special cycle on the AMD system bus.
7. The Northbridge disconnects the AMD system bus when probe activity ceases.
8. The Northbridge passes the Stop Grant special cycle to the PCI bus.
9. The Southbridge recognizes the Stop Grant special cycle and recognizes that the processor is in a Stop Grant state.
10. The Southbridge recognizes a resume event (an interrupt for example).
11. The Southbridge deasserts STPCLK# to the processor and asserts INTR to the processor.
12. The processor reconnects the AMD system bus.
13. The operating system reads the PM_TMR in the Southbridge.

Note: that if during C2 while the AMD system bus is disconnected, if the Northbridge receives bus master request (from a PCI bus master for example) the Northbridge must:

1. Grant the bus master request, but re-try the PCI bus master initiated cycle while the AMD system bus is disconnected.
2. Initiate an AMD system bus connect sequence so that it can probe the processor's caches.
3. Service the bus master requested access to memory.
4. After all bus master activity stops, the Northbridge must disconnect the AMD system bus again to enable the processor to return to its power saving state.

## C3 Processor Power State: Stop Grant Caches NOT Snoopable

C3 like C1 and C2 is an ACPI defined processor power saving state that occurs during the working state. During C1, C2, C3 the system appears on and working to the user. The user has no indication that the processor is entering and exiting the C1, C2, and C3 processor power saving states.

**The following sequence is associated with C3:**

1. The operating system determines the processor is Idle.
2. The operating system determines that all bus masters are idle by reading the ACPI defined BM_STS bit in the PM1_STS register in the Southbridge. If the BM_STS bit is 1 then there is bus master activity, and the operating system will use the C2 processor state instead of the C3 processor state. If the BM_STS bit is 0 then no Bus Master activity is occurring, and the operating system can proceed with entering the C3 processor state.
3. The operating system writes the ACPI defined ARB_DIS bit in the PM2_CNT register to a 1 to prevent bus masters from being granted the PCI and AGP busses. The ARB_DIS bit and PM2_CNT register reside in the Northbridge.
4. The operating system reads the ACPI defined PM_TMR (power management Timer) in the Southbridge.
5. The operating system reads the ACPI defined P_LVL3 register in the Southbridge.
6. The Southbridge asserts STPCLK# to the processor.

7. The Northbridge disconnects the AMD system bus. (The Northbridge can place system memory into self-refresh mode before passing the stop grant special cycle to the PCI bus.)
8. The Northbridge passes the stop grant special cycle to the PCI bus.
9. The Southbridge recognizes the stop grant special cycle and asserts DCSTOP# to the Northbridge.
10. The Southbridge asserts CPUSTOP# to force the VID MUX to select the Sleep VID[4:0] that causes the DC to DC to drive the processor to its sleep voltage during C3.
11. The Southbridge can use PCI CLKRUN# protocol to stop the PCI clock during the C3 state.
12. The Southbridge or the Northbridge can use STPAGP# and AGPBUSY# to stop the AGP clock during C3.
13. A resume event is detected by Southbridge. (This could be an interrupt a bus master request, or any other enabled resume event.)
14. The Southbridge de-asserts CPUSTOP# that forces the K7VCCDC/DC to ramp K7VCCback up to the voltage specified by Mobile AMD Athlon and Mobile AMD Duron processor's VID[4:0] outputs.
15. The Southbridge de-asserts DCSTOP# to the Northbridge.
16. The processor ramps its core grid back up to operating frequency and then initiates AMD system bus connect.
17. The Southbridge de-asserts STPCLK# to the processor as well as the PCISTP# and STPAGP# signals if asserted.

The following timing diagram shows the timing requirements associated with C3 and reducing the Processor voltage during C3:

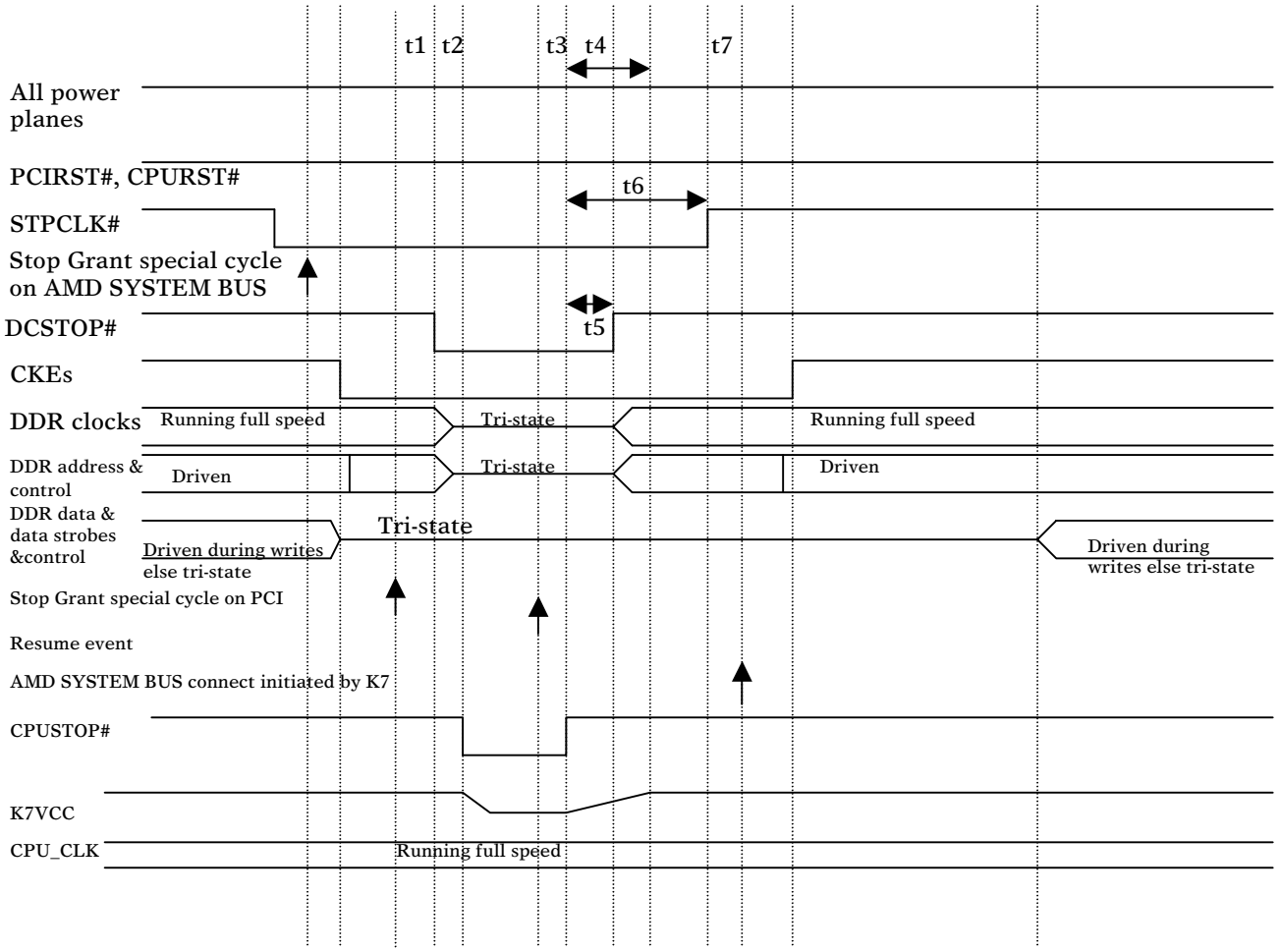


**Figure 4. C3 State with Processor Voltage Reduction Timing Diagram**

***Notes:***

1) *Not drawn to scale*
2) *CPU_CLK cannot be stopped to processor or AMD system bus.*
3) *If the AMD system bus sequences an STP_AGP# signal to the external AGP graphics device for stopping the AGP clock during C3, this signal must be asserted for two RTC clocks (which is about 61us) before the AGP clock to the graphics chip is stopped. The ability to stop the AGP clock during C3 is dependent on the chipset implementation, the clock synthesis chip, and the graphics chip all supporting this.*
4) *The AGP device must also provide an AGP_BUSY# signal which must be asserted anytime the AGP device needs the AGP clock to be running, specifically when it needs to access memory which will cause a probe of the processor's caches. This AGP_BUSY# signal like all PCI REQ# signals must force the ACPI defined BM_STS bit in the AMD system bus to be asserted went AGP_BUSY# is asserted. BM_STS is used by the operating system to determine whether or not to use the C3 processor state, and is also used to exit the C3 processor state.*

**Table 7. C3 Timing**

| | | Minimum | Maximum | Notes |
|---|---|---|---|---|
| t1 | Stop Grant special cycle on PCI to DCSTOP# assertion | 1RTC clock period (30.5 µs) | | |
| t2 | DCSTOP# assertion to CPUSTOP# assertion. When CPUSTOP# is asserted, the VID Mux selects the Sleep VID[4:0]. | 0 ns | | |
| t3 | Resume event to CPUSTOP# de-assertion | 0 ns | | |
| t4 | CPUSTOP# deassertion to K7VCC transition from C3/sleep voltage to operating voltage complete. When CPUSTOP# is de-asserted, the VID Mux selects the processor VID[4:0] outputs. | | 100 µs | 1 |
| t5 | CPUSTOP# deassertion to DCSTOP# deassertion | 0 ns | | |
| t6 | CPUSTOP# deassertion to STPCLK# deassertion | 200 µs | | 2 |
| t7 | Approximate delay from STPCLK# deassertion to processor initiating AMD system bus reconnect. | 5 µs. (divide by 128) | 15 µs. (divide by 512) | |

***Notes:***

1) *It is required that the DC to DC for Mobile AMD Athlon and Mobile AMD Duron processors be capable of transitioning from the C3/S1 voltage to the processor-specified voltage within 100µs of CPUSTOP# being de-asserted.*
2) *The period between CPUSTOP# deassertion and STPCLK# deassertion is dictated by t4 and the time it takes from DCSTOP# deassertion to the Northbridge clocks running. 200µs gives significant margin assuming that t4 is met, and the Northbridge clocks are gated, but no PLL re-sync time is required.*
3) *Chipset vendors with alternate timing should discuss this with your AMD representative.*

### STP_AGP# and AGP_BUSY# and Stopping the AGP Clock During C3.

Stopping the AGP clock during C3/S1 depends on support from the chipset. Stopping the AGP clock can save a small number of milliwatts and is an optimization not a required feature.

If it is desirable to stop the AGP# clock to the graphics chip, some graphics vendors support an AGP_BUSY#/STP_AGP# protocol. If this AGP_BUSY# protocol is to be used, then:

1. AGP_BUSY# assertion must cause BM_STS assertion in the Southbridge's ACPI PM1_STS register. This can be accomplished by connecting AGP_BUSY# to a PCI REQ# input on the Southbridge that will cause BM_STS to be asserted when AGP_BUSY# is asserted.

2. STP_AGP# can be connected to a signal from the Southbridge that is asserted on entry to C3, S1 and deeper sleep states. It is required that at least a two RTC clock delay (61µs) is inserted between STPAGP# assertion and the AGP clock to the graphics chip being stopped.

## S1 Sleep State (Power On Suspend / Stand by).

The Windows® operating systems refer to S1 as Stand by.

**S1 Facts:**

1. The display is black and the system appears off to the user except for an LED/LCD to indicate the system is in a sleep state.
2. The operating system calls all device drivers and places all devices into D3 before placing the system into S1. This prevents all bus master activity.
3. The operating system does not use the ACPI defined ARB_DIS (arbiter disable) bit in the PM2_CNT (power Management 2 Control) register during the S1 state.
4. The processor and Northbridge 100 MHz input clocks from the clock synthesis chip run throughout the S1 state.
5. CPUSTOP# or equivalent signal is used to select the sleep voltage for the processor during the S1 state.
6. The PCI clock will be stopped during S1 (this comes for free with PCI CLKRUN# protocol).
7. No resets are asserted during or upon exiting the S1 sleep state.
8. The operating system writes the SLP_TYP[2:0] field to the value specified by the _S1 object and writes the SLP_EN bit to a one in the ACPI defined PM1_CNT (power management 1 control register) to place the system into the S1 sleep state.

**S1 entry /exit sequence:**

1. The operating system determines or is prompted to place the system into the S1 sleep state (The operating system calls this Stand by).
2. The operating system calls all drivers of all devices to place them into the D3 state.

3. The operating system reads the PM_TMR in the Southbridge
4. The operating system writes _S1 value to the SLP_TYP[2:0] field and writes SLP_EN bit to a 1 in the Southbridge PM1_CNT register.
5. Southbridge asserts STPCLK# to the processor.
6. Processor enters Stop Grant state.
7. Processor issues Stop Grant special cycle on the AMD system bus.
8. Northbridge allows AMD system bus to disconnect.
9. Northbridge places memory in self refresh mode.
10. Northbridge issues Stop Grant special cycle on the PCI bus.
11. Southbridge asserts DCSTOP# to the Northbridge to reduce the Northbridge power consumption. The Northbridge uses this signal to:
    a. Tri–state DDR signals except for CKEs. This saves termination resistor power for all DDR signals including DDR clocks.
    b. Gate internal clocks for lowest possible power consumption.
12. Southbridge asserts CPUSTOP# to cause K7VCC to be reduced to the sleep level.
13. Southbridge also asserts PCISTOP# to the clock synthesis chip to stop the PCI clocks with the exception of possibly a free running PCI clock that some Southbridges require during the S1 sleep state.

**The exit from S1 is as follows:**

1. An enabled resume event is detected.
2. PCISTOP# and CPUSTOP# are de-asserted.
3. DCSTOP# is de-asserted.
4. After a delay sufficient for K7VCCto ramp back up to its operational level (as dictated by the processor's VID[4:0] outputs), STPCLK# is asserted.
5. The processor ramps its clock grid back to its operational frequency.

6. The processor initiates an AMD system bus connect and continues code execution.

The timing diagram for the S1 sleep state is the same as for the C3 power state, except that the PCI clocks will definitely be shut off since all wake-up events are from PME#, power button, LID switch, etc. and do not require the PCI clock.

## S3 Sleep State Support (Suspend to RAM/Stand by)

Windows operating systems refer to S3 as Stand by.

Support for the S3 state is optional for Mobile systems per the PC2001 Design Guide Rev 0.7.

**If S3 is implemented, the following applies:**

1. PCI RESET# and CPU RESET# are asserted before power is removed from the "RUN" planes.
2. S3 saves significant power when compared to S1.

**The sequence for entry to S3 is as follows:**

1. The operating system determines or is prompted to place the system into the S3 sleep state (The operating system calls this Stand by).
2. The operating system calls all drivers of all devices to place them into the D3 state.
3. The operating system writes the SLP_TYP[2:0] and SLP_TYP fields in the Southbridge PM1_CNT register with the value specified by the _S3 object supplied by the BIOS.
4. Southbridge asserts STPCLK# to the processor.
5. Processor enters Stop Grant state.
6. Processor issues Stop Grant special cycle on the AMD system bus.
7. Northbridge allows AMD system bus to disconnect.
8. Northbridge places memory in self-refresh mode.
9. Northbridge issues Stop Grant special cycle on the PCI bus.
10. Southbridge asserts DCSTOP# to the Northbridge to reduce the Northbridge power consumption. The Northbridge uses this signal to:

a. Tri-state DDR signals except for CKEs. This saves termination resistor power for all DDR signals including DDR clocks.

b. Gate internal clocks for lowest possible power consumption.

c. Isolates logic that will be powered off (Run planes) from logic that will remain powered (Suspend planes).

11. One RTC clock later the Southbridge asserts PCI RESET# and CPU RESET#.

12. One RTC clock after asserting PCI RESET#, the Southbridge de-asserts PWRON# to turn off the "Run planes". Suspend and Always planes remain powered. CPU RESET# and PCI RESET# remain asserted by the Southbridge throughout S3.

**The resume sequence from S3 is as follows:**

1. An enabled resume event is detected by the Southbridge. This could be a sleep button press or function key combination on the internal keyboard of the notebook.
2. The Southbridge asserts PWRON# to turn the run planes back on. Resume sequencing from S3 is the same as power up sequencing described in section 2.1.1 except that the Suspend planes are powered throughout the S3 state as is required to keep system memory in self refresh mode. The duration of the resume sequence is determined by the power good indications for the "run" planes, as it is at power on.
3. After the power-up reset sequence completes, the processor will fetch code from its reset vector and BIOS POST routine code will be executed.
4. BIOS will determine that this is a resume from S3, sequence system memory out of self-refresh mode, and return control to the operating system by jumping to the Firmware Waking Vector provided by the operating system in the ACPI Fixed Description Table.
5. The operating system loads the drivers for all of the devices, handles the wake event, and resumes execution.

## ACPI S4 (Suspend to Disk, Hibernate) Support.

Windows operating systems refer to S4 as Hibernate. There are two types of support for S4, S4BIOS and S4OS. Windows® 98 and previous operating systems support S4BIOS in which the BIOS is responsible for saving the system memory image to the hard disk. Windows® 2000 and subsequent operating systems use S4OS in which the operating system is responsible for saving and restoring the system memory image to and from the hard disk.

As in the S3 case, PCIRST# and CPURST# are asserted before power is removed from the "Run" planes, in the S4 case however, the Suspend planes (which power system memory and a portion of the Northbridge) are also powered off. Thus during S4 only the "always" planes are powered. Typically, the always planes power a portion of the embedded controller such that battery management can occur during the S4 state, as well as monitoring the power button.

## ACPI S5 (Soft Off, Shutdown) Support

The S5, Soft Off, state is very similar to the S4 state from a hardware perspective, however the system context is not saved to the hard disk, all resume events are disabled except power button, and a full POST and operating system Boot is required when S5 is exited.

# Appendix B: ACPI Required Registers

## ACPI Required Registers in Northbridges

Section "4.7.3.4 Power Management 2 Control (PM2_CNT)" of the ACPI 1.0b defines the PM2_CNT register and the ARB_DIS (arbiter disable) bit. Northbridges are required to implement the PM2_CNT register and ARB_DIS bit so that the C3 state can be used.

When the ARB_DIS bit is set, once the Northbridge disconnects the AMD system bus in response to the stop grant special cycle, it must not initiate an AMD system bus reconnect, only the processor is allowed to initiate an AMD system bus reconnect in this case. (The processor will initiate an AMD system bus reconnect in response to the Southbridge de-asserting STPCLK#.)

## ACPI Required Registers in Southbridges

The following sections of the ACPI 1.0b specification describe required "Fixed Feature" registers that must be implemented in the Southbridge. These registers are owned by the ACPI driver, and must not be written by non-ACPI driver or operating system software. Refer to the ACPI 1.0b specification for more details regarding these registers.

4.7.3.1.1 Power Management 1 Status Registers

4.7.3.1.2 Power Management 1 Enable Registers

4.7.3.2.1 Power Management 1 Control Registers

4.7.3.3 Power Management Timer (PM_TMR)

The Power Management Timer is clocked from a free running oscillator that is asynchronous to the processor clock and system bus. The first revision of all chipsets have failed to properly implement this timer because they have not taken into account that accesses initiated by the processor occur asynchronously to the timer count. Failures reading this timer have resulted when a processor read (via the PCI Bus) occurs when the PM_TMR register is being up-dated.

It is the responsibility of the chipset manufacturer to ensure that reads of the PM_TMR not to return invalid count information if the read occurs at the same time that the counter is incrementing.

Chipset vendors must ensure that reads of the PM_TMR always return valid data.

System vendors must verify that the chipset they select properly implements the PM_TMR register.

4.7.3.5 Processor Register Block (P_BLK)

4.7.3.5.1 Processor Control (P_CNT): 32

4.7.3.5.2 Processor LVL2 Register (P_LVL2): 8

Reads of this register place the processor into the C2 state.

4.7.3.5.3 Processor LVL3 Register (P_LVL3): 8

Reads of this register place the processor into the C3 state.

4.7.4.1.1.1 General-Purpose Event 0 Status Register

4.7.4.1.1.2 General-Purpose Event 0 Enable Register

**System Reset Register**

The Southbridge also needs a register in I/O space or PCI configuration space that can be written to cause a full system reset (CPU RESET# and PCI RESET# assertion).

For this purpose, Intel and AMD Southbridges have a system reset that can be initiated by a write to I/O address CF9h that is an 8 bit reset register. 3rd party chipset company's should only use CF9h if they have cross license agreements with Intel that allow them to copy Intel chipset features.

# Appendix C: Standard Power Sequencing Guidelines

Notebook PCs have more power planes than ever. Questions about what the required power sequence is come up each time AMD designs a chip or a motherboard. To ensure that the power sequence requirements for various chips work with each other in the context of a PC, we need to agree on standard power sequencing guidelines that AMD, 3rd party Chip, motherboard, and power supply vendors can depend on and design to. These basic guidelines should be followed.

**Terminology:**

There are 3 classes of power planes in PCs: always planes, run planes, and suspend planes.

**Always planes** for notebook PCs are derived from the AC adapter/main battery voltage. Always planes include 5VALW (typically to the embedded controller), +3.3VAUX to mini PCI slots (also referred to as 3VDUAL), and 2.5VAUX (and lower voltages) that will be used by the future Southbridge/I/O hub devices. Always planes are powered during the S0 (working), S1 (Power on Suspend/Standby), S3 (Suspend to RAM/Standby), S4 (Suspend to Disk/Hibernated, and S5 (Softies) states. Always planes are not powered during G3 (Mechanical Off). Always planes can be switched to derive their power from a run plane during the S0 and S1 states, as is the case with 3VDUAL.

**Run planes** for notebook PCs are generally derived from the suspend voltage outputs of the system's DC to DC converters. For example, 3.3VRUN and 5VRUN are derived from 3.3VSUS and 5VSUS through FETs. Run planes are powered during the S0 and S1 states. All run planes are powered off during the S3, S4, S5, and G3 states. Examples of run voltages include the processor core voltage (for the processor and AMD system bus), VCC_AGP, and 3.3VRUN for the PCI bus.

**Suspend planes** are powered during S0, S1, and S3. Suspend planes are derived from the AC adapter input/Main battery output. An example of a suspend planes include VCC_2.5, DDR_VREF, and VTTDDR that power part of the Northbridge and the DDR SDRAM.

Note: some systems append ALW, RUN, or SUS to the name of each power plane to identify the class of plane.

Guidelines AMD should follow and have third parties follow:

1. Always planes are powered before Suspend planes.
2. Suspend planes are powered before Run planes.
3. Higher voltages are powered before lower voltages for a given class of power plane (always, run, or suspend).
4. Note: “before” allows for voltage planes to be ramping up at the same time, but ensures that the sequence is not reversed.
5. Devices must be designed to accommodate operation given these power-sequencing guidelines. This includes ensuring that a device will not have problems (including CMOS latchup) based on the sequencing called out by items 1 through 3.
6. Devices like Northbridges that use a suspend plane must limit their suspend plane power consumption during power-on when the run planes are not yet powered to close to their S3 state power consumption.

**Examples of these guidelines already in use:**

1. DDR SDRAM require that their 2.5 volt VDD inputs are powered before their 1.25 volt VREF inputs are powered. This is an example of higher voltages being powered before lower voltages within a given class of power plane.
2. 3.3VRUN is powered before K7VCC.