# Stratix 10 MX (DRAM System-in-Package) Product Table

| | Product Line | MX 1100 | MX 1650 | MX 1650 | MX 2100 | MX 2100 |
|---|---|---|---|---|---|---|
| **Resources** | Logic elements (LEs)[1] | 1,092,000 | 1,624,000 | 1,624,000 | 2,005,000 | 2,005,000 |
| | Adaptive logic modules (ALMs) | 370,080 | 550,540 | 550,540 | 679,680 | 679,680 |
| | ALM registers | 1,480,320 | 2,202,160 | 2,202,160 | 2,718,720 | 2,718,720 |
| | Hyper-Registers from HyperFlex™ architecture | Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric | | | | |
| | Programmable clock trees synthesizable | Hundreds of synthesizable clock trees | | | | |
| | HBM2 high-bandwidth DRAM memory (GBytes) | 4 | 8 | 16 | 8 | 16 |
| | eSRAM memory blocks | 1 | 2 | 2 | 2 | 2 |
| | eSRAM memory size (Mb) | 45 | 90 | 90 | 90 | 90 |
| | M20K memory blocks | 4,401 | 5,851 | 5,851 | 6,501 | 6,501 |
| | M20K memory size (Mb) | 86 | 114 | 114 | 127 | 127 |
| | MLAB memory size (Mb) | 6 | 8 | 8 | 11 | 11 |
| | Variable-precision digital signal processing (DSP) blocks | 2,520 | 3,145 | 3,145 | 3,744 | 3,744 |
| | 18 x 19 multipliers | 5,040 | 6,290 | 6,290 | 7,488 | 7,488 |
| | Peak fixed-point performance (TMACS)[2] | 10.1 | 12.6 | 12.6 | 15.0 | 15.0 |
| | Peak floating-point performance (TFLOPS)[3] | 4.0 | 5.0 | 5.0 | 6.0 | 6.0 |
| **I/O and Architectural Features** | Secure device manager | AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection | | | | |
| | Hard processor system[4] | Quad-core 64 bit ARM® Cortex®-A53 up to 1.5 GHz with 32 KB I/D cache, NEON™ coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I²C x5, general-purpose timers x7, watchdog timer x4 | | | | |
| | Maximum user I/O pins | 448 | 592 | 592 | 592 | 592 |
| | LVDS pairs 1.6 Gbps (RX or TX) | 216 | 288 | 288 | 288 | 288 |
| | Total full duplex transceiver count | 48 | 96 | 96 | 96 | 96 |
| | Dual mode 56Gbps PAM-4 / 30 Gbps NRZ transceiver count | 0 | 48 | 48 | 48 | 48 |
| | GXT NRZ transceiver count (up to 30 Gbps) | 48 | 48 | 48 | 48 | 48 |
| | PCI Express® (PCIe®) hard intellectual property (IP) blocks (Gen3 x16) | 2 | 2 | 2 | 2 | 2 |
| | 100G Ethernet MAC + FEC hard IP blocks | 0 | 8 | 8 | 8 | 8 |
| | Memory devices supported | DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys | | | | |
| **Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count[5, 6]** | | | | | | |
| F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch) | | 448,16,216,48 | – | – | – | – |
| F2912 pin (55 mm x 55 mm, 1.0 mm pitch) | | – | 592,16,288,96 | 592,16,288,96 | 592,16,288,96 | 592,16,288,96 |

Notes:

1. LE counts valid in comparing across Altera devices, and are conservative vs. competing FPGAs.
2. Fixed-point performance assumes the use of pre-adder.
3. Floating-point performance is IEEE 754 compliant single precision.
4. Quad-core ARM Cortex-A53 hard processor system present in all Stratix® 10 MX devices.
5. A subset of pins for each package are used for high-voltage, 3.0 V and 2.5 V interfaces.
6. All data is preliminary, and may be subject to change without prior notice.

592,16,288,96  Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

━━━━━  Indicates pin migration path.

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| Product Line | MX 1100 | MX 1650 | MX 2100 |
|---|---|---|---|
| Processor | | Quad-core 64 bit ARM Cortex-A53 MPCore™ processor | |
| Maximum processor frequency | | 1.5 GHz[1] | |
| Processor cache and co-processors | | L1 instruction cache (32 KB)<br>L1 data cache (32 KB)<br>Level 2 cache (1MB) shared<br>Floating-point unit (FPU) single and double precision<br>ARM Neon™ media engine<br>ARM CoreSight™ debug and trace technology<br>System Memory Management Unit (SMMU)<br>Cache Coherency Unit (CCU) | |
| Scratch pad RAM | | 256 KB | |
| HPS DDR memory | | DDR4, DDR3, and LP DDR3 [Up to 64 bit with error correction code (ECC)] | |
| Direct memory access (DMA) controller | | 8 channel | |
| EMAC | | 3X 10/100/1000 EMAC with integrated DMA | |
| USB on-the-go (OTG) controller | | 2X USB 2.0 OTG with integrated DMA | |
| UART controller | | 3X UART 16550 compatible | |
| Serial peripheral interface (SPI) controller | | 4X SPI | |
| I²C controller | | 5X I²C | |
| Quad SPI flash controller | | 1X SIO, DIO, QIO SPI flash supported | |
| SD/SDIO/MMC controller | | 1X eMMC 4.5 with DMA and CE-ATA support | |
| NAND flash controller | | 1X ONFI 1.0 or later<br>8 and 16 bit support | |
| General-purpose timers | | 4X | |
| Software-programmable general-purpose I/Os (GPIOs) | | Maximum 62 GPIOs | |
| Direct shared I/Os | | 48 I/Os to connect HPS peripherals directly to I/O | |
| Watchdog timers | | 4X | |
| Security | | Secure boot, Advanced Encryption Standard (AES), secure hash algorithm, and secure device manager | |

Notes:
1. With overdrive feature.

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