Stratix™ Memory Board 2

April 2004, VER. 0.3 Datasheet

Introduction

The Stratix™ Memory Board 2 (SMB2) is a demonstration board designed to showcase high-speed memories (DDR-II SDRAM and QDR-II SRAM) with the Stratix™ FPGA using Intellectual Property (IP). It will also be the Applications Characterization platform and a Demonstration platform for Field Application Engineering for the Stratix™ FPGA device. Designers can use the Stratix™ Memory Board 2 to prototype and develop high-speed applications for Stratix™ FPGAs interfaces with DDR-II x 16 SDRAM, QDR-II x 18 SRAM, DDR-II SDRAM DIMM Module, Flash, or SRAM memories.

Features

The Stratix™ Memory Board 2 (SMB2) is intended for testing, demonstrating and characterizing high-speed memory controller IP using Altera's Stratix ™ FPGA. This section lists the elements included on the board

Devices

The Stratix™ Memory Board 2 (SMB2) contains one Stratix™ device. The bottom banks of the Stratix™ device interface to DDR-II SDRAM operating at 200 MHz (400 Mb/s/pin) and QDR-II SRAM operating at 200 MHz (400 Mb/s/pin) and the top banks interface to a DDR-II SDRAM DIMM Module operating at 200 MHz (400 Mb/s/pin). There is a Flash ROM controlled by a MAX CPLD to program the Stratix™ device. There is 1MB of asynchronous SRAM, a 10/100 Ethernet port, and 2 RS-232 ports for communications.

One Altera Stratix™ FPGA Device (EP1S40F1020-C5)

- 80 transmit and 80 receive source synchronous channels
- 1,020-pin FineLine BGA package
- 41,250 LEs
- 3,423,744 RAM bits (417KB)
- 12 PLLs (8 Fast and 4 Enhanced)
- 10 transmit and 10 receive medium speed channels
- 112 DSP block 9-bit elements
- 781 user I/O
- SMA interfaces for external I/O

One Altera MAX™ CPLD Device (EPM7256AETC144)

Memory Devices

- Two Micron Technology DDR-II SDRAM, 16M x 16 Memory Devices (MT47H16FG-5E)
- Two Cypress Semiconductor QDR-II SRAM, 1M x 18 Memory Devices (CY7C1313V18-200BZC)
- One DDR-II SDRAM DIMM Module, 32M x 72, Memory Device (MT9HTF3272-40E)
- One Flash 128Mb Memory Device (AM29LV128MH113REI)
- Two SRAM 256K x 16 Memory Devices (IDT71V416S10PH)

Configuration

Configuration of the board includes mulitple modes for programming for the Stratix™ and MAX devices on the board.

- The Flash will be used to store configuration data or be used as non-volatile memory.
- Configuration interfaces include fast passive parallel/passive serial and JTAG connectors for configuration using the ByteBlaster™ II cable.
- Switches to select different configuration modes.
- 10/100 Ethernet connection for remote/local updates for configuration purposes through the RJ-45 connector.

Clocks

Clocks are generated using on-board crystal oscillators and clock drivers or external clocks can be provided through SMA connectors. Each board contains three crystal oscillators.

- External clocks via SMA
- Clocks via on-board oscillators and clock drivers
- Clock outputs to SMAs for test/trigger
- A divide-by-20 circuit uses a high-speed external clock as input through an SMA.
- A divide-by-2 circuit is useful in SFI-5 applications.

Interfaces

The Stratix™ FPGA device interfaces to several different external memories at various data rates.

- Two DDR-II SDRAM running at 150 MHz.
- Two QDR-II SRAM running at 167 MHz.
- DIMM socket using DDR-II SDRAM running at 150 MHz.
- Two SRAM Memory
- One Flash Memory
- 10/100 Ethernet media access control physical interface (MAC PHY) using an RJ-45 connector for the cable connection.

Digital Analysis/Instrumentation Connections

In addition, the Stratix™ have source synchronous connections to connectors such as SMAs for high-speed interfaces.

- RS-232 Interface for debug and register access
- Tektronix and Agilent logic analyzer connectors

Power

Power will be brought in through a 9V-20V DC adapter power jack or individual banana jacks for the unregulated power sources.

- Regulators
- Banana jacks for the unregulated power sources
- Socketed fuses switch between banana jacks and regulated power coming from on-board regulators

User I/O Formats

- Eight User LEDs
- Two seven-segment displays

- Sixteen switches for user logic functions
- Six push buttons for user logic functions

Expansion Interfaces

- One 80-pin right angle expansion header (J51) for connection to Stratix II configuration boards
- Three Proto Headers (J31, J32, J37) for use with the Santa Cruz board

General Description

The Stratix™ Memory Board 2 (SMB2) is a demonstration board designed to showcase high-speed memories (DDR-II SDRAM and QDR-II SRAM) with the Stratix™ FPGA using Intellectual Property (IP). It will also be the Applications Characterization platform and a Demonstration platform for Field Application Engineering for the Stratix™ FPGA device. Designers can use the Stratix™ Memory Board 2 to prototype and develop high-speed applications for Stratix™ FPGAs interfaces with DDR-II x 16 SDRAM, QDR-II x 18 SRAM, DDR-II SDRAM DIMM Module, Flash, or SRAM memories. Use of this board can shorten the time to market for applicable designs. The board can demonstrate several IP cores, such as double data rate (DDR) SDRAM, quad data rate (QDR) SRAM, RS-232, and Nios® microprocessors.

Designers can use the SMB2 to prototype and verify high-speed designs that use Altera® devices. The high-speed transceivers are divided up and routed to different I/O connectors for high-speed interfaces. The board can be used stand-alone or plugged into a connector compatible backplane.

Components and Interfaces

Figure 1 shows a top view of the Stratix™ Memory Board 2.

Figure 1. Stratix™ Memory Board 2 Components & Interfaces

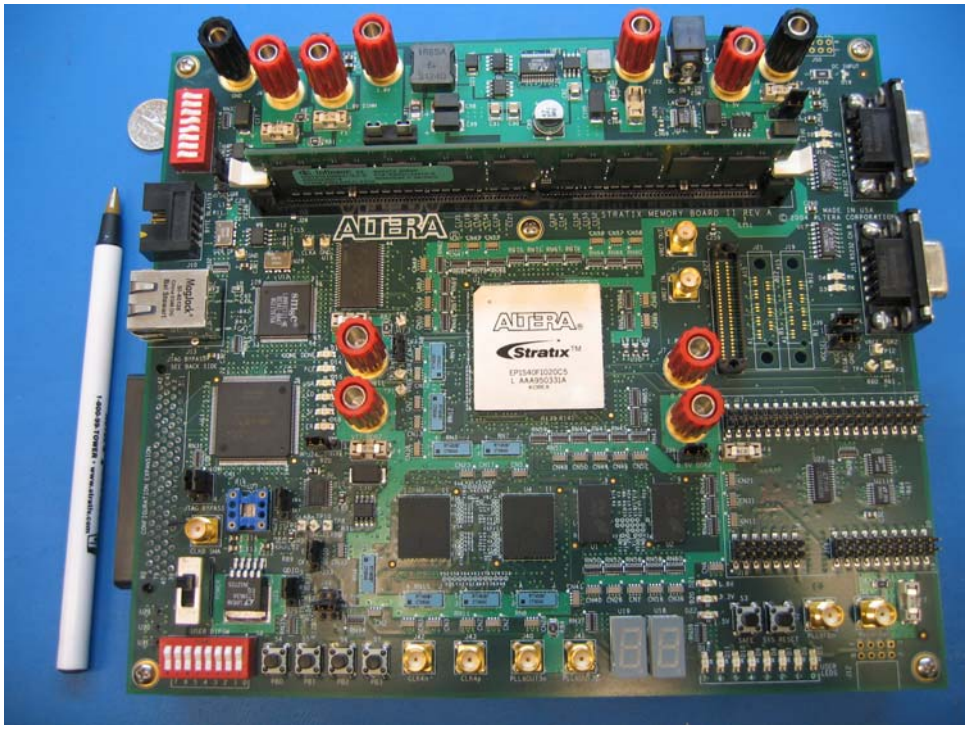


Table 1 describes the major components on the SMB2 and the related interfaces.

Table 1. SMB2 Components and Interfaces

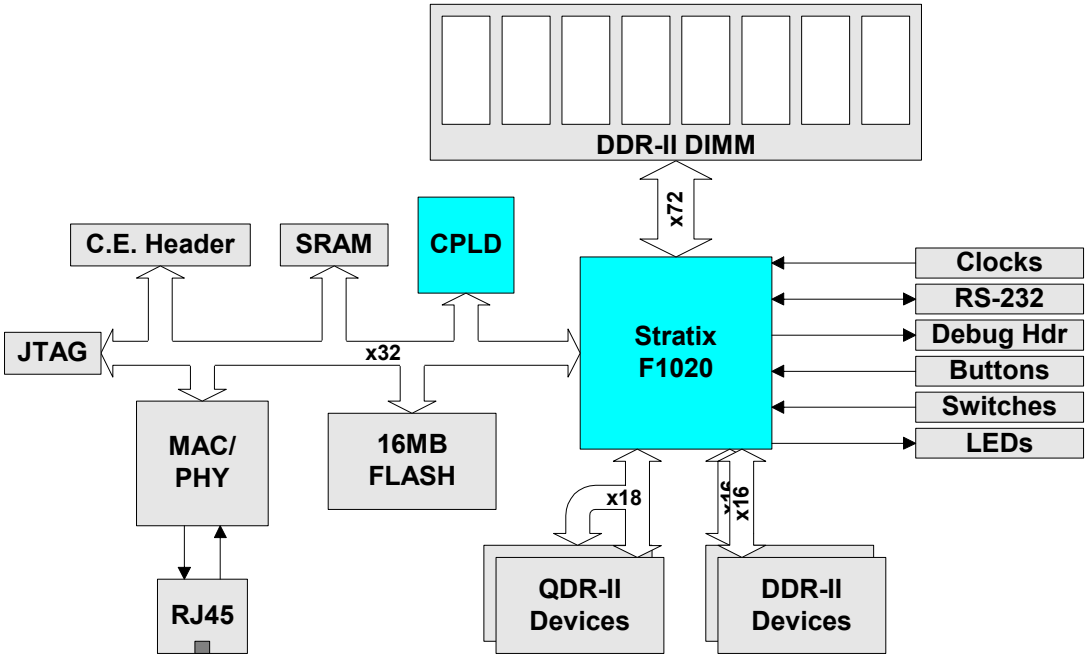
Type	Component/ Interface	Board Reference	Description
FPGA	Stratix ™ device	U7	Altera Stratix ™ device, FBGA-1020, EP1S40F1020-C5
Memory	DDR-II SDRAM	U1, U2	Micron 16M x 16, 200MHz, 1.8V, FBGA-84, MT47H16M16FG-5E
	QDR-II SRAM	U3, U4,J49	Cypress 1M x 18, 200MHz, 1.4V-1.9V, FBGA-165, CY7C1313V18-200BZC
	DDR-II SDRAM DIMM Module	J28	Micron 32M x 72, 200MHz, 1.8V, 240-pin DIMM, MT8HTF3272AG-40E
	Flash	U14	AMD 128 Mb, 8M x16 TSOP-56, AM29LV128MH113REI
	SRAM	U13, U15	Cypress 4Mb, 256K x 16, TSOPII-44, CY7C1041CV33-10ZC
Configuration	MAX CPLD	U11,J48	Altera MAX™ CPLD device, 144-pin TQFP, EPM7256AETC144,
	Level Translators	U29,U30,U31	1.8V to 3.3V level translators for PGM signals
	JTAG	J10,J11,J12,J27, J50	JTAG test and interface select control by jumper and ByteBlaster
	DIP Switches	S1	Configuration DIP switches. Refer to Control section in this table and see Tables 11.
	Pushbuttons	S2-S7	Configuration pushbuttons. Refer to Control section in this table and see Table 13.
Clock	System Clock OSC.	U26,U9:Buffer	33.33 MHz clock oscillator and buffer
	High-speed Clock Oscillator	U27,U10,J23, J24,J25,J26,J39	100.00 MHz clock oscillator and buffer
Control	System Reset Pushbutton	S2,U32	Reset hardware and reconfigure Stratix device. U32 is the pushbutton debouncer for all pushbuttons.
	Safe Pushbutton	S3	Safe Mode, loads the Stratix™ with factory default configuration
	DIP Switch	S1	Configuration DIP switch settings. See Tables 11
User Settings/ Indictors	User DIP Switches	S8	User defined octal DIP switches
	User Pushbuttons	S4,S5,S6,S7	User defined pushbuttons
	7-Segment Displays	U18,U19	User 2-digit 7-segment displays
	User LEDs	D5,D6,D7, D8,D9,D10, D11,D12	Eight yellow user defined LEDs. LEDs are lit when logic 0 is driven to them.
Configuration Indictors	Status LEDs	D13,D14,D15, D16,D17,D18	CONFIG_DONEn, FLASH_CEn, USER_DESIGNn, LOADINGn, SAFE_DESIGNn, ERRORn
Power Indictors	DC Input OK	D19	Blue LED used to indicate that the board input power is OK
	3.3V Power	D20	Green LED used to indicate 3.3V power is good
	1.8V Power	D21	Green LED used to indicate 1.8V power is good
	1.5V Power	D22	Green LED used to indicate 1.5V power is good
Power	3.3V, 1.8V Power	U23,J1,J2,J5,J7, J30,J31,J34,J35	Dual Switching regulator for the 3.3V and 1.8V power supplies
	1.5V Power	U24,J9,J32	Switching regulator for the 1.5V power supply
	1.5V/1.8V Power	U25,J3,J29,J33	Adjustable linear regulator for the QDR-II IO power supply

Table 1. SMB2 Components and Interfaces			
Type	**Component/ Interface**	**Board Reference**	**Description**
	0.9V Power	U5,U6,U8,J4,J6, J8,J36,J37,J38	Linear regulators for the VTT power supplies
	Power Connector	J22	9V-20V DC Input power supply jack
	Power Switch	SW1	Power Switch to turn the 3.3V and 1.8V power supplies on
System Monitoring	Temperature Sense	U20	Measures Stratix ™ and board temperature
	Voltage Sense	U22	Measures the current drawn by the 1.5V, 1.8V, 1.8V_DIMM, 0.9V DIMM, 1.8V_DDRII, VDD_QDRII_INT, VDD_QDRII_IO, and 3.3V power supplies
	Power-On Reset	U21	Monitors the 3.3V, 1.8V, and 1.5V power supplies
IO	10/100 Ethernet	U12,U28,J13	10/100 Ethernet MAC/PHY. 25.00 MHz crystal oscillator, RJ45 connector with LED indictors.
Serial IO	RS-232	J14,J15	DB9 connectors
		U16,U17	RS-232 Serial interface level shifter
	RS-232 Tx LEDs	D1,D3	RS-232 transmitter active yellow LEDs
	RS-232 Rx LEDs	D2,D4	RS-232 receiver active yellow LEDs
Nios Peripheral	Expansion Prototype Card	J16,J17,J18	Interface to Expansion Prototype Card
Debug	Agilent Debug Header	J20	Agilent E5390A Debug Logic Analyzer Header
	Tektronix Debug Headers	J19,J21	Tektronix P6860 Debug Logic Analyzer Header

Functional Description

Figure 2 shows a block diagram of the Stratix™ Memory Board 2.

Figure 2. Stratix™ Memory Board 2 Block Diagram



Connector Function Summary

Table 2 shows the functions of the connectors on the SMB2.

Table 2. Stratix™ Memory Board 2 Connectors

Connector	Stratix™ Device	Not Device Specific
Stratix™ device	U7	
Three Debug Proto Headers (see the "Debug Proto Headers" section)	J16,J17,J18	
Logic Analyzer (see the "Logic Analyzer Connectors" section)	J19,J20,J21	
LED display (see the "Seven-Segment Displays" section)	U18,U19	
Configuration Expansion Connectors (see the "Configuration Expansion Connector" section)		J12,J27,J50
10/100 Ethernet		J13
RS-232		J14,J15

Switch & Jumper Functions

Table 3 summarizes the function of each switch and jumper on the SMB2.

Table 3. SMB2 Switches & Jumpers

I/O Function	Stratix™ Device	Not Device Specific	Jumper Connections
Power switch		SW1	
System Reset	S2		
Safe	S3		
User Push Buttons		S4,S5,S6,S7	
DIP switch for selecting options (see the "Octal Dual-in Line Package (DIP) Switches" section)	S1	S8	
Configuration Expansion Headers (see the "Configuration Expansion" section)		J12,J27,J50	
VCCSEL: J48, Pin 1-2 connects to 3.3V through 10 kOhm, Pin 2-3 ties signal to GND.	AJ14		J48 to (Stratix™) U7I.AJ14
PLL_ENA: J39, , Pin 1-2 ties signal to 3.3V through 10 kOhm, Pin 2-3 ties signal to GND.	AF19		J39 to (Stratix™) U7J.AF19
QDR-II impedance (ZQ) select: J49. Pin J49.1 – J49.2 ties 301Ω to GND Pin J49.3 – J49.4 ties 249Ω to GND Pin J49.5 – J49.6 ties (open/User option resistance) to GND.			J49 to U3.H11 and U4.H11 (QDR-II ZQ)
100 MHz Osc select: J23, Pin 1-2 selects SMT Clock, Pin 2-3 selects Socket Clock.			J23 to U27 (SMT Osc), and J25 (Osc Socket)
100 MHz SMA select: J24, Pin 1-2 selects Ocs Clock, Pin 2-3 selects SMA Clock.			J24 to U10.12
JTAG Bypass Jmpers: J11, Pin 3-4 selects Stratix™ , Pins 1-3, 2-4 selects MAX & Stratix™ , Pins 3-5, 4-6 selects Exp & Stratix™ .			J11.1 to U11.4, J11.2 to U11.104, J11.3 to J10.9, J11.4 to U7I.D16, J11.5 to J50.8 J11.6 to J50.6
1.5V Stratix™ Regulator Shutdown: J32, Pin 1-2 shutdowns U24 regulator, Pin 2-3 enables U24.			J32.2 to U24.4
QDRII IO Regulator Shutdown: J33, Pin 1-2 enables U25 regulator, Pin 2-3 shutdowns U25 regulator.			J33.2 to U24.1
QDRII IO Voltage Select: J29, Pin 1-2 selects 1.5V, Pin 2-3 selects 1.8V.			J29.2 to U25.5
1.8V Regulator Shutdown: J34, Pin 1-2 enables U23 regulator 1, Pin 2-3 shutdowns U23 regulator 1.			J34.2 to U23.1
3.3V Regulator Shutdown: J35, Pin 1-2 enables U23 regulator 2, Pin 2-3 shutdowns U23 regulator 2.			J35.2 to U23.15

Table 3. SMB2 Switches & Jumpers			
I/O Function	**Stratix™ Device**	**Not Device Specific**	**Jumper Connections**
DDRII VTT1 Regulator Shutdown: J36, Pin 1-2 enables U5 regulator, Pin 2-3 shutdowns U5 regulator.			J36.2 to U5.2
QDRII VTT2 Regulator Shutdown: J37, Pin 1-2 enables U6 regulator, Pin 2-3 shutdowns U6 regulator.			J37.2 to U6.2
DIMM VTT3 Regulator Shutdown: J38, Pin 1-2 enables U8 regulator, Pin 2-3 shutdowns U8 regulator.			J38.2 to U8.2

Development Board Stratix™ Device

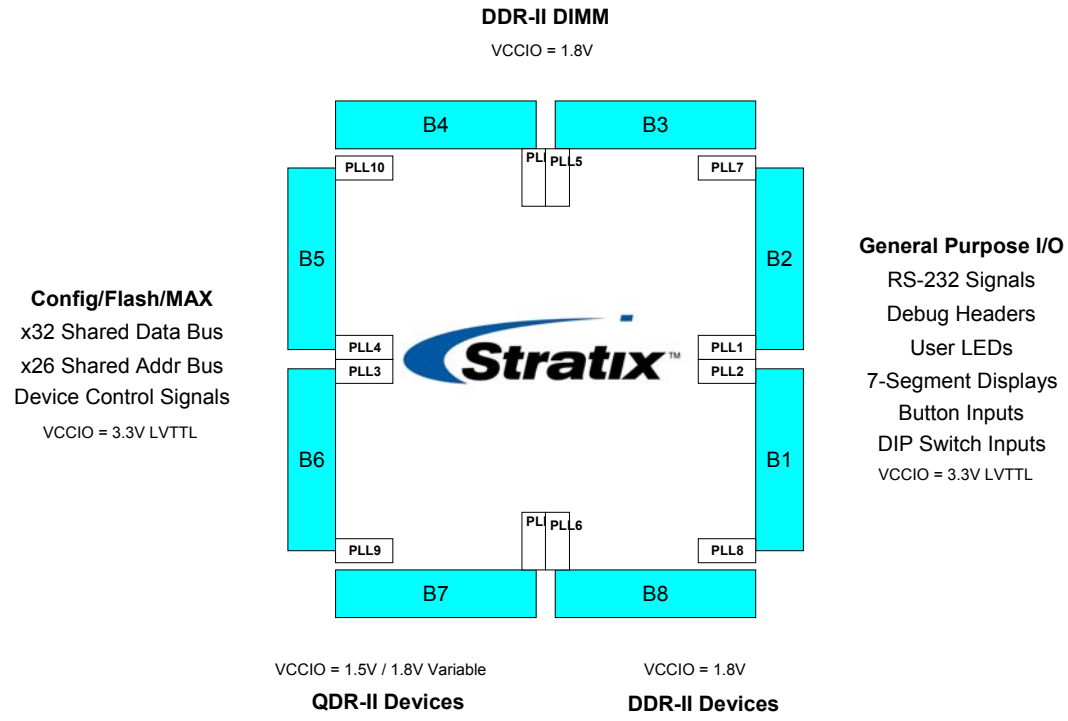
The Altera Stratix™ device combines the latest in silicon features to achieve industry-leading performance in internal speed, I/O speeds, and internal memory density. The development board is designed for one 1,020-pin FineLine BGA packages, is an EP1S40F1020C5 device. The EP1S40 device is the size option that allow additional high-speed differential logic (HSDI) interface capability, as well as additional PLLs, memory, and logic elements (LEs). Table 4 shows the device features.

Table 4. SMB2 Stratix™ Device Features

Feature	EP1S40
LEs	41,250
RAM bits	3,423,744 (417 KB)
PLLs	12 PLLs (8 fast and 4 enhanced)
Transmitter and receiver source synchronous channels	80
Medium speed channels	10 receivers 10 transmitters
User I/O pins	773

Figure 3 shows the Stratix™ I/O Bank Diagram.

Figure 3. Stratix™ I/O Bank Diagram



Board Layer Stack-Up

The Stratix™ Memory Board 2 consists of 12 layers of FR4 material for a combined width of 0.062 inches. The board layer stack-up is shown in Table 5.

Table 5. SMB2 Layer Stack-Up *Note (1)*

Layer Number	Layer Type	Description	Thickness & Tolerances	
			Copper Thickness (Mils)	Laminate (Mils)
1	Mix	Foil	0.6	
		Pre-pregnate		3
2	GND Plane		1.2	
		Core		4
3	Signal		0.6	
		Pre-pregnate		6
4	Signal		0.6	
		Core		4
5	1.5V Plane		1.2	
		Pre-pregnate		4
6	Signal		0.6	
		Core		6
7	Signal		0.6	
		Pre-pregnate		4
8	3.3V Plane		1.2	
		Core		4
9	Signal		0.6	
		Pre-pregnate		6
10	Signal		0.6	
		Core		4
11	Split Plane		1.2	
		Pre-pregnate		3
12	Mix	Foil	0.6	

Note to Table 5:
(1) 0.5 oz of copper is equivalent to a 0.6-mils trace width.

Power Sources

The SMB2 board's power design is based on a single DC input with on-board regulators generating the other required lower voltages. In addition to the on-board regulators, fuse isolated banana jacks are provided for all unique voltages for characterization purposes.The board has seven power regulators:

- Three switching regulators
- Four linear regulators

Table 6 lists the power sources used on the SMB2 Development Board.

Table 6. SMB2 Regulators					
Reference Designator	**Type**	**Voltage Output (V)**	**Description**	**Manufacturer**	**Part Number**
U23	Switching regulator	3.3	Stratix™ IO VCC, clock oscilators and buffers, 10/100 Ethernet components, proto-expansion header, RS232 components, SRAMs, flash memory, Stratix™ configuration components, user switches, seven-segment displays, LEDs, MDIO, temperature and voltage sense.	Linear Technologies	LTC3728EG
U23	Switching regulator	1.8	Stratix™ IO and PLL VCC, DDR-II SDRAM VDD, QDR-II SRAM Internal VDD, DDR-II SDRAM DIMM VDD	Linear Technologies	LTC3728EG
U24	Switching regulator	1.5	Stratix™ PLL and Internal VCC	Linear Technologies	LT3150CGN
U25	Linear regulator	1.5/1.8	QDR-II SRAM IO Power	Linear Technologies	LT1963AEQ
U5	Linear regulator	0.9	DDR-II SDRAM VTT	National Semiconductor	LP2996MR
U6	Linear regulator	0.75/0.9	QDR-II SRAM VTT	National Semiconductor	LP2996MR
U8	Linear regulator	0.9	DDR-II SDRAM DIMM VTT	National Semiconductor	LP2996MR

The board can powered in two different ways:

1. 9V-20V DC input (J22)

2. Bench power supplies (various banana jacks)

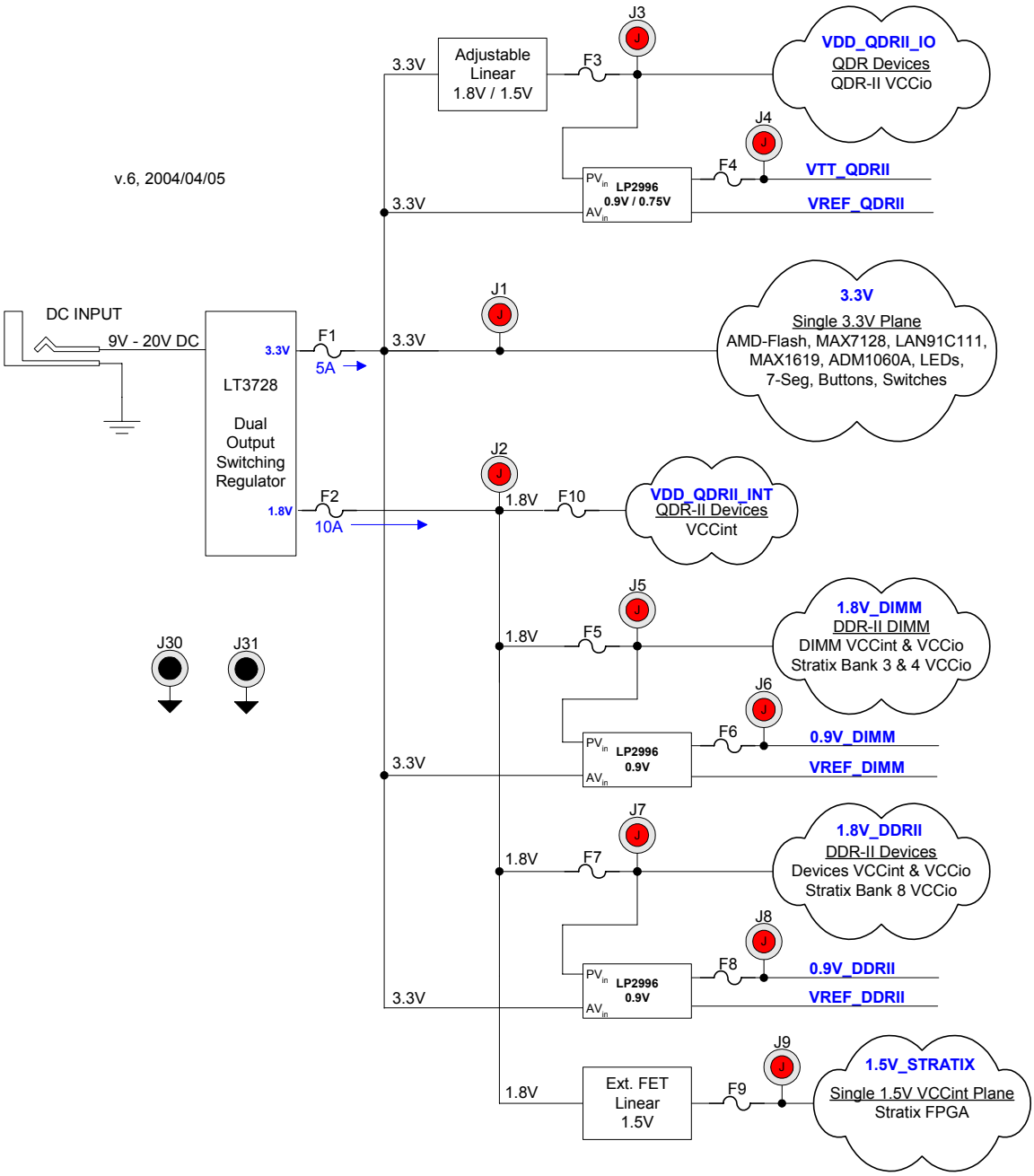
9V-20V DC input

A 9V-20V DC input is provided by a right-angle 2.5mm power jack with a 5.5mm barrel. The incoming DC voltage is regulated down to 3.3V and 1.8V by a dual switching power supply. From these voltages all other on-board voltages are generated.

Bench Power Supplies

Socketed fuses are provided to isolate the voltage planes from the regulators to allow bench supplies to power these sections using banana jacks. The bench supply inputs are placed after the other power supplies (whether linear or switching supplies) on the board in order to allow current draw measurements. Figure 4 below shows a block diagram of the power supply generation and distribution.

Figure 4. Power Supply Block Diagram



Power Planes

Bench power supplies provide an easy way to measure the current draw on each power plane. When one plane is being powered by the bench supply, all other planes still draw current from the DC power input. Upon applying power to the board, the power LED should be on.

Table 7 shows the procedure for powering individual planes through bench power supplies. In the instructions in Table7, only remove the fuse listed in the "Instructions" column. Leave the other fuses on the board.

Table 7. Procedure for Powering Individual Power Planes through Bench Power Supplies		
Power Plane	**Power Plane Using Bench Power Supplies**	**Instructions**
3.3V	Stratix™ IO, clock oscillators and buffers, 10/100 Ethernet components, proto-expansion header, RS232 components, SRAMs, flash memory, Stratix™ configuration components, user switches, seven-segment displays, LEDs, MDIO, temperature and voltage sense.	Remove fuse F1. Apply (+3.3V, GND) to (J1, J31)
1.8V	Stratix™ IO and PLL VCC, DDR-II SDRAM VDD, QDR-II SRAM Internal VDD, DDR-II SDRAM DIMM VDD	Remove fuse F2. Apply (+1.8V, GND) to (J2, J30)
QDRII_IO	QDR-II SRAM IO power	Remove fuse F3. Apply (+1.8V or +1.5V, GND) to (J3, J30)
VTT_QDRII	QDR-II SRAM termination power	Remove fuse F4. Apply (+0.9 or +0.75V, GND) to (J4, J30)
1.8V_DIMM	DDR-II DIMM power	Remove fuse F5. Apply (+1.8V, GND) to (J5, J30)
0.9V_DIMM	DDR-II DIMM termination power	Remove fuse F6. Apply (+0.9V, GND) to (J6, J30)
1.8V_DDRII	DDR-II SDRAM power	Remove fuse F7. Apply (+1.8V, GND) to (J7, J31)
0.9V_DDRII	DDR-II SDRAM termination power	Remove fuse F8. Apply (+0.9V, GND) to (J8, J31)
1.5V_ STRATIX™	Stratix™ Internal and PLL power	Remove fuse F9. Apply (+1.5V, GND) to (J9, J31)

System Monitoring

The SMB2 includes several chips designed for real-time system monitoring on the board to increase the ability to provide more information about a design or potential demo without requiring a great deal of equipment. This includes the Stratix™ temperature, various system voltages, and various power rails current consumption.

Temperature Sense

A Maxim 1619 temperature sense chip can read subtle changes in voltage drop across the Stratix™ temperature sense diode circuit. This is useful for doing on-the-fly temperature reading by chip designs versus manual measurements. A two-wire SMBus interface provides the interface to the Stratix™. The MAX1619 comes in a QSOP-16 and has the following features:

- Two measurement channels
  - Local (MAX1619)
  - Remote (Stratix™)
  - +/-2°C accuracy
- Programmable over/under temperature outputs
- SMBus interface for real-time readings

Voltage Sense/Current Sense

A Linear Technologies 2418 Differential A/D converter is used to measure the voltages across sense

resistors feeding various planes to allow real-time monitoring of current draw. This device has 8 differential inputs that can also be single-ended to allow for voltage monitoring. A 4-wire SPI interface provides to interface to to the Stratix™. The following power rails can be measured on the fly:

- 1.5V Stratix™ VCCint Power
- 1.8V Entire 1.8V Rail Power
- 1.8V_DIMM DIMM Power & Stratix™ Bank 3/4 VCCio Power
- 0.9V_DIMM DIMM VTT Rail Power
- 1.8V_DDRII DDR-II Power & Stratix™ Bank 8 VCCio Power
- VDD_QDRII_INT QDR-II VCCint Power
- VDD_QDRII_IO QDR-II VCCio Power & Stratix™ Bank 7 VCCio Power
- 3.3V Entire 3.3V Rail Power

Power-On Reset

A Linear Tech LTC2901 Quad Voltage Watchdog device is used to control power-up sequencing and system power-on-reset. This device is used in mode 10 and will allow the monitoring of the following voltages only:

- 3.3V (from switching supply)
- 1.8V (fromswitching supply)
- 1.5V (derived from 1.8V)

The LTC2901 will wait 50ms after the above voltages reach the acceptable threshold before releasing a reset signal to the MAX CPLD in order to hold off the Stratix™ FPGA configuration process until all voltages are stable.

Configuration

The Stratix™ device on SMB2 is configured from Flash as the primary method. The MAX CPLD contains the required state machine and control logic to accomplish this task. Configuration of both the MAX and Stratix™ is also supported directly on SMB2 using the standard JTAG header (see JTAG section for more detail).

The required file sizes for the Stratix™ device is 3,273,391 bytes for the hexout file, 1,528,528 bytes for the SOF file and 1,557,393 bytes for the RBF file. The "RBF" is the raw binary configuration file size that would be programmed into Flash. The flash device is 16MB and thus will allow up to 8 configuration files for the Stratix™ device to be stored in even (power-of-2) offsets in flash along with additional space for other uses such as NIOS object-code or other non-volatile data. Alternatively, the flash could be filled with a "safe" factory design and a custom demo design with support for up to 12MB of space for demo data such as a video file and/or web page file structure.

MAX 7256AE Configuration System Controller

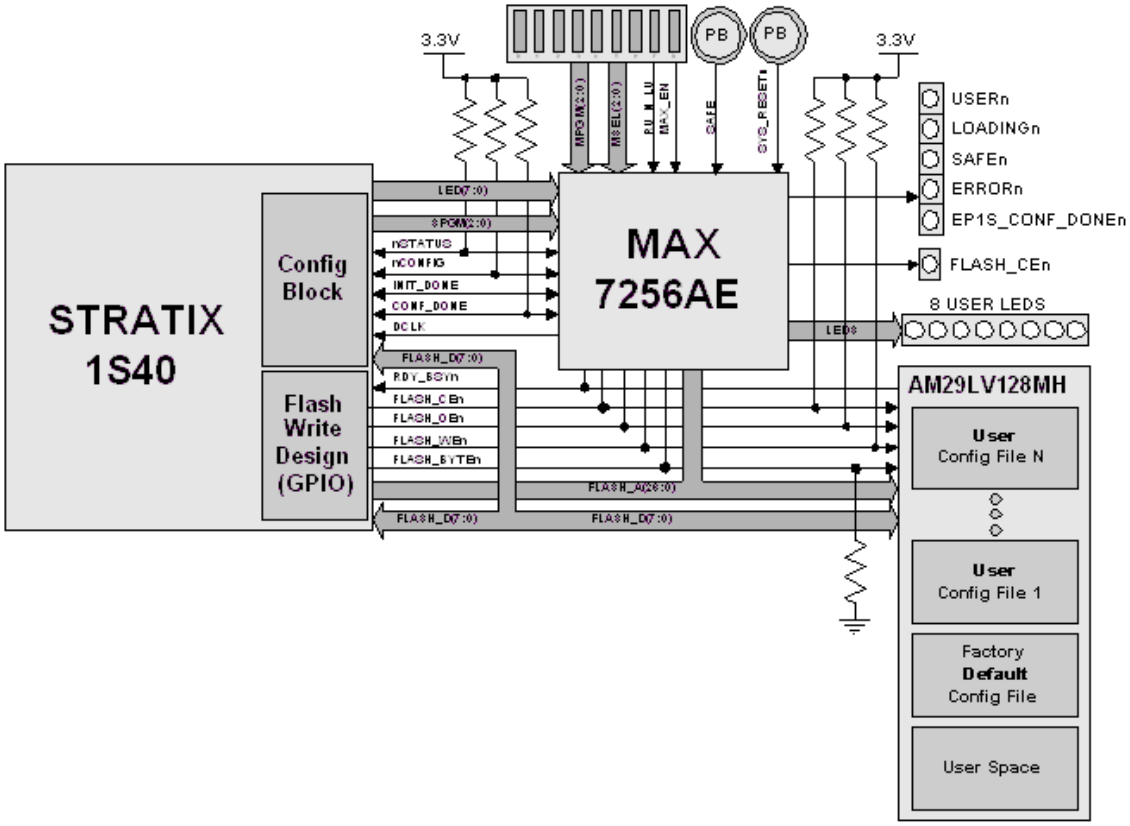
The system configuration controller is the EPM7256AETC144-7. This is a 3.3V device that provides more than enough logic resources for configuration and system control. Support for devices larger than the target Stratix™ device (80KLEs) is necessary on SMB2 in order to provide debugging of the general circuit before the creation of the Stratix™ -II version of this board in the future.

The signals listed in Table 8 below are relative to the MAX chip design. They include both system control and configuration signals and dedicated function pins for configuration. The "TYPE" shall be considered relative to the MAX Device insofar as the I/O setting and direction.

Table 8. CPLD I/O Requirements		
Signal Name	**Description**	**Type**
FSE_A(25:0)	Shared Bus Address (Flash)	LVTTL Output (26 bits)
FSE_D(15)	Shared Bus Address (used as a byte-address for Flash when in byte-mode, data when in word-mode)	LVTTL Output
FSE_D(7:0)	Shared Bus Data (Flash)	LVTTL Input (8 bits)
CONFIG_D(7:0)	Config Data	LVTTL Output (8 bits)
FLASH_CEn	Flash Chip Enable	LVTTL Output
FLASH_WEn	Flash Write Enable	LVTTL Output
FLASH_OEn	Flash Output Enable	LVTTL Output
FLASH_RDY_BSYn	Flash Ready / not BUSY	Open Drain Input*
FLASH_RESETn	Flash Reset Output	LVTTL Output*
FLASH_BYTEn	FLASH Byte-Mode / Word-Mode Select	LVTTL Output*
MPGM(2:0)	DIP switch Configuration File Select	LVTTL Input (3 bits)
SPGM(2:0)	Stratix™ Configuration File Select	LVTTL Input (3 bits)
SYS_RESETn	System Reset	LVTTL Input
SAFEn	Safe-Mode Reset	LVTTL Input
ENET_VLBUSn	Ethernet Visa-Local-Bus Mode Select	LVTTL Output
ENET_SRDYn	Ethernet S-Ready	LVTTL Output
ENET_RESET	Ethernet Reset	LVTTL Output
RUnLU	Remote/Local Mode Select	LVTTL Input
MSEL2	Remote/Local Mode Select	LVTTL Input
MAX_EN	MAX config enable	LVTTL Input
SW_RESERVED(3:0)	Reserved (Stratix™→CPLD)	LVTTL Input (4 bits)
OSC_A	Oscillator A (Config Clk)	LVTTL Input (GCLK1)
USER_LED(7:0)	LED Buffer Input	LVTTL Input (8 bits)
FLASH_CE_LEDn	LED Buffer Output	LVTTL Output
USER_LED_DRV(7:0)	LED Buffer Output	LVTTL Output (8 bits)
EP1S_CONF_DONEn	LED Buffer Output	LVTTL Output
EP1S_CONF_DONE	Stratix™ CONFIG DONE	Open Drain Input
EP1S_nCONFIG	Stratix™ nCONFIG	Open Drain Bidir
EP1S_nSTATUS	Stratix™ nSTATUS	Open Drain Input
TCK	JTAG Clock	n/a
TMS	JTAG Mode Select	n/a
TDI	JTAG Data In	n/a
TDO	JTAG Data Out	n/a
VCCINT	Internal Power, 3.3V	Power
VCCIO	I/O Power, 3.3V	Power
GND	Ground	Ground
MAX CPLD I/O Totals	89 I/O pins	

A general block diagram of the MAX/Flash configuration system is shown Figure 5 below. This figure does not show the extra signals involved in the use of the Configuration Expansion Header and Board, nor does it show the other devices on the "Shared Bus" as are shown in the diagram in the respective section of this document.

Figure 5. MAX/Flash Configuration Block Diagram



Flash Memory Map

Table 9 show an example memory map. This memory map is a generic starting place and not necessarily a definitive map. User Code Space and areas marked "other" are reserved for NIOS software images and other binary files for use in demos and otherwise.

It should be noted that configuration files can be placed closer to one another than shown below. This is accomplished by increasing the complexity of the configuration state machine to start counting on non-power-of-two address offsets. For example, a file of just over 2MB needs 4MB to be placed in a power-of-two offset base address. This assures the smallest possible address counter. Alternative the counter could start at 3MB with a slightly larger counter or even at 2.5MB with a larger-yet counter.

Table 9. Stratix™ / 16MB Flash Memory Map	
Block Name	**Address**
PLD Design 5 / Other	0x0FFF.FFFF 0x0E00.0000
PLD Design 4 / Other	0x0DFF.FFFF 0x0C00.0000
PLD Design 3 / Other	0x0BFF.FFFF 0x0A00.0000
PLD Design 2 / Other	0x09FF.FFFF 0x0800.0000
PLD Design 1	0x07FF.FFFF 0x0600.0000
PLD Design 0	0x05FF.FFFF 0x0400.0000
Safe Design	0x03FF.FFFF 0x0200.0000
User Code Space	0x01FF.FFFF 0x0000.0000

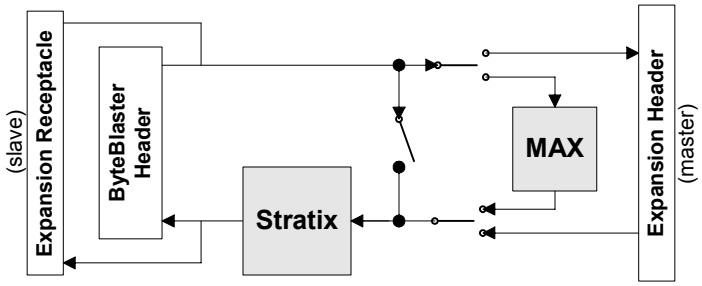
JTAG

A single 10-pin keyed, right-angle, shrouded, keyed header is provided for configuring the MAX CPLD and Stratix™ in a single JTAG chain using ByteBlaster-II and compatible JTAG programming adapters. The JTAG Header is the Molex 39-26-7108. By default the Stratix™ is the only JTAG device in the chain. A JTAG Bypass Jumper header is on the board in order to isolate the MAX from the chain since configuring the MAX is done infrequently. The JTAG Bypass settings are listed in Table 10 below.

Table 10. JTAG Bypass Jumpers		
Devices in Chain	**Shunt 1**	**Shunt 2**
Stratix™	Pin3 – Pin4	-N/A-
MAX and Stratix™	Pin1 – Pin3	Pin2 – Pin4
Expansion and Stratix™	Pin3 – Pin5	Pin4 – Pin6

This JTAG Chain can be expanded to multiple SMB2 boards or other boards that support the Configuration Expansion Header. Two 100-mil jumpers are provided to either include or exclude the Expansion Header and anything connected to it's chain (on another board). Whatever board is on the end of the chain (furthest from the board that has the ByteBlaster plugged in) will bypass the expansion header to loop the signals back through the return path. This extended chain could consist of all Stratix™ devices or all MAX devices or both. SMB2 is limited in this as its JTAG output pins are powered from a 1.8V bank and a MAX cannot read its output but a ByteBlaster-II can. Figure 6 below shows this JTAG chain graphically.

Figure 6. JTAG Chain



Configuration Expansion Connector

For various configuration testing and characterization there is a right-angle connector on the board known as the Configuration Expansion Connector. This 80-pin SCSI-type connector supports other means of configuration such as EPC devices and EPCS devices from a separate board. MAX/Flash and MSEL pins are already located on the mainboard (SMB2) so they are not needed on the Configuration Expansion Board (see following section) that will mate to this connector.

JTAG Expansion Connectors

A pair of right-angle connectors (one header and one receptacle) is supplied on the board to allow the JTAG chain to be extended to multiple boards for loading, testing, and JTAG checkout for more complicated chains. The header/receptacle pair connects ground but not power and uses only a 2x4 array. The pinouts connects the master's TDO pin to the slave's TDI pin and connects TCK and TMS directly though.

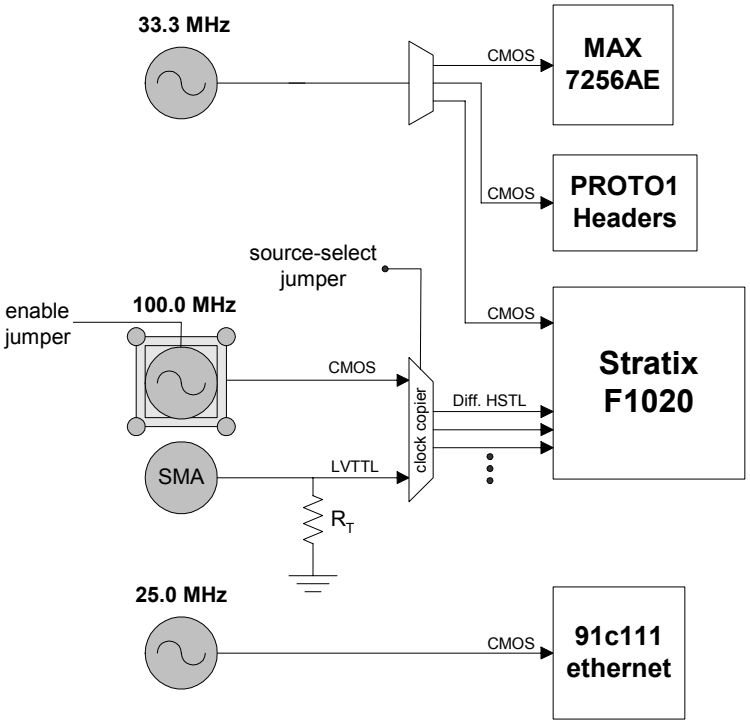
Clocking

Because of the large number of memories and other devices there is a fairly complicated clocking structure for the Stratix™ Memory Board 2. This includes clock sources as well as clock destinations. The board has the following three crystal oscillators:

- (U26) is a 33.33-MHz crystal oscillator and is used for configuration and is also driven to the Stratix™ for general system clocking needs. There is a low-skew clock buffer (U9) for clock distribution.
- (U27) is a 100-MHz crystal oscillator used for low-jitter, high speed applications in the Stratix™. This is the primary clock source for most Stratix™ designs. This oscillator has a dual-footprint that allows the user to add their oscillator by disabling the on-board device through a jumper. This clock system is buffered using a differential HSTL clock buffer (U10) that drives the Stratix™ top and bottom bank clock inputs for use with GPLLs. These target banks also operate using SSTL_18 or HSTL_18. There is also an SMA connector as a secondary input to the HSTL clock buffer. This input is very useful for sweeping frequencies to verify Fmax performance of designs. Alternatively, the Stratix™ can be configured to use these clocks as single-ended inputs.
- (U28) is a 25-MHz crystal oscillator used in the Ethernet MAC/PHY interface

Additionally, there are several differential clock inputs and outputs to the Stratix™ from SMA connectors. The oscillators and clock buffers are shown in Figure 7 below.

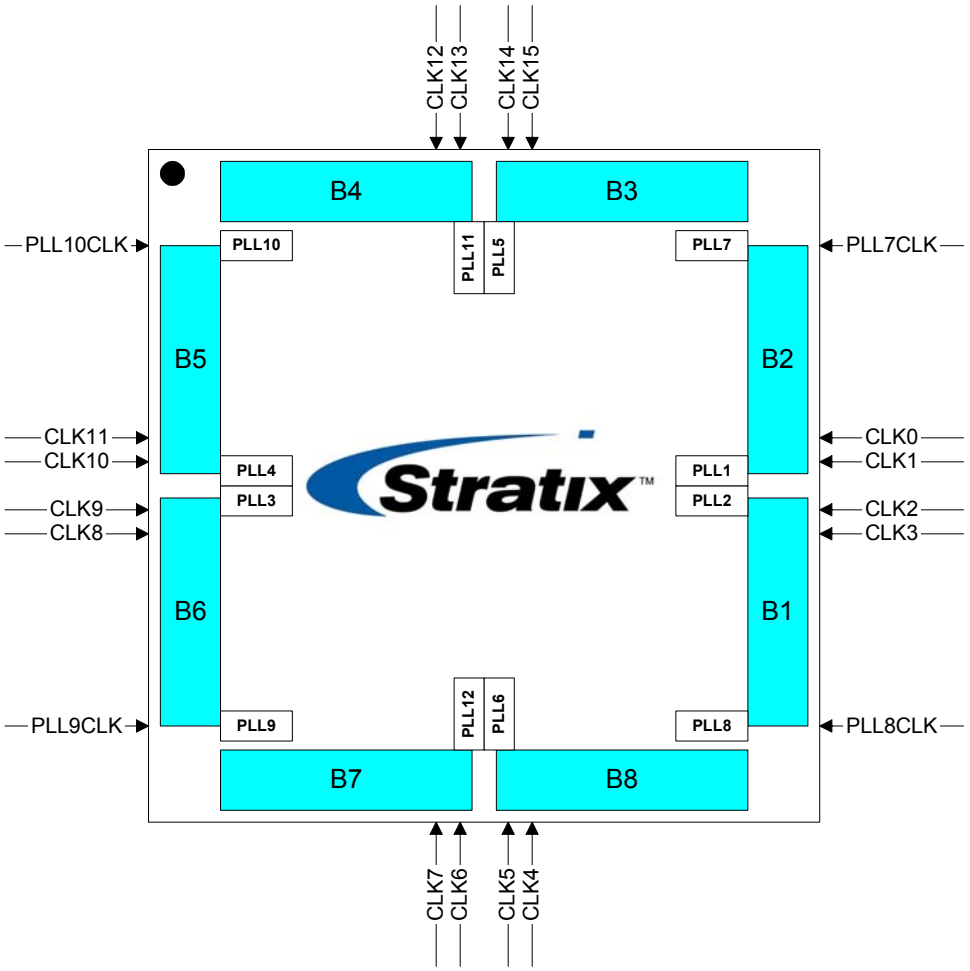
Figure 7. Clock Oscillators and Buffers



Stratix™ PLL and Clocking Features

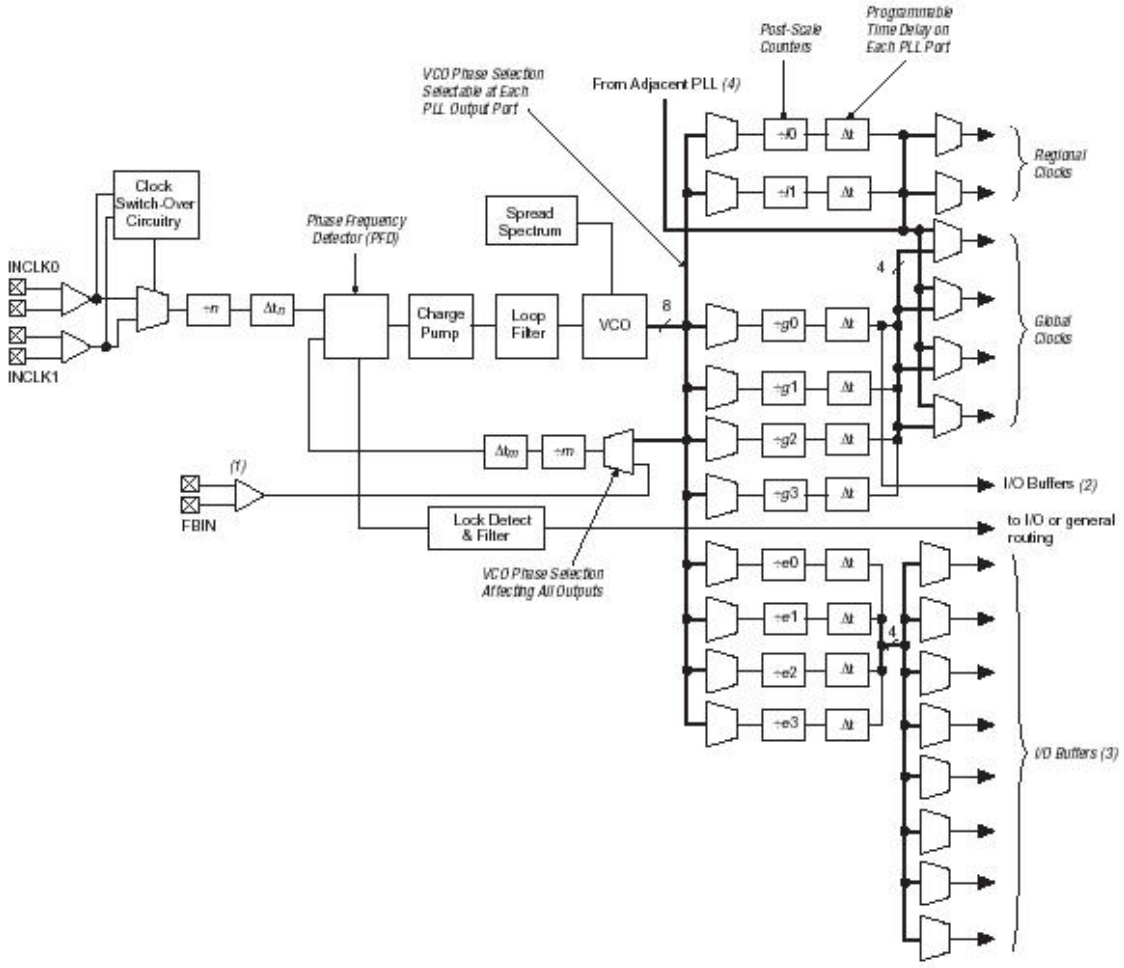
The Stratix™ has 16 dedicated clock inputs that access 16 global clock networks (CLK(0..15) and 8 regional clock networks (4 per quadrant). There are also 8 dedicated fast regional clock input pins that can have smaller pin-to-LE delays for special purposes. Figure 8 below outlines this clocking scheme. Pin 1A is the upper left-hand corner in Figure 8 (PACKAGE-TOP referenced).

Figure 8. Stratix™ PLL and Clocking Resources



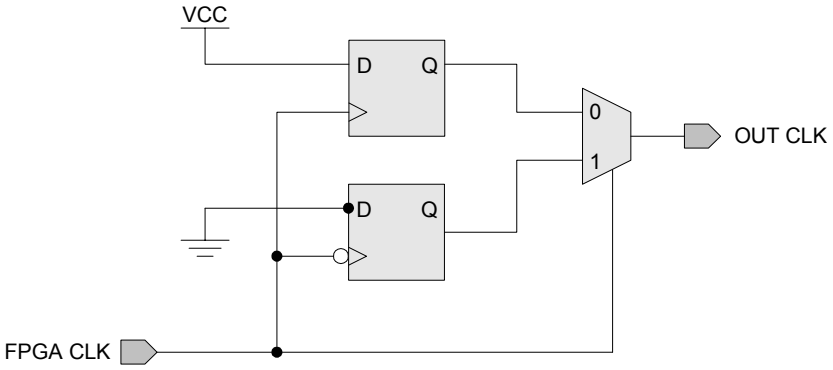
The Stratix™ device has 4 "Enhanced PLLs". These include PLL5 and PLL11 on the top of the chip and PLL6 and PLL12 on the bottom of the chip. They can drive any of the global or regional clock networks. PLL5 and PLL6 each connect to their own dedicated block of 8 clock outputs (or 4 differential outputs). Each output block has its own power supply so they can be split among different I/O standards such as 1.5V HSTL on one block and 2.5V SSTL on another block. Enhanced PLLs can drive FPLL inputs through global clock networks as well. The connections between Enhanced PLLs, clock inputs, and clock outputs are fairly detailed. These connections are shown in Figure 9 below.

Figure 9. Enhanced PLL External Clock Outputs



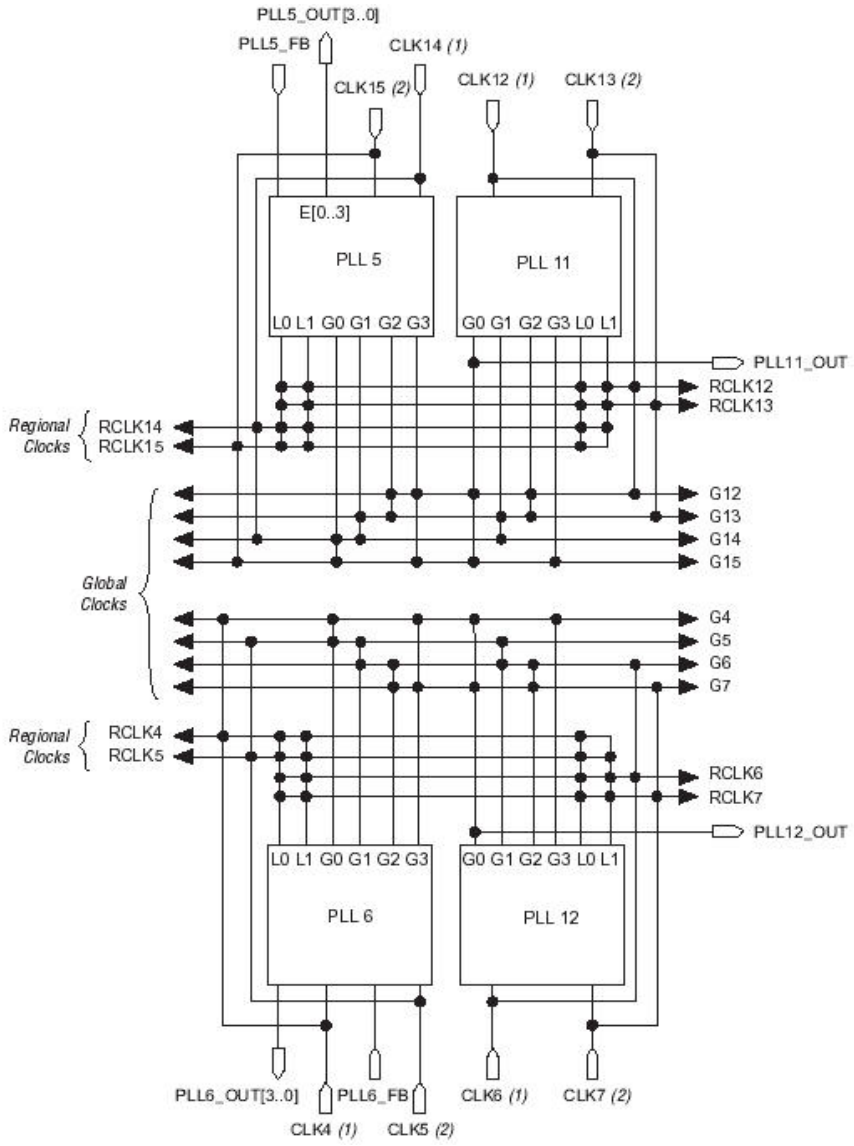
Any PLL, either Enhanced or Fast, can drive all registers in the Stratix™ , including I/O registers. One can create a convenient clock output for DDR applications by clocking an I/O register programmed with the ALTDDIO Megafunction such that it drives a pre-programmed "1" on one clock edge and a pre-programmed "0" on another. Figure 10 shows this output buffer configuration in a Stratix™ device where the "OUT CLK" is the board-level clock to the memory.

Figure 10. ALTDDIO I/O Register External Clock Output



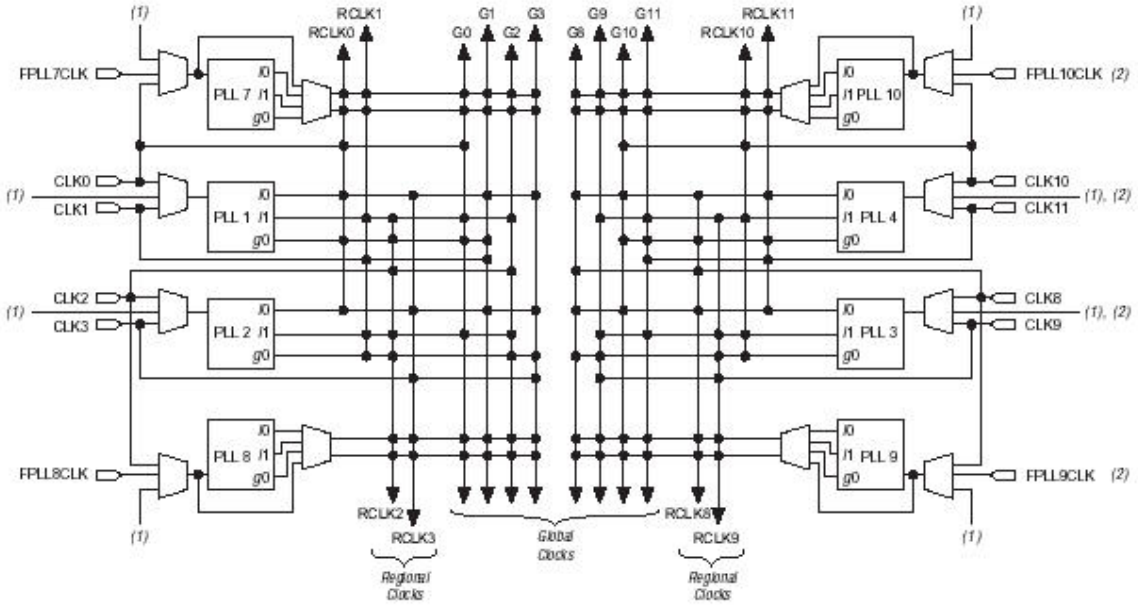
The connections between Enhanced PLLs, dedicated clock inputs, and internal global and regional clocks are fairly detailed. These connections are shown in Figure 11 below.

Figure 11. Enhanced PLL Inputs and Stratix™ Clock Networks



The Stratix™ device has 8 Fast PLLs. The FPLLs have dedicated connections to the SERDES blocks for up to 840Mb/s I/O speeds using differential standards. SMB2 does not require the use of FPLLs with SERDES but these FPLLs can be used to drive internal clock networks to clock internal and I/O registers. These can be used in conjunction with enhanced PLLs to create clock shifts to skew input and output datapaths to overcome input setup times and clock-to-outputs times in order to meet timing on these interfaces for DDR memories. The connections between PLLs, clock inputs, and internal clock networks are are shown in Figure 12 below.

Figure 12. Fast PLL Inputs and Stratix™ Clock Networks



DDR-II SDRAM DIMM Clocks

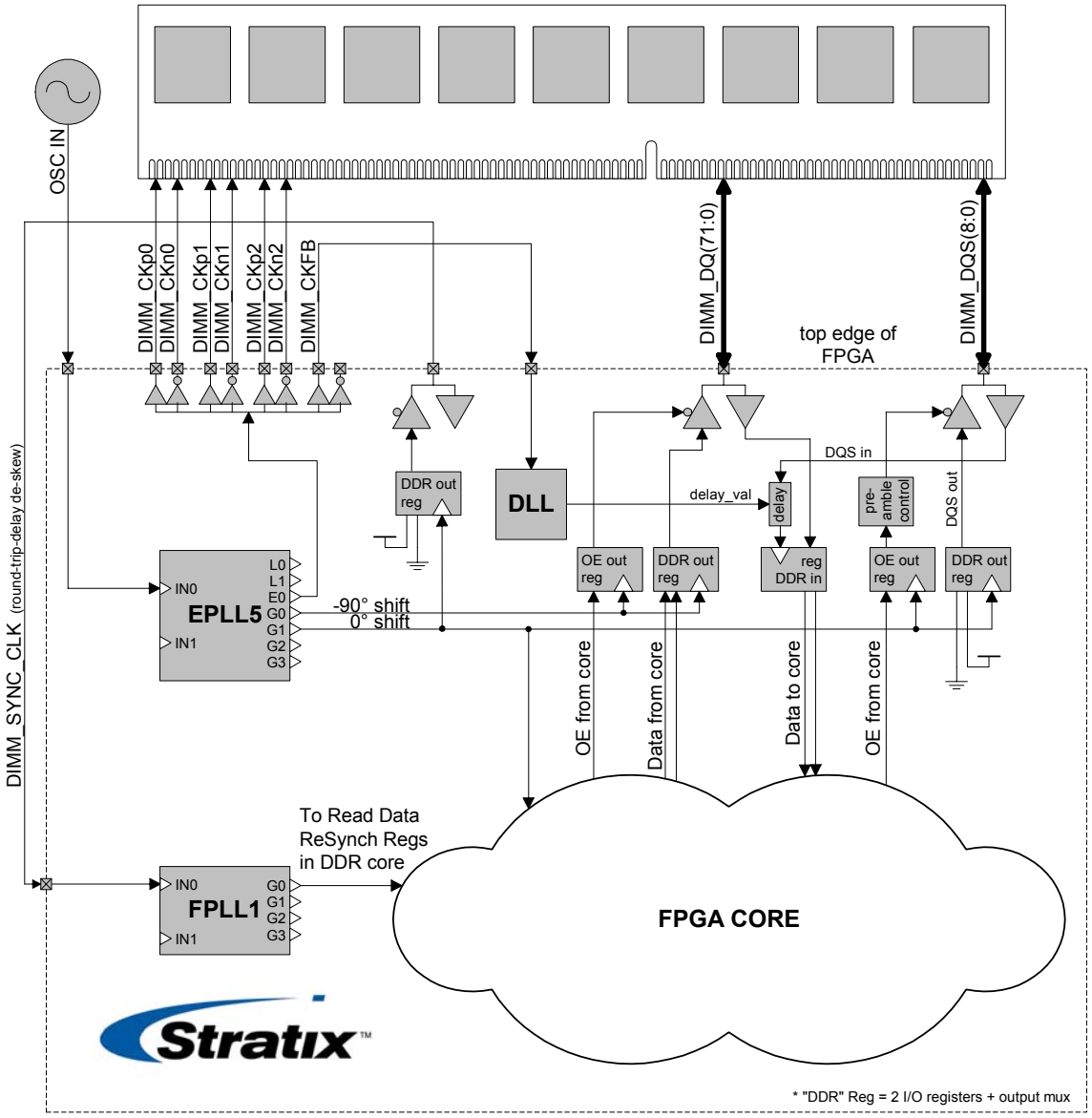
The DDR-II SDRAM DIMM requires 3 Differential 1.8V SSTL clock inputs to drive the DDR-II Devices' clock input pins. These are driven from the Stratix™ device directly to the DIMM. They can be realized using either ALTDDIO style clock outputs or from dedicated Enhanced PLL clock outputs. SMB2 uses Enhanced PLL 5 External Clock outputs for the system clock portion on the DIMM. Single-sided DIMMs have three loads per pin pair three 200Ω termination resistors as described in the JEDEC specifications. Double-sided DIMMs double the loads. The termination resistors are located on the DIMM itself so there is no need for them on SMB2 directly.

The DDR-II SDRAM DIMM also requires a set of DQS signals that act as clocks for the DQ data bits. There is a single DQS signal per byte of DQ data (8 DQS and 64 DQ or 9 DQS for 72 DQ for ECC DIMMs). The Stratix™ drives DQS and DQ signals on writes and the DIMM drives these on reads. There are dedicated pins on Stratix™ that can receive and drive DQS signals with correct timing for a specific set of DQ pins. These are described in device pin tables and are already marked in the existing schematic symbol. DDR-II DIMMs support differential DQS but Stratix™ does not support this.

Lastly, there are two feedback clocks required. The upper two banks of the Stratix™ (banks 3 and 4) require a reference clock input for on-chip DLLs involved in the DQS clocking circuitry. A clock of the exact same frequency as the DIMM and Stratix™ DDR registers must be driven into one of the global clock inputs on this edge of the chip (CLK12, CLK13, CLK14, or CLK15). In this case the Stratix will drive a 4th copy of the DDR output clocks above into one of these inputs. This input is then designated as the "DDR Ref Clock" in Quartus. A differential signal is actually used but it is terminated such that it can be run in either single-ended or differential input modes for testing. The DIMM_SYNC_CLK is used to match board-level skew of the round trip delay (DIMM_CK + DQS). This is used to help re-synchronize read data back to the core clock phase.

A diagram of the clocking setup is shown in the Figure 13 below.

Figure 13. DDR_II SDRAM DIMM Clocking Diagram



On-Board DDR-II SDRAM Device Clocks

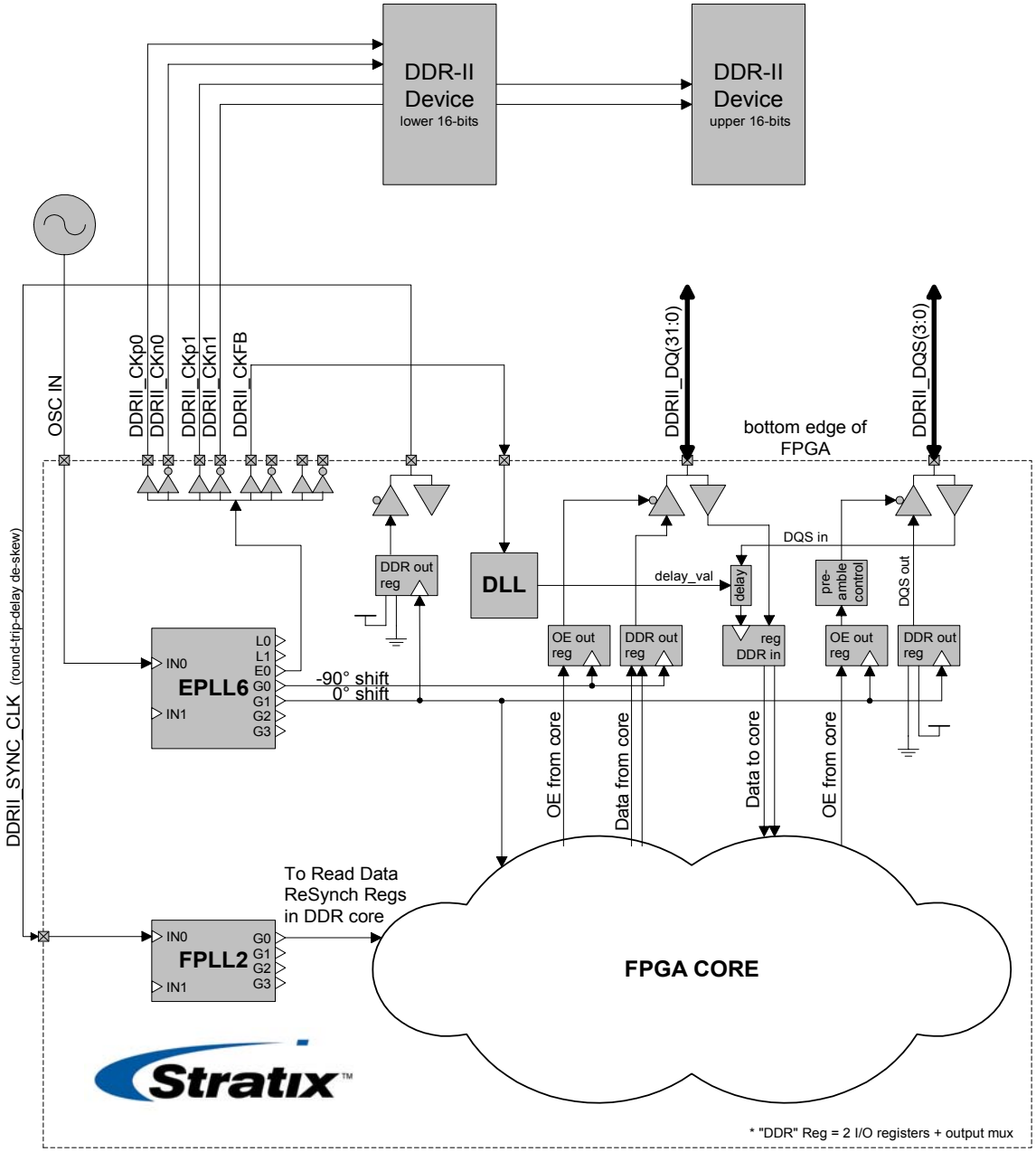
The DDR-II devices require a single 1.8V Differential SSTL clock input to each device. There are two x16 devices creating a 32 bit bus so there will be two clock output pairs. These are driven from the Stratix™ directly to each memory device. These two outputs can be realized using either ALTDDIO style clock outputs or from dedicated Enhanced PLL clock outputs. The current design uses the Enhanced PLL 6 External Clock outputs.

The DDR-II devices also require a set of DQS signals that act as clocks for the DQ data bits. There is a single DQS signal per byte of DQ data (UDQS for DQ(15:8) and LDQS for DQ(7:0)). Stratix™ drives DQS and DQ signals on writes and the DDR-IIdevices drive these on reads. There are dedicated pins on Stratix™ that can receive and drive DQS signals with correct timing for a specific set of DQ pins. These are described in device pin tables and are already marked in the existing schematic symbol. DDR-II devices support differential DQS but Stratix™ does not support this.

Lastly, Bank 8 of the Stratix™ (lower right when looking from PACKAGE TOP) requires a reference clock input for on-chip DLLs involved in the DQS clocking circuitry. A clock of the exact same frequency as the DDR-II devices and Stratix™ DDR registers must be driven into one of the global clock inputs on this edge of the chip (CLK4, CLK5, CLK6, or CLK7). In this case the Stratix will drive a 3rd copy back into one of these inputs. This input is then designated as the "DDR Ref Clock" in Quartus. A differential signal is actually used but it is terminated such that it can be run in either single-ended or differential input modes for testing. The DDRII_SYNC_CLK is used to match board-level skew of the round trip delay (DDRII_CK + DQS). This is used to help re-synchronize read data back to the core clock phase.

A diagram of the clocking setup is shown in the Figure 14 below.

Figure 14. DDR_II SDRAM Clocking Diagram



On-Board QDR-II SRAM Device Clocks

The QDR-II SRAM devices require at least two clocks to operate. What seems like differential read and write clocks are actually two pairs of 180°-shifted single-ended HSTL clocks. They are used individually within the QDR-II SRAM device. The QDR-II SRAM also has the option of using what is called an echo clock for read data. This is a similar pair of single-ended clocks being driven from the QDR-II SRAM back to the Stratix™ device.

The write clocks are called K/K#, the read clocks are C/C#, and the echo clocks are called CQ/CQ#. These K/K# and C/C# outputs can be driven from the Stratix™ device using either ALTDDIO style clock outputs or from dedicated Enhanced PLL clock outputs. The echo clocks are driven (optionally) by the SRAM. The current design uses the ALTDDIO style clock outputs that can be phase-shifted to adjust for T_{CO} delays to maximize performance.

There are two main approaches to read clocking that are being used on SMB2. The first method is to use the echo clocks as inputs to the DQS-based DDR circuitry as done in the DDR-II designs. The second method is to use the echo clocks. There is no reason in QDR-II to drive the C/C# read clocks because of the availability of the echo clocks CQ/CQ#. The timing margins are much better with echo clocks than the round-trip delay calculations required with read clocking. The C/C# read clocks have thus been tied to VCCio through a resistor and are not used on SMB2.

For PLL-based read clocking the echo clocks need to be driven to dedicated PLL input pins. Although these are not differential signals it is intended to receive them as a differential input to the PLL. This method will at least average any positive-to-negative clock skew versus simply single-ending only the positive signal. This will only be done with device 1's echo clocks and it will be assumed that these two devices are aligned in time as opposed to using an entire PLL per device for read clocking.

For DQS-based clocking the echo clocks need to be driven to a dedicated DQS input. Stratix™ does not support dual-DQS inputs (one positive edge DQS and one negative-edge DQS) so only a single input (the positive signal CQ) will be connected to the DQS input pin. This will be the CQ output from device 0. DQS-based clocking of an 18-bit bus requires the use of the single x32-capable DQS pin available in Bank 7 of the Stratix™ . Output clocking of x32 interfaces is not an issue. Only the inputs have special hard-ties between DQS pins and DQ pins for x8, x16, and x32 support. The DLL also requires a reference clock of exactly the same frequency of the QDR-II interface to be driven into one of the clock inputs on this edge of the chip (CLK4, CLK5, CLK6, or CLK7). This input is then designated as the "DDR Ref Clock" in Quartus. Due to limited resources, the DDRII feedback clock will be used for QDRII operation. This is the only reason EPLL6 is shown in Figure 15 below.

For either read clock option (PLL versus DQS) the Stratix™ will need to be outputting the K/K# HSTL clock pair because the QDR-II SRAM creates CQ/CQ# based on K/K# inputs. As long as the K/K# inputs meet the input specs of the QDR-II devices, they should output them accordingly (i.e. the output skew is directly related to the input skew from Stratix™ ALTDDIO outputs). The advantage of using the echo clocks is that the read timing becomes more predictable because round-trip board-delay is removed from the equation except for trace-length matching as in other source-synchronous systems. DQS-based clocking for QDR is intended to be the primary method. SMB2 tries both methods for testing purposes.

Lastly, there is one more feedback clock required for highest speeds. This is called the core resynchronization clock QDRII_SYNC_CLK. The DDRII_SYNC_CLK is used to match board-level skew of the round trip delay (QDRII_K + DQRII_CQ). This is used to help re-synchronize read data back to the core clock phase.

The DQS-based approach is shown in Figure 15 and the PLL-based approach is shown in Figure 16 below.

Figure 15. QDR_II SRAM Clocking using DQS Read Clock

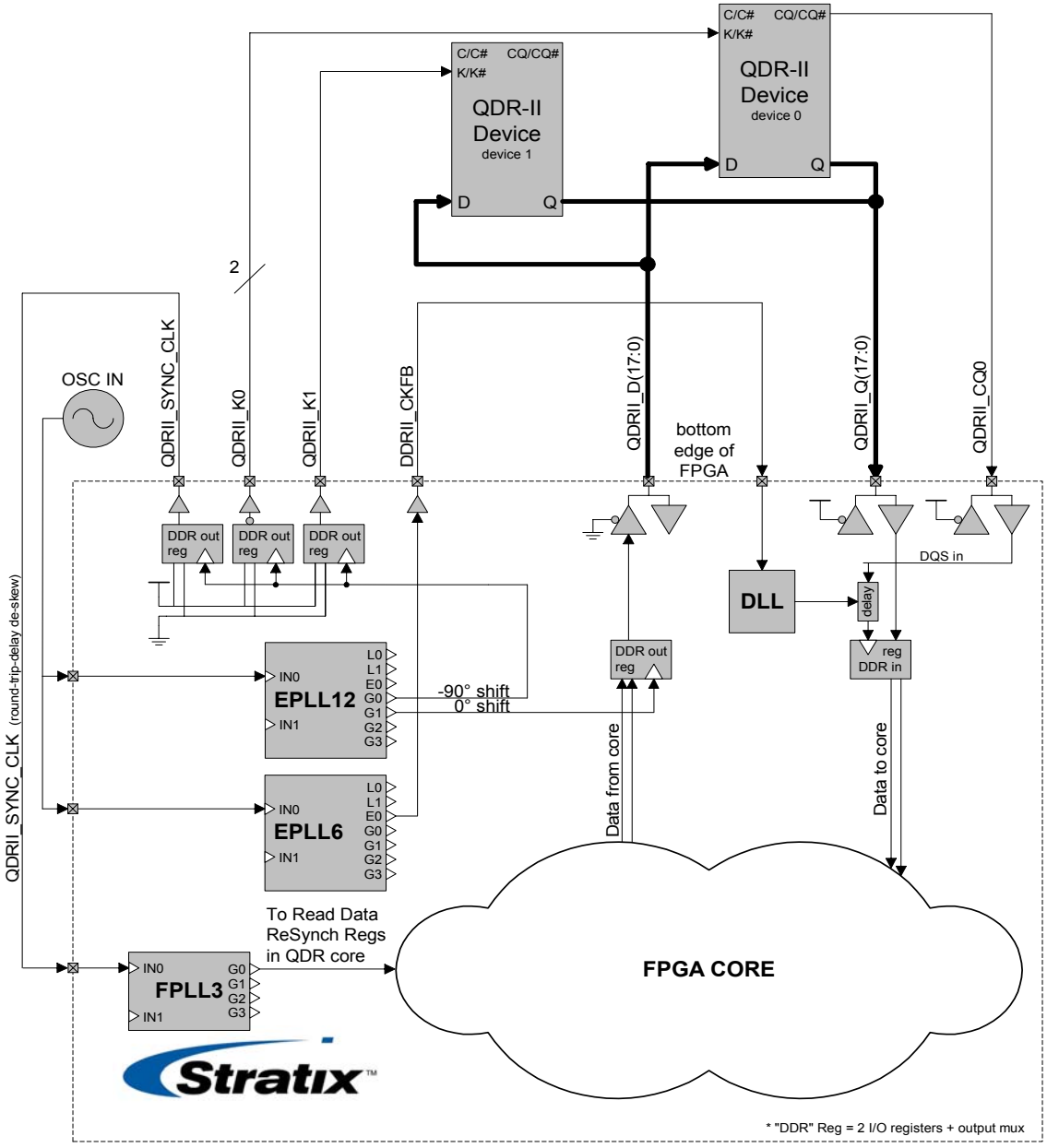
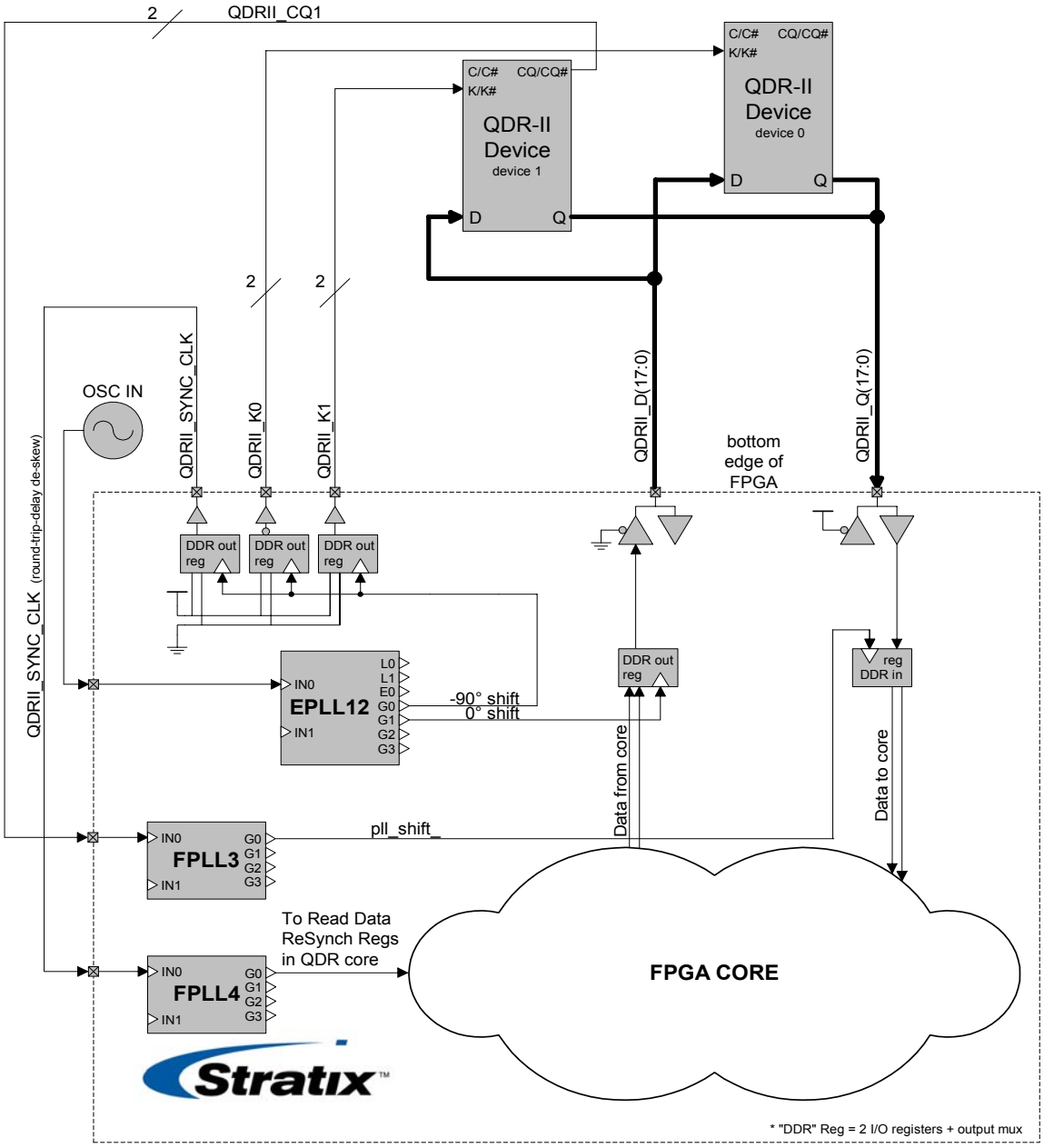


Figure 16. QDR_II SDRAM Clocking using PLL Read Clock



User I/O Standards

Board Settings DIP Switches

An 8-position DIP Switch allows the user to configure board-specific options. These are not available to the user for general programmable use as they affect hard-wired function pins for various devices. The RUnLU and MSEL switches are only used if a user wants to use the Remote/Local update block in Stratix to initiate reconfiguration and, if so, in which mode. The MSEL2 pin tells the MAX configuration controller to use the DIP switch PLD image pointer (MPGM(2:0) switches) when ON and to use the special Stratix SPGM(2:0) pins when OFF.

The MPGM(2:0) pins select one of eight possible PLD configuration file images in Flash to load upon power-up or SYS_RESETn. The Stratix™ can also point to the configuration file using it's PGM(2:0) pins (using ALT_REMOTE IP block in Stratix™) that drive the SPGM(2:0) nets on the board. The functions of each switch are listed below and Tables 11 lists the pin assignment for each switch.

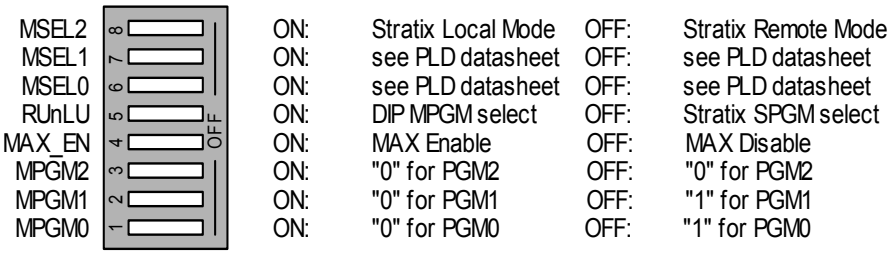


Table 11. Board Settings DIP Switch Connections

Signal Name	Dip Switch Pin	Connection
MPGM0	S1.1	U11.101
MPGM1	S1.2	U11..102
MPGM2	S1.3	U11.103
MAX_EN	S1.4	U11.97, J27.54
RUnLU	S1.5	U7I.AF14, U11.22
MSEL0	S1.6	U7I.AG18
MSEL1	S1.7	U7I.AE18
MSEL2	S1.8	U7I.AE19

User DIP Switches

The Stratix™ device is connected to an 8-position DIP switch, allowing the user to configure several common options. These DIP switches are for reference design functions and general purpose use. Tables 12 lists the pin assignment for each switch.

- When a switch is in the ON position a "0" is selected for the option.
- When the switch is in the OFF position, a "1" is selected for the option.

Table 12. Stratix™ User DIP Switch Pinouts		
Signal Name	**Dip Switch Pin**	**Stratix™ Connection**
USER_DIPSW0	S8.1	U7A.AC30
USER_DIPSW1	S8.2	U7A.AC29
USER_DIPSW2	S8.3	U7A.AD31
USER_DIPSW3	S8.4	U7A.AD32
USER_DIPSW4	S8.5	U7A.AC31
USER_DIPSW5	S8.6	U7A.AB32
USER_DIPSW6	S8.7	U7A.AA29
USER_DIPSW7	S8.8	U7A.AA28

Push Button Switches

Push buttons Switches are provided for system reset, safe mode, and for user defined functions. Table 13 lists the assignment for each push button.

Table 13. Push Button Pinout			
Signal Name	**Function**	**Push Button Number**	**Board Connection**
PB_SYS_RESETn	System Reset, loads Stratix™ with configuration data from MPGM(3:0) address	S2	U7A.AE29, U11.128, J17.1
PB_SAFEn	Safe Mode, loads the Stratix™ with factory default configuration data	S3	U7A.AE30, U11.117
PB_USER_PB0	User Defined	S4	U7.G23
PB_USER_PB1	User Defined	S5	U7.D28
PB_USER_PB2	User Defined	S6	U7.E26
PB_USER_PB3	User Defined	S7	U7.G24

User LEDs

Eight Yellow SM1206 surface mount LEDs (SM1206) are provided for general purpose use. The MAX7256AE is used as a buffer between the Stratix™ and diodes as the diodes have a forward voltage (V_{FD}) of 2.1 V and require a 20-mA current to output light at the recommended levels. Table 14 lists the assignment for each LED.

- A logic 0 is driven on the I/O port to turn the LED ON.
- A logic 1 is driven on the I/O port to turn the LED OFF.

Table 14. User LED Pinout		
Signal Name	**Reference Description**	**Stratix™ Connection**
USER_LED0	D5	U7A.AB30
USER_LED1	D6	U7A.AB31
USER_LED2	D7	U7A.AA30
USER_LED3	D8	U7A.AA31
USER_LED4	D9	U7A.Y29

Table 14. User LED Pinout		
Signal Name	**Reference Description**	**Stratix™ Connection**
USER_LED5	D10	U7A.Y30
USER_LED6	D11	U7AY31
USER_LED7	D12	U7A.Y32

Status LEDs

Blue, Green, Yellow, and Red surface mount LED's indicate status as shown in Table 15.

Table 15. Status LEDs			
Signal Name	**Description**	**Color**	**Ref. Des.**
DC_INPUT_OK	DC Input power is OK	Blue	D19
CONFIG_DONE_LEDn	Stratix™ is configured	Green	D13
FLASH_CE_LEDn	Flash is being accessed	Yellow	D14
USER_DESIGNn	User Configuration is loaded	Green	D15
LOADING_LEDn	Stratix™ configuration is loading	Green	D16
SAFE_DESIGN_LEDn	Stratix™ default configuration is loaded	Yellow	D17
ERROR_LEDn	System Error has occured	Red	D18
ENET_LNKn	Ethernet Link Indicator	Green	J13.10
ENET_RCVn	Ethernet Receive Indicator	Yellow	J13.12
RS232A_TXD	RS-232 Ch A Transmit	Yellow	D1
RS232A_RXD	RS-232 Ch A Receive	Yellow	D2
RS232B_TXD	RS-232 Ch B Transmit	Yellow	D3
RS232B_RXD	RS-232 Ch B Receive	Yellow	D4

Seven-Segment Displays

Two seven-segment LED displays are provided for the user. Each display is controlled directly by the Stratix™ device. Each segment of the display can be illuminated by driving the connected device's I/O pin with a logic 0. Tables 16 shows the display segment (model LDS-A324RI) and assignments for the seven-segment displays.

Table 16. Seven-Segment Display Pinouts			
Display Segment	**Display Connection**	**Signal Name**	**Stratix™ Connection**
1-A	U18.10	DIG_1_A	U7F.AC6
1-B	U18.9	DIG_1_B	U7F.AC5
1-C	U18.8	DIG_1_C	U7F.AC8
1-D	U18.5	DIG_1_D	U7F.AC7
1-E	U18.4	DIG_1_E	U7F.AB6
1-F	U18.2	DIG_1_F	U7F.AB7
1-E	U18.3	DIG_1_G	U7F.AA7
1-DP	U18.7	DIG_1_DP	U7F.AA6
2-A	U19.10	DIG_2_A	U7F.AE8
2-B	U19.9	DIG_2_B	U7F.AE7
2-C	U19.8	DIG_2_C	U7F.AD5
2-D	U19.5	DIG_2_D	U7F.AD6
2-E	U19.4	DIG_2_E	U7F.AE5
2-F	U19.2	DIG_2_F	U7F.AE6
2-G	U19.3	DIG_2_G	U7F.AD7
2-DP	U19.7	DIG_2_DP	U7F.AD8

10/100 Ethernet MAC/PHY

The board has an external 10/100 Ethernet MAC with integrated PHY. The controller is a Standard Microsystems LAN91C111 with support for both 10Mb and 100Mb Ethernet. SOPC Builder 2.0 and beyond provide default support for this component including a functional TCP/IP stack and device driver as well as example software for web servers and testing of the device.

The LAN91C111 requires a 25MHz reference clock. This is generated by a sub-miniature surface-mount 25.000 MHz oscillator. An integrated RJ45 connector with built-in magnetics and activity/link LEDs is used along with the MAC/PHY chip.

The signals listed in Tables 17 are relative to the Stratix™ device as far as the I/O setting and direction.

Table 17. Ethernet I/O Signals			
Signal Name	**Description**	**Stratix™ Type**	**Connector**
FSE_A(15:1)	Shared Bus Address (enet)	LVTTL input	
FSE_D(31:0)	Shared Bus Data (enet)	LVTTL bidir	
ENET_BEn(3:0)	Byte Enables	LVTTL input	
ENET_ADSn	Address Strobe	LVTTL input	
ENET_AEN	Address Enable	LVTTL input	
ENET_VLBUSn	Visa-Local-Bus Mode Select	LVTTL input	
ENET_SRDYn	S-Ready	LVTTL output	
ENET_RESET	Reset	LVTTL input	
ENET_LCLK	Local Clock	LVTTL input	
ENET_IOCHRDY	IO Character Ready	LVTTL output	
ENET_RDYRTNn	Ready Return	LVTTL input	

Table 17. Ethernet I/O Signals			
Signal Name	**Description**	**Stratix™ Type**	**Connector**
ENET_INTRQ0	Interrupt Output	LVTTL output	
ENET_LDEVn	Local Device Select	LVTTL output	
ENET_IORn	Read Strobe	LVTTL input	
ENET_IOWn	Write Strobe	LVTTL input	
ENET_DATACSn	Data Chip Select	LVTTL input	
ENET_CYCLEn	Cycle Select	LVTTL input	
ENET_W_Rn	Write/Read Select	LVTTL input	
ENET_TXD_P	Transmit Data – Positive		J13.1
ENET_TXD_N	Transmit Data – Negative		J13.3
ENET_RXD_P	Receive Data – Positive		J13.4
ENET_RXD_N	Receive Data – Negative		J13.6

RS-232 Ports

The board provides two standard RS-232 serial interfaces. Female DB9 connectors are used with standard PC serial port pin outs. Dedicated level-shifting buffers (U16 and U`17) are used to translate between LVTTL and RS-232 levels.

The signals listed in Tables 18 are relative to the RS-232/DB-9 specification and the "Stratix™ Type" should be considered relative to the Stratix™ device as far as the I/O setting and direction.

Table 18. RS-232 Connector Pinout for the Stratix™ Device				
Signal Name	**Description**	**Stratix™ Type**	**Stratix™ Connection**	**Connector**
RS232A_TXD	Transmit data	LVTTL output	U7A.AG29	J14.2
RS232A_RTS	Request to send	LVTTL output	U7A.AG30	J14.7
RS232A_RXD	Receive data	LVTTL input	U7A.AG32	J14.3
RS232A_CTS	Clear to send	LVTTL input	U7A.AG31	J14.8
GND	GND	GND		J14.5
RS232B_TXD	Transmit data	LVTTL output	U7A.AF29	J15.2
RS232B_RTS	Request to send	LVTTL output	U7A.AF30	J15.7
RS232B_RXD	Receive data	LVTTL input	U7A.AF31	J15.3
RS232B_CTS	Clear to send	LVTTL input	U7A.AF32	J15.8
GND	GND	GND		J15.5

Debug Port, Agilent and Tektronix Logic Analyzer Connectors

There is a single debug port on the Stratix™ that provides access to several different debug connectors used by popular logic analyzers from Agilent and Tektronix and to a single Altera Daughter Card interface (called PROTO1 in schematic). The three interfaces are bussed together to conserve I/O resources.

Altera Daughter Cards are available for many different applications including A/D and D/A boards, a VGA driver, a camera input to a FireWire or USB port. You can even connect a standard disk drive directly to the long header of the three with a ribbon cable.

Besides being a generally useful expansion slot, the large, 100-mil dual-row headers used for this daughter card format are extremely useful for attaching scope leads or wire-wrapping other devices to since they are large compared to the other fine-pitch headers on the board. This can facilitate prototyping of just about anything using this card.

The soft-touch probes from both Agilent and Tektronix are connector-less so that they do not require board-level components. This reduces both cost and signal integrity issues. The typical loading for these technologies is less than 1pF when installed.

The speed of this debug port is limited only by the I/O standard limitations of the Stratix™ and the amount of capacitance being driven. Though impractical, the use of both soft-touch debug probes simultaneously results in only 2pF above the capacitance of the traces themselves.

Daughter cards may vary in loading and function so they may need to be un-plugged for attaining the highest speeds (LVTTL runs around 250MHz) or for use at all for general debugging. Details of each interface are found in Table 19 below.

Table 19. Debug Port, Agilent andTektronix Logic Analyzer Connector to Stratix™ Pinouts

Signal Name	Stratix™ Connection	Debug Port	Agilent Logic Analyzer Connector	Tektronix Logic Analyzer Connector
PROTO_IO0	U7B.T31	J17.3	J20.B1	J19.A1
PROTO_IO1	U7B.T32	J17.4	J20.A1	J19.A3
PROTO_IO2	U7B.R29	J17.5	J20.B2	J19.B1
PROTO_IO3	U7B.R30	J17.6	J20.A2	J19.B3
PROTO_IO4	U7B.R31	J17.7	J20.B4	J19.A4
PROTO_IO5	U7B.R32	J17.8	J20.A4	J19.A6
PROTO_IO6	U7B.P32	J17.9	J20.B5	J19.B4
PROTO_IO7	U7B.P31	J17.10	J20.A5	J19.B6
PROTO_IO8	U7B.P30	J17.11	J20.B7	J19.A7
PROTO_IO9	U7B.P29	J17.12	J20.A7	J19.A9
PROTO_IO10	U7B.N32	J17.13	J20.B8	J19.B7
PROTO_IO11	U7B.N31	J17.14	J20.A8	J19.B9
PROTO_IO12	U7B.N30	J17.15	J20.B10	J19.A10
PROTO_IO13	U7B.N29	J17.16	J20.A10	J19.A12
PROTO_IO14	U7B.M30	J17.17	J20.B11	J19.B10
PROTO_IO15	U7B.M31	J17.18	J20.A11	J19.B12
PROTO_IO16	U7B.L31	J17.21	J20.B13	J19.A13
PROTO_IO17	U7B.L30	J17.23	J20.A13	J19.A15
PROTO_IO18	U7B.M29	J17.25	J20.B15	J21.A1
PROTO_IO19	U7B.M28	J17.27	J20.A15	J21.A3
PROTO_IO20	U7B.L32	J17.28	J20.B16	J21.B1
PROTO_IO21	U7B.K31	J17.29	J20.A16	J21.B3
PROTO_IO22	U7B.J31	J17.31	J20.B18	J21.A4
PROTO_IO23	U7B.J32	J17.32	J20.A18	J21.A6
PROTO_IO24	U7B.K29	J17.33	J20.B19	J21.B4
PROTO_IO25	U7B.K30	J17.35	J20.A19	J21.B6
PROTO_IO26	U7B.J30	J17.36	J20.B21	J21.A7
PROTO_IO27	U7B.J29	J17.37	J20.A21	J21.A9

Table 19. Debug Port, Agilent andTektronix Logic Analyzer Connector to Stratix™ Pinouts				
Signal Name	**Stratix™ Connection**	**Debug Port**	**Agilent Logic Analyzer Connector**	**Tektronix Logic Analyzer Connector**
PROTO_IO28	U7B.H32	J17.39	J20.B22	J21.B7
PROTO_IO29	U7B.H31	J16..4	J20.A22	J21.B9
PROTO_IO30	U7B.G32	J16.5	J20.B24	J21.A10
PROTO_IO31	U7B.G31	J16.6	J20.A24	J21.A12
PROTO_IO32	U7B.H29	J16.7	J20.B25	J21.B10
PROTO_IO33	U7B.H30	J16.8	J20.A25	J21.B12
PROTO_IO34	U7B.G30	J16.9	J20.B27	J21.A13
PROTO_IO35	U7B.G29	J16.10	J20.A27	J21.A15
PROTO_IO36	U7B.F32	J16.11		
PROTO_IO37	U7B.R26	J16.12		
PROTO_IO38	U7B.R25	J16.13		
PROTO_IO39	U7B.R24	J16.14		
SYS_RESETn	U7A.AE29	J17.1		
CLKA_SCRUZ	U9.7	J18.9		
CLK_TO_SCRUZ	U7A.W30	J18.11		
CLK_FROM_SCRUZ	U7J.T29	J18.13		
SCRUZ_CARDSELn	U7B.R23	J17.38		
DC_INPUT		J18.1		
3.3V		J16.2, J18.5, 7		
GND		J16.1, J17.2, 19, 22, 24, 26, 30, 34, 40, J18.2, 4, 6, 8, 10, 12, 14, 16, 18, 20	J20.A3, B3, A6, B6, A9, B9, A12, B12, A14, B14, A17, B17, A20, B20, A23, B23, A26, B26	J19.A2, B2, A5, B5, A8, B8, A11, B11, A14 J21.A2, B2, A5, B5, A8, B8, A11, B11, A14

ByteBlaster II Cable Connector Pinout

Tables 20 shows the pinout for the ByteBlaster II cable connectors on the Stratix™ Memory Board 2.

Table 20. ByteBlaster II Pinout for JTAG Header	
Signal Name	**Pin Number**
JTAG_TCK	J10.1
GND	J10.2
3.3V	J10.4, J10.6
JTAG_CONN_TDI	J10.3
JTAG_TMS	J10.5
No Connect	J10.7, J10.8
JTAG_CONN_TDO	J10.9
GND	J10.10

DDR-II SDRAM DIMM Connector Pinout

Table 21 shows the pinout for the DDR-II SDRAM DIMM connector (J28) on the Stratix™ Memory Board 2.

Table 21. DDR-II SDRAM DIMM Pinout

Signal Name	DIMM Pin Number	Stratix™ Connection
DIMM_CLK_P0	185	B16
DIMM_CLK_N0	186	A16
DIMM_CLK_P1	137	B17
DIMM_CLK_N1	138	A17
DIMM_CLK_P2	220	B18
DIMM_CLK_N2	221	A18
DIMM_CKE0	52	H19
DIMM_CKE1	171	H20
DIMM_WEn	73	G21
DIMM_CASn	74	F22
DIMM_RASn	192	F21
DIMM_CSn0	193	G22
DIMM_CSn1	76	F23
DIMM_ODT0	195	G23
DIMM_ODT1	77	G24
DIMM_SDA	119	K23
DIMM_SCL	120	J23
DIMM_RESETn	18	K21
DIMM_BA0	71	G20
DIMM_BA1	190	F20
DIMM_BA2	54	F19
DIMM_A0	188	J15
DIMM_A1	183	J14
DIMM_A2	63	H14
DIMM_A3	182	J13
DIMM_A4	61	H13
DIMM_A5	60	G12
DIMM_A6	180	F12
DIMM_A7	58	K13
DIMM_A8	179	H12
DIMM_A9	177	G10
DIMM_A10	70	F13
DIMM_A11	57	J11
DIMM_A12	176	H11
DIMM_A13	196	G13
DIMM_A14	174	J9
DIMM_A15	173	H9
DIMM_DM0	125	F7

Table 21. DDR-II SDRAM DIMM Pinout		
Signal Name	**DIMM Pin Number**	**Stratix™ Connection**
DIMM_DM1	134	F8
DIMM_DM2	146	F9
DIMM_DM3	155	F10
DIMM_DM4	202	F24
DIMM_DM5	211	F25
DIMM_DM6	223	F26
DIMM_DM7	232	C29
DIMM_DM8	164	C14
DIMM_DQS0	7	C5
DIMM_DQS1	16	E7
DIMM_DQS2	28	A7
DIMM_DQS3	37	D11
DIMM_DQS4	84	D20
DIMM_DQS5	93	D22
DIMM_DQS6	105	B26
DIMM_DQS7	114	B27
DIMM_DQS8	46	D12
DIMM_DQ0	3	D5
DIMM_DQ1	4	C3
DIMM_DQ2	9	E5
DIMM_DQ3	10	C4
DIMM_DQ4	122	D4
DIMM_DQ5	123	A4
DIMM_DQ6	128	B4
DIMM_DQ7	129	B3
DIMM_DQ8	12	D6
DIMM_DQ9	13	C6
DIMM_DQ10	21	B5
DIMM_DQ11	22	C7
DIMM_DQ12	131	A5
DIMM_DQ13	132	D7
DIMM_DQ14	140	A6
DIMM_DQ15	141	B6
DIMM_DQ16	24	B7
DIMM_DQ17	25	D8
DIMM_DQ18	30	B8
DIMM_DQ19	31	E9
DIMM_DQ20	143	A8
DIMM_DQ21	144	C9
DIMM_DQ22	149	C8
DIMM_DQ23	150	D9

Table 21. DDR-II SDRAM DIMM Pinout		
Signal Name	**DIMM Pin Number**	**Stratix™ Connection**
DIMM_DQ24	33	E11
DIMM_DQ25	34	B9
DIMM_DQ26	39	D10
DIMM_DQ27	40	C10
DIMM_DQ28	152	A9
DIMM_DQ29	153	B11
DIMM_DQ30	158	C11
DIMM_DQ31	159	B10
DIMM_DQ32	80	A20
DIMM_DQ33	81	B20
DIMM_DQ34	86	C20
DIMM_DQ35	87	E20
DIMM_DQ36	199	B21
DIMM_DQ37	200	C21
DIMM_DQ38	205	D21
DIMM_DQ39	206	A22
DIMM_DQ40	89	B22
DIMM_DQ41	90	C22
DIMM_DQ42	95	B23
DIMM_DQ43	96	C23
DIMM_DQ44	208	A24
DIMM_DQ45	209	E22
DIMM_DQ46	214	B24
DIMM_DQ47	215	D23
DIMM_DQ48	98	D24
DIMM_DQ49	99	A25
DIMM_DQ50	107	C24
DIMM_DQ51	108	B25
DIMM_DQ52	217	C25
DIMM_DQ53	218	D25
DIMM_DQ54	226	A26
DIMM_DQ55	227	E24
DIMM_DQ56	110	C26
DIMM_DQ57	111	A28
DIMM_DQ58	116	A27
DIMM_DQ59	117	D26
DIMM_DQ60	229	C27
DIMM_DQ61	230	B28
DIMM_DQ62	235	D27
DIMM_DQ63	236	E26
DIMM_CB0	42	A11

Table 21. DDR-II SDRAM DIMM Pinout		
Signal Name	**DIMM Pin Number**	**Stratix™ Connection**
DIMM_CB1	43	B12
DIMM_CB2	48	C12
DIMM_CB3	49	C13
DIMM_CB4	161	D13
DIMM_CB5	162	E13
DIMM_CB6	167	A13
DIMM_CB7	168	B13
VREF_DIMM	1	
1.8V_DIMM	51	
1.8V_DIMM	53	
1.8V_DIMM	56	
1.8V_DIMM	59	
1.8V_DIMM	62	
1.8V_DIMM	64	
1.8V_DIMM	67	
1.8V_DIMM	69	
1.8V_DIMM	72	
1.8V_DIMM	75	
1.8V_DIMM	78	
1.8V_DIMM	170	
1.8V_DIMM	172	
1.8V_DIMM	175	
1.8V_DIMM	178	
1.8V_DIMM	181	
1.8V_DIMM	184	
1.8V_DIMM	187	
1.8V_DIMM	189	
1.8V_DIMM	191	
1.8V_DIMM	194	
1.8V_DIMM	197	
1.8V_DIMM	238	
VSS	2	
VSS	5	
VSS	8	
VSS	11	
VSS	14	
VSS	17	
VSS	20	
VSS	23	
VSS	26	
VSS	29	

Table 21. DDR-II SDRAM DIMM Pinout		
Signal Name	**DIMM Pin Number**	**Stratix™ Connection**
VSS	32	
VSS	35	
VSS	38	
VSS	41	
VSS	44	
VSS	47	
VSS	50	
VSS	65	
VSS	66	
VSS	79	
VSS	82	
VSS	85	
VSS	88	
VSS	91	
VSS	94	
VSS	97	
VSS	100	
VSS	103	
VSS	106	
VSS	109	
VSS	112	
VSS	115	
VSS	118	
VSS	121	
VSS	124	
VSS	127	
VSS	130	
VSS	133	
VSS	136	
VSS	139	
VSS	142	
VSS	145	
VSS	148	
VSS	151	
VSS	154	
VSS	157	
VSS	160	
VSS	163	
VSS	166	
VSS	169	
VSS	198	

Table 21. DDR-II SDRAM DIMM Pinout		
Signal Name	**DIMM Pin Number**	**Stratix™ Connection**
VSS	201	
VSS	204	
VSS	207	
VSS	210	
VSS	213	
VSS	216	
VSS	219	
VSS	222	
VSS	225	
VSS	228	
VSS	231	
VSS	234	
VSS	237	
GND (SA0)	239	
GND (SA1)	240	
GND (SA2)	101	
N.C.	6	
N.C.	15	
N.C.	19	
N.C.	27	
N.C.	36	
N.C.	45	
N.C.	55	
N.C.	68	
N.C.	83	
N.C.	92	
N.C.	102	
N.C.	104	
N.C.	113	
N.C.	126	
N.C.	135	
N.C.	147	
N.C.	156	
N.C.	165	
N.C.	203	
N.C.	212	
N.C.	224	
N.C.	233	

Stratix™ Pinout

Table 22 shows the Stratix™ device pinout alphabetical by both signal name and pin number.

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
1.5v_stratix	D3		A2	gnd
1.5v_stratix	D30		A4	dimm_dq5
1.5v_stratix	H16		A5	dimm_dq12
1.5v_stratix	J16		A6	dimm_dq14
1.5v_stratix	M12		A7	dimm_dqs2
1.5v_stratix	M14		A8	dimm_dq20
1.5v_stratix	M19		A9	dimm_dq28
1.5v_stratix	M21		A10	gnd
1.5v_stratix	N13		A11	dimm_cb0
1.5v_stratix	N15		A12	1.8v_dimm
1.5v_stratix	N18		A13	dimm_cb6
1.5v_stratix	N20		A14	1.8v_dimm
1.5v_stratix	P12		A15	dimm_ckfb_n
1.5v_stratix	P14		A16	dimm_ck_n0
1.5v_stratix	P16		A17	dimm_ck_n1
1.5v_stratix	P17		A18	dimm_ck_n2
1.5v_stratix	P19		A19	clkb_pll5_p
1.5v_stratix	P21		A20	dimm_dq32
1.5v_stratix	R13		A21	1.8v_dimm
1.5v_stratix	R15		A22	dimm_dq39
1.5v_stratix	R18		A23	gnd
1.5v_stratix	R20		A24	dimm_dq44
1.5v_stratix	R22		A25	dimm_dq49
1.5v_stratix	T9		A26	dimm_dq54
1.5v_stratix	T14		A27	dimm_dq58
1.5v_stratix	T16		A28	dimm_dq57
1.5v_stratix	T17		A29	vrefio_loopout
1.5v_stratix	T19		A30	1.8v_dimm
1.5v_stratix	U14		A30	1.8v_dimm
1.5v_stratix	U16		A31	gnd
1.5v_stratix	U17		B1	gnd
1.5v_stratix	U19		B2	gnd
1.5v_stratix	U24		B3	dimm_dq7
1.5v_stratix	V11		B4	dimm_dq6
1.5v_stratix	V13		B5	dimm_dq10
1.5v_stratix	V15		B6	dimm_dq15
1.5v_stratix	V18		B7	dimm_dq16
1.5v_stratix	V20		B8	dimm_dq18
1.5v_stratix	W14		B9	dimm_dq25
1.5v_stratix	W16		B10	dimm_dq31
1.5v_stratix	W17		B11	dimm_dq29
1.5v_stratix	W19		B12	dimm_cb1
1.5v_stratix	Y13		B13	dimm_cb7
1.5v_stratix	Y15		B14	nc
1.5v_stratix	Y18		B15	dimm_ckfb_p
1.5v_stratix	Y20		B16	dimm_ck_p0

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
1.5v_stratix	AD16		B17	dimm_ck_p1
1.5v_stratix	AF16		B18	dimm_ck_p2
1.5v_stratix	AJ3		B19	clkb_pll5_n
1.5v_stratix	AJ30		B20	dimm_dq33
1.8v_ddrii	AA21		B21	dimm_dq36
1.8v_ddrii	AB17		B22	dimm_dq40
1.8v_ddrii	AB21		B23	dimm_dq42
1.8v_ddrii	AC17		B24	dimm_dq46
1.8v_ddrii	AC22		B25	dimm_dq51
1.8v_ddrii	AE17		B26	dimm_dqs6
1.8v_ddrii	AM21		B27	dimm_dqs7
1.8v_ddrii	AM30		B28	dimm_dq61
1.8v_dimm	A12		B29	vrefio_loopin
1.8v_dimm	A14		B30	vrefio_smaout
1.8v_dimm	A21		B31	gnd
1.8v_dimm	A30		B32	gnd
1.8v_dimm	A30		C1	3.3v
1.8v_dimm	E28		C2	3.3v
1.8v_dimm	H17		C3	dimm_dq1
1.8v_dimm	K15		C4	dimm_dq3
1.8v_dimm	K16		C5	dimm_dqs0
1.8v_dimm	K17		C6	dimm_dq9
1.8v_dimm	K22		C7	dimm_dq11
1.8v_dimm	L17		C8	dimm_dq22
1.8v_dimm	L19		C9	dimm_dq21
1.8v_dimm	M10		C10	dimm_dq27
3.3v	C1		C11	dimm_dq30
3.3v	C2		C12	dimm_cb2
3.3v	C31		C13	dimm_cb3
3.3v	C32		C14	dimm_dm8
3.3v	M1		C15	clkb_pll11_n
3.3v	M32		C16	config_d3
3.3v	T10		C17	nc
3.3v	T23		C18	dimm_ckfb_n
3.3v	U10		C19	gnd
3.3v	U23		C20	dimm_dq34
3.3v	AA1		C21	dimm_dq37
3.3v	AA32		C22	dimm_dq41
3.3v	AK1		C23	dimm_dq43
3.3v	AK2		C24	dimm_dq50
3.3v	AK31		C25	dimm_dq52
3.3v	AK32		C26	dimm_dq56
alertn	V32		C27	dimm_dq60
clk_from_scruz	T29		C28	gnd
clk4_n	AL19		C29	dimm_dm7
clk4_p	AM19		C30	vrefio_smain
clka_pll10	T6		C31	3.3v
clkb_pll11_n	C15		C32	3.3v
clkb_pll11_p	D15		D1	gnd_pll

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
clkb_pll12_n	AJ15		D2	vcca_pll1
clkb_pll12_p	AK15		D3	1.5v_stratix
clkb_pll5_n	B19		D4	dimm_dq4
clkb_pll5_p	A19		D5	dimm_dq0
clkb_pll6_n	AJ19		D6	dimm_dq8
clkb_pll6_p	AK19		D7	dimm_dq13
config_cen	AF18		D8	dimm_dq17
config_ceon	AH15		D9	dimm_dq23
config_cs	AG19		D10	dimm_dq26
config_csn	AC19		D11	dimm_dqs3
config_d0	E14		D12	dimm_dqs8
config_d1	F14		D13	dimm_cb4
config_d2	F15		D14	config_wsn
config_d3	C16		D15	clkb_pll11_p
config_d4	G19		D16	jtag_stratix_tdi
config_d5	J19		D17	gnd
config_d6	K19		D18	dimm_ckfb_p
config_d7	J20		D19	nc
config_dclk	E19		D20	dimm_dqs4
config_rsn	AB18		D21	dimm_dq38
config_ry_byn	AA19		D22	dimm_dqs5
config_wsn	D14		D23	dimm_dq47
cpld_user0	AC3		D24	dimm_dq48
cpld_user1	AC4		D25	dimm_dq53
cpld_user2	AE2		D26	dimm_dq59
cpld_user3	AE1		D27	dimm_dq62
crc_error	AF20		D28	nc
csense_sck	V29		D29	nc
csense_sdi	W32		D30	1.5v_stratix
csense_sdo	W31		D31	vcca_pll1
ddrii_a_r0	AF23		D32	gnd_pll
ddrii_a_r1	AH19		E1	nc
ddrii_a_r10	AH18		E2	nc
ddrii_a_r11	AJ20		E3	gnd_pll
ddrii_a_r12	AK18		E4	nc
ddrii_a_r13	AL20		E5	dimm_dq2
ddrii_a_r14	AM20		E6	vref_dimm
ddrii_a_r15	AL21		E7	dimm_dqs1
ddrii_a_r2	AF22		E8	vref_dimm
ddrii_a_r3	AJ18		E9	dimm_dq19
ddrii_a_r4	AG21		E10	vref_dimm
ddrii_a_r5	AH20		E11	dimm_dq24
ddrii_a_r6	AG20		E12	vref_dimm
ddrii_a_r7	AK20		E13	dimm_cb5
ddrii_a_r8	AJ21		E14	config_d0
ddrii_a_r9	AK21		E15	jtag_tms
ddrii_ba_r0	AF21		E16	vcca_pll1
ddrii_ba_r1	AE21		E17	gnd_pll
ddrii_ba_r2	AE20		E18	tempdiode_p

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
ddrii_casn_r	AE23		E19	config_dclk
ddrii_ck_n0	AM16		E20	dimm_dq35
ddrii_ck_n1	AK16		E21	vref_dimm
ddrii_ck_p0	AL16		E22	dimm_dq45
ddrii_ck_p1	AJ16		E23	vref_dimm
ddrii_cke_r	AD21		E24	dimm_dq55
ddrii_ckfb_n	AK17		E25	vref_dimm
ddrii_ckfb_n	AL15		E26	dimm_dq63
ddrii_ckfb_p	AJ17		E27	vref_dimm
ddrii_ckfb_p	AM15		E28	1.8v_dimm
ddrii_csn_r0	AF24		E29	nc
ddrii_csn_r1	AE24		E30	gnd_pll
ddrii_dm0	AM22		E31	nc
ddrii_dm1	AG22		E32	nc
ddrii_dm2	AG23		F1	fse_a2
ddrii_dm3	AG24		F2	fse_a3
ddrii_dq0	AL22		F3	nc
ddrii_dq1	AK22		F4	nc
ddrii_dq10	AK24		F5	nc
ddrii_dq11	AL25		F6	gnd
ddrii_dq12	AK25		F7	dimm_dm0
ddrii_dq13	AJ25		F8	dimm_dm1
ddrii_dq14	AJ24		F9	dimm_dm2
ddrii_dq15	AH24		F10	dimm_dm3
ddrii_dq16	AK26		F11	nc
ddrii_dq17	AM28		F12	dimm_a_r6
ddrii_dq18	AM27		F13	dimm_a_r10
ddrii_dq19	AJ26		F14	config_d1
ddrii_dq2	AL23		F15	config_d2
ddrii_dq20	AK27		F16	jtag_conn_tdi
ddrii_dq21	AL28		F17	gnd_pll
ddrii_dq22	AJ27		F18	tempdiode_n
ddrii_dq23	AH26		F19	dimm_ba_r2
ddrii_dq24	AM29		F20	dimm_ba_r1
ddrii_dq25	AL29		F21	dimm_rasn_r
ddrii_dq26	AL30		F22	dimm_casn_r
ddrii_dq27	AK29		F23	dimm_csn_r1
ddrii_dq28	AJ29		F24	dimm_dm4
ddrii_dq29	AJ28		F25	dimm_dm5
ddrii_dq3	AK23		F26	dimm_dm6
ddrii_dq30	AK30		F27	vref_dimm
ddrii_dq31	AH28		F28	nc
ddrii_dq4	AM24		F29	nc
ddrii_dq5	AH22		F30	nc
ddrii_dq6	AL24		F31	nc
ddrii_dq7	AJ23		F32	proto1_io36
ddrii_dq8	AM26		G1	fse_a6
ddrii_dq9	AM25		G2	fse_a7
ddrii_dqs0	AJ22		G3	fse_a0

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
ddrii_dqs1	AL26		G4	fse_a1
ddrii_dqs2	AL27		G5	fse_d1
ddrii_dqs3	AK28		G6	fse_d0
ddrii_odt_r	AD24		G7	nc
ddrii_rasn_r	AD23		G8	nc
ddrii_sync_clk	U29		G9	gnd
ddrii_sync_clk	AB24		G10	dimm_a_r9
ddrii_wen_r	AD22		G11	ddrupdrt_out
ddrupdnb_out	AF11		G12	dimm_a_r5
ddrupdnb_out	AG12		G13	dimm_a_r13
ddrupdrt_out	G11		G14	jtag_tck
ddrupdrt_out	H10		G15	jtag_trstn
dig_1_a	AC6		G16	ep1s_statusn
dig_1_b	AC5		G17	vcca_pll1
dig_1_c	AC8		G18	ep1s_config_done
dig_1_d	AC7		G19	config_d4
dig_1_dp	AA6		G20	dimm_ba_r0
dig_1_e	AB6		G21	dimm_wen_r
dig_1_f	AB7		G22	dimm_csn_r0
dig_1_g	AA7		G23	dimm_odt_r0
dig_2_a	AE8		G24	dimm_odt_r1
dig_2_b	AE7		G25	nc
dig_2_c	AD5		G26	nc
dig_2_d	AD6		G27	nc
dig_2_dp	AD8		G28	nc
dig_2_e	AE5		G29	proto1_io35
dig_2_f	AE6		G30	proto1_io34
dig_2_g	AD7		G31	proto1_io31
dimm_a_r0	J15		G32	proto1_io30
dimm_a_r1	J14		H1	fse_a8
dimm_a_r10	F13		H2	fse_a9
dimm_a_r11	J11		H3	fse_a4
dimm_a_r12	H11		H4	fse_a5
dimm_a_r13	G13		H5	fse_d4
dimm_a_r14	J9		H6	fse_d5
dimm_a_r15	H9		H7	fse_d3
dimm_a_r2	H14		H8	fse_d2
dimm_a_r3	J13		H9	dimm_a_r15
dimm_a_r4	H13		H10	ddrupdrt_out
dimm_a_r5	G12		H11	dimm_a_r12
dimm_a_r6	F12		H12	dimm_a_r8
dimm_a_r7	K13		H13	dimm_a_r4
dimm_a_r8	H12		H14	dimm_a_r2
dimm_a_r9	G10		H15	gnd_pll
dimm_ba_r0	G20		H16	1.5v_stratix
dimm_ba_r1	F20		H17	1.8v_dimm
dimm_ba_r2	F19		H18	gnd
dimm_casn_r	F22		H19	dimm_cke_r0
dimm_cb0	A11		H20	dimm_cke_r1

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
dimm_cb1	B12		H21	nc
dimm_cb2	C12		H22	nc
dimm_cb3	C13		H23	nc
dimm_cb4	D13		H24	gnd
dimm_cb5	E13		H25	gnd
dimm_cb6	A13		H26	nc
dimm_cb7	B13		H27	gnd
dimm_ck_n0	A16		H28	nc
dimm_ck_n1	A17		H29	proto1_io32
dimm_ck_n2	A18		H30	proto1_io33
dimm_ck_p0	B16		H31	proto1_io29
dimm_ck_p1	B17		H32	proto1_io28
dimm_ck_p2	B18		J1	fse_a15
dimm_cke_r0	H19		J2	fse_a14
dimm_cke_r1	H20		J3	fse_a10
dimm_ckfb_n	A15		J4	fse_a11
dimm_ckfb_n	C18		J5	fse_d8
dimm_ckfb_p	B15		J6	fse_d9
dimm_ckfb_p	D18		J7	fse_d6
dimm_csn_r0	G22		J8	fse_d7
dimm_csn_r1	F23		J9	dimm_a_r14
dimm_dm0	F7		J10	nc
dimm_dm1	F8		J11	dimm_a_r11
dimm_dm2	F9		J12	enddrt_in
dimm_dm3	F10		J13	dimm_a_r3
dimm_dm4	F24		J14	dimm_a_r1
dimm_dm5	F25		J15	dimm_a_r0
dimm_dm6	F26		J16	1.5v_stratix
dimm_dm7	C29		J17	gnd
dimm_dm8	C14		J18	ep1s_confign
dimm_dq0	D5		J19	config_d5
dimm_dq1	C3		J20	config_d7
dimm_dq10	B5		J21	nc
dimm_dq11	C7		J22	gnd
dimm_dq12	A5		J23	dimm_scl
dimm_dq13	D7		J24	nc
dimm_dq14	A6		J25	nc
dimm_dq15	B6		J26	nc
dimm_dq16	B7		J27	gnd
dimm_dq17	D8		J28	gnd
dimm_dq18	B8		J29	proto1_io27
dimm_dq19	E9		J30	proto1_io26
dimm_dq2	E5		J31	proto1_io22
dimm_dq20	A8		J32	proto1_io23
dimm_dq21	C9		K1	gnd
dimm_dq22	C8		K2	fse_a17
dimm_dq23	D9		K3	fse_a13
dimm_dq24	E11		K4	fse_a12
dimm_dq25	B9		K5	fse_d12

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
dimm_dq26	D10		K6	fse_d13
dimm_dq27	C10		K7	fse_d11
dimm_dq28	A9		K8	fse_d10
dimm_dq29	B11		K9	nc
dimm_dq3	C4		K10	nc
dimm_dq30	C11		K11	nc
dimm_dq31	B10		K12	enddrt_in
dimm_dq32	A20		K13	dimm_a_r7
dimm_dq33	B20		K14	nc
dimm_dq34	C20		K15	1.8v_dimm
dimm_dq35	E20		K16	1.8v_dimm
dimm_dq36	B21		K17	1.8v_dimm
dimm_dq37	C21		K18	nc
dimm_dq38	D21		K19	config_d6
dimm_dq39	A22		K20	nc
dimm_dq4	D4		K21	dimm_resetn
dimm_dq40	B22		K22	1.8v_dimm
dimm_dq41	C22		K23	dimm_sda
dimm_dq42	B23		K24	dimm_sync_clk
dimm_dq43	C23		K25	nc
dimm_dq44	A24		K26	nc
dimm_dq45	E22		K27	nc
dimm_dq46	B24		K28	nc
dimm_dq47	D23		K29	proto1_io24
dimm_dq48	D24		K30	proto1_io25
dimm_dq49	A25		K31	proto1_io21
dimm_dq5	A4		K32	gnd
dimm_dq50	C24		L1	fse_a16
dimm_dq51	B25		L2	fse_a20
dimm_dq52	C25		L3	fse_a21
dimm_dq53	D25		L4	gnd
dimm_dq54	A26		L5	nc
dimm_dq55	E24		L6	fse_d14
dimm_dq56	C26		L7	fse_d15
dimm_dq57	A28		L8	gnd
dimm_dq58	A27		L9	nc
dimm_dq59	D26		L10	nc
dimm_dq6	B4		L11	nc
dimm_dq60	C27		L12	nc
dimm_dq61	B28		L13	nc
dimm_dq62	D27		L14	gnd
dimm_dq63	E26		L15	gnd
dimm_dq7	B3		L16	gnd_pll
dimm_dq8	D6		L17	1.8v_dimm
dimm_dq9	C6		L18	gnd
dimm_dqs0	C5		L19	1.8v_dimm
dimm_dqs1	E7		L20	nc
dimm_dqs2	A7		L21	nc
dimm_dqs3	D11		L22	nc

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
dimm_dqs4	D20		L23	nc
dimm_dqs5	D22		L24	nc
dimm_dqs6	B26		L25	vref_dimm
dimm_dqs7	B27		L26	nc
dimm_dqs8	D12		L27	nc
dimm_odt_r0	G23		L28	nc
dimm_odt_r1	G24		L29	gnd
dimm_rasn_r	F21		L30	proto1_io17
dimm_resetn	K21		L31	proto1_io16
dimm_scl	J23		L32	proto1_io20
dimm_sda	K23		M1	3.3v
dimm_sync_clk	K24		M2	fse_a22
dimm_sync_clk	T27		M3	fse_a23
dimm_wen_r	G21		M4	fse_a18
enddrb_in	AC12		M5	fse_a19
enddrb_in	AE12		M6	fse_d16
enddrt_in	J12		M7	fse_d17
enddrt_in	K12		M8	fse_d18
enet_adsn	W7		M9	fse_d19
enet_aen	W8		M10	1.8v_dimm
enet_ben0	V8		M11	nc
enet_ben1	V7		M12	1.5v_stratix
enet_ben2	V5		M13	gnd
enet_ben3	V6		M14	1.5v_stratix
enet_cyclen	V9		M15	gnd
enet_datacsn	V10		M16	gnd
enet_intrq0	W10		M17	gnd
enet_iochrdy	W9		M18	gnd
enet_iorn	Y10		M19	1.5v_stratix
enet_iown	Y9		M20	gnd
enet_lclk	W5		M21	1.5v_stratix
enet_ldevn	W6		M22	nc
enet_rdyrtnn	Y7		M23	nc
enet_srdyn	Y5		M24	gnd
enet_vlbusn	Y6		M25	gnd
enet_w_rn	Y8		M26	nc
ep1s_config_done	G18		M27	gnd
ep1s_confign	J18		M28	proto1_io19
ep1s_init_done	AE15		M29	proto1_io18
ep1s_statusn	G16		M30	proto1_io14
flash_byten	AB3		M31	proto1_io15
flash_cen	Y4		M32	3.3v
flash_oen	Y3		N1	fse_a26
flash_resetn	AA2		N2	gnd
flash_ry_byn	AB2		N3	fse_a24
flash_wen	AA3		N4	fse_a25
fse_a0	G3		N5	fse_d22
fse_a1	G4		N6	fse_d23
fse_a10	J3		N7	fse_d26

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
fse_a11	J4		N8	fse_d27
fse_a12	K4		N9	fse_d21
fse_a13	K3		N10	fse_d20
fse_a14	J2		N11	nc
fse_a15	J1		N12	gnd
fse_a16	L1		N13	1.5v_stratix
fse_a17	K2		N14	gnd
fse_a18	M4		N15	1.5v_stratix
fse_a19	M5		N16	gnd
fse_a2	F1		N17	gnd
fse_a20	L2		N18	1.5v_stratix
fse_a21	L3		N19	gnd
fse_a22	M2		N20	1.5v_stratix
fse_a23	M3		N21	gnd
fse_a24	N3		N22	nc
fse_a25	N4		N23	nc
fse_a26	N1		N24	gnd
fse_a3	F2		N25	nc
fse_a4	H3		N26	nc
fse_a5	H4		N27	nc
fse_a6	G1		N28	nc
fse_a7	G2		N29	proto1_io13
fse_a8	H1		N30	proto1_io12
fse_a9	H2		N31	proto1_io11
fse_d0	G6		N32	proto1_io10
fse_d1	G5		P1	gnd
fse_d10	K8		P2	nc
fse_d11	K7		P3	gnd
fse_d12	K5		P4	gnd
fse_d13	K6		P5	fse_d29
fse_d14	L6		P6	fse_d28
fse_d15	L7		P7	gnd
fse_d16	M6		P8	gnd
fse_d17	M7		P9	fse_d24
fse_d18	M8		P10	fse_d25
fse_d19	M9		P11	nc
fse_d2	H8		P12	1.5v_stratix
fse_d20	N10		P13	gnd
fse_d21	N9		P14	1.5v_stratix
fse_d22	N5		P15	gnd
fse_d23	N6		P16	1.5v_stratix
fse_d24	P9		P17	1.5v_stratix
fse_d25	P10		P18	gnd
fse_d26	N7		P19	1.5v_stratix
fse_d27	N8		P20	gnd
fse_d28	P6		P21	1.5v_stratix
fse_d29	P5		P22	nc
fse_d3	H7		P23	nc
fse_d30	R10		P24	nc

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
fse_d31	R9		P25	gnd
fse_d4	H5		P26	nc
fse_d5	H6		P27	gnd
fse_d6	J7		P28	nc
fse_d7	J8		P29	proto1_io9
fse_d8	J5		P30	proto1_io8
fse_d9	J6		P31	proto1_io7
gnd	A2		P32	proto1_io6
gnd	A10		R1	nc
gnd	A23		R2	nc
gnd	A31		R3	nc
gnd	B1		R4	nc
gnd	B2		R5	gnd
gnd	B31		R6	gnd
gnd	B32		R7	nc
gnd	C19		R8	nc
gnd	C28		R9	fse_d31
gnd	D17		R10	fse_d30
gnd	F6		R11	nc
gnd	G9		R12	gnd
gnd	H18		R13	1.5v_stratix
gnd	H24		R14	gnd
gnd	H25		R15	1.5v_stratix
gnd	H27		R16	gnd
gnd	J17		R17	gnd
gnd	J22		R18	1.5v_stratix
gnd	J27		R19	gnd
gnd	J28		R20	1.5v_stratix
gnd	K1		R21	vref_dimm
gnd	K32		R22	1.5v_stratix
gnd	L4		R23	scruz_cardseln
gnd	L8		R24	proto1_io39
gnd	L14		R25	proto1_io38
gnd	L15		R26	proto1_io37
gnd	L18		R27	gnd
gnd	L29		R28	gnd
gnd	M13		R29	proto1_io2
gnd	M15		R30	proto1_io3
gnd	M16		R31	proto1_io4
gnd	M17		R32	proto1_io5
gnd	M18		T1	gnd
gnd	M20		T2	gnd
gnd	M24		T3	nc
gnd	M25		T4	gnd
gnd	M27		T5	nc
gnd	N2		T6	clka_pll10
gnd	N12		T7	gnd_pll
gnd	N14		T8	vcca_pll2
gnd	N16		T9	1.5v_stratix

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
gnd	N17		T10	3.3v
gnd	N19		T11	nc
gnd	N21		T12	gnd
gnd	N24		T13	gnd
gnd	P1		T14	1.5v_stratix
gnd	P3		T15	gnd
gnd	P4		T16	1.5v_stratix
gnd	P7		T17	1.5v_stratix
gnd	P8		T18	gnd
gnd	P13		T19	1.5v_stratix
gnd	P15		T20	gnd
gnd	P18		T21	gnd
gnd	P20		T22	gnd_pll
gnd	P25		T23	3.3v
gnd	P27		T24	gnd_pll
gnd	R5		T25	vcca_pll1
gnd	R6		T26	gnd_pll
gnd	R12		T27	dimm_sync_clk
gnd	R14		T28	nc
gnd	R16		T29	clk_from_scruz
gnd	R17		T30	nc
gnd	R19		T31	proto1_io0
gnd	R27		T32	proto1_io1
gnd	R28		U1	nc
gnd	T1		U2	qdrii_sync_clk
gnd	T2		U3	qdrii_cq_n1
gnd	T4		U4	qdrii_cq_p1
gnd	T12		U5	sram_ben0
gnd	T13		U6	sram_ben1
gnd	T15		U7	gnd_pll
gnd	T18		U8	vcca_pll2
gnd	T20		U9	gnd_pll
gnd	T21		U10	3.3v
gnd	U12		U11	gnd_pll
gnd	U13		U12	gnd
gnd	U15		U13	gnd
gnd	U18		U14	1.5v_stratix
gnd	U20		U15	gnd
gnd	U21		U16	1.5v_stratix
gnd	U31		U17	1.5v_stratix
gnd	V14		U18	gnd
gnd	V16		U19	1.5v_stratix
gnd	V17		U20	gnd
gnd	V19		U21	gnd
gnd	V25		U22	nc
gnd	V27		U23	3.3v
gnd	V28		U24	1.5v_stratix
gnd	W3		U25	vcca_pll1
gnd	W4		U26	gnd_pll

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
gnd	W13		U27	tsense_smb_clk
gnd	W15		U28	tsense_smb_data
gnd	W18		U29	ddrii_sync_clk
gnd	W20		U30	nc
gnd	W25		U31	gnd
gnd	Y1		U32	nc
gnd	Y2		V1	sram_ben3
gnd	Y14		V2	sram_ben2
gnd	Y16		V3	sram_oen
gnd	Y17		V4	sram_csn
gnd	Y19		V5	enet_ben2
gnd	AA8		V6	enet_ben3
gnd	AA9		V7	enet_ben1
gnd	AA16		V8	enet_ben0
gnd	AA17		V9	enet_cyclen
gnd	AA24		V10	enet_datacsn
gnd	AA25		V11	1.5v_stratix
gnd	AA26		V12	nc
gnd	AA27		V13	1.5v_stratix
gnd	AB5		V14	gnd
gnd	AB14		V15	1.5v_stratix
gnd	AB19		V16	gnd
gnd	AB22		V17	gnd
gnd	AB28		V18	1.5v_stratix
gnd	AC1		V19	gnd
gnd	AC18		V20	1.5v_stratix
gnd	AC32		V21	vref_ddrii
gnd	AD17		V22	nc
gnd	AD20		V23	nc
gnd	AE3		V24	nc
gnd	AF1		V25	gnd
gnd	AF2		V26	nc
gnd	AF4		V27	gnd
gnd	AF5		V28	gnd
gnd	AF6		V29	csense_sck
gnd	AF7		V30	nc
gnd	AF8		V31	overtempn
gnd	AF17		V32	alertn
gnd	AF25		W1	nc
gnd	AF26		W2	sram_wen
gnd	AF27		W3	gnd
gnd	AF28		W4	gnd
gnd	AH7		W5	enet_lclk
gnd	AJ13		W6	enet_ldevn
gnd	AK13		W7	enet_adsn
gnd	AL1		W8	enet_aen
gnd	AL2		W9	enet_iochrdy
gnd	AL31		W10	enet_intrq0
gnd	AL32		W11	nc

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
gnd	AM2		W12	nc
gnd	AM10		W13	gnd
gnd	AM23		W14	1.5v_stratix
gnd	AM31		W15	gnd
gnd_pll	D1		W16	1.5v_stratix
gnd_pll	D32		W17	1.5v_stratix
gnd_pll	E3		W18	gnd
gnd_pll	E17		W19	1.5v_stratix
gnd_pll	E30		W20	gnd
gnd_pll	F17		W21	nc
gnd_pll	H15		W22	nc
gnd_pll	L16		W23	nc
gnd_pll	T7		W24	nc
gnd_pll	T22		W25	gnd
gnd_pll	T24		W26	nc
gnd_pll	T26		W27	nc
gnd_pll	U7		W28	nc
gnd_pll	U9		W29	nc
gnd_pll	U11		W30	n26029053
gnd_pll	U26		W31	csense_sdo
gnd_pll	AB16		W32	csense_sdi
gnd_pll	AE16		Y1	gnd
gnd_pll	AH3		Y2	gnd
gnd_pll	AH16		Y3	flash_oen
gnd_pll	AH17		Y4	flash_cen
gnd_pll	AH30		Y5	enet_srdyn
gnd_pll	AJ1		Y6	enet_vlbusn
gnd_pll	AJ32		Y7	enet_rdyrtnn
jtag_conn_tdi	F16		Y8	enet_w_rn
jtag_stratix_tdi	D16		Y9	enet_iown
jtag_tck	G14		Y10	enet_iorn
jtag_tms	E15		Y11	nc
jtag_trstn	G15		Y12	nc
msel0	AG18		Y13	1.5v_stratix
msel1	AE18		Y14	gnd
msel2	AE19		Y15	1.5v_stratix
n26029053	W30		Y16	gnd
nc	B14		Y17	gnd
nc	C17		Y18	1.5v_stratix
nc	D19		Y19	gnd
nc	D28		Y20	1.5v_stratix
nc	D29		Y21	nc
nc	E1		Y22	nc
nc	E2		Y23	nc
nc	E4		Y24	nc
nc	E29		Y25	nc
nc	E31		Y26	nc
nc	E32		Y27	nc
nc	F3		Y28	nc

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
nc	F4		Y29	user_led4
nc	F5		Y30	user_led5
nc	F11		Y31	user_led6
nc	F28		Y32	user_led7
nc	F29		AA1	3.3v
nc	F30		AA2	flash_resetn
nc	F31		AA3	flash_wen
nc	G7		AA4	nc
nc	G8		AA5	nc
nc	G25		AA6	dig_1_dp
nc	G26		AA7	dig_1_g
nc	G27		AA8	gnd
nc	G28		AA9	gnd
nc	H21		AA10	vref_qdrii
nc	H22		AA11	nc
nc	H23		AA12	qdrii_a7
nc	H26		AA13	nc
nc	H28		AA14	vdd_qdrii_io
nc	J10		AA15	qdrii_k_p0
nc	J21		AA16	gnd
nc	J24		AA17	gnd
nc	J25		AA18	qdrii_bwsn0
nc	J26		AA19	config_ry_byn
nc	K9		AA20	spgm2
nc	K10		AA21	1.8v_ddrii
nc	K11		AA22	nc
nc	K14		AA23	vref_ddrii
nc	K18		AA24	gnd
nc	K20		AA25	gnd
nc	K25		AA26	gnd
nc	K26		AA27	gnd
nc	K27		AA28	user_dipsw7
nc	K28		AA29	user_dipsw6
nc	L5		AA30	user_led2
nc	L9		AA31	user_led3
nc	L10		AA32	3.3v
nc	L11		AB1	nc
nc	L12		AB2	flash_ry_byn
nc	L13		AB3	flash_byten
nc	L20		AB4	nc
nc	L21		AB5	gnd
nc	L22		AB6	dig_1_e
nc	L23		AB7	dig_1_f
nc	L24		AB8	vref_qdrii
nc	L26		AB9	nc
nc	L27		AB10	nc
nc	L28		AB11	qdrii_a6
nc	M11		AB12	nc
nc	M22		AB13	qdrii_a10

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
nc	M23		AB14	gnd
nc	M26		AB15	qdrii_rpsn1
nc	N11		AB16	gnd_pll
nc	N22		AB17	1.8v_ddrii
nc	N23		AB18	config_rsn
nc	N25		AB19	gnd
nc	N26		AB20	nc
nc	N27		AB21	1.8v_ddrii
nc	N28		AB22	gnd
nc	P2		AB23	nc
nc	P11		AB24	ddrii_sync_clk
nc	P22		AB25	vref_ddrii
nc	P23		AB26	nc
nc	P24		AB27	nc
nc	P26		AB28	gnd
nc	P28		AB29	nc
nc	R1		AB30	user_led0
nc	R2		AB31	user_led1
nc	R3		AB32	user_dipsw5
nc	R4		AC1	gnd
nc	R7		AC2	nc
nc	R8		AC3	cpld_user0
nc	R11		AC4	cpld_user1
nc	T3		AC5	dig_1_b
nc	T5		AC6	dig_1_a
nc	T11		AC7	dig_1_d
nc	T28		AC8	dig_1_c
nc	T30		AC9	qdrii_a9
nc	U1		AC10	nc
nc	U22		AC11	nc
nc	U30		AC12	enddrb_in
nc	U32		AC13	qdrii_a12
nc	V12		AC14	qdrii_a18
nc	V22		AC15	qdrii_k_p1
nc	V23		AC16	vdd_qdrii_io
nc	V24		AC17	1.8v_ddrii
nc	V26		AC18	gnd
nc	V30		AC19	config_csn
nc	W1		AC20	nc
nc	W11		AC21	nc
nc	W12		AC22	1.8v_ddrii
nc	W21		AC23	nc
nc	W22		AC24	nc
nc	W23		AC25	nc
nc	W24		AC26	nc
nc	W26		AC27	nc
nc	W27		AC28	nc
nc	W28		AC29	user_dipsw1
nc	W29		AC30	user_dipsw0

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
nc	Y11		AC31	user_dipsw4
nc	Y12		AC32	gnd
nc	Y21		AD1	nc
nc	Y22		AD2	nc
nc	Y23		AD3	nc
nc	Y24		AD4	nc
nc	Y25		AD5	dig_2_c
nc	Y26		AD6	dig_2_d
nc	Y27		AD7	dig_2_g
nc	Y28		AD8	dig_2_dp
nc	AA4		AD9	qdrii_a4
nc	AA5		AD10	qdrii_a19
nc	AA11		AD11	nc
nc	AA13		AD12	qdrii_a11
nc	AA22		AD13	qdrii_a13
nc	AB1		AD14	qdrii_a16
nc	AB4		AD15	qdrii_k_n0
nc	AB9		AD16	1.5v_stratix
nc	AB10		AD17	gnd
nc	AB12		AD18	spgm0
nc	AB20		AD19	nc
nc	AB23		AD20	gnd
nc	AB26		AD21	ddrii_cke_r
nc	AB27		AD22	ddrii_wen_r
nc	AB29		AD23	ddrii_rasn_r
nc	AC2		AD24	ddrii_odt_r
nc	AC10		AD25	nc
nc	AC11		AD26	nc
nc	AC20		AD27	nc
nc	AC21		AD28	nc
nc	AC23		AD29	user_pb2
nc	AC24		AD30	nc
nc	AC25		AD31	user_dipsw2
nc	AC26		AD32	user_dipsw3
nc	AC27		AE1	cpld_user3
nc	AC28		AE2	cpld_user2
nc	AD1		AE3	gnd
nc	AD2		AE4	nc
nc	AD3		AE5	dig_2_e
nc	AD4		AE6	dig_2_f
nc	AD11		AE7	dig_2_b
nc	AD19		AE8	dig_2_a
nc	AD25		AE9	qdrii_a3
nc	AD26		AE10	nc
nc	AD27		AE11	qdrii_a8
nc	AD28		AE12	enddrb_in
nc	AD30		AE13	qdrii_a15
nc	AE4		AE14	qdrii_a14
nc	AE10		AE15	ep1s_init_done

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
nc	AE22		AE16	gnd_pll
nc	AE25		AE17	1.8v_ddrii
nc	AE26		AE18	msel1
nc	AE27		AE19	msel2
nc	AE28		AE20	ddrii_ba_r2
nc	AF3		AE21	ddrii_ba_r1
nc	AG1		AE22	nc
nc	AG2		AE23	ddrii_casn_r
nc	AG3		AE24	ddrii_csn_r1
nc	AG4		AE25	nc
nc	AG5		AE26	nc
nc	AG7		AE27	nc
nc	AG8		AE28	nc
nc	AG25		AE29	sys_resetn
nc	AG26		AE30	safen
nc	AG27		AE31	user_pb0
nc	AG28		AE32	user_pb1
nc	AH1		AF1	gnd
nc	AH2		AF2	gnd
nc	AH4		AF3	nc
nc	AH29		AF4	gnd
nc	AH31		AF5	gnd
nc	AH32		AF6	gnd
nc	AJ12		AF7	gnd
nc	AL13		AF8	gnd
nio_pullup	AF15		AF9	qdrii_a0
overtempn	V31		AF10	qdrii_a5
pll_ena	AF19		AF11	ddrupdnb_out
pll6_fb_n	AM17		AF12	qdrii_wpsn0
pll6_fb_p	AL17		AF13	qdrii_a17
pll6_out3_n	AM18		AF14	runlu
pll6_out3_p	AL18		AF15	nio_pullup
porsel	AG15		AF16	1.5v_stratix
proto1_io0	T31		AF17	gnd
proto1_io1	T32		AF18	config_cen
proto1_io10	N32		AF19	pll_ena
proto1_io11	N31		AF20	crc_error
proto1_io12	N30		AF21	ddrii_ba_r0
proto1_io13	N29		AF22	ddrii_a_r2
proto1_io14	M30		AF23	ddrii_a_r0
proto1_io15	M31		AF24	ddrii_csn_r0
proto1_io16	L31		AF25	gnd
proto1_io17	L30		AF26	gnd
proto1_io18	M29		AF27	gnd
proto1_io19	M28		AF28	gnd
proto1_io2	R29		AF29	rs232b_txd
proto1_io20	L32		AF30	rs232b_rts
proto1_io21	K31		AF31	rs232b_rxd
proto1_io22	J31		AF32	rs232b_cts

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
proto1_io23	J32		AG1	nc
proto1_io24	K29		AG2	nc
proto1_io25	K30		AG3	nc
proto1_io26	J30		AG4	nc
proto1_io27	J29		AG5	nc
proto1_io28	H32		AG6	vref_qdrii
proto1_io29	H31		AG7	nc
proto1_io3	R30		AG8	nc
proto1_io30	G32		AG9	qdrii_a1
proto1_io31	G31		AG10	qdrii_a2
proto1_io32	H29		AG11	qdrii_bwsn1
proto1_io33	H30		AG12	ddrupdnb_out
proto1_io34	G30		AG13	qdrii_rpsn0
proto1_io35	G29		AG14	spgm1
proto1_io36	F32		AG15	porsel
proto1_io37	R26		AG16	vcca_pll2
proto1_io38	R25		AG17	vcca_pll2
proto1_io39	R24		AG18	msel0
proto1_io4	R31		AG19	config_cs
proto1_io5	R32		AG20	ddrii_a_r6
proto1_io6	P32		AG21	ddrii_a_r4
proto1_io7	P31		AG22	ddrii_dm1
proto1_io8	P30		AG23	ddrii_dm2
proto1_io9	P29		AG24	ddrii_dm3
qdrii_a0	AF9		AG25	nc
qdrii_a1	AG9		AG26	nc
qdrii_a10	AB13		AG27	nc
qdrii_a11	AD12		AG28	nc
qdrii_a12	AC13		AG29	rs232a_txd
qdrii_a13	AD13		AG30	rs232a_rts
qdrii_a14	AE14		AG31	rs232a_cts
qdrii_a15	AE13		AG32	rs232a_rxd
qdrii_a16	AD14		AH1	nc
qdrii_a17	AF13		AH2	nc
qdrii_a18	AC14		AH3	gnd_pll
qdrii_a19	AD10		AH4	nc
qdrii_a2	AG10		AH5	qdrii_d8
qdrii_a3	AE9		AH6	vref_qdrii
qdrii_a4	AD9		AH7	gnd
qdrii_a5	AF10		AH8	vref_qdrii
qdrii_a6	AB11		AH9	qdrii_d13
qdrii_a7	AA12		AH10	vref_qdrii
qdrii_a8	AE11		AH11	qdrii_q15
qdrii_a9	AC9		AH12	vref_qdrii
qdrii_bwsn0	AA18		AH13	vdd_qdrii_io
qdrii_bwsn1	AG11		AH14	user_pb3
qdrii_cq_n1	U3		AH15	config_ceon
qdrii_cq_p0	AK8		AH16	gnd_pll
qdrii_cq_p1	U4		AH17	gnd_pll

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
qdrii_d0	AK4		AH18	ddrii_a_r10
qdrii_d1	AL3		AH19	ddrii_a_r1
qdrii_d10	AJ8		AH20	ddrii_a_r5
qdrii_d11	AM8		AH21	vref_ddrii
qdrii_d12	AJ11		AH22	ddrii_dq5
qdrii_d13	AH9		AH23	vref_ddrii
qdrii_d14	AJ9		AH24	ddrii_dq15
qdrii_d15	AK9		AH25	vref_ddrii
qdrii_d16	AM11		AH26	ddrii_dq23
qdrii_d17	AL12		AH27	vref_ddrii
qdrii_d2	AK5		AH28	ddrii_dq31
qdrii_d3	AJ4		AH29	nc
qdrii_d4	AK3		AH30	gnd_pll
qdrii_d5	AM4		AH31	nc
qdrii_d6	AL4		AH32	nc
qdrii_d7	AM7		AJ1	gnd_pll
qdrii_d8	AH5		AJ2	vcca_pll2
qdrii_d9	AL7		AJ3	1.5v_stratix
qdrii_k_n0	AD15		AJ4	qdrii_d3
qdrii_k_n1	AK14		AJ5	qdrii_q0
qdrii_k_p0	AA15		AJ6	qdrii_q8
qdrii_k_p1	AC15		AJ7	qdrii_q2
qdrii_q0	AJ5		AJ8	qdrii_d10
qdrii_q1	AM6		AJ9	qdrii_d14
qdrii_q10	AL10		AJ10	qdrii_q17
qdrii_q11	AL11		AJ11	qdrii_d12
qdrii_q12	AK10		AJ12	nc
qdrii_q13	AM9		AJ13	gnd
qdrii_q14	AL9		AJ14	vccsel
qdrii_q15	AH11		AJ15	clkb_pll12_n
qdrii_q16	AL8		AJ16	ddrii_ck_p1
qdrii_q17	AJ10		AJ17	ddrii_ckfb_p
qdrii_q2	AJ7		AJ18	ddrii_a_r3
qdrii_q3	AL6		AJ19	clkb_pll6_n
qdrii_q4	AM5		AJ20	ddrii_a_r11
qdrii_q5	AK7		AJ21	ddrii_a_r8
qdrii_q6	AL5		AJ22	ddrii_dqs0
qdrii_q7	AK6		AJ23	ddrii_dq7
qdrii_q8	AJ6		AJ24	ddrii_dq14
qdrii_q9	AK11		AJ25	ddrii_dq13
qdrii_rpsn0	AG13		AJ26	ddrii_dq19
qdrii_rpsn1	AB15		AJ27	ddrii_dq22
qdrii_sync_clk	U2		AJ28	ddrii_dq29
qdrii_sync_clk	AM13		AJ29	ddrii_dq28
qdrii_wpsn0	AF12		AJ30	1.5v_stratix
qdrii_wpsn1	AM14		AJ31	vcca_pll2
rs232a_cts	AG31		AJ32	gnd_pll
rs232a_rts	AG30		AK1	3.3v
rs232a_rxd	AG32		AK2	3.3v

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
rs232a_txd	AG29		AK3	qdrii_d4
rs232b_cts	AF32		AK4	qdrii_d0
rs232b_rts	AF30		AK5	qdrii_d2
rs232b_rxd	AF31		AK6	qdrii_q7
rs232b_txd	AF29		AK7	qdrii_q5
runlu	AF14		AK8	qdrii_cq_p0
safen	AE30		AK9	qdrii_d15
scruz_cardseln	R23		AK10	qdrii_q12
spgm0	AD18		AK11	qdrii_q9
spgm1	AG14		AK12	vdd_qdrii_io
spgm2	AA20		AK13	gnd
sram_ben0	U5		AK14	qdrii_k_n1
sram_ben1	U6		AK15	clkb_pll12_p
sram_ben2	V2		AK16	ddrii_ck_n1
sram_ben3	V1		AK17	ddrii_ckfb_n
sram_csn	V4		AK18	ddrii_a_r12
sram_oen	V3		AK19	clkb_pll6_p
sram_wen	W2		AK20	ddrii_a_r7
sys_resetn	AE29		AK21	ddrii_a_r9
tempdiode_n	F18		AK22	ddrii_dq1
tempdiode_p	E18		AK23	ddrii_dq3
tsense_smb_clk	U27		AK24	ddrii_dq10
tsense_smb_data	U28		AK25	ddrii_dq12
user_dipsw0	AC30		AK26	ddrii_dq16
user_dipsw1	AC29		AK27	ddrii_dq20
user_dipsw2	AD31		AK28	ddrii_dqs3
user_dipsw3	AD32		AK29	ddrii_dq27
user_dipsw4	AC31		AK30	ddrii_dq30
user_dipsw5	AB32		AK31	3.3v
user_dipsw6	AA29		AK32	3.3v
user_dipsw7	AA28		AL1	gnd
user_led0	AB30		AL2	gnd
user_led1	AB31		AL3	qdrii_d1
user_led2	AA30		AL4	qdrii_d6
user_led3	AA31		AL5	qdrii_q6
user_led4	Y29		AL6	qdrii_q3
user_led5	Y30		AL7	qdrii_d9
user_led6	Y31		AL8	qdrii_q16
user_led7	Y32		AL9	qdrii_q14
user_pb0	AE31		AL10	qdrii_q10
user_pb1	AE32		AL11	qdrii_q11
user_pb2	AD29		AL12	qdrii_d17
user_pb3	AH14		AL13	nc
vcca_pll1	D2		AL14	vdd_qdrii_io
vcca_pll1	D31		AL15	ddrii_ckfb_n
vcca_pll1	E16		AL16	ddrii_ck_p0
vcca_pll1	G17		AL17	pll6_fb_p
vcca_pll1	T25		AL18	pll6_out3_p
vcca_pll1	U25		AL19	clk4_n

Table 22. Stratix™ Pinout				
Alphabetical by Signal Name			**Alphabetical by Pin Number**	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
vcca_pll2	T8		AL20	ddrii_a_r13
vcca_pll2	U8		AL21	ddrii_a_r15
vcca_pll2	AG16		AL22	ddrii_dq0
vcca_pll2	AG17		AL23	ddrii_dq2
vcca_pll2	AJ2		AL24	ddrii_dq6
vcca_pll2	AJ31		AL25	ddrii_dq11
vccsel	AJ14		AL26	ddrii_dqs1
vdd_qdrii_io	AA14		AL27	ddrii_dqs2
vdd_qdrii_io	AC16		AL28	ddrii_dq21
vdd_qdrii_io	AH13		AL29	ddrii_dq25
vdd_qdrii_io	AK12		AL30	ddrii_dq26
vdd_qdrii_io	AL14		AL31	gnd
vdd_qdrii_io	AM3		AL32	gnd
vdd_qdrii_io	AM12		AM2	gnd
vref_ddrii	V21		AM3	vdd_qdrii_io
vref_ddrii	AA23		AM4	qdrii_d5
vref_ddrii	AB25		AM5	qdrii_q4
vref_ddrii	AH21		AM6	qdrii_q1
vref_ddrii	AH23		AM7	qdrii_d7
vref_ddrii	AH25		AM8	qdrii_d11
vref_ddrii	AH27		AM9	qdrii_q13
vref_dimm	E6		AM10	gnd
vref_dimm	E8		AM11	qdrii_d16
vref_dimm	E10		AM12	vdd_qdrii_io
vref_dimm	E12		AM13	qdrii_sync_clk
vref_dimm	E21		AM14	qdrii_wpsn1
vref_dimm	E23		AM15	ddrii_ckfb_p
vref_dimm	E25		AM16	ddrii_ck_n0
vref_dimm	E27		AM17	pll6_fb_n
vref_dimm	F27		AM18	pll6_out3_n
vref_dimm	L25		AM19	clk4_p
vref_dimm	R21		AM20	ddrii_a_r14
vref_qdrii	AA10		AM21	1.8v_ddrii
vref_qdrii	AB8		AM22	ddrii_dm0
vref_qdrii	AG6		AM23	gnd
vref_qdrii	AH6		AM24	ddrii_dq4
vref_qdrii	AH8		AM25	ddrii_dq9
vref_qdrii	AH10		AM26	ddrii_dq8
vref_qdrii	AH12		AM27	ddrii_dq18
vrefio_loopin	B29		AM28	ddrii_dq17
vrefio_loopout	A29		AM29	ddrii_dq24
vrefio_smain	C30		AM30	1.8v_ddrii
vrefio_smaout	B30		AM31	gnd