The Programmable Solutions Company®

Stratix Memory Board II

Layout Guidelines
Rev 1.0

High-Speed End Applications
02/11/2004

REVISION HISTORY

DATE	REV	Comments
12/17/2003	0.1	Created
01/12/2004	0.2	Added form factor, stackup, power, clocks, DDR-II Devices and DDR-II DIMM critical traces rules
01/13/2004	0.3	Added Component-Side Placement Diagram
01/19/2004	0.4	Added QDR-II critical traces rules, added addressing traces rules for QDR-II Devices
01/25/2004	0.5	Updated DDR-II critical traces rules, added clock-to-address/control ratio to all memory critical traces rules, added silkscreen and logo information, added edge-component placement rules
01/27/2004	0.6	Added <mem_type>_SYNC_CLK to clock list for QDRII, DDRII, and DIMM, Updated Y-routing diagrams for QDRII and DDRII, Relaxed QDRII Address line matching spec.
02/11/2004	1.0	Added further clock definitions and rules, added SYNC clock routing rules and FB_CLK routing rules. Added dual switching power supply placement and layout guide. Changed QDR-II Clocks to single-ended from Diff Pairs.

TABLE OF CONTENTS

1. Form Factor

1.1. Overall Form Factor

SMB2 should be approximately 7” x 8”

1.2. Keepouts

Board-Edge shall be component-free for 0.125”
Edge-Components are an exception to this and are covered in the edge components section.

1.3. Tooling and Mounting Holes

Four 0.125” plated mounting holes shall be placed in the four corners of the board (0.250” pad)
One 0.125” plated mounting hole shall be placed between the DIMM and Stratix (0.250” pad)

1.4. Breakaways

None are currently planned.

2. Construction

PCB shall use high-temp FR4
Controlled Impedance
- – All signal planes to be 50-ohms single ended impedance +/- 10%
- – All signal planes to be 100-ohms differential impedance +/- 10%

12-layer, 92-mil finished PCB thickness

2.1. Geometries

2.1.1. Trace Geometries

5 mil trace (min)
5 mil space (min)

2.1.2. Via Geometries

10 mil drill (min, typ)
TEST VIA to have 35-mil pad on bottom-side
Special STAR_VIA components are special test VIAs actually placed in the schematic
-These vias are used to break-out multiple loaded address/control signals from a datapath signal for use in special length-matching requirements. See critical routing section for more details.

2.2. Stackup

2.2.1. Overview

8 Routing / 8 Power

1	**Signal**
2	**GND**
3	**Signal**
4	**Signal**
5	**1.5V_STRATIX**
6	**Signal**
7	**Signal**
8	**3.3V**
9	**Signal**
10	**Signal**
11	**Split Power (3 planes)**
12	**Signal**

2.2.2. Signal Planes

2.2.3. Power Planes

The following power signals must be routed as planes:

1) GND
2) 3.3V
3) 1.5V_STRATIX

The following power signals should be routed in a single split plane with 20-mil gaps of separation:

4) 1.8V_DIMM
5) 1.8V_DDRII
6) VDD_QDRII_IO

The approximate split is shown in Figure 2-1 below. See the Placement Diagram for more details on top-side components.

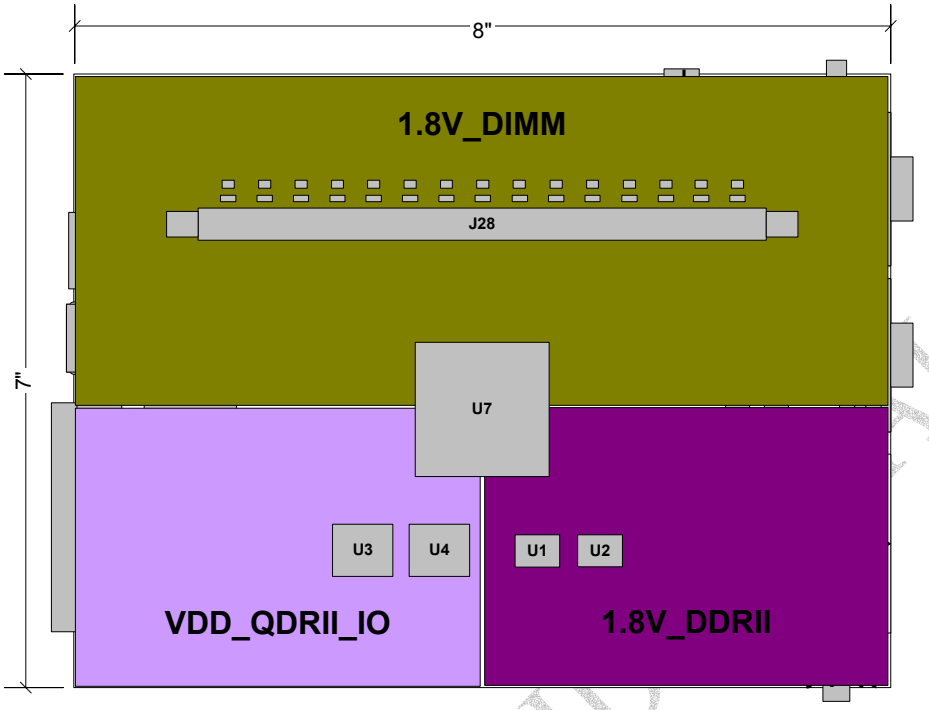


Figure 2-1 Split Plane Architecture

The following power signals should be routed as 750-mil power traces on signal layers:

7) 1.8V

The following power signals should be routed as islands or 250-mil power traces on signal layers:

8) VDD_QDRII_INT
9) 0.9V_DIMM
10) 0.9V_DDRII
11) VTT_QDRII
12) DC_INPUT

The following power signals should be routed as islands or 100-mil power traces on signal layers:

13) VCCA_PLL1
14) VCCA_PLL2
15) 3.3V_OSCA
16) 3.3V_OSCB
17) 3.3V_CLKA
18) 3.3V_CLKB
19) 1.8V_CLKB
20) AGND

Aggregate trace width is the main consideration for the 250-mil traces. Use top-bottom layers to double up two 125-mil traces with some via stitching where needed.

VCCA_PLLx power traces can be 50-mils upon entering the BGA via grid. The traces that snake around the outside of the Stratix BGA should try to keep 100-mil thickness.

2.3. In-Circuit Test Requirements

1. 100% breakout to a minimum of 1 test via per net
    - Through-hole component pin counts as a test via
    - Exceptions to this are unused BGA pins (no via required)
    - Further exceptions to be approved by the responsible design engineer
2. Test VIA defined in via geometries section.

2.4. Fiducials

1. Two fiducials to be placed on opposite corners of PCB, top AND bottom side.
2. All fine-pitch components to have at least one fiducial per instance (see 3.2).

3. Component Placement

3.1. General Placement Rules

3.1.1. Surface-Mount

BGA to Surface-mount must have minimum 150-mil clearance.

3.1.2. Through-Hole

Through-hole to Surface-mount on bottom side clearance must be greater than 200-mils.

3.2. Fine Pitch Components

These components should have local Fiducials and silkscreen pin markings every 10 pins with a pin number label on every corner for regular QFP/TSOP pinned-packages and labels on every row and column for BGA packages.

No.	Component Name	Ref Des
1	EP1S40F1020	U7
2	EPM7256AE	U11
3	MT47H16M16	U1, U2
4	CY7C1313V18	U3, U4
5	ICS85214	U10
6	LAN91C111	U12
7	AM29LV128	U14
8	LTC2901	U21
9	LTC2418	U22

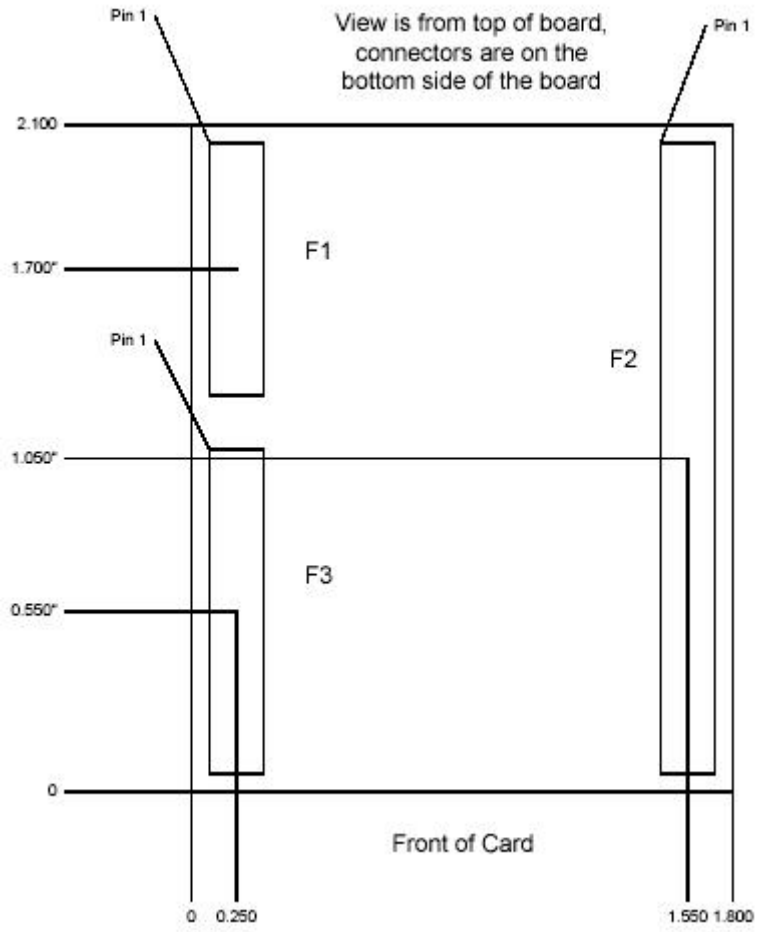
3.3. Special Components

3.4. Connectors

3.4.1. Altera Daughter Card "PROTO1" (J16, J17, J18)

The 3.3V Altera Daughter Card interconnect is made up of three 100-mil headers. These are arranged in two columns. The two columns are made up of one combo 2x7 + 2x10 and the other is made up of a single 2x20.

These are to be placed according to the *placement drawing*. Relative placement is according to the drawing below. The “front of card” as shown is to align with the PCB edge.



3.4.2. Banana Jacks (J1-J8, J30-J31)

The banana jacks shall be placed no closer than 0.500” center-to-center.

3.4.3. RS-232 (J14, J15)

The RS-232 connectors should be placed with a slight overhang to the PCB edge. The faceplate of the connectors should be either flush to the PCB edge of hand over up to 1/8” from the PCB edge.

3.4.4. RJ-45 (J13)

The RJ-45 connector should be placed on the PCB edge with a 1/8” overhang.

3.4.5. Byte Blaster Header (J10)

The Byte-Blaster connector should placed on the PCB edge with a 1/8” overhang.

3.4.6. Configuration Expansion Header (J27)

The Configuration Expansion Header should placed on the PCB edge with a 0.230” overhang.

3.4.7. JTAG Expansion Connectors (J12, J50)

The JTAG Expansion Connectors should be placed on the PCB edge with an approximate 1/8” overhang. They should be able to mate with each other if two Stratix Memory Boards were connected edge-to-edge.

3.4.8. DC Input Connector (J22)

The DC Input Connector should be placed on the PCB edge with a 1/8” overhang.

3.5. Test Points

The following test points are through-hole 25-mil square-pin posts. They should have a silkscreen outline around the base plastic. The geometry for these should be TP_060SQ040.

```
TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13
```

The following test points are special vias that are exposed on the top-side and bottom-side with a 30-mil pad:

STAR_VIA

3.6. Height Restrictions

Anything placed within the outline of the Altera Daughter Card (see 3.4.1) must be no taller than 1/4” tall due to the daughter cards that plug into this set of connectors. The overall height of the adjoining parallel PCB that would plug into this interface is ½” (surface-to-surface) but we must allow for daughter card components on the bottom-side of up to 3/16” and an air gap of 1/16”. Placement height within the interface outline must limited to 3/16”.

3.7. Placement Drawings

3.7.1. Top Side

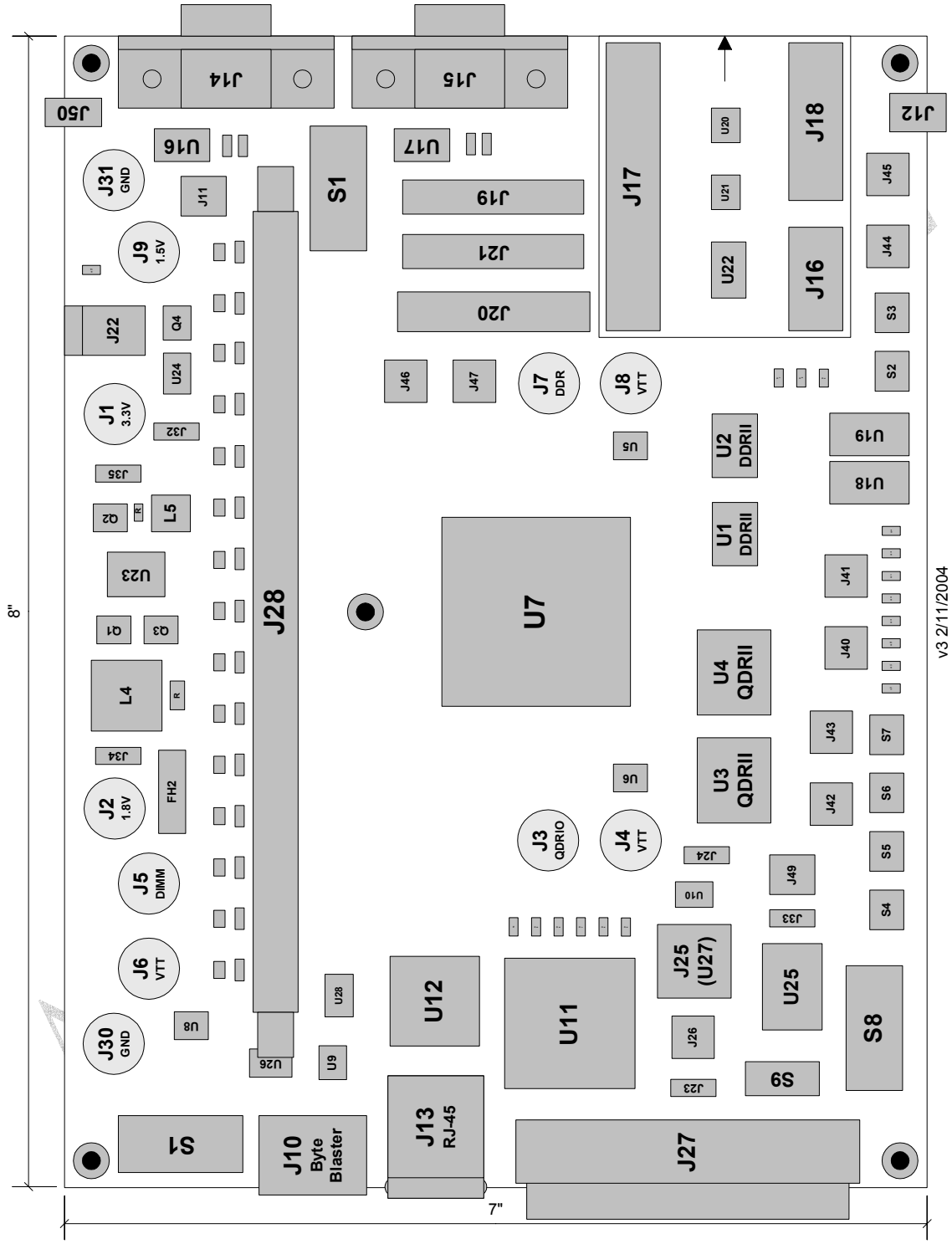


Figure 3-1

3.7.2. Bottom Side

No bottom-side drawing will be supplied. Mostly passives will be placed on the bottom such as decoupling caps and resistors. The only potential active components for the bottom are the Flash (U14) and one of the two SRAM components (either U13 or U15) in a top-bottom mount. This will depend on actual placement with real part sizes and Keepouts. Other bottom-side components must be approved by the responsible engineer.

3.7.3. Switching Power Supply

Figure 3-2 shows an approximate placement for major components within the dual-output switching power supply used to create both 1.8V and 3.3V controlled by U23.

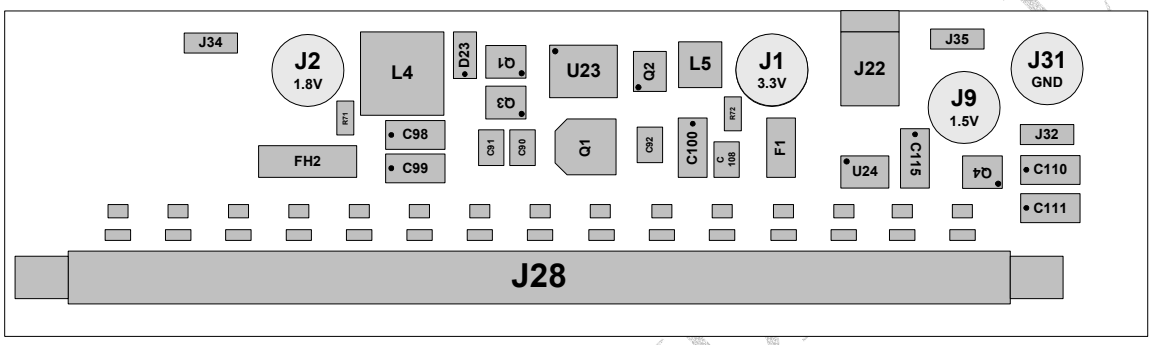


Figure 3-2

Figure 3-3 shows an approximate placement for top-layer copper pour regions between these components. For ties between these poured islands and a plane there must be multiple vias used (at least 6 if not 8 or 10) for high-current and low resistance and inductance.

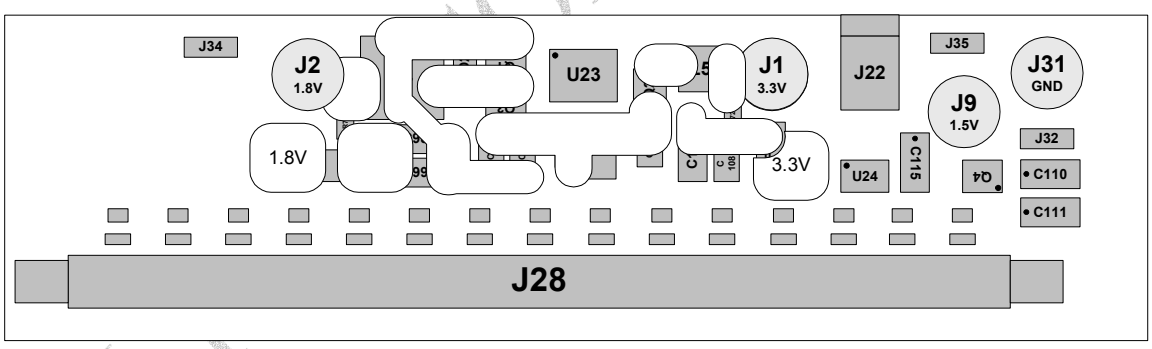


Figure 3-3

4. Routing Rules

4.1. General

1. Use 45 degree angles (no 90 degree corners)
2. No T-junctions greater than 250 mils
3. No T-junctions for critical nets or clocks (see critical traces section) unless otherwise specified.

4.2. Power Traces

The following power signals should be routed as islands or 250-mil power traces:

1) 0.9V_DIMM
2) 0.9V_DDRII
3) VTT_QDRII
4) DC_INPUT

The following power signals should be routed as islands or 100-mil power traces:

5) VCCA_PLL1
6) VCCA_PLL2
7) 3.3V_OSCA
8) 3.3V_OSCB
9) 3.3V_CLKA
10) 3.3V_CLKB
11) 1.8V_CLKB

See the power section for other potential notes on power traces.

4.3. Clocks

The following signals are designated as clocks.

-They are to be routed on inner layers with outer-layer run lengths being held to under 500 mils.
-These signals should maintain a 10-mil spacing from other nets.
-Differential clocks should maintain a length-matching between P and N signals of +/- 15 mils.
-Differential clocks with SMAs should route as a Diff Pair and break-out to SMAs right at the connectors.

Some termination resistor placement is mentioned below as well on a per-clock basis.

4.3.1. Oscillators

1)	CLKA_OSC	33.333 MHz	Oscillator to be close to destination pin
2)	CLKB_OSC	100.000 MHz	Oscillator to be close to destination pin
3)	CLK_25MHz	25.000MHz	Oscillator to be close to destination pin

4.3.2. SMA

4)	CLKB_SMA	350 MHz MAX	R34 close to U10 (buffer)
5)	CLK4_P	350 MHz MAX	Diff Pair (P/N) input to U7
	CLK4_N	350 MHz MAX	R102, R103 close to U7
6)	PLL6_FB_P	267 MHz MAX	Diff Pair (P/N) input to U7
	PLL6_FB_N	267 MHz MAX	R29, R101 close to U7
7)	PLL6_OUT3_P	267 MHz MAX	Diff Pair (P/N) output to SMAs
	PLL6_OUT3_N	267 MHz MAX	

4.3.3. Clock Buffers

8)	CLKA_TP	33.333 MHz	TP5,TP6 close to U9, buffer test point
9)	CLKA_SCRUZ	33.333 MHz	R58,C79 close to J18
10)	CLKA_CPLD	33.333 MHz	R14 close to U9
11)	CLKA_PLL10	33.333 MHz	R15 close to U9
12)	CLKB_TP_P	100.000 MHz	Diff Pair (P/N) buffer test points
	CLKB_TP_N	100.000 MHz	TP8,TP9,TP10 close to U10
13)	CLKB_PLL6_P	100.000 MHz	Diff Pair (P/N) Stratix inputs
	CLKB_PLL6_N	100.000 MHz	R22,R23 close to U7
14)	CLKB_PLL12_P	100.000 MHz	Diff Pair (P/N)
	CLKB_PLL12_N	100.000 MHz	R26,R27 close to U7
15)	CLKB_PLL11_P	100.000 MHz	Diff Pair (P/N)
	CLKB_PLL11_N	100.000 MHz	R24,R25 close to U7
16)	CLKB_PLL5_P	100.000 MHz	Diff Pair (P/N)
	CLKB_PLL5_N	100.000 MHz	R32,R33 close to U7

4.3.4. Memory Clocks

17)	DIMM_CK_P0	267 MHz	Diff Pair (P/N)
	DIMM_CK_N0	267 MHz	
18)	DIMM_CK_P1	267 MHz	Diff Pair (P/N)
	DIMM_CK_N1	267 MHz	
19)	DIMM_CK_P2	267 MHz	Diff Pair (P/N)
	DIMM_CK_N2	267 MHz	
20)	DIMM_CKFB_P	267 MHz	Diff Pair (P/N), Stratix DLL Ref Clock
	DIMM_CKFB_N	267 MHz	R131,R132 close to U7
21)	DIMM_SYNC_CLK	267 MHz	R134 close to U7, Core Re-Sync Clock
22)	DDRII_CK_P0	267 MHz	Diff Pair (P/N)
23)	DDRII_CK_N0	267 MHz	
24)	DDRII_CK_P1	267 MHz	Diff Pair (P/N)
25)	DDRII_CK_N1	267 MHz	
26)	DDRII_CKFB_P	267 MHz	Diff Pair (P/N), Stratix DLL Ref Clock
	DDRII_CKFB_N	267 MHz	R129,R130 close to U7
27)	DDRII_SYNC_CLK	267 MHz	R135 close to U7, Core Re-Sync Clock
28)	QDRII_K_P0	250 MHz	Single-ended
29)	QDRII_K_N0	250 MHz	Single-ended
30)	QDRII_K_P1	250 MHz	Single-ended
31)	QDRII_K_N1	250 MHz	Single-ended
32)	QDRII_CQ_P0	250 MHz	Single-ended
33)	QDRII_CQ_P1	250 MHz	Single-ended
34)	QDRII_CQ_N1	250 MHz	Single-ended
35)	QDRII_SYNC_CLK	250 MHz	R133 close to U7, Core Re-Sync Clock

4.4. Critical Traces

4.4.1. DDR-II Devices

The following signals run between the DDR-II Devices (U1, U2) and the Stratix FPGA (U7). Signals with similar names such as DDRII_A and DDRII_A_R are the same trace separated by a series resistor. In these cases the overall net length is actually the sum of the two nets. The address/command group signals are bussed to both devices. The remaining signals are point-to-point with the exception of some signals having series resistors.

Address/Command Group

Address =	DDRII_A(15:0)	DDRII_A_R(15:0)
Bank Addr =	DDRII_BA(2:0)	DDRII_BA_R(2:0)
Command =	DDRII_RASn	DDRII_RASn_R
	DDRII_CASn	DDRII_CASn_R
	DDRII_WEn	DDRII_WEn_R

Control Group

Chip Selects =	DDRII_CSn(1:0)	DDRII_CSn_R(1:0)
Clock Enable =	DDRII_CKE(1:0)	DDRII_CKE_R(1:0)
On-Die Term Enable =	DDRII_ODT(1:0)	DDRII_ODT_R(1:0)

Data Group

Data =	DDRII_DQ(31:0)
Data Mask =	DDRII_DM(3:0)
Data Strobe =	DDRII_DQS(3:0)

Clock Group

Diff. Clocks =	DDRII_CK_P0	DDRII_CK_N0	(diff pair)
	DDRII_CK_P1	DDRII_CK_N1	(diff pair)
	DDRII_CKFB_P	DDRII_CKFB_N	(diff pair)

From the above signals a set of groups are made. Each group represents a byte of data and an associated clock and mask control. These will become match groups.

Byte Lane Groups

Lane 0 =	DDRII_DQ(7:0)	DDRII_DM(0)	DDRII_DQS(0)
Lane 1 =	DDRII_DQ(15:8)	DDRII_DM(1)	DDRII_DQS(1)
Lane 2 =	DDRII_DQ(23:16)	DDRII_DM(2)	DDRII_DQS(2)
Lane 3 =	DDRII_DQ(31:24)	DDRII_DM(3)	DDRII_DQS(3)

Feedback Clocks

Core-to-DQS Re-sync Clock =	DDRII_SYNC_CLK		(single-ended)
DLL Reference Clock =	DDRII_CKFB_P	DDRII_CKFB_N	(diff. pair)

Routing Rules

1. All signals within a given “Byte Lane Group” should be matched length from the pin on the Stratix (U7) to the pin on DDR Device (U1 or U2). Maximum deviation is +/- 0.050 inches.
2. Keep the distance from the pin on the DDR Device (U1 or U2) to the termination resistor pack (to 0.9V_DDRII) to less than 750 mils.
3. Keep the distance from the pin on Stratix (U7) to the termination resistor pack (to 0.9V_DDRII) to less than 1250 mils.

4. All signals must match lengths between pins (as in (1) above) within +/- 0.250 inches (address, control, data, all byte groups, etc…) Only nets within a byte lane group must be matched tighter as in rule 1. Feedback Clocks are an exception – see rule 10.
5. All signals (other than Address/Command Group) are to maintain a spacing that is based on its parallelism with other nets. This is as follows:
    a. 5 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    b. 10 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    c. 15 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
6. All signals are to maintain 20 mil separation from other, non-related nets
7. All signals must have a total length of less than 6 inches.
8. All signals listed in the Address/Command Group should maintain a spacing that is based on its parallelism with other nets but more stringent than in rule 5(a/b/c) above. This is as follows:
    a. 10 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    b. 15 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    c. 20 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
9. All signals in the Clock Group must be routed differentially (5 mil trace, 10-15 mil space on centers) and be equal to or up to 100-mils longer than signals in the Address/Command Group.
10. Feedback clock DDRII_SYNC_CLK should be within 100-mils of the average length of the Byte Lane Groups. Feedback clock pair DDRII_CKFB_P and DDRII_CKFB_N (diff pair) have no length-matching restrictions though they should be kept as short as possible. Because these signals have termination resistors they will have to exit the BGA grid and come back in to accommodate the resistor placement. All signals in the Feedback Clocks group drive out of the Stratix (U7) and then back into the Stratix (U7).
11. All signals that are double-loaded (one connection to Stratix and two connections to DDR-II) such as address, command and control should be routed in a Y-shaped connection with the memory-side termination resistor. The general idea is shown in Figure 4-1

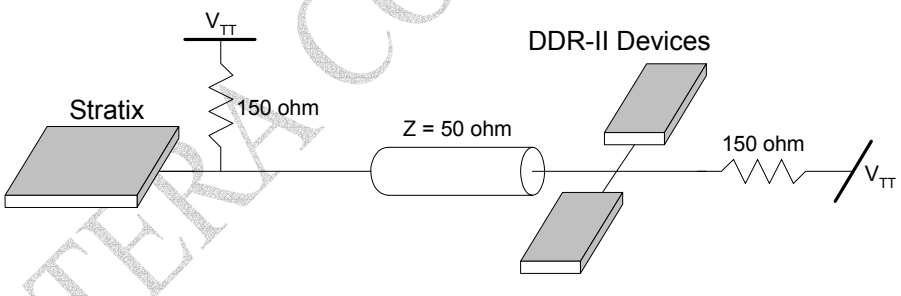


Figure 4-1

12. Within a given Y-shaped connection as described in the previous rule there must be some symmetry and matching within stubs in these traces. These stubs are shown in Figure 4-2 below. In this case the leg L1 should be a majority of the trace. Legs L2 and L3 should be matched within +/- 0.030 inches. The length rule for matching within a group (read group or write group) is NOT the total length of this trace. It is the length of EITHER L1 and L2 or L1 and L3. The connection in the center where all four stubs come together should be routed as shown below (not a 90-degree connection but a 45 degree connection). Leg L4 should be less than 0.750 inches.

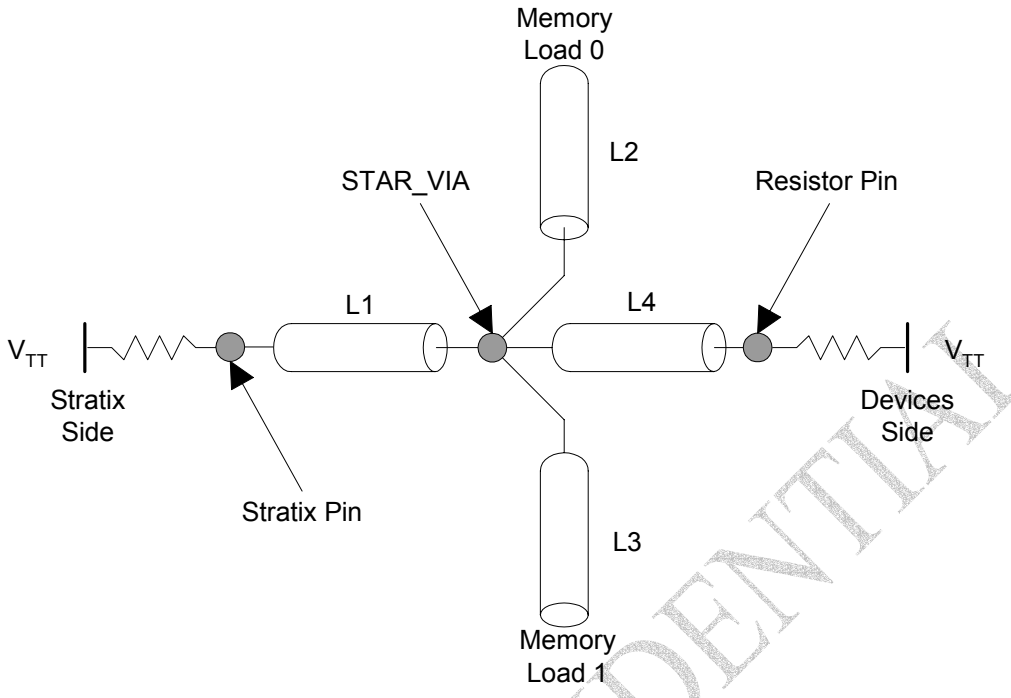


Figure 4-2

4.4.2. QDR-II Devices

The following signals run between the QDR-II Devices (U3, U4) and the Stratix FPGA (U7). The trace groups are similar to the DDR-II Devices but the data group signals are double-loaded and here the control signals have a copy for each of the two devices.

Address Group

Address =	QDRII_A(18:0)

Control Group

Write Port Select =	QDRII_WPS(1:0)
Read Port Select =	QDRII_RPS(1:0)
Byte Write Select =	QDRII_BWS(1:0)

Data Group

Write Data =	QDRII_D(17:0)
Read Data =	QDRII_Q(17:0)

Clock Group

Write Clocks =	QDRII_K_P(1:0)	2 rising edge data clocks
	QDRII_K_N(1:0)	2 falling edge data clock
Read Clocks (PLL) =	QDRII_CQ_P(1)	1 rising edge data clock
	QDRII_CQ_N(1)	1 falling edge data clock
Read Clocks (DQS) =	QDRII_CQ_P(0)	1 rising edge data clock (falling edge ignored)

From the above signals a set of groups are made. Each group represents a byte of data and an associated clock and mask control. These will become groups of signals that are length-matched as described below.

QDR-II Match Groups

Write Group =	QDRII_D(17:0)	QDRII_K_P(1:0)	QDRII_K_N(1:0)
Read Group =	QDRII_Q(17:0)	QDRII_CQ_P(1:0)	QDRII_CQ_N(1:0)

Feedback Clocks

Core-to-DQS Re-sync Clock =	QDRII_SYNC_CLK		(single-ended)
DLL Reference Clock =	DDRII_CKFB_P	DDRII_CKFB_N	(ignore in QDR)

Routing Rules

1. All signals within a given "QDR-II Match Group" should be matched length from the pin on the Stratix (U7) to the pin on QDR Device (U3 or U4). Maximum deviation is +/- 0.050 inches. See rule 9 and rule 10 below for clarification on double-loaded signals.
2. Keep the distance from the pin on the QDR Device (U3 or U4) to the termination resistor pack (to VTT_QDRII) to less than 750 mils.
3. Keep the distance from the pin on Stratix (U7) to the termination resistor pack (to VTT_QDRII) to less than 1250 mils.
4. **ALL** signals must match lengths between pins (as in (1) above) within +/- 0.200 inches (address, control, data, clocks, etc…) Only nets within a match group must be matched tighter as in rule 1. Feedback clocks are exceptions to this rule – see rule 9.
5. All signals are to maintain a spacing that is based on its parallelism with other nets. This is as follows:
    a. 5 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    b. 10 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    c. 15 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
6. All signals are to maintain 20 mil separation from other, non-related nets
7. All signals must have a total length of less than 4 inches.
8. All signals in the Clock Group should be routed single-ended even though they may seem like differential clocks based on their naming conventions. As clock signals they must follow spacing rules as outlined in the CLOCKS section of this document.
9. Feedback clock QDRII_SYNC_CLK should be within 100-mils of the average length of the Byte Lane Groups. Feedback clock pair DDRII_CKFB_P and DDRII_CKFB_N are covered in DDRII secion. Because these signals have termination resistors they will have to exit the BGA grid and come back in to accommodate the resistor placement. All signals in the Feedback Clocks group drive out of the Stratix (U7) and then back into the Stratix (U7).
10. All signals that are double-loaded (one connection to Stratix and two connections to QDR-II) such as address and data should be routed in a Y-shaped or T-shaped connection with the memory-side termination resistor. The general idea is shown in Figure 4-3.

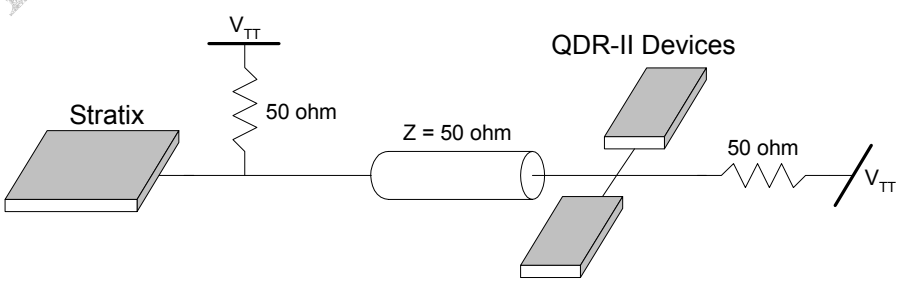


Figure 4-3

11. Within a given Y-shaped connection as described in the previous rule there must be some symmetry and matching within stubs in these traces. These stubs are shown in Figure 4-4 below. In this case the leg L1 should be a majority of the trace. Legs L2 and L3 should be matched within +/- 0.030 inches. The length rule for matching within a group (read group or write group) is NOT the total length of this trace. It is the length of EITHER L1 and L2 or L1 and L3. The connection in the center where all four stubs come together should be routed as shown below (not a 90-degree connection but a 45 degree connection). Leg L4 should be less than 0.750 inches.

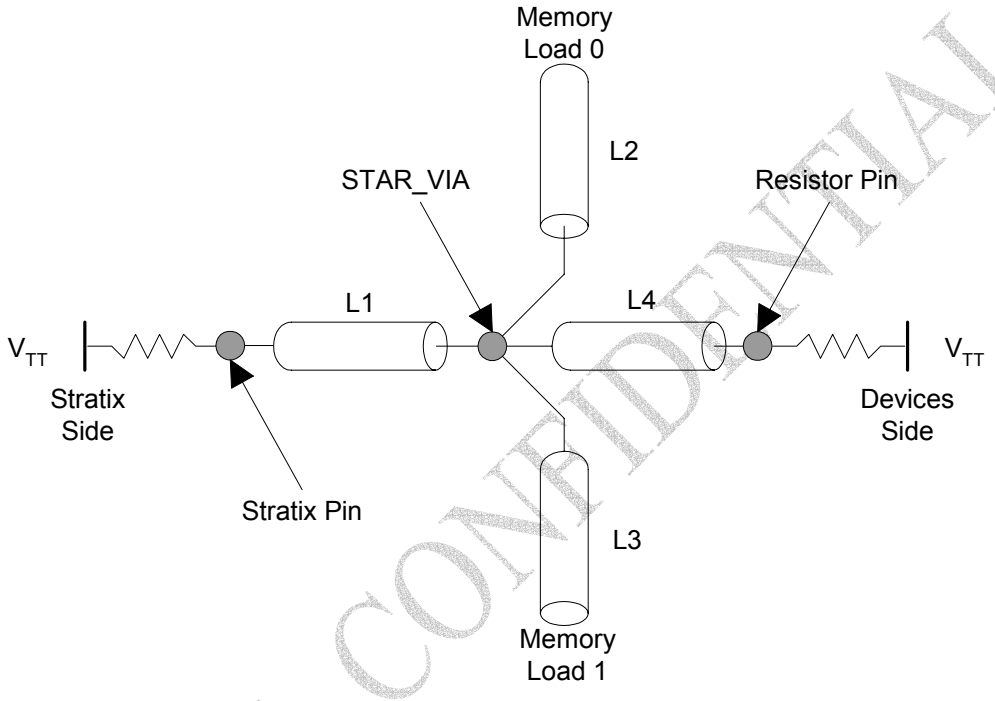


Figure 4-4

4.4.3. DDR-II DIMM

The following signals run between the DDR-II DIMM (J28) and the Stratix FPGA (U7). Signals with similar names such as DIMM_A and DIMM_A_R are the same trace separated by a series resistor. In these cases the overall net length is actually the sum of the two nets.

Address/Command Group

Address =	DIMM_A(15:0)	DIMM_A_R(15:0)
Bank Addr =	DIMM_BA(2:0)	DIMM_BA_R(2:0)
Command =	DIMM_RASn	DIMM_RASn_R
	DIMM_CASn	DIMM_CASn_R
	DIMM_WEn	DIMM_WEn_R

Control Group

Chip Selects =	DIMM_CSn(1:0)	DIMM_CSn_R(1:0)
Clock Enable =	DIMM_CKE(1:0)	DIMM_CKE_R(1:0)
On-Die Term Enable =	DIMM_ODT(1:0)	DIMM_ODT_R(1:0)

Data Group

Data =	DIMM_DQ(63:0)
Data Mask =	DIMM_DM(8:0)
Data Strobe =	DIMM_DQS(8:0)
Check Bits =	DIMM_CB(7:0)

Clock Group

Diff. Clocks =	DIMM_CK_P0	DIMM_CK_N0	(diff pair)
	DIMM_CK_P1	DIMM_CK_N1	(diff pair)
	DIMM_CK_P2	DIMM_CK_N2	(diff pair)

Byte Lane Groups

Lane 0 =	DIMM_DQ(7:0)	DIMM_DM(0)	DIMM_DQS(0)
Lane 1 =	DIMM_DQ(15:8)	DIMM_DM(1)	DIMM_DQS(1)
Lane 2 =	DIMM_DQ(23:16)	DIMM_DM(2)	DIMM_DQS(2)
Lane 3 =	DIMM_DQ(31:24)	DIMM_DM(3)	DIMM_DQS(3)
Lane 4 =	DIMM_DQ(39:32)	DIMM_DM(4)	DIMM_DQS(4)
Lane 5 =	DIMM_DQ(47:40)	DIMM_DM(5)	DIMM_DQS(5)
Lane 6 =	DIMM_DQ(55:48)	DIMM_DM(6)	DIMM_DQS(6)
Lane 7 =	DIMM_DQ(63:56)	DIMM_DM(7)	DIMM_DQS(7)
Lane 8 =	DIMM_CB(7:0)	DIMM_DM(8)	DIMM_DQS(8)

Feedback Clocks

Core-to-DQS Re-sync Clock =	DIMM_SYNC_CLK		(single-ended)
DLL Reference Clock =	DIMM_CKFB_P	DIMM_CKFB_N	(diff pair)

Routing Rules

1. All signals within a given "Byte Lane Group" should be matched length from the pin on the Stratix (U7) to the pin on DDR DIMM (J28). Maximum deviation is +/- 0.050 inches.
2. Keep the distance from the pin on the DDR DIMM (J28) to the termination resistor pack (pull-up to 0.9V_DIMM) to less than 750 mils.
3. Keep the distance from the pin on Stratix (U7) to the termination resistor pack (pull-up to 0.9V_DIMM or Series Resistor) to less than 1250 mils.
4. All signals must match lengths between pins (as in (1) above) within +/- 0.250 inches (address, control, data, all byte groups, etc…). Only nets within a byte lane group must be matched tighter as in rule 1. Feedback clocks are different – see rule 10.
5. All signals (other than Address/Command Group) are to maintain a spacing that is based on its parallelism with other nets. This is as follows:
    d. 5 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    e. 10 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    f. 15 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
6. All signals are to maintain 20 mil separation from other, non-related nets
7. All signals must have a total length of less than 6 inches.
8. All signals listed in the Address/Command Group should maintain a spacing that is based on its parallelism with other nets but more stringent than in rule 5(a/b/c) above. This is as follows:
    g. 10 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    h. 15 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    i. 20 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
9. All signals in the Clock Group must be routed differentially (5 mil trace, 10-15 mil space on centers) and be equal to or up to 100-mils longer than signals in the Address/Command Group.
10. Feedback clock DIMM_SYNC_CLK should be within 100-mils of the average length of the Byte Lane Groups. Feedback clock pair DIMM_CKFB_P and DIMM_CKFB_N (diff pair) have no length-matching restrictions though they should be kept as short as possible. Because

these signals have termination resistors they will have to exit the BGA grid and come back in to accommodate the resistor placement. All signals in the Feedback Clocks group drive out of the Stratix (U7) and then back into the Stratix (U7).

5. Silkscreen

5.1. Reference Designators

1. All components to have reference designators placed so they are visible after assembly.
2. Where space is not available a reference designator must be placed as close as possible with a visible line pointing to the component being referenced.
3. Pin 1 should be de-marked with a silkscreen dot and a numeric “1” next to the actual pin.

5.2. Company Name and Logos

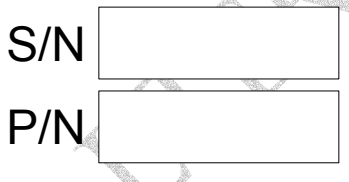
The Altera Logo is to be placed on the top-side and be at least 1.5” wide.

5.3. Board Name and Revision

1. The name “**Stratix Memory Board II**” is to be placed on the top-side and be at least 1.5” wide. If possible it should be placed directly beneath and centered to the Altera Logo. A revision should be labeled near the board name as “**Rev A**”.

5.4. Serial and Part Numbers

A 3/8” x 1 ¼” box shall be drawn for both a serial number and part number sticker and be placed on the bottom-side and labeled as shown below.



5.5. Copyright and Country of Origin

1. The board shall display “MADE IN THE USA” on the bottom side.
2. A copyright symbol should be placed next to “ALTERA” on the bottom-side as shown below.

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