The Programmable Solutions Company®

SMB1 Memory Termination Specification

Termination Specification
Rev 0.1

High-Speed End Applications
6/1/2004

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REVISION HISTORY

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1. Introduction

1.1. Overview

With increasing speeds of memory devices, good termination is important in maintaining memory performance. This document defines the termination techniques we are proposing to use for all the high-speed memories of SMB1, which are RLDRAM II CIO and SIO, DDR I devices, and DDR I modules.

1.2. Objectives

The primary purpose of this document is to detail how each memory type will be terminated. Some of the same memory types will have different termination schemes so that each type of termination can be tested to find the one that shows best performance. This document will take into account simulations performed on each termination scheme, as well. The goal of this document is to distribute our plan for memory termination to get an approval by various groups in Altera.

2. Termination and I/O Standards

2.1. Stub Series Terminated Logic (SSTL2) I/O Standard

On the SMB1, the DDR I memories use SSTL2 I/O standard. SSTL2 I/O termination scheme is defined in many ways in the JEDEC standard EIJ/JESD8-9. The figure below (Figure 2-1) shows one such implementation (SSTL2 class II).

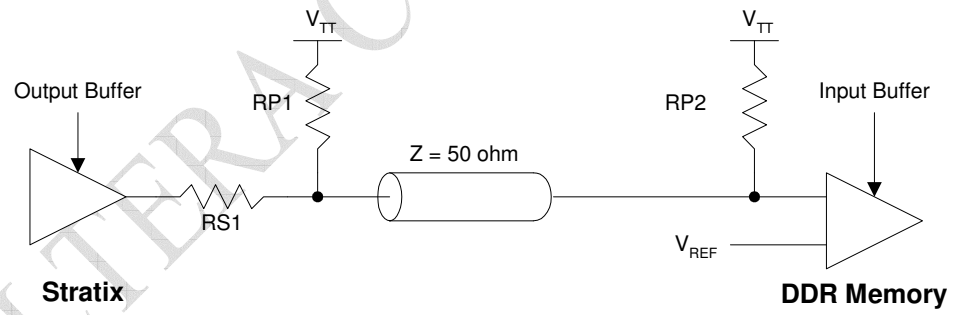
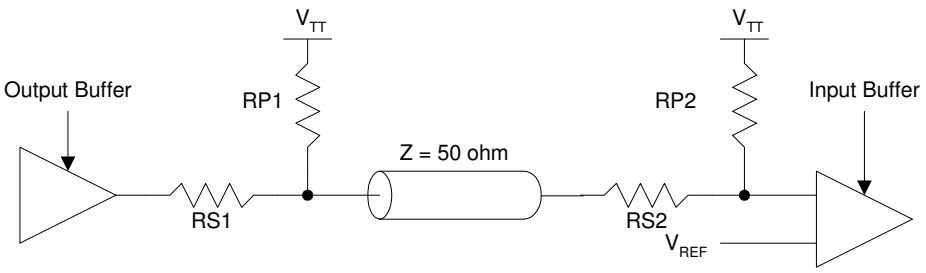


Figure 2-1: SSTL2 Class II Termination

Here, RS1 is 25 ohms, RP1 and RP2 are 50 ohms, VTT is 1.25V and VREF is 1.25V, the output buffer is Stratix, and the input buffer is DDR I.

For SSTL2 class I, RP1 s not used. In some cases, RS1 could be located closer to the input buffer. So, to satisfy all possible cases for SSTL2, you would require a circuit as shown in figure 2-2 below.



Note: Only RS1 or RS2 will be installed at one time.

Figure 2-2: SSTL2 Class II Complete Termination

In this circuit, only RS1 or RS2 will be used at the same time. Using this circuit for all DDR I devices would require too many components, would cause the signals to have too many discontinuities, and would cause problems for layout. The alternative would be to have each DDR I memory devices (SMB1 has four DDR I devices on the board) use different termination schemes. This way, only one device is affected at any one time. Also, because all termination schemes are available for testing, the best one can be determined.

Figure 2-3 shows all the circuit types necessary for SSTL2 termination.

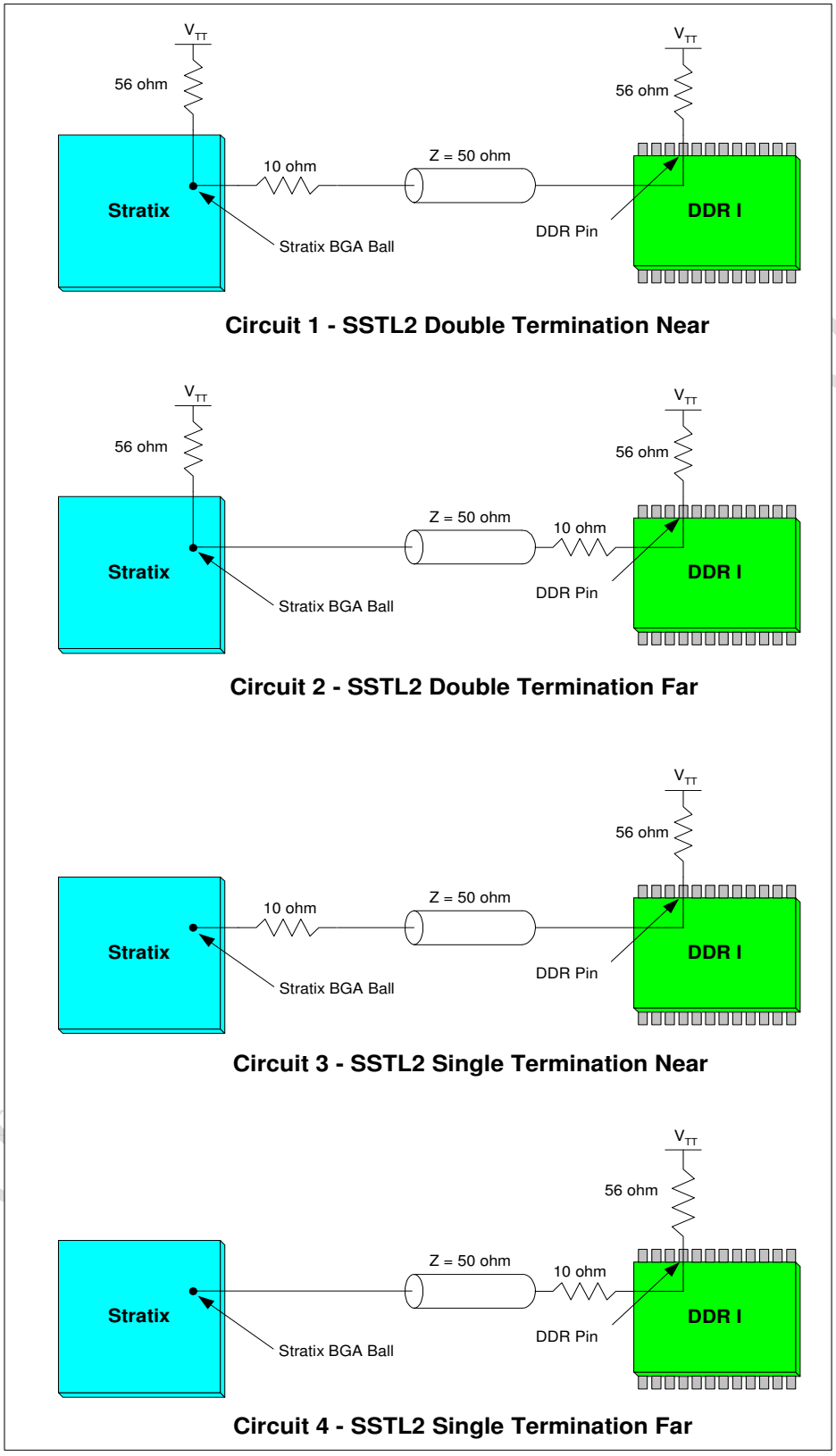


Figure 2-3: SSTL2 Termination Circuits

For best routing purposes, the best results occur when the pull-up resistors are placed as fly-by. That is, as in the case of circuit 1, the trace from the series resistor is routed to the Stratix BGA ball and then another trace routes from the BGA ball to the pull-up resistor. These traces fly by the BGA ball. The same applies to the DDR side, as well. Using this fly-by technique eliminates discontinuities associated by stubs, which degrade the signal quality. Although SSTL2 uses 25 and 50 ohm resistors for series and pull-ups respectively, we are using 10 and 56 ohm resistors because this is what Micron Technology suggested based on their simulations. We also used these values and termination scheme for the DDR I module on the Stratix GX Development Board which operates at 400 Mega Transfers per second. If other values are needed, they can easily be swapped for the ones currently on the board. The SSTL2 termination was altered by the suggestion by Micron because this scheme yielded the best results. They are addressing this to the JEDEC Standardization Council.

For the DDR I devices, we will be using circuits 1 through 4 based on the direction of the signals. Bidirectional signals refer to Data, Data Strobe (DQS), and Data Mask signals. Unidirectional signals refer to address and control signals. Although for DDR I devices, the address termination scheme may change since it is shared by all the DDR I devices (this would be based on simulations).

For DDR I modules, as in the case with the Stratix GX Development Board, we will be using circuits 3 and 4 for unidirectional and bidirectional signals.

2.2. High Speed Transceiver Logic (HSTL) I/O Standard

On the SMB1, there are two types of RLDRAM II devices; common I/O (CIO) and separate I/O (SIO) and they use HSTL I/O standard. HSTL I/O standard is defined in the JEDEC standard EIJ/JESD8-6. The figure below (Figure 2-4) shows one such implementation (HSTL2 Class II).

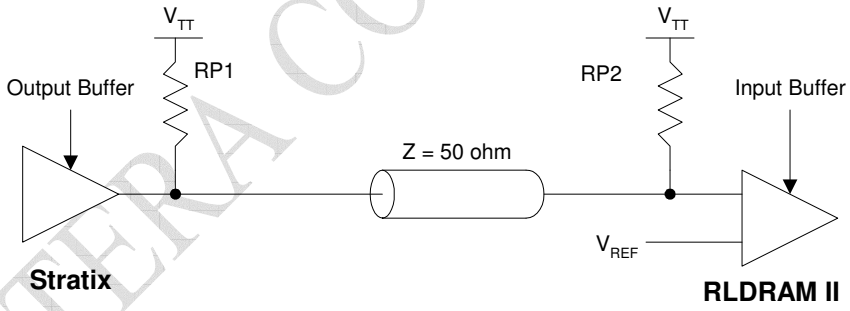
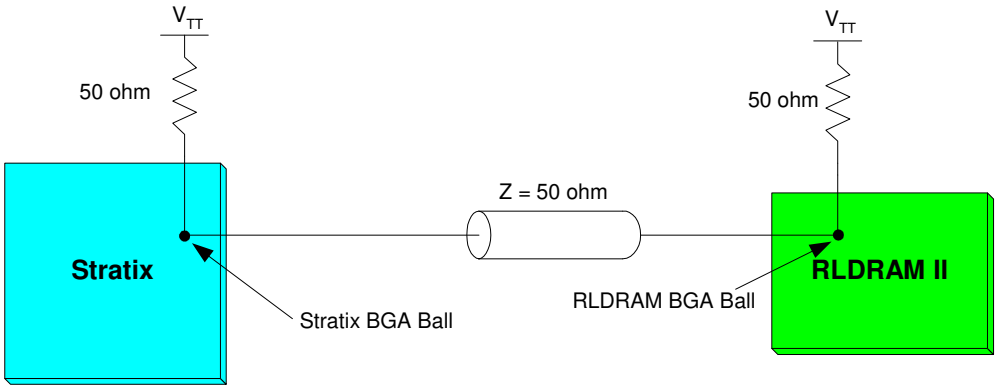
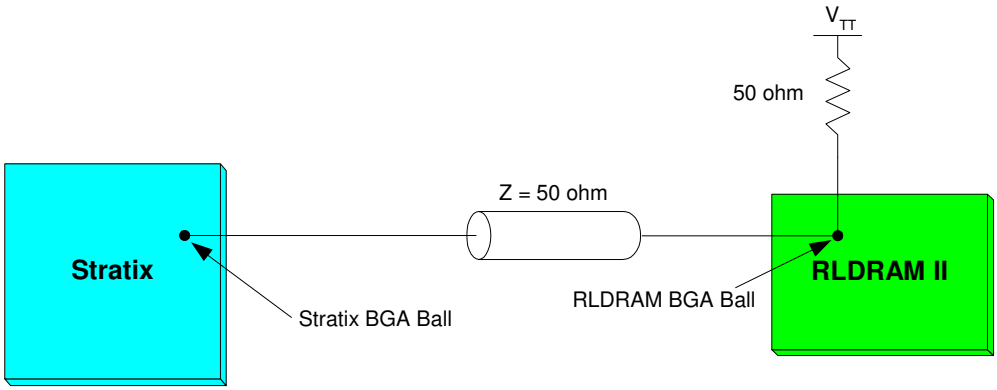


Figure 2-4: HSTL2 Class II Termination

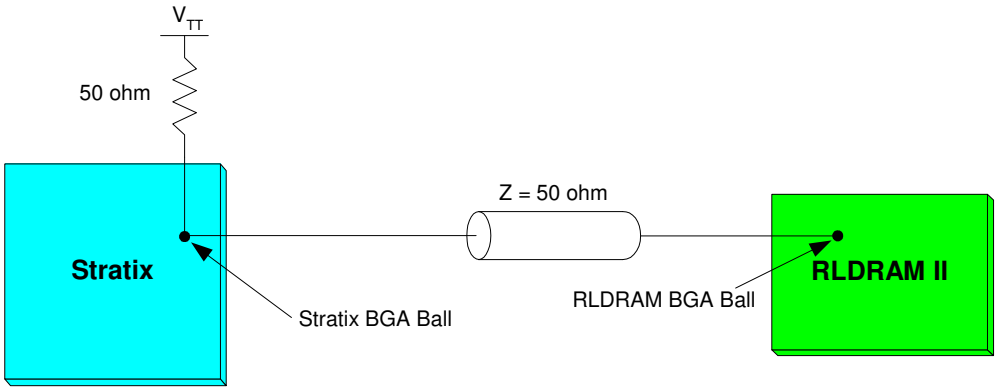
Here RP1 and RP2 are 50 ohm, VTT is 0.90 or 0.75 V, VREF is 0.90 or 0.75 V, the output buffer is Stratix, and the input buffer is RLDRAM II.
The following figure (Figure 2.5) shows the different types of termination required for HSTL termination.



Circuit 5 - HSTL2 Double Termination



Circuit 6 - HSTL2 Single Termination Far



Circuit 7 - HSTL2 Single Termination Near

Figure 2-5: HSTL2 Termination Circuits

For RLDRAM II CIO, circuits 5 and 6 will be used for bidirectional and unidirectional signals, respectively. For RLDRAM II SIO, circuits 6 and 7 will be used. Because RLDRAM II SIO

devices are unidirectional circuit 6 will be used for write data, address, and control signals and circuit 7 will be used for read data.

Table 2-1 summarizes how each memory will be terminated based on the direction of the signal.

Device	Signal Type	Circuit Type
DDR A	Bidirectional Unidirectional	Circuit 1 Circuit 3
DDR B	Bidirectional Unidirectional	Circuit 2 Circuit 3
DDR C	Bidirectional Unidirectional	Circuit 3 Circuit 3
DDR D	Bidirectional Unidirectional	Circuit 4 Circuit 3
DDR DIMM	Bidirectional Unidirectional	Circuit 4 Circuit 3
RLDRAM CIO	Bidirectional Unidirectional	Circuit 5 Circuit 6
RLDRAM SIO	Unidirectional Write Unidirectional Read	Circuit 6 Circuit 7

Table 2-1: SMB1 Termination Schemes

3. Conclusion

In conclusion, by adopting these schemes for memory termination, we can test for each type and determine which one will have the best performance. By having different termination types for each DDR I memory devices, we can test each type without affecting the overall performance of the DDR devices.