Stratix™ Memory Board 1

May 2004, Ver. 1.0 **Datasheet**

Introduction

The Stratix™ Memory Board 1 (SMB1) is a demonstration board designed to showcase high-speed memories (DDR-I and RLDRAM-II) with the Stratix™ FPGA using Intellectual Property (IP). It will also be the Applications Characterization platform and a Demonstration platform for Field Application Engineering for the Stratix™ FPGA device. Designers can use the SMB1 to prototype and develop high-speed applications for Stratix™ FPGA's interfaces with RLDRAM-II Combined Input/Output (CIO), RLDRAM-II Separate Input/Output (SIO), DDR-I x 16, DDR-I Module, Flash, or SRAM memories.

Features

The SMB1 is intended for testing, demonstrating and characterizing high-speed memory controller IP using Altera's Stratix ™FPGA. This section lists the elements included on the board.

Devices

The SMB1 contains one Stratix™ device. The bottom and side banks of the Stratix device interfaces to DDR-I which operates up to 200 MHz, and the top banks interface to RLDRAM-II CIO and SIO operating at either 300 MHz or up to 400 MHz. There is a Flash ROM with a MAX device to program the Stratix device.

One Altera Stratix™ FPGA Device (EP1S40F1020-C5)

- 80 transmit and 80 receive source synchronous channels
- 1,020-pin FineLine BGA package
- 41,250 LEs
- 3,423,744 RAM bits (417KB)
- 12 PLLs (8 Fast and 4 Enhanced)
- 10 transmit and 10 receive medium speed channels
- 112 DSP block 9-bit elements
- 781 user I/O
- SMA interfaces for external I/O

One Altera MAX™ CPLD Device (EPM7256AETC144)

Memory Devices

- One Micron Technology RLDRAM-II, SIO, 16M x 18 Memory Device (MT49H16M18CFM-2.5)
- Two Micron Technology RLDRAM-II, CIO, 16M x 18 Memory Devices (MT49H16M18FM-2.5)
- Four DDR-I SDRAM 4M x 16, Memory Devices (MT46V16M16TG-5B)
- One DDR-I SDRAM DIMM, 32M x 72 Memory Device (MT9VDDT3272AG-40B)
- One Flash 128Mb Memory Device (AM29LV128MH113REI)
- Two SRAM 256K x 16 Memory Devices (IDT71V416S10PH)

Configuration

Configuration of the board includes mulitple modes for programming the Stratix™ and MAX devices on the board.

- The Flash will be used to store configuration data or be used as non-volatile memory.
- Configuration interfaces include JTAG for configuration using the ByteBlaster™ II cable.
- Switches to select different configuration modes.
- 10/100 Ethernet connection for remote/local updates for configuration purposes through the RJ-45 connector.

Clocks

Clocks are generated using on-board crystal oscillators and clock drivers or external clocks can be provided through SMA connectors. Each board contains two VCO's and one crystal oscillator.

- External clocks via SMA
- Clocks via on-board oscillators (100 MHz, 33.3 MHz, and 25 MHz) and clock drivers
- Clocks via oscillator socket

Interfaces

The Stratix FPGA device interfaces to several different external memories at various data rates.

- DIMM socket using DDR-I SDRAM running at 200 MHz.
- Four DDR-I SDRAM devices running at 150 MHz.
- Two RLDRAM-II CIO device running at 200 MHz.
- One RLDRAM-II SIO devices running at 200 MHz.
- Two SRAM Memory devices
- One Flash Memory device
- 10/100 Ethernet media access control physical interface (MAC PHY) using an RJ-45 connector for the cable connection.

Digital Analysis/Instrumentation Connections

The SMB1 provides various interface options for test and debug. The Tektronix and Agilent logic connectors are not installed on the SMB1 but may be installed when needed.

- RS-232 Interface for debug and register access
- Tektronix and Agilent logic analyzer connectors

Power

Power will be brought in through a 16V Universal AC adapter power jack or individual banana jacks for the unregulated power sources.

- 16V Universal AC adapter
- Regulators
- Banana jacks for the unregulated power sources
- Socketed fuses switch between banana jacks and regulated power coming from on-board regulators

User I/O Formats

- Eight user LEDs, four power monitor LEDs, one power supply LED, and eight status LEDs.
- Two seven-segment displays

- Three octal DIP switches. Two for user logic functions, and one for configuration
- Six push buttons for user logic functions; three general purpose, system reset, user reset, safe configuration push buttons.

Expansion Interfaces

- One 80-pin right angle expansion header (J51) for connection to Stratix II configuration boards
- Three Proto Headers (J31, J32, J37) for use with the Santa Cruz board

General Description

The SMB1 is a demonstration board designed to showcase high-speed memories (DDR-I and RLDRAM-II) with the Stratix™ FPGA using Intellectual Property (IP). Designers can use the SMB1 to prototype and develop high-speed applications for Stratix™ FPGAs interfaces with RLDRAM-II SIO, RLDRAM-II CIO, DDR-I x 16, DDR-I Module, Flash, or SRAM memories. The board can demonstrate several IP cores, such as RLDRAM-II, 10/100 Ethernet MAC with intergrated PHY using an RJ-45 connector, Double Data Rate (DDR) SDRAM, RS-232, and Nios® microprocessors.

Components and Interfaces

Figure 1 shows a top view of the SMB1.

Figure 1. SMB1 Top View

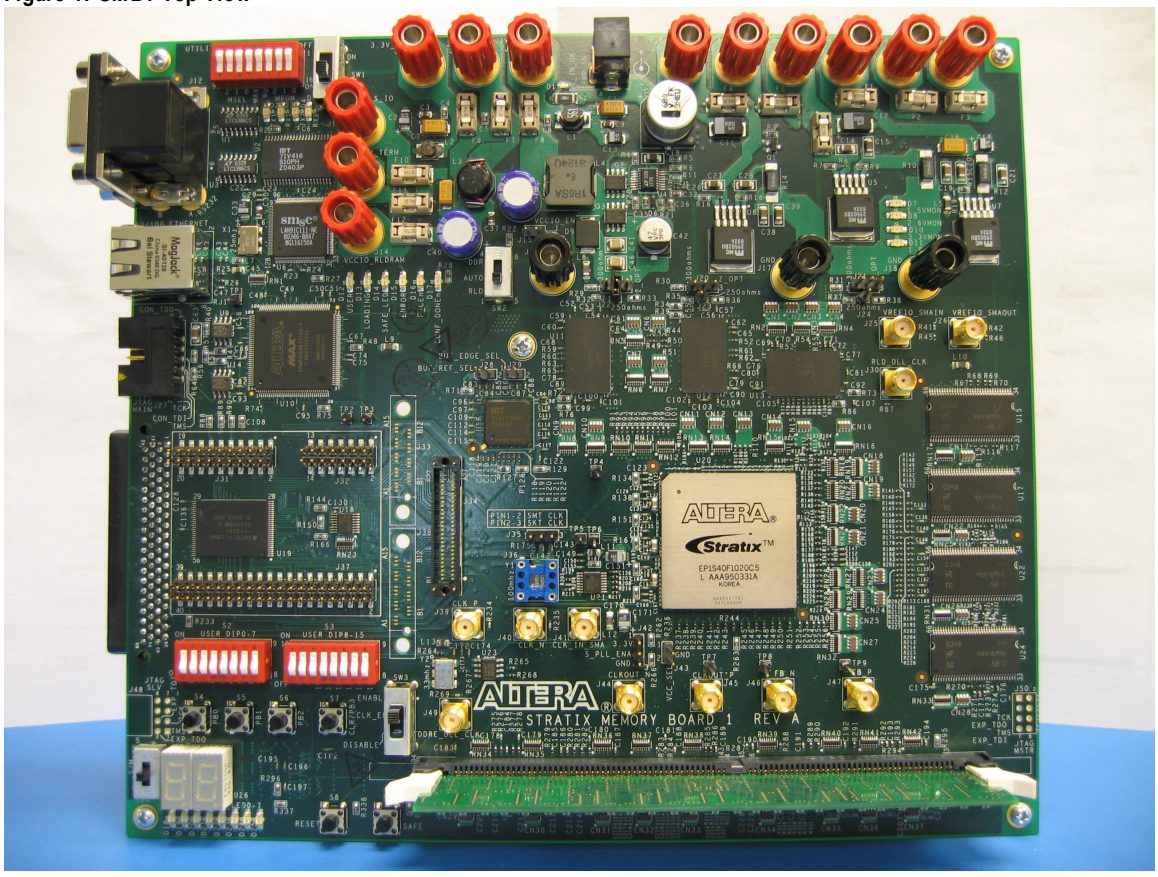


Table 1 describes the major components on the SMB1 and the related interfaces.

Table 1. SMB1 Components and Interfaces

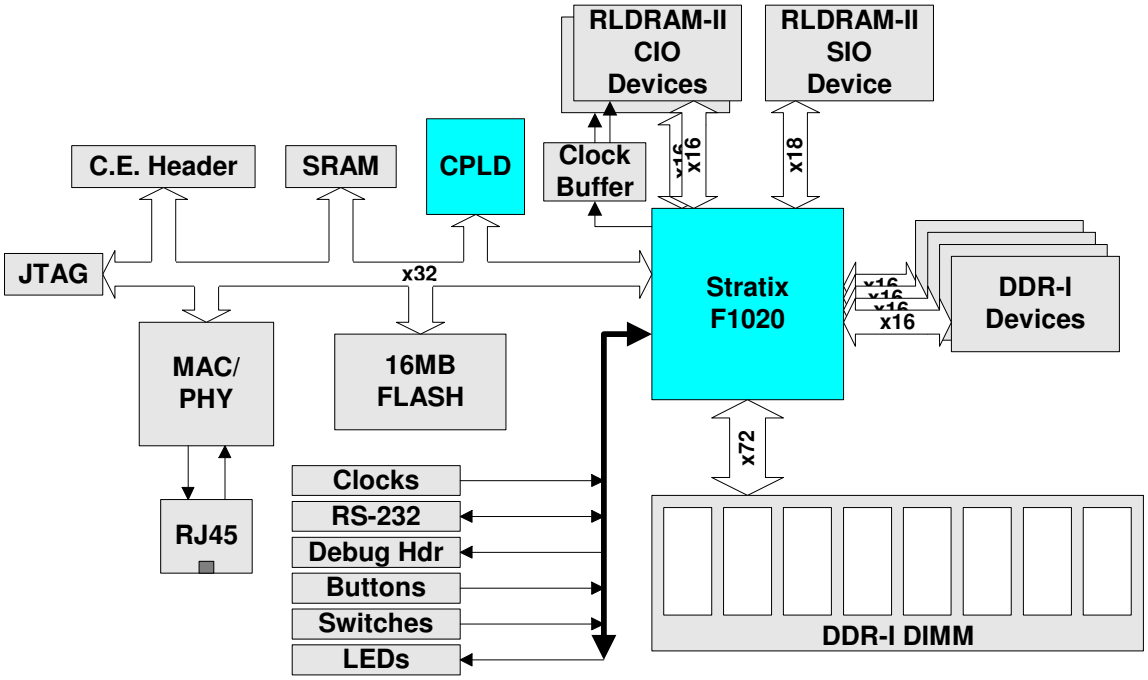
Type	Component/ Interface	Board Reference	Description
FPGA	Stratix device	U20	Altera Stratix ™ device, FBGA-1020, EP1S40F1020-C5
Memory	RLDRAM-II, SIO	U13	Micron 16M x 18, 400MHz, 2.5V, FBGA-144, MT49H16M18CFM-2.5
	RLDRAM-II, CIO	U11, U12	Micron 16M x 18, 400MHz, 2.5V, FBGA-144, MT49H16M18FM-2.5
	DDR-I SDRAM	U15,U17,U22, U24	Micron 4M x 16, 133MHz, 2.5V, 66-pin, MT46V16M16TG-5B
	DDR-I SDRAM DIMM	U27	Micron 32M x 72, 200MHz, 2.6V,184-pin DIMM, MT9VDDT3272AG-40B
	Flash	U19	128 Mb, 8M x16 TSOP-56, (Advanced Micro Devices, AM29LV128MH113REI)
	SRAM	U2,U30	4Mb, 256K x 16, TSopII-44, (IDT, IDT71V416S10PH)
Configuration	MAX CPLD Device	U10	Altera MAX™ CPLD device, 144-pin TQFP, EPM7256AETC144
	JTAG	J51,J50,J48,J27 SW4	JTAG test and interface select control by switch and ByteBlaster
	DIP Switches	S1,S7,S9	Configuration DIP switches. Refer to Control section in this table and see Tables 13 - 15
	Pushbuttons		Configuration pushbuttons. Refer to Control section in this table and see Table 16
Clock	System Clock OSC.	Y2	33.33 MHz clock oscillator
	High-speed Clock Oscillator	Y1:SMD, J36:Socket, J35:OSC Select	100.00 MHz clock oscillator. When connecting pins 1 and 2 of jumper J35 the SMD CLK is selected. When pins 2 and 3 of jumper J35 are connected the socket oscillator is selected. SW3 must also be set to CLK_EN in order for one of these oscillators to be selected. SW3 allows the option to use an on board oscillator or to use the SMA (J41) clock input
		J41, SW3, U21	SMA clock input. Switch SW3 uses the clock buffer (U21) to select between using the on board high speed oscillator or the SMA clock input
Control	System Reset Pushbutton	S8,U34	Reset hardware and reconfigure Stratix device. U34 is the pushbutton debouncer for all pushbuttons
	Device Clear Pushbutton	S7	Clears Stratix device without reconfiguring Stratix device
	DIP Switch	S1	Configuration DIP switch settings. See Tables 13 - 15
	Safe Pushbutton	S9	SAFEn, Safe Mode, loads the Stratix device with factory default configuration
User Settings/ Indictors	User DIP Switches	S2,S3	User defined octal DIP switches
	User Pushbuttons	S4,S5,S6	User defined pushbuttons
	User LEDs	D18,D19,D20, D21,D22,D23, D24,D25	Eight yellow user defined LEDs. LEDs are lit when logic 0 is driven to them
Configuration Indictors	Status LEDs	D12,D13,D14, D15,D16,D17	USERn, LOADINGn, SAFEn, ERRORn, EPS1_CONF_DONEn, FLASHn.
Power Indictors	Power Supply	D1	Blue LED used to indicate that the board is powered on
	3.3V Power	D10	Green LED used to indicate 3.3V power is good

Table 1. SMB1 Components and Interfaces			
Type	**Component/ Interface**	**Board Reference**	**Description**
	2.6V Power	D8	Green LED used to indicate 2.6V power is good
	1.8V Power	D11	Green LED used to indicate 1.8V power is good
	1.5V Power	D7	Green LED used to indicate 1.5V power is good
Power	Power Connector	J4	16V Universal power supply jack
	Power Switch	SW1	Power Switch to turn the board power on
IO	10/100 Ethernet	U6,X1,RJ1	10/100 Ethernet MAC/PHY. 25.00 MHz crystal oscillator, RJ45 connector with LED indictors.
Serial IO	RS-232	J12	Dual DB9 connector
		U1,U3	RS-232 Serial interface level shifter
	RS-232 Tx LEDs	D2,D4	RS-232 transmitter active indicators
	RS-232 Rx LEDs	D3,D5	RS-232 receiver active indicators
Nios Peripheral	Expansion Prototype Card	J31,J32,J37	Interface to Expansion Prototype Card
Debug	Agilent Debug Header	J34	Agilent E5387-68701 Debug Logic Analyzer Header
	Tektronix Debug Headers	J38,J33	Tektronix P6860 Debug Logic Analyzer Header

Functional Description

Figure 2 shows a block diagram of the SMB1.

Figure 2. SMB1 Block Diagram



Connector Function Summary

Table 2 shows the functions of the connectors on the SMB1.

Table 2. SMB1 Connectors

Connector	Stratix Device	Not Device Specific
Three Debug Proto Headers (see the "Debug Proto Connectors" section)	J31,J32,J37	
Logic Analyzer (see the "Debug Proto Connectors" section)	J33,J34,J38	
Configuration Expansion Headers (see the "Configuration Expansion Connector" section)		J48,J50,J51
10/100 Ethernet		RJ1
RS-232		J12

Switch and Jumper Functions

Table 3 summarizes the function of each switch and jumper on the SMB1.

Table 3. SMB1 Switches and Jumpers

I/O Function	Stratix Device	Not Device Specific	Jumper Connections
Power switch		SW1	
RLDRAM-II Power Select		SW2	
100.00-MHz Oscillator/SMA switch		SW3	
JTAG Device Select		SW4	
DIP switch for selecting options (see the "User DIP Switches" section)	S2, S3	S1	
Configuration Expansion Headers (see the "Configuration Expansion Connector" section)		J48,J50,J51	
VCC_SEL: J43, Pin 1-2 connects to 3.3V through 1 kOhm to GND.	Pin AJ14		J43 to (Stratix) U20.AJ14
S_PLL_SEL: J42, , Pin 1-2 ties signal to 3.3V through 1 kOhm, Pin 2-3 ties signal to GND.	Pin AF19		J42 to (Stratix) U20.AF19
RLDRAM-II SIO impedance (ZQ) select: J21, J24. Pin J24.1 – J21.2 ties 250Ω to GND for 50Ω impedance Pin J21.1 – J21.2 ties 300Ω to GND for 60Ω impedance Pin J21.2 – J21.3 ties uninstalled resistor to GND for user impedance selection			J21, J24 to U13.V2 (RLDRAM-II, SIO)
RLDRAM-II CIO impedance (ZQ) select: J20, J23. Pin J23.1 – J20.2 ties 250Ω to GND for 50Ω impedance Pin J20.1 – J20.2 ties 300Ω to GND for 60Ω impedance Pin J20.2 – J20.3 ties uninstalled resistor to GND for user impedance selection			J20, J23 to U12.V2 (RLDRAM-II, CIO)
RLDRAM-II CIO impedance (ZQ) select: J19, J22. Pin J22.1 – J19.2 ties 250Ω to GND for 50Ω impedance Pin J19.1 – J19.2 ties 300Ω to GND for 60Ω impedance Pin J19.2 – J19.3 ties uninstalled resistor to GND for user impedance selection			J19, J22 to U11.V2 (RLDRAM-II, CIO)
100 MHz VCO select: J35, Pin 1-2 selects SMT Clock, Pin 2-3 selects Socket Clock.			J35 to Y1 (SMT VCO), and J36 (VCO Socket)

Table 3. SMB1 Switches and Jumpers			
I/O Function	**Stratix Device**	**Not Device Specific**	**Jumper Connections**
BUF_EDGE_SEL: J29 Pin 1-2 selects negative edge			J29 to U16.H3 (Clock Buffer)
BUF_REF_SEL: J28 Pin 1-2 selects REF 0			J28 to U16.D1 (Clock Buffer)
VCCIO Enable: J15, Pin 1-2 connects to GND.			J15 to (MAX) U10.92

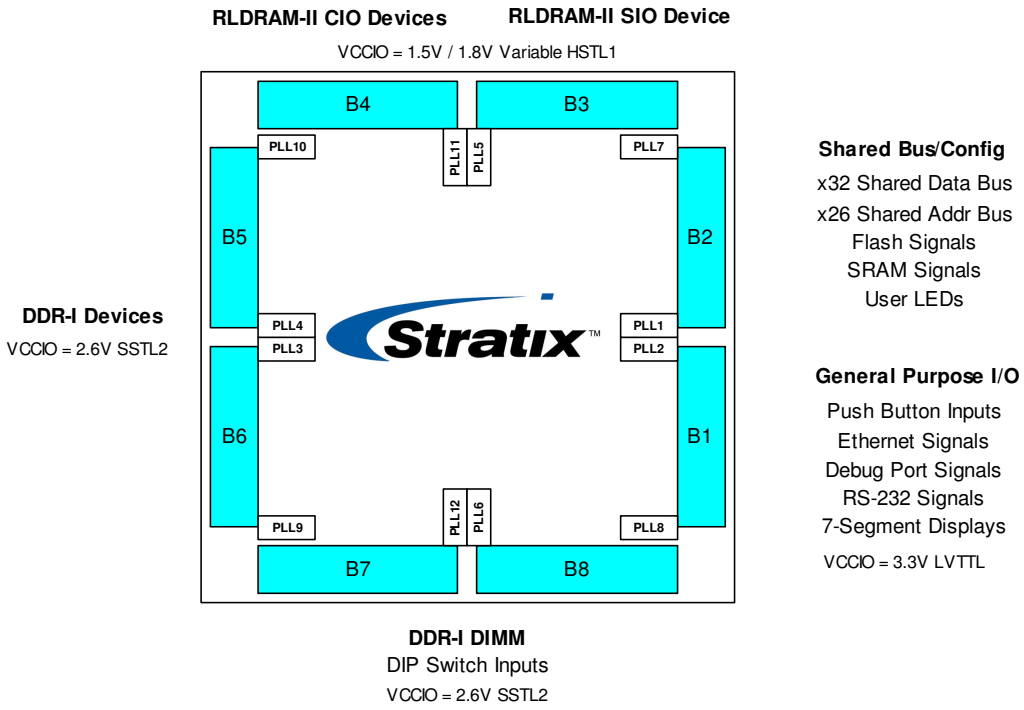
Development Board Stratix Device

The Altera Stratix device combines the latest in silicon features to achieve industry-leading performance in internal speed, I/O speeds, and internal memory density. The development board is designed for one 1,020-pin FineLine BGA package, the EP1S40F1020-C5 device. The EP1S40 device is the size option that allows additional high-speed differential logic (HSDI) interface capability, as well as additional PLLs, memory, and logic elements (LEs). Table 4 shows the device features.

Table 4. SMB1 Device Features	
Feature	**EP1S40**
LEs	41,250
RAM bits	3,423,744 (417 KB)
PLLs	12 PLLs (8 fast and 4 enhanced)
Transmitter and receiver source synchronous channels	80
Medium speed channels	10 receivers 10 transmitters
User I/O pins	781

Figure 3 shows the Stratix I/O bank diagram.

Figure 3. Stratix Bank Diagram



Board Layer Stack-Up

The SMB1 consists of 12 layers of FR4 material for a combined width of 0.065 inches. The board layer stack-up is shown in Table 5.

Table 5. SMB1 Layer Stack-Up Note (1)

Layer Number	Layer Type	Description	Thickness & Tolerances	
			Copper Thickness (Mils)	Laminate (Mils)
1	Mix (sig)	Foil	0.6	
		Pre-pregnate		3
2	GND Plane		1.2	
		Core		4
3	Signal		0.6	
		Pre-pregnate		6
4	Signal		0.6	
		Core		4
5	Plane		1.2	
		Pre-pregnate		4
6	Signal		0.6	

Table 5. SMB1 Layer Stack-Up Note (1)				
Layer Number	Layer Type	Description	Thickness & Tolerances	
			Copper Thickness (Mils)	Laminate (Mils)
		Core		6
7	Signal		0.6	
		Pre-pregnate		4
8	Plane		1.2	
		Core		4
9	Signal		0.6	
		Pre-pregnate		6
10	Signal		0.6	
		Core		4
11	Plane		1.2	
		Pre-pregnate		3
12	Mix (sig)	Foil	0.6	

Note to Table 5:

(1) 0.5 oz of copper is equivalent to a 0.6-mils trace width.

Power Sources

The SMB1 board's power design is based on a single DC input with on-board regulators generating the other required lower voltages. In addition to the on-board regulators, fuse isolated banana jacks are provided for all unique voltages for characterization purposes. The board has seven power regulators:

- One switching regulator
- Six linear regulators

Table 6 lists the power sources used on the SMB1 Development Board.

Table 6. SMB1 Regulators					
Reference Designator	Type	Voltage Output (V)	Description	Manufacturer	Part Number
U4	Switching regulator	3.3	Master supply for all regulators	Linear Technologies	LTC1778_SSOP16
U5	Linear regulator	1.5	Stratix, VCCINT	Micrel	MIC29502BU
U7	Linear regulator	2.5	RLDRAM-II, VEXT	Micrel	MIC29502BU
U8	Linear regulator	1.5	Stratix PLL internal	Micrel	MIC29502BU
U32	Linear regulator	1.8	RLDRAM-II, VDD	Micrel	MIC29502BU

Table 6. SMB1 Regulators					
Reference Designator	Type	Voltage Output (V)	Description	Manufacturer	Part Number
U33	Linear regulator	2.6/1.8	RLDRAM-II 1.8V, Stratix VCCIO or DDR, 2.6V VDD/VDDQ	Micrel	MIC29502BU
U31	Linear regulator	1.3/0.9	Termination regulator (VTT and VREF)	National Semiconductor	LP2996MR

Power Supply

The board can be powered in two different ways:

1. 16V Universal AC/DC Power Jack (J4)

2. Bench power supplies (various banana jacks)

16V Universal AC/DC Power input

A 16V AC/DC power input is provided by a right-angle 2.5mm power jack with a 5.5mm barrel. The incoming DC voltage is regulated down to 3.3V by a switching power supply. From these voltages all other on-board voltages are generated.

Bench Power Supplies

Socketed fuses are provided to bypass the 16V Universal power supply in order to isolate the voltage planes from the regulators to allow bench supplies to power these sections using banana jacks. The bench supply inputs are placed after the other power supplies (whether linear or switching supplies) on the board in order to allow current draw measurements.

Power Planes

Bench power supplies provide an easy way to measure the current draw on each power plane. When one plane is being powered by the bench supply, all other planes still draw current from the DC power input. Upon applying power to the board, the power LED should be on.

Table 7 shows the procedure for powering individual planes through bench power supplies. In the instructions in Table 7, only remove the fuse listed in the "Instructions" column. Leave the other fuses on the board.

Table 7. Procedure for Powering Individual Power Planes Through Bench Power Supplies		
Power Plane	Power Plane Using Bench Power Supplies(1)	Instructions
1.5V_PLL	Stratix PLL, Except VCC PLL5_OUTp/n and VCC_PLL6_OUTp/n	Remove fuse F4. Apply (+1.5V, GND) to (J5, J16)
3.3V_PLL	Stratix VCC_PLL6_OUTp/n	Remove fuse F6. Apply (+3.3V, GND) to (J1, J16)

Table 7. Procedure for Powering Individual Power Planes Through Bench Power Supplies		
Power Plane	**Power Plane Using Bench Power Supplies(1)**	**Instructions**
1.5V_INT	Stratix VCCINT	Remove fuse F9. Apply (+1.5V, GND) to (J7, J17)
VCC_S_IO	Stratix I/O power, Banks 1, 2, 3, 4, 7, & 8, and VCC_PLL5_OUTp/n	Remove fuse F10. Apply (+1.8V or +2.6V, GND) to (J11, J17)
3.3V_S_IO	Stratix I/O power, Banks 5, & 6	Remove fuse F8. Apply (+3.3V, GND) to (J3, J17)
2.5V	RLDRAM-II VEXT power input	Remove fuse F1. Apply (+2.5V, GND) to (J8, J17)
2.6V_TERM	DDR-I or RLDRAM-II termination regulator input voltage	Remove fuse F11. Apply (+1.8V or +2.6V, GND) to (J13, J17)
VTT	DDR-I or RLDRAM-II Vtt voltage	Remove fuse F2. Apply (+0.9V or +1.3V, GND) to (J9, J17)
VREF	Reference voltage for DDR-I or RLDRAM-II	Remove fuse F3. Apply (+1.8V or +2.6V, GND) to (J10, J18)
VCCIO_RLDRAM	RLDRAM-II VDDQ	Remove fuse F12. Apply (+1.8V, GND) to (J14, J18)
1.8V	RLDRAM-II supply (VDD)	Remove fuse F5. Apply (+1.8V, GND) to (J6, J18)
3.3V	Stratix I/O, MAX, and misc.	Remove fuse F7. Apply (+3.3V, GND) to (J2, J17)

Note to Table 7:

(1) Power plane which will use bench power supply rather than the DC power supply.

System Monitoring

The SMB1 includes several chips designed for real-time monitoring on the board to increase the ability to provide more information about a design or potential demo without requiring a great deal of equipment. This includes the Stratix FPGA temperature, various system voltages, and overall system power consumption. The following sections detail the ASSPs used to add this functionality.

Temperature Sense

The Maxim 1619 temperature sense chip that can read subtle changes in voltage drop across the Stratix temperature sense diode circuit. This is useful in doing on-the-fly temperature reading by chip designs versus manual measurements. The MAX1619 comes in a QSOP-16 and has the following features:

- Two measurement channels
  - Local (MAX1619)
  - Remote (Stratix)
  - +/- 2°C accuracy
- Programmable over/under temperature outputs
- SMBus interface for real-time readings

Power Sense

A linear Tech LTC2901 Quad Voltage Watchdog device will be employed to monitor the board voltages. The 3.3V, 1.8V, 1.5V, and 2.6V monitoring signals are connected to Green LEDs to provide immediate visual voltage status. This device will be used in mode 10 and will allow the monitoring of the following voltages only:

- 3.3V (From switching supply)
- 1.8V (From switching supply)
- 1.5V (Derived from 1.8V)
- 2.6V

Current Sense

The Stratix device has 10pF loads on all lines that are used. Assuming 2 Amps for the LVTTL I/O and using the Stratix Power Calculator, the current draw for each application is tabulated in Table 8.

Table 8. SMB1 Current Draw

Regulator/ Application Voltage (V)	DDR-I DIMM (A)	DDR-I x16 (A)	RLDRAM-II SIO (A)	RLDRAM-II CIO (A)	Stratix VCCINT (A)	Stratix VCCIO (A)	LVTTL Access-ories (A)	Max I (A)
3.3						1.836	2	3.836
2.5 / 2.6	2.1	0.553	0.1	0.1				2.1
1.25	1.875	0.872						1.875
1.5					1.017			1.017
1.8			1.0	1.0				1.0
1.8 / 1.5			1.0	1.0				1.0
0.9 / 0.75			1.026	1.278				1.278
3.3V Total Current	8.828	6.278	7.879	8.131				

Configuration

The Stratix™ device on SMB1 is configured from Flash as the primary method. The MAX CPLD contains the required state machine and control logic to accomplish this task. Configuration of both the MAX and Stratix™ is also supported directly on SMB1 using the standard JTAG header (See JTAG section for more detail).

The required file sizes for the Stratix™ device is 3,273,391 bytes for the hexout file, 1,528,528 bytes for the SOF file and 1,557,393 bytes for the RBF file. The "RBF" is the raw binary configuration file size that would be programmed into Flash. The flash device is 16MB and thus will allow up to 8 configuration files for the Stratix™ device to be stored in even (power-of-2) offsets in flash along with additional space for other uses such as NIOS object-code or other non-volatile data. Alternatively, the flash could be filled with a "safe" factory design and a custom demo design with support for up to 12MB of space for demo data such as a video file and/or web page file structure.

MAX7256AE Configuration System Controller

The system configuration controller is the EPM7256AETC144-7. This is a 3.3V device that provides more than enough logic resources for configuration and system control. Support for devices larger than the target Stratix™ device (80K LEs) is necessary on SMB1 in order to provide debugging of the general circuit before the creation of the Stratix™ -II version of this board in the future.

The signals listed in Table 9 are relative to the MAX chip design. They include both system control and configuration signals and dedicated function pins for configuration. The "TYPE" shall be considered relative to the MAX Device insofar as the I/O setting and direction.

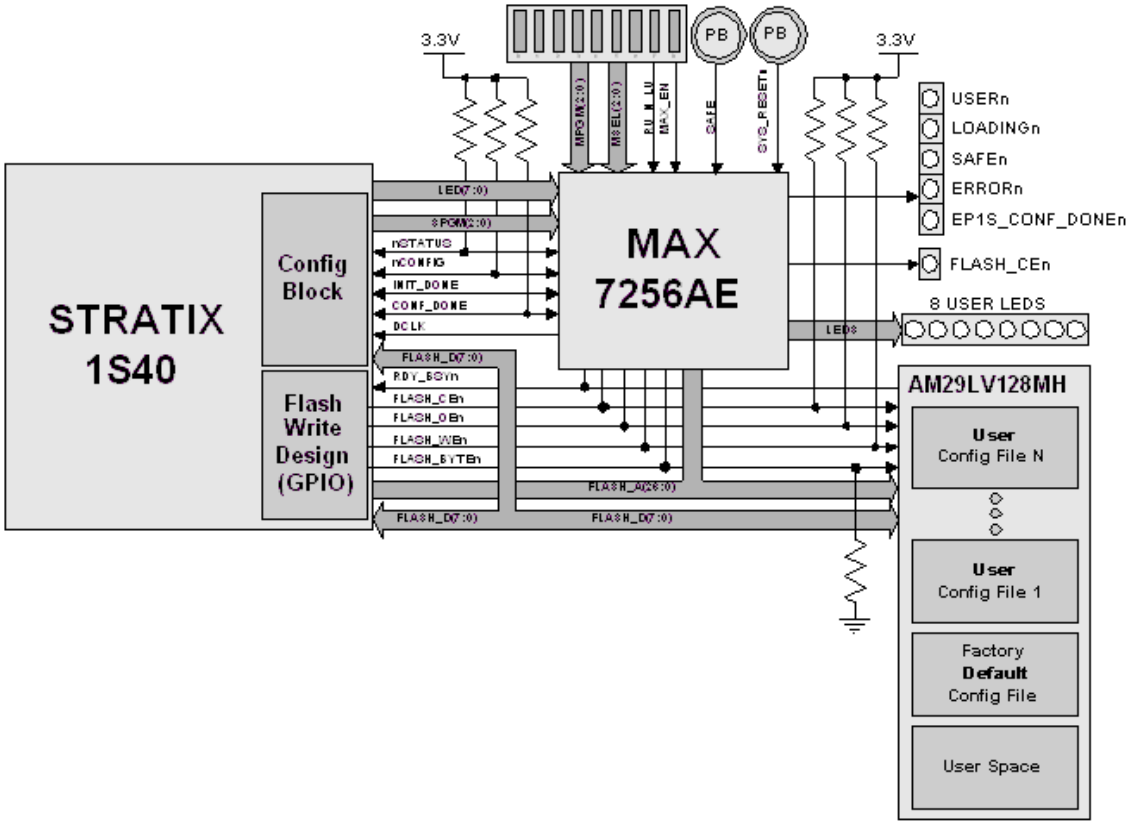
Table 9. CPLD I/O Requirements

Signal Name	Description	Type
FSE_A(26:0)	Shared Bus Address (Flash)	LVTTL Output (27 bits)
FSE_D(7:0)	Shared Bus Data (Flash)	LVTTL Input (8 bits)
CONFIG_D(7:0)	Config Data	LVTTL Output (8 bits)
FLASH_CEn	Flash Chip Enable	LVTTL Output
FLASH_WEn	Flash Write Enable	LVTTL Output
FLASH_OEn	Flash Output Enable	LVTTL Output
FLASH_RDY_BSYn	Flash Ready / not BUSY	Open Drain Input*
FLASH_RESETn	Flash Reset Output	LVTTL Output*
FLASH_BYTEn	FLASH Byte-Mode / Word-Mode Select	LVTTL Output*
MPGM(2:0)	DIP switch Configuration File Select	LVTTL Input (3 bits)
PGM(2:0)	Stratix™ Configuration File Select	LVTTL Input (3 bits)
SYS_RESETn	System Reset	LVTTL Input
SAFE	Safe-Mode Reset	LVTTL Input
ENET_RESET	Ethernet Reset	LVTTL Output
RU_N_LU	Remote/Local Mode Select	LVTTL Input
MSEL(2:0)	Remote/Local Mode Select	LVTTL Input (3 bits)
MAX_EN	MAX config enable	LVTTL Input
CLK(2:1)_OUT_MAX	Input Clock	LVTTL Input (GCLK1)
CONFIG_DCLK	Config Clk	
LED(7:0)	LED Buffer Input	LVTTL Input (8 bits)
FLASH_CE_LEDn	LED Buffer Output	LVTTL Output
USER_LEDn	LED Buffer Output	LVTTL Output
LOADING_LEDn	LED Buffer Output	LVTTL Output
SAFE_LEDn	LED Buffer Output	LVTTL Output
ERROR_LEDn	LED Buffer Output	LVTTL Output
MAX_LED(7:0)	LED Buffer Output	LVTTL Output (8 bits)
EP1S_INIT_DONE	Configuration Init done	
EP1S_CONF_DONEn	LED Buffer Output	LVTTL Output
EP1S_CONF_DONE	Stratix™ CONFIG DONE	Open Drain Input
EP1S_CONFIGn	Stratix™ nCONFIG	Open Drain Bidir
EP1S_STATUSn	Stratix™ nSTATUS	Open Drain Input
3.3V_MON	3.3V Monitor Input	
2.6V_MON	2.6V Monitor Input	
VCCIO_ENABLE	VCCIO regulator enable	
SELECT_RLDRAMn	RLDRAM VCCIO Enable	
CPLD_USER(1:0)	CPLD User Pins	
RLD_PWR	RLDRAM VDD Power Enable	
JTAG_TCK	JTAG Clock	n/a
JTAG_TMS	JTAG Mode Select	n/a
JTAG_MAX_TDI	JTAG Data In	n/a

Table 9. CPLD I/O Requirements		
Signal Name	**Description**	**Type**
JTAG_MAX_TDO	JTAG Data Out	n/a
3.3V	Internal Power, 3.3V	Power
GND	Ground	Ground
MAX CPLD I/O Totals	122 I/O pins	

A general block diagram of the MAX/Flash configuration system is shown Figure 4. This figure does not show the extra signals involved in the use of the Configuration Expansion Header and Board, nor does it show the other devices on the "Shared Bus" as are shown in the diagram in the respective section of this document.

Figure 4. MAX/Flash Configuration Block Diagram



Flash Memory Map

Table 10 show an example memory map. This memory map is a generic starting place and not necessarily a definitive map. User Code Space and areas marked "other" are reserved for NIOS software images and other binary files for use in demos and otherwise.

It should be noted that configuration files can be placed closer to one another than shown below. This is

accomplished by increasing the complexity of the configuration state machine to start counting on non-power-of-two address offsets. For example, a file of just over 2MB needs 4MB to be placed in a power-of-two offset base address. This assures the smallest possible address counter. Alternatively the counter could start at 3MB with a slightly larger counter or even at 2.5MB with a larger-yet counter.

Table 10. Stratix™ / 16MB Flash Memory Map	
Block Name	**Address**
PLD Design 5 / Other	0x0FFF.FFFF 0x0E00.0000
PLD Design 4 / Other	0x0DFF.FFFF 0x0C00.0000
PLD Design 3 / Other	0x0BFF.FFFF 0x0A00.0000
PLD Design 2 / Other	0x09FF.FFFF 0x0800.0000
PLD Design 1	0x07FF.FFFF 0x0600.0000
PLD Design 0	0x05FF.FFFF 0x0400.0000
Safe Design	0x03FF.FFFF 0x0200.0000
User Code Space	0x01FF.FFFF 0x0000.0000

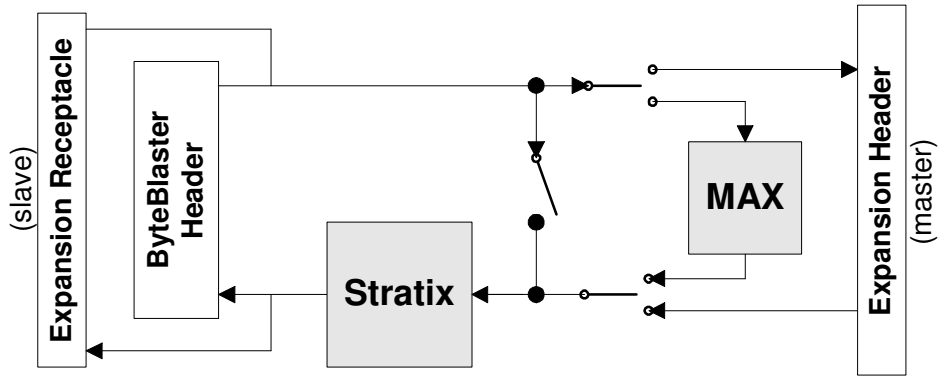
JTAG

A single 10-pin keyed, right-angle, shrouded, header is provided for configuring the MAX CPLD and Stratix FPGA in a single JTAG chain using ByteBlaster-II and compatible JTAG programming adapters. The JTAG Header is the Molex 39-26-7108. A Double pole triple throw Switch (SW4) is used to select which device is attached to the JTAG chain. This switch allows either the Stratix, MAX, or the JTAG expansion header to be configured. The JTAG Bypass settings are listed below.

Table 11. JTAG Bypass Switch	
Devices in Chain	**Position**
Stratix™	1 (near pin 1)
MAX and Stratix™	2
Expansion and Stratix™	3

This JTAG Chain will be able to expand to multiple SMB1 boards or other boards that support the Configuration Expansion Header. Whatever board is on the end of the chain (furthest from the board that has the ByteBlaster plugged in) would bypass the expansion header to loop the signals back through the return path. SMB1 is limited in this as its JTAG output pins are powered from a 1.8V bank and a MAX cannot read its output but a ByteBlaster-II can. Figure 5 shows this JTAG chain graphically.

Figure 5. JTAG Chain



Configuration Expansion Connector

For various configuration testing and characterization there is a right-angle connector on the board known as the Configuration Expansion Connector. This 80-pin SCSI-type connector supports other means of configuration such as EPC devices and EPCS devices from a separate board. MAX/Flash and MSEL pins are already located on the mainboard (SMB1) so they are not needed on the Configuration Expansion Board that will mate to this connector.

JTAG Expansion Connectors

A pair of right-angle connectors (one header and one receptacle) is supplied on the board to allow the JTAG chain to be extended to multiple boards for loading, testing, and JTAG checkout for more complicated chains. The header/receptacle pair connects ground but not power and uses only a 2x4 array. The pinout connects the master's TDO pin to the slave's TDI pin and connects TCK and TMS directly through.

Clocking

The clocking circuitry design of the SMB1 is very complicated and has been designed with flexibility and user friendliness in mind. The clocks are passed through logic translators and routed to the appropriate destinations as shown in Figure 6. The board has the following oscillators:

- (X1) is a 25-MHz crystal used in the MAC/PHY, 10/100 Ethernet interface.
- (Y1) is a 100.00-MHz oscillator for the high speed interface.
    - The user has the option of using an SMD or using the socket (J36) to allow flexible oscillator use. Another option is to use the SMA (J41) connector input. This is meant as the primary clock source. This oscillator has a dual-footprint that allows a user to add in their own crystal by disabling the on-board device through a jumper. This increases reliability and allows the use of higher-quality SMT crystals that are readily available. It can be easily replaced with custom frequency oscillators from many different vendors. This clock system is buffered using a LVCMOS clock buffer. The **SMA (J41)** is a secondary input to the Stratix through the above LVCMOS clock buffer and is terminated with a 50-ohm resistor to ground. Only one input can be used at any given time. This input is very useful for sweeping frequencies to verify Fmax performance of designs.
- (Y2) is a 33.33-MHz used for general purpose and configuration clocking to the Stratix device through a clock buffer to provide a lower-jitter clock to more sources for greater flexibility. The entire 33MHz clock system is LVTTL.

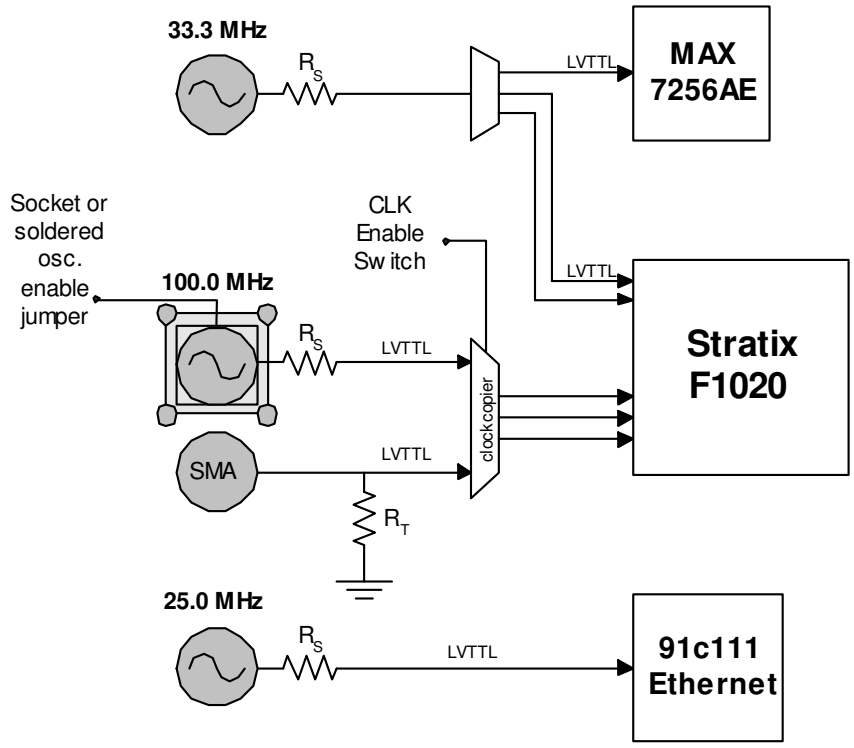
In addition to the crystal inputs, there are SMA connectors to provide alternative ways to clock the board. Additionally, there are several differential clock inputs from SMA connectors.

See Table 12 for the complete list of clock nets and their descriptions.

Table 12. SMB1 Clock Nets

Clock Name	Origin	Destination	Description
CLK_OSC_A	Oscillator (Y2)	Clock Buffer (U23)	33.33 MHz system/configuration input clock for the Stratix device.
CLK_OSC_B	Oscillator (Y1) or (J36)	Clock Buffer (U21)	100.00 MHz high speed clock for the Stratix device.
CLK_IN_SMA	SMA (J41)	Clock Buffer (U21)	High speed clock input for the Stratix device. This clock maybe used instead of the on board oscillator.
CLK_25MHz	Crystal Osc (X1)	Ethernet (U6)	25.00 MHz input clock to the LAN91C111 device, XTAL1, pin 127.
SMA_CLK_P SMA_CLK_N	SMA (J39) SMA (J40)	Stratix device (U20)	Differential clock input to the Stratix device, CLK11p, and CLK11n.
SMA_FB_P SMA_FB_N	SMA (J47) SMA (J46)	Stratix device (U20)	Differential clock input to the Stratix device, PLL6_FBp, and PLL6_FBn.
DDRE_SMA_DLL_CLK	SMA (J49)	Stratix device (U20)	DDRE DLL clock input to the Stratix device, CLK7p.
RLD_SMA_DLL_CLK	SMA (J30)	Stratix device (U20)	RLDRAM DLL clock input to the Stratix device, CLK13p.
VREFIO_SMAIN	SMA (J25)	Stratix device (U20)	VREFIO clock input to the Stratix device, Bank 1, pin U22.
VREFIO_SMAOUT	Stratix device (U20)	SMA (J26)	VREFIO clock output from the Stratix device, Bank 1, pin W22
CLKOUT_P CLKOUT_N	Stratix device (U20)	SMA (J44) SMA (J45)	Differential output clock from the Stratix device, PLL6_OUT0_P, PLL6_OUT0_N.

Figure 6. Stratix Development Board Clocking Circuitry Note (1)



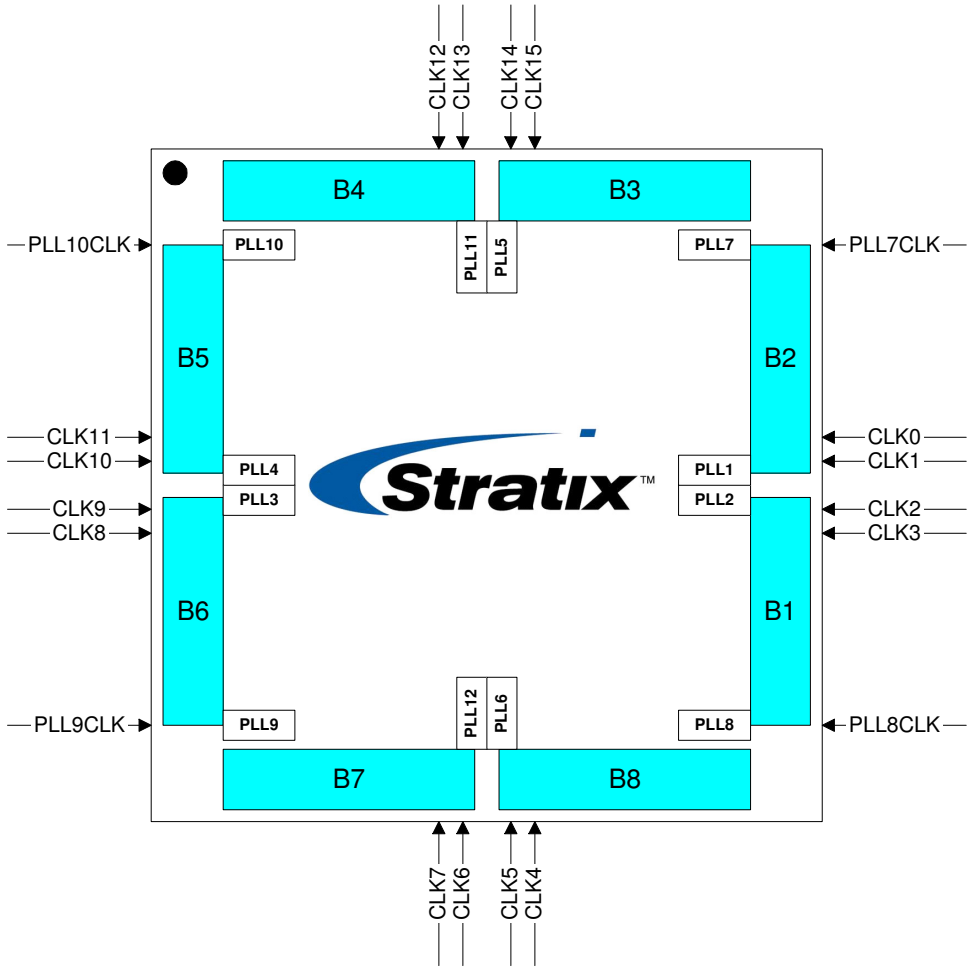
Note to Figure 6:
(1) Figure 6 only shows the important blocks of the clocking network. See the board schematics for details.

Stratix PLL and Clocking Features

The Stratix has 16 dedicated clock inputs that access 16 global clock networks (CLK(0..15) and 8 regional clock networks (4 per quadrant). There are also 8 dedicated fast regional clock input pins that can have smaller pin-to-LE delays for special purposes.

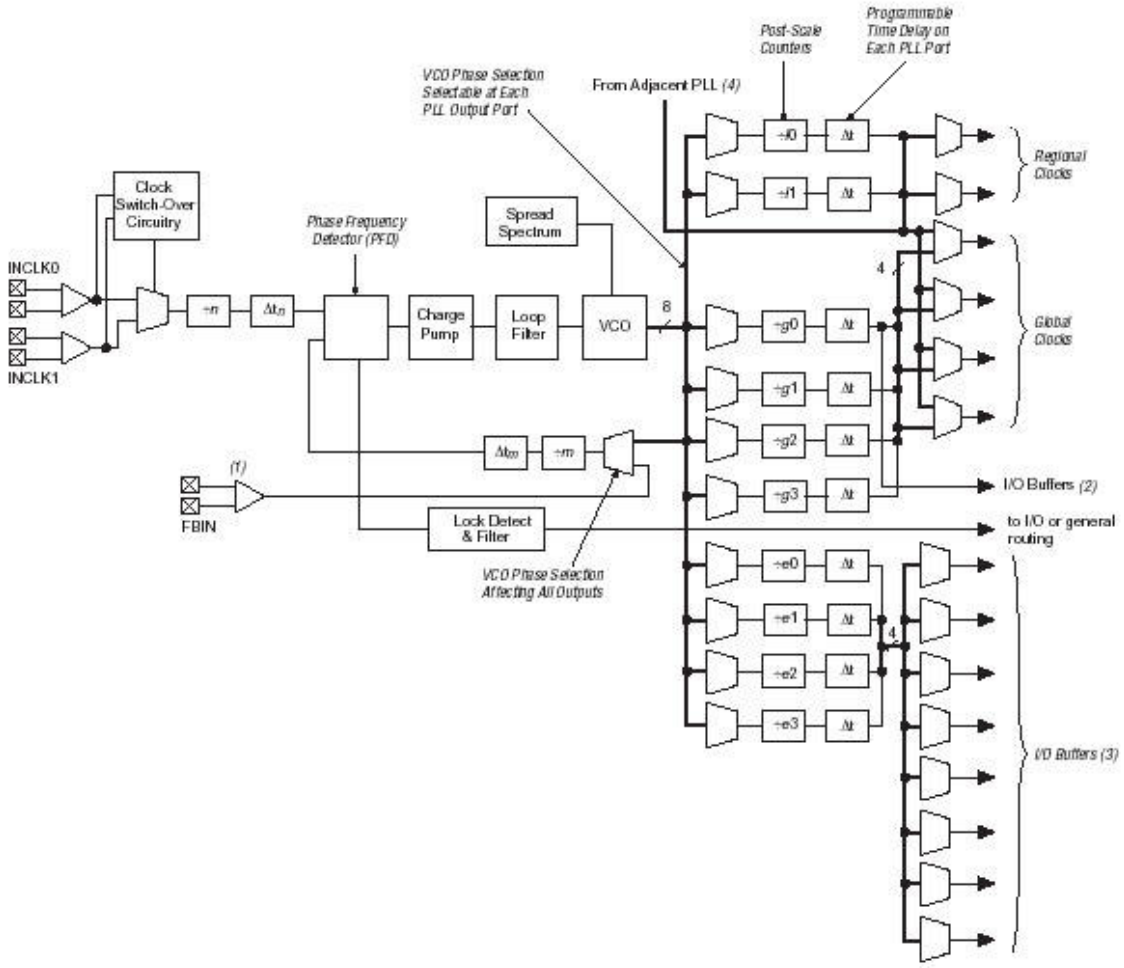
Figure 7 outlines this clocking scheme. Pin 1A is the upper left-hand corner in Figure 7 (PACKAGE-TOP referenced).

Figure 7. Stratix PLL and Clocking Resources



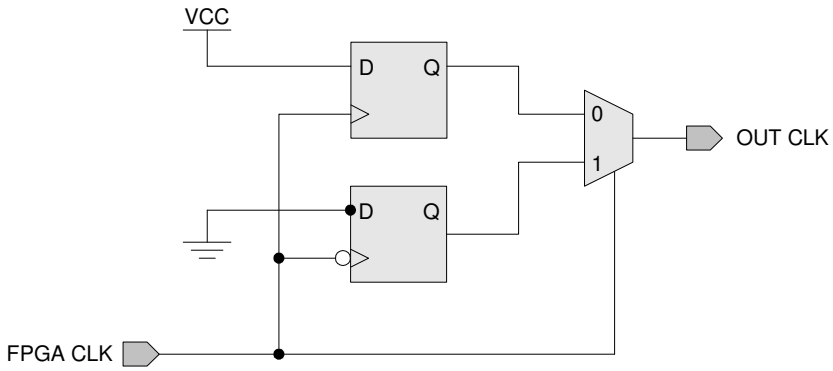
The 1S40 Stratix device has four "Enhanced PLLs." These include PLL5 and PLL11 on the top of the chip and PLL6 and PLL12 on the bottom of the chip. They can drive any of the global or regional clock networks. PLL5 and PLL6 each connect to their own dedicated block of 8 clock outputs (or 4 differential outputs). Each output block has its own power supply so it can be split among different I/O standards such as 1.5V HSTL on one block and 2.5V SSTL on another block. Enhanced PLLs can drive FPLL inputs through global clock networks as well. The connections between Enhanced PLLs, clock inputs, and clock outputs are fairly detailed. These connections are shown in Figure 8.

Figure 8. Enhanced PLLs, Input and Output Clocking Connections



Any PLL, either Enhanced or Fast, can drive all registers in the FPGA, including I/O registers. One can create a convenient clock output for DDR applications by clocking an I/O register programmed with the ALTDDIO Megafunction such that it drives a pre-programmed "1" on one clock edge and a pre-programmed "0" on another. Figure 9 shows this output buffer configuration in a Stratix device where the "OUT CLK" is the board-level clock to the memory.

Figure 9. ALTDDIO I/O Register External Clock Output



RLDRAM-II Clocking

Figure 10 shows the clocking block diagram for the RLDRAM-II SIO device. The EPLL5 drives the DK and CK clocks with a DDR IO register. To minimize skew, both clocks are connected together on the RLDRAM-II devices. The same top-side DLL as the RLDRAM CIO devices is used and the SIO interface's feedback clock comes from a DDR IO register. Figure 11 shows the RLDRAM-II CIO device's clock diagram. The EPLL5 drives the RLDC clock buffers (zero delay buffer) reference clocks (one differential pair (RLDC_REF) from dedicated clock output pins and one single ended (RLDC_CK_OUT) from DDR IO register). The RLDRAM clock buffer drives each CIO device's clocks. One DDR IO register drives the RLDRAM devices DLL clock and the RLDRAM CIO feedback comes from the clock buffer.

Figure 10. RLDRAM-II SIO Clocking Block Diagram

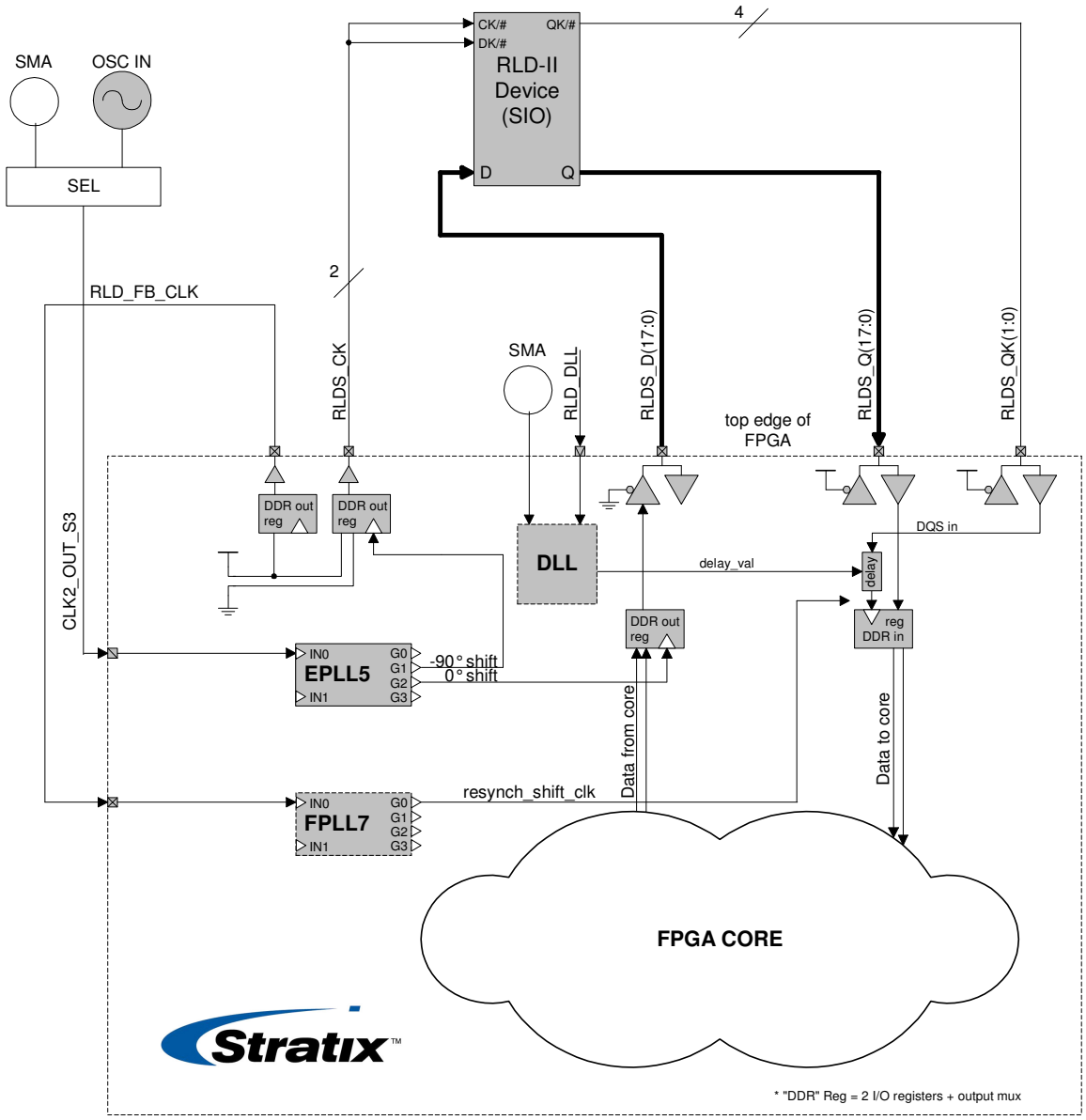


Figure 11. RLDRAM-II CIO Clocking Block Diagram

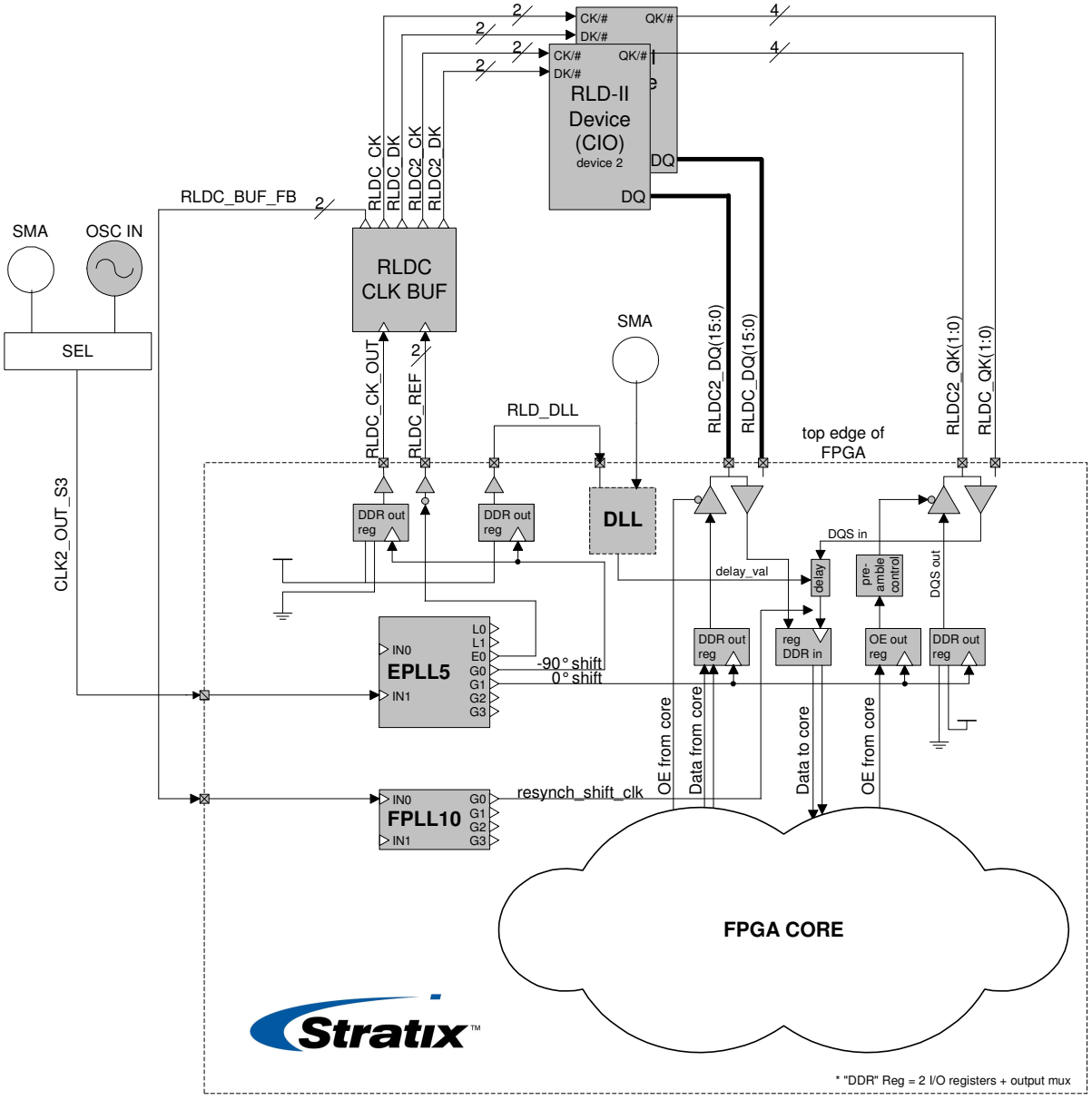


Figure 12. DDR-I DIMM Clocking Block Diagram

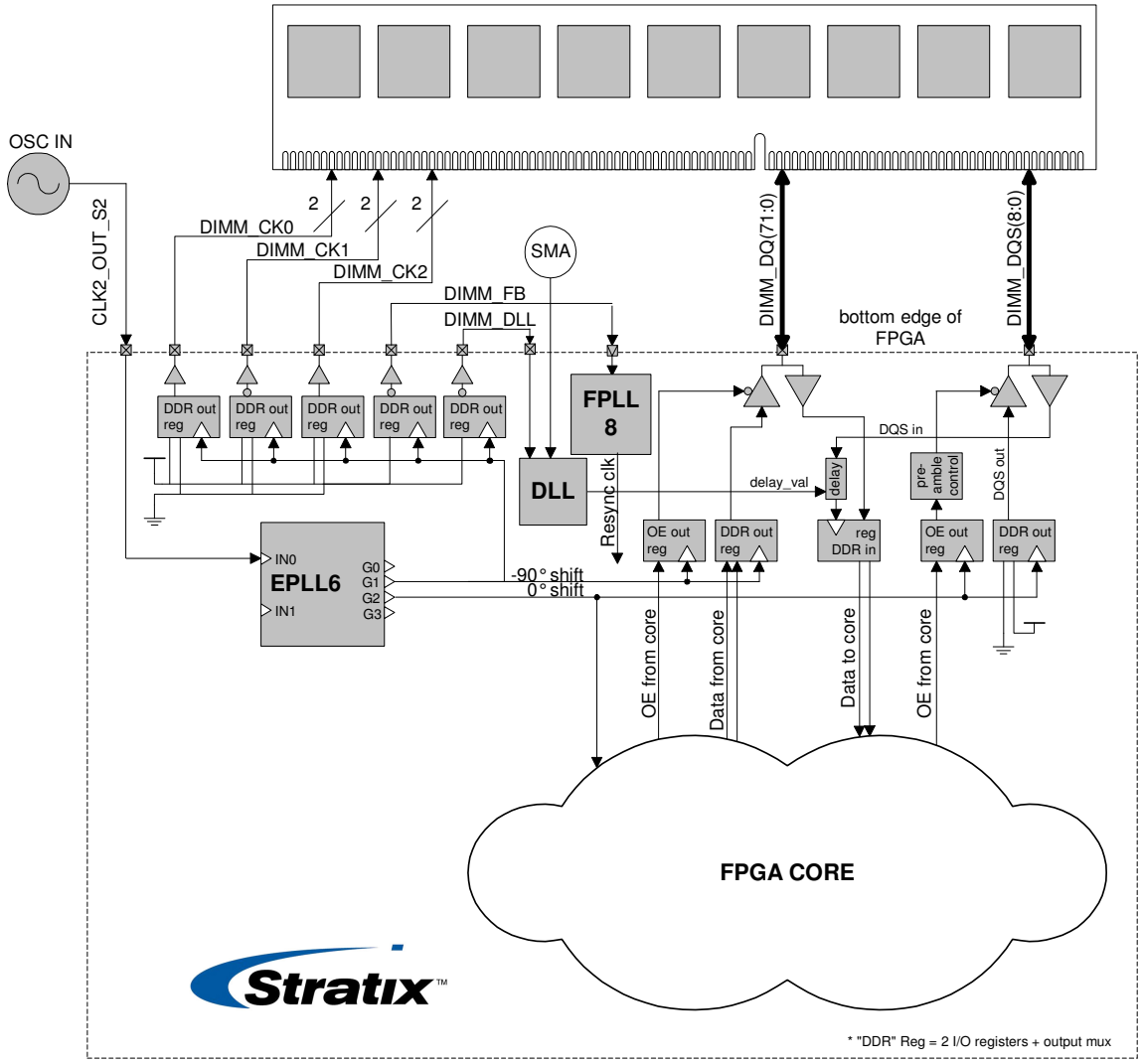
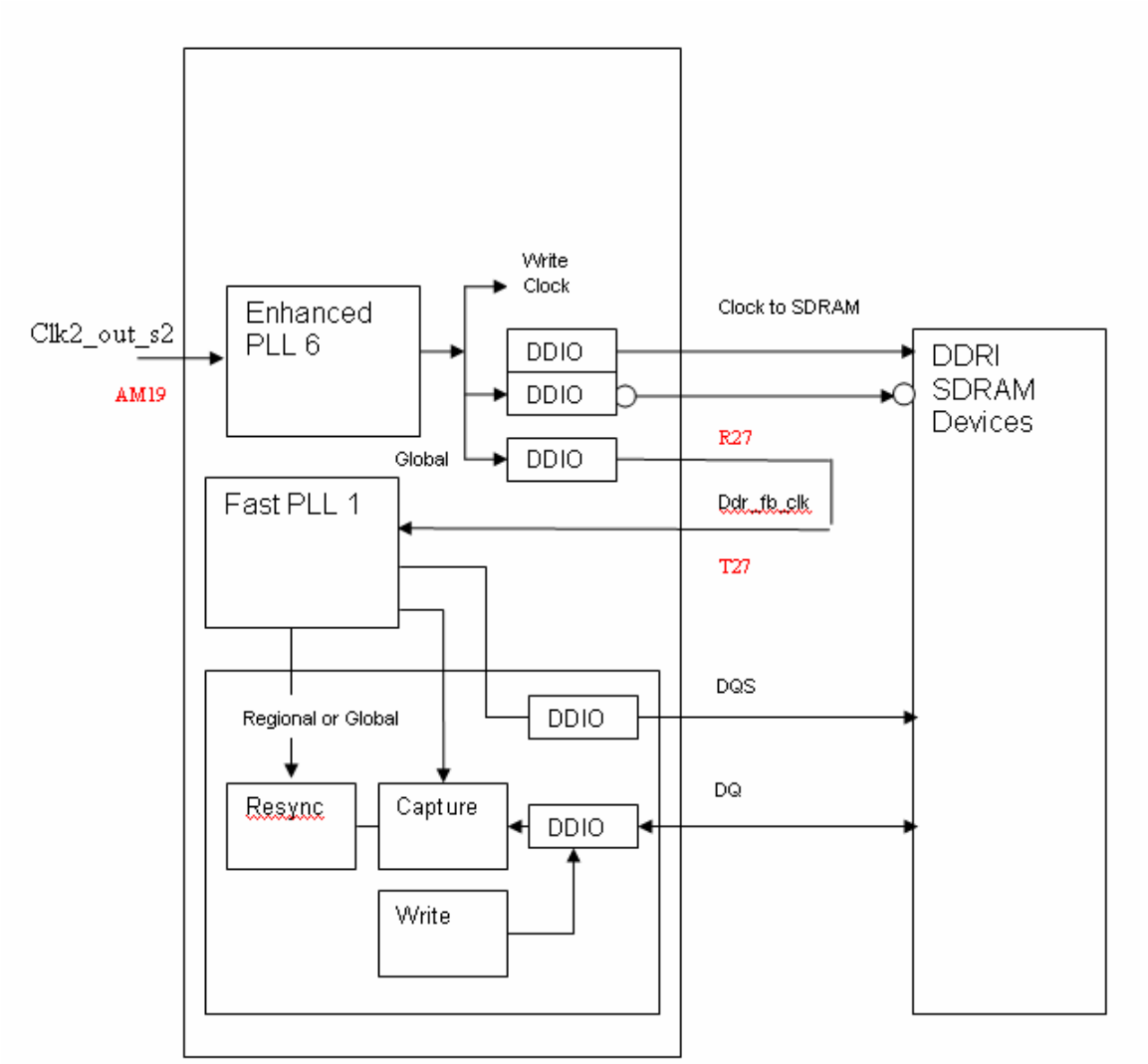


Figure 13. DDR-I SDRAM Device Clocking Block Diagram



User I/O Standards

Board setting DIP Switch

An 8-position DIP switch allows the user to configure board specific options. These are not available to the user for general programmable use as they affect hard-wired function pins for various devices. The RU_N_LU and MSEL switches are only used if a user wants to use the Remote/Local update block in Stratix to initiate reconfiguration and, if so, in which mode. The MSEL2 pin tells the MAX configuration controller to use the DIP switch PLD image pointer (MPGM(2:0) switches) when ON and to use the special Stratix SPGM(2:0) pins when OFF.

The MPGM(2:0) pins select one of eight possible PLD configuration file images in Flash to load upon power-up or SYS_RESETn. The Stratix can also point to the configuration file using its PGM(2:0) pins (using ALT_REMOTE IP block in Stratix) that drive the SPGM(2:0) nets on the board. Table 13 lists the pin assignment for each switch.

- When a switch is in the ON position a "0" is selected for the option.
- When the switch is in the OFF position, a "1" is selected for the option.

Table 13. Stratix DIP Switch Pinouts (S1)

Signal Name	Dip Switch (S1) Pin	Max (U10), Stratix (U20) Pin	DIP Position "ON"	DIP Position "OFF"
MPGM0	16	U10.101	"0" for PGM0	"1" for PGM0
MPGM1	15	U10.102	"0" for PGM1	"1" for PGM1
MPGM2	14	U10.103	"0" for PGM2	"1" for PGM2
Ru_N_LU	13	U10.45, U20.AF14	DIP MPGM Select	Stratix SPGM select
MAX_EN	12	U10.97	MAX Enable	MAX Disable
MSEL0	11	U10.93, U20.AG18	See PLD Datasheet	See PLD Datasheet
MSEL1	10	U10.94, U20.AE18	See PLD Datasheet	See PLD Datasheet
MSEL2	9	U10.96, U20AE19	Stratix Local Mode	Stratix Remote Mode
GND	1	NA		
GND	2	NA		
GND	3	NA		
GND	4	NA		
GND	5	NA		
GND	6	NA		
GND	7	NA		
GND	8	NA		

User DIP Switches

The two user DIP switches are for reference design functions and general purpose use. Tables 14 and 15 lists the pin assignment for each switch.

- When a switch is in the ON position a "0" is selected for the option.
- When the switch is in the OFF position, a "1" is selected for the option.

Table 14. Stratix DIP Switch Pinouts (S2)

Signal Name	Dip Switch (S2) Pin	Stratix (U20) Pin
DIP0	16	AB19
DIP1	15	AD20
DIP2	14	AE20
DIP3	13	AD19
DIP4	12	AJ18
DIP5	11	AH18
DIP6	10	AK18

Table 14. Stratix DIP Switch Pinouts (S2)		
Signal Name	**Dip Switch (S2) Pin**	**Stratix (U20) Pin**
DIP7	9	AA21
GND	1	NA
GND	2	NA
GND	3	NA
GND	4	NA
GND	5	NA
GND	6	NA
GND	7	NA
GND	8	NA

Table 15. Stratix DIP Switch Pinouts (S3)		
Signal Name	**Dip Switch (S3) Pin**	**Stratix (U20) Pin**
DIP8	16	AB21
DIP9	15	AD22
DIP10	14	AC21
DIP11	13	AB20
DIP12	12	AB24
DIP13	11	AC24
DIP14	10	AC23
DIP15	9	AD24
GND	1	NA
GND	2	NA
GND	3	NA
GND	4	NA
GND	5	NA
GND	6	NA
GND	7	NA
GND	8	NA

Push Buttons

Push buttons are provided for board-level reset, device-wide reset, and for user defined functions. Table 16 lists the assignment for each push button and LED.

Table 16. Push Button Pinout

Signal Name	Function	Push Button Number	FPGA Connection
SYS_RESET_n	Global reset-resets board, loads FPGA with configuration data from MPGM(3:0) address	S8	U20.AG5
SAFE	Resets board, loads FPGA with factory default configuration data	S9	U10.117
PB0	Stratix device, user defined	S4	U20.AG8
PB1	Stratix device, user defined	S5	U20.AH2
PB2	Stratix device, user defined	S6	U20.AH1
PB_DEV_CLRn (PB3)	Stratix device clear	S7	U20.AH14

General Purpose LEDs

Yellow, surface mount LEDs (SM1206) are provided for general purpose use. The MAX 7256AE acts as a buffer between the Stratix FPGA and diodes, as the diodes have a forward voltage (V_{FD}) of 2.1 V and require a 20-mA current to output light at the recommended levels. Table 17 lists the assignment for each users LED.

- A logic 0 is driven on the I/O port to turn the LED ON.
- A logic 1 is driven on the I/O port to turn the LED OFF.

Table 17. User LED Pin out

Signal Name	Reference Description	Stratix FPGA, MAX Connection
LED0	D18	FPGA: U20.R10 MAX: U10.55 (input), U10.106 (output)
LED1	D19	FPGA: U20.R9 MAX: U10.56 (input), U10.107 (output)
LED2	D20	FPGA: U20.R5 MAX: U10.60 (input), U10.108 (output)
LED3	D21	FPGA: U20.R6 MAX: U10.61 (input), U10.109 (output)
LED4	D22	FPGA: U20.P7 MAX: U10.62 (input), U10.110 (output)
LED5	D23	FPGA: U20.P8 MAX: U10.63 (input), U10.111 (output)
LED6	D24	FPGA: U20.R7 MAX: U10.65 (input), U10.112 (output)
LED7	D25	FPGA: U20.R8

Table 17. User LED Pin out		
Signal Name	**Reference Description**	**Stratix FPGA, MAX Connection**
		MAX: U10.82 (input), U10.113 (output)

Status LEDs

Surface mount LED's (SM1206) indicate the status as shown in Table 18.

Table 18. Status LEDs			
Signal Name	**Description**	**Ref. Des.**	**LED Color**
DC_INPUT_OK	Indicates input power supply is on.	D1	Blue
FLASH_CEn	Indicates flash is enabled	D16	Yellow
USER_LEDn	User status LEDs	D12	Green
LOADING_LEDn	Indicates the Stratix configuration is loading	D13	Green
SAFE_LEDn	Indicates that the default configuration is loaded	D14	Yellow
ERROR_LEDn	Indicates a system error has occured	D15	Red
EP1S_CONF_DONEn	Indicates Stratix configuration is finished	D17	Green
3.3V_MON	Indicates 3.3V power is available on the board	D10	Green
2.6V_MON	Indicates 2.6V power is available on the board	D8	Green
1.8V_MON	Indicates 1.8V power is available on the board	D11	Green
1.5V_MON	Indicates 1.5V power is available on the board	D7	Green
RS232 Port A TX	Indicates RS232 Port A is transmitting	D2	Yellow
RS232 Port A RX	Indicates RS232 Port A is receivng	D3	Yellow
RS232 Port B TX	Indicates RS232 Port B is transmitting	D4	Yellow
RS232 Port B RX	Indicates RS232 Port B is receivng	D5	Yellow
Ethernet lLnk	Indicates that the Ethernet link is established	RJ1	Green
Ethernet Active	Indicates that data transfer is in progress	RJ1	Yellow

Seven-Segment Displays

Two single digit, seven-segment LED displays are provided for the user. Each display is controlled by the Stratix device. Each segment of the display can be illuminated by driving the connected device's I/O pin with a logic 0. Table 19 shows the display segments and assignments for the seven-segment displays through a buffer/driver.

Table 19. Stratix Seven-Segment Display Pinouts			
Display Segment	**Display Connection**	**Signal Name**	**FPGA Connection**
A_SEGA	U25.10	DIG_1_A	U20.AC5
B_SEGA	U25.9	DIG_1_B	U20.AC8

Table 19. Stratix Seven-Segment Display Pinouts			
Display Segment	**Display Connection**	**Signal Name**	**FPGA Connection**
C_SEGA	U25.8	DIG_1_C	U20.AC7
D_SEGA	U25.5	DIG_1_D	U20.AB6
E_SEGA	U25.4	DIG_1_E	U20.AB7
F_SEGA	U25.2	DIG_1_F	U20.AA7
G_SEGA	U25.3	DIG_1_G	U20.AA6
DP_SEGA	U25.7	DIG_1_DP	U20.AA8
A_SEGB	U25.10	DIG_2_A	U20.AE7
B_SEGB	U25.9	DIG_2_B	U20.AD5
C_SEGB	U25.8	DIG_2_C	U20.AD6
D_SEGB	U25.5	DIG_2_D	U20.AE5
E_SEGB	U25.4	DIG_2_E	U20.AE6
F_SEGB	U25.2	DIG_2_F	U20.AD7
G_SEGB	U25.3	DIG_2_G	U20.AD8
DP_SEGB	U25.7	DIG_2_DP	U20.AC6

10/100 Ethernet MAC/PHY Interface

The SMB1 has an external 10/100 Ethernet MAC with integrated PHY interface. The controller is a standard Microsystems LAN91C111 with support for both 10Mb and 100Mb Ethernet. SOPC Builder 2.0 and beyond provide default support for this component including a functional TCP/IP stack and device driver as well as example software for web servers and testing of the device.

The LAN91C111 requires a 25MHz clock, which will be generated by a sub-miniature surface-mount 25.000 MHz oscillator. An integrated RJ45 connector with built-in magnetics and activity/link LEDs is used along with the MAC/PHY chip. The signals listed below are relative to the LAN91C111 specification and the "TYPE" shall be considered relative to the Stratix device for the I/O setting and direction. describes the Ethernet signals and their I/O types that they use.

The signals listed in Table 20 are relative to the Stratix™ device as far as the I/O setting and direction.

Table 20. Ethernet I/O Signals			
Signal Name	**Description**	**Stratix™ Type**	**Connector**
FSE_A(15:1)	Shared Bus Address (enet)	LVTTL input	
FSE_D(31:0)	Shared Bus Data (enet)	LVTTL bidir	
ENET_BEn(3:0)	Byte Enables	LVTTL input	
ENET_ADSn	Address Strobe	LVTTL input	
ENET_AEN	Address Enable	LVTTL input	
ENET_VLBUSn	Visa-Local-Bus Mode Select	LVTTL input	
ENET_SRDYn	S-Ready	LVTTL output	
ENET_RESET	Reset	LVTTL input	
ENET_LCLK	Local Clock	LVTTL input	
ENET_IOCHRDY	IO Character Ready	LVTTL output	
ENET_RDYRTNn	Ready Return	LVTTL input	

Table 20. Ethernet I/O Signals			
Signal Name	**Description**	**Stratix™ Type**	**Connector**
ENET_INTRQ0	Interrupt Output	LVTTL output	
ENET_LDEVn	Local Device Select	LVTTL output	
ENET_IORn	Read Strobe	LVTTL input	
ENET_IOWn	Write Strobe	LVTTL input	
ENET_DATACSn	Data Chip Select	LVTTL input	
ENET_CYCLEn	Cycle Select	LVTTL input	
ENET_W_Rn	Write/Read Select	LVTTL input	
ENET_TXD_P	Transmit Data – Positive		RJ1.1
ENET_TXD_N	Transmit Data – Negative		RJ1.3
ENET_RXD_P	Receive Data – Positive		RJ1.4
ENET_RXD_N	Receive Data – Negative		RJ1.6

RS-232 Port

A dual female DB9 connector will be provided along with supporting RS-232 transceivers to implement a standard RS-232 serial UART channel in the Stratix FPGA. The DB9 is pinned out the same as a data terminal device and requires only a standard cable (no null modem required for PC interface). The two COM Ports will be known as Port A and Port B. A dedicated level-shifting buffer will be used to translate between LVTTL and RS-232 levels.

The signals listed in Table 21 are relative to the RS-232/DB-9 specification and the "FPGA Type" should be considered relative to the Stratix as far as the I/O setting and direction are concerned.

Table 21. RS-232 Connector Pinout for the Stratix Device				
Signal Name	**Description**	**FPGA Type**	**FPGA Connection**	**Connector**
RS232A_TXD	Transmit data	LVTTL output	U20.Y9	J12A
RS232A_RTS	Request to send	LVTTL output	U20.W5	J12A
RS232A_RXD	Receive data	LVTTL input	U20.W6	J12A
RS232A_CTS	Clear to send	LVTTL input	U20.Y7	J12A
RS232B_TXD	Transmit data	LVTTL output	U20.Y8	J12B
RS232B_RTS	Request to send	LVTTL output	U20.Y5	J12B
RS232B_RXD	Receive data	LVTTL input	U20.Y6	J12B
RS232B_CTS	Clear to send	LVTTL input	U20.AA9	J12B

RS-232 Connector Interface

Table 22 shows the pinouts for the RS-232 connectors on the SMB1. Since this is a dual dB9 connector each RS232 level shifter on port A and port B has the same pinout to the Stratix and the DB9 connector. In the table below the "x" is the variable that represents nets connected to port A (J12A) or port B (J12B).

Table 22. RS-232 Connector (J12A and J12B) to Stratix Device Pinout (U1 and U3)		
Signal Name Where "x" = A or B	**U1 and U3 Pin Number**	**Pin J12 Same pin for part J12A and J12B**
C1+ (0.1uF)	1	N/A
V+ (0.1uF)	2	N/A
C1- (0.1uF)	3	N/A
C2+ (0.1uF)	4	N/A
C2- (0.1uF)	5	N/A
V- (0.1uF)	6	N/A
RS232x1_CTS	7	8
RS232x1_RTS	8	7
RS232x_RTS	9	N/A
RS232x_CTS	10	N/A
RS232x_TXD	11	N/A
RS232x_RXD	12	N/A
RS232x1_RXD	13	3
RS232x1_TXD	14	2
GND	15	N/A
VCC (3.3V, 0.1uF)	16	N/A

Debug Proto Connectors

The evaluation board possesses various connectors for debug use. There is one Agilent E5387A logic analyzer probe (J24), and two Tektronix P6860 logic analyzer probe connectors, (J33, J38) which are not installed on the board until required. In addition, there are three Samtec connectors used to connect to the Santa Cruz board (J32, J31, and J37).

There will be a single debug port on the Stratix that provides access to several different debug connectors used by popular logic analyzers from Agilent and Tektronix. The three interfaces will be bussed together to conserve I/O resources. The soft-touch probes from both Agilent and Tektronix are connector-less so that they do not require board-level components. This reduces both cost and signal integrity issues. The typical loading for these technologies is less than 1pF when installed. The speed of this debug port is limited only by the I/O standard limitations of the FPGA and the amount of capacitance being driven. Though impractical, the use of both soft-touch debug probes simultaneously results in only 2pF above the capacitance of the traces themselves.

Daughter cards may vary in loading and function so they may need to be un-plugged for attaining the highest speeds (LVTTL runs around 250MHz) or for use at all for general debug. A diagram helping to illustrate the route-through concept is shown in Figure 14.

Figure 14. Debug Proto Header Connections

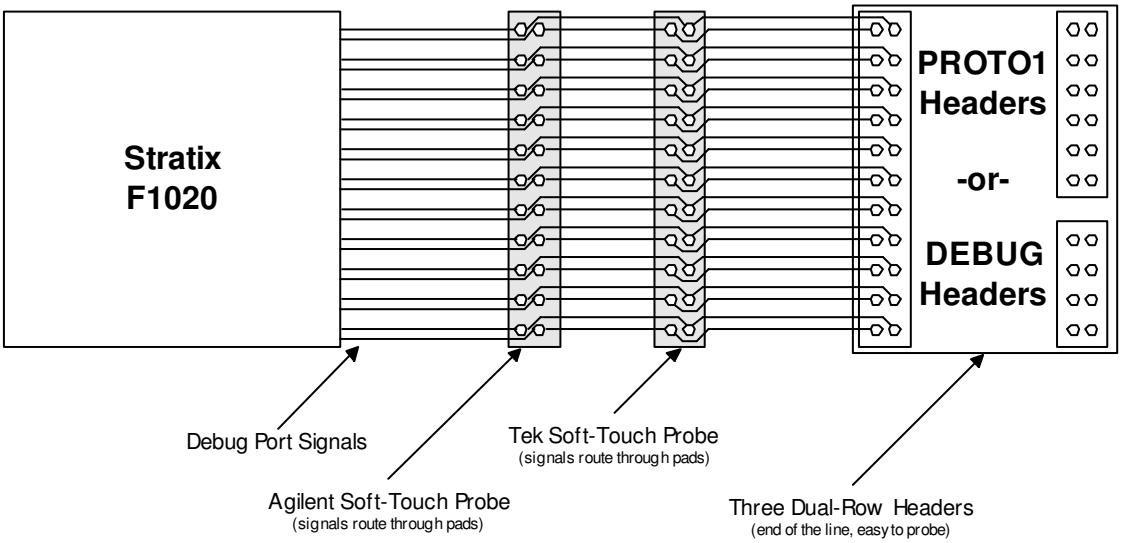


Table 23 lists the signals provided to these connectors.

Table 23. Debug Proto Header Connectors

Signal Name	Stratix (U20)	Agilent Logic Analyzer Connector (J34)	Tektronix Logic Analyzer Connectors (J33, J38)	Santa Cruz Connectors (J32, J31, J37)
PROTO1_IO0	AG3	B1	J33.A1	J37.3
PROTO1_IO1	AG4	A1	J33.A3	J37.4
PROTO1_IO2	AG2	B2	J33.B1	J37.5
PROTO1_IO3	AG1	A2	J33.B3	J37.6
PROTO1_IO4	AF3	B4	J33.A4	J37.7
PROTO1_IO5	AF4	A4	J33.A6	J37.8
PROTO1_IO6	AF1	B5	J33.B4	J37.9
PROTO1_IO7	AF2	A5	J33.B6	J37.10
PROTO1_IO8	AE3	B7	J33.A7	J37.11
PROTO1_IO9	AE4	A7	J33.A9	J37.12
PROTO1_IO10	AE1	B8	J33.B7	J37.13
PROTO1_IO11	AE2	A8	J33.B9	J37.14
PROTO1_IO12	AC4	B10	J33.A10	J37.15
PROTO1_IO13	AC3	A10	J33.A12	J37.16
PROTO1_IO14	AD4	B11	J33.B10	J37.17
PROTO1_IO15	AD3	A11	J33.B12	J37.18
PROTO1_IO16	AD1	A13	J33.A13	J37.21
PROTO1_IO17	AD2	B13	J33.A15	J37.23
PROTO1_IO18	AB1	B15	J38.A1	J37.25
PROTO1_IO19	AC2	A15	J38.A3	J37.27
PROTO1_IO20	AA5	B16	J38.B1	J37.28

Table 23. Debug Proto Header Connectors				
Signal Name	**Stratix (U20)**	**Agilent Logic Analyzer Connector (J34)**	**Tektronix Logic Analyzer Connectors (J33, J38)**	**Santa Cruz Connectors (J32, J31, J37)**
PROTO1_IO21	AA4	A16	J38.B3	J37.29
PROTO1_IO22	AB2	B18	J38.A4	J37.31
PROTO1_IO23	AB3	A18	J38.A6	J37.32
PROTO1_IO24	AA2	B19	J38.B4	J37.33
PROTO1_IO25	AA3	A19	J38.B6	J37.35
PROTO1_IO26	Y3	B21	J38.A7	J37.36
PROTO1_IO27	Y4	A21	J38.A9	J37.37
PROTO1_IO28	Y1	B22	J38.B7	J37.39
PROTO1_IO29	Y2	A22	J38.B9	J32.4
PROTO1_IO30	W3	B24	J38.A10	J32.5
PROTO1_IO31	W4	A24	J38.A12	J32.6
PROTO1_IO32	W1	B25	J38.B10	J32.7
PROTO1_IO33	W2	A25	J38.B12	J32.8
PROTO1_IO34	V3	A27	J38.A13	J32.9
PROTO1_IO35	V4	B27	J38.A15	J32.10
PROTO1_IO36	V1	NA	NA	J32.11
PROTO1_IO37	V2	NA	NA	J32.12
PROTO1_IO38	U6	NA	NA	J32.13
PROTO1_IO39	U5	NA	NA	J32.14
PROTO1_IO40	AE8	NA	NA	J32.3
SCRUZ_CLK_OSC_A	NA	NA	NA	J31.9
CLK_TO_CRUZ	AL18	NA	NA	J31.11
CLK_FROM_CRUZ	AB5	NA	NA	J31.13
CRUZ_CARDSELn	R11	NA	NA	J37.38

ByteBlaster II Cable Connector Interface

Table 24 shows the pinouts for the ByteBlaster II cable connectors on the SMB1 Development Board.

Table 24. ByteBlaster II Pinout for JTAG Header	
Signal Name	**Pin Number**
JTAG_TCK	J27.1
GND	J27.2
JTAG_CONN_TDI	J27.3
3.3V	J27.4
JTAG_TMS	J27.5
3.3V	J27.6
NC	J27.7, J27.8
JTAG_CONN_TDO	J27.9

GND	J27.10

Memory Interfaces

Shared Bus Interface

SMB1 will employ the same shared-bus architecture as found on the NIOS Boards made for Stratix and Cyclone. This allows for a 3X reduction in pins for asynchronous peripherals and memories. This bus shares address and data for the following components:

- Flash
- SRAM
- LAN91C111 Ethernet MAC/PHY

The signals for the shared bus are listed in Table 25.

Flash Interface

The 128Mb AMD Uniform Sector Flash Memory device (AM29LV128MH113RE) will be the non-volatile memory for this board. SMB1 will have a footprint for an AMD Flash device that supports CFI programming algorithms and has a common TSOP-56 pinout that is expandable from 8MB up to 128MB in a single package.

This device also offers the BYTEn signal that allows addressing in either byte or word mode. This feature allows for use as a configuration memory with a direct 8-bit link to the Stratix configuration pins and then a word interface for faster/wider data reads when configuration is complete. This flash qualifies as part of the "Shared Bus" circuit. This is part of a requirement for memories from the "NIOS Stamp" that increases this board's ability to run some of the same or similar reference designs.

SRAM Interface

SMB1 will have two 256K x16 SRAM devices as part of the "Shared Bus." These devices are wired in parallel to provide a 256K x32 interface to the Stratix (1MB contiguous space).

Flash, SRAM, Ethernet Shared Bus Pinout

Table 25 shows the pinouts for the flash, SRAM memory and Ethernet connections to the Stratix FPGA on the SMB1 Development Board.

Table 25. Flash, SRAM, Ethernet Shared Bus Pinout

Signal Name	Stratix Pin Number (U20)	Flash Pin Number (U19)	SRAM Pin Number (U2,U30)	Etnernet Pin Number (U6)
FSE_A0	F5	51	1	78
FSE_A1	E4	31	2	79
FSE_A2	E2	26	3	80
FSE_A3	E1	25	4	81

Table 25. Flash, SRAM, Ethernet Shared Bus Pinout				
Signal Name	**Stratix Pin Number (U20)**	**Flash Pin Number (U19)**	**SRAM Pin Number (U2,U30)**	**Etnernet Pin Number (U6)**
FSE_A4	F3	24	5	82
FSE_A5	F4	23	18	83
FSE_A6	G3	22	19	84
FSE_A7	G4	21	20	85
FSE_A8	F1	20	21	86
FSE_A9	F2	10	22	87
FSE_A10	H3	9	23	88
FSE_A11	H4	8	24	89
FSE_A12	G1	7	25	90
FSE_A13	G2	6	26	91
FSE_A14	H1	5	27	92
FSE_A15	H2	4	42	
FSE_A16	J3	3	43	
FSE_A17	J4	54	44	
FSE_A18	K4	19		
FSE_A19	K3	18		
FSE_A20	J2	11		
FSE_A21	J1	12		
FSE_A22	L1	15		
FSE_A23	K2	2		
FSE_A24	M4	1		
FSE_A25	M5	56		
FSE_A26	L2	55		
FSE_D0	G7	35	U2.7	107
FSE_D1	G8	37	U2.8	106
FSE_D2	G6	39	U2.9	105
FSE_D3	G5	41	U2.10	104
FSE_D4	H8	44	U2.13	102
FSE_D5	H7	46	U2.14	101
FSE_D6	H5	48	U2.15	100
FSE_D7	H6	50	U2.16	99
FSE_D8	J7		U2.29	76
FSE_D9	J8		U2.30	75
FSE_D10	J5		U2.31	74
FSE_D11	J6		U2.32	73
FSE_D12	K8		U2.35	71
FSE_D13	K7		U2.36	70
FSE_D14	K5		U2.37	69
FSE_D15	K6		U2.38	68
FSE_D16	L6		U30.7	66
FSE_D17	L7		U30.8	65

Table 25. Flash, SRAM, Ethernet Shared Bus Pinout				
Signal Name	**Stratix Pin Number (U20)**	**Flash Pin Number (U19)**	**SRAM Pin Number (U2,U30)**	**Etnernet Pin Number (U6)**
FSE_D18	M6		U30.9	64
FSE_D19	M7		U30.10	63
FSE_D20	M8		U30.13	61
FSE_D21	M9		U30.14	60
FSE_D22	N10		U30.15	59
FSE_D23	N9		U30.16	58
FSE_D24	N5		U30.29	56
FSE_D25	N6		U30.30	55
FSE_D26	P9		U30.31	54
FSE_D27	P10		U30.32	53
FSE_D28	N7		U30.35	51
FSE_D29	N8		U30.36	50
FSE_D30	P6		U30.37	49
FSE_D31	P5		U30.38	48
FLASH_CEN	M3	32		
FLASH_OEN	N3	34		
FLASH _WEN	N4	13		
GND				
FLASH _RDY_BSYn	N1	17		
FLASH_RESETn	L3	14		
FLASH_BYTEn	U10.23	53		
FLASH_WPn		16		

DDR-I SDRAM Device Memory Interface

The SMB1 contains four DDR-I x16 SDRAM devices (part number Micron MT46V16M16TG-5B or Samsung K4H561638F-TCCC) connected to the Stratix side banks (banks 1 and 2) that support 150 MHz double data rate (DDR). It has 4 Meg x 16 x 4 banks and is available in a 66-pin TSOP (400 mil width, 0.65mm pin pitch) package.

The I/O standard for the DDR-I x16 SDRAM is 2.5V SSTL_2 Class II. This requires SSTL2 VTT (1.25V center-rail voltage termination) on each line. Refer to the SMB1 Memory Termination Specification for the DDR-I termination scheme.

This termination scheme allows for all types of characterization for the DDR-I devices in the side banks. By removing resistors or exchanging them for zero ohm values all SSTL_2 class terminations can be tested to find the optimum configuration for DDR-I.

The Stratix device controls all of the signals that are routed to the DDR device through the DDR SDRAM controller core.

DDR-I Device Memory Pinout

Table 26 shows the pinout for each of the four DDR-I Devices on the SMB1 to the Stratix device.

Table 26. DDR-I (A - D) Pin Out

		DDR-I Devices A - D				
Signal Name	**Shared Pins**	**Device A**	**Device B**	**Device C**	**Device D**	**Stratix Pin Number**
ddra_a[0]	29					V29
ddra_a[1]	30					V30
ddra_a[2]	31					V31
ddra_a[3]	32					V32
ddra_a[4]	35					T32
ddra_a[5]	36					R32
ddra_a[6]	37					T31
ddra_a[7]	38					R31
ddra_a[8]	39					R30
ddra_a[9]	40					T28
ddra_a[10]	28					V28
ddra_a[11]	41					R29
ddra_a[12]	42					R28
ddra_ba[0]	26					U27
ddra_ba[1]	27					U28
ddra_casn	22					V27
ddra_ck_n	46					M28
ddra_ck_p	45					N27
ddra_cke		44				G32
ddra_csn		24				K31
ddra_dq[0]		2				H31
ddra_dq[1]		4				J28
ddra_dq[2]		5				J30
ddra_dq[3]		7				J29
ddra_dq[4]		8				H30
ddra_dq[5]		10				H29
ddra_dq[6]		11				H28
ddra_dq[7]		13				J31
ddra_dq[8]		54				F32
ddra_dq[9]		56				E32
ddra_dq[10]		57				F29
ddra_dq[11]		59				E31
ddra_dq[12]		60				F30
ddra_dq[13]		62				F31
ddra_dq[14]		63				E29
ddra_dq[15]		65				F28
ddra_ldm		20				J32
ddra_ldqs		16				H32
ddra_rasn	23					W26
ddra_udm		47				G31
ddra_udqs		51				G30

Table 26. DDR-I (A - D) Pin Out						
		DDR-I Devices A - D				
Signal Name	Shared Pins	Device A	Device B	Device C	Device D	Stratix Pin Number
ddra_wen	21					V26
ddrb_cke			44			M31
ddrb_csn			24			P32
ddrb_dq[0]			2			N28
ddrb_dq[1]			4			N29
ddrb_dq[2]			5			N30
ddrb_dq[3]			7			N31
ddrb_dq[4]			8			P27
ddrb_dq[5]			10			P28
ddrb_dq[6]			11			P29
ddrb_dq[7]			13			P30
ddrb_dq[8]			54			L32
ddrb_dq[9]			56			L31
ddrb_dq[10]			57			L30
ddrb_dq[11]			59			K30
ddrb_dq[12]			60			K29
ddrb_dq[13]			62			K28
ddrb_dq[14]			63			L27
ddrb_dq[15]			65			K27
ddrb_ldm			20			N32
ddrb_ldqs			16			P31
ddrb_udm			47			M30
ddrb_udqs			51			M29
ddrc_cke				44		Y32
ddrc_csn				24		AA31
ddrc_dq[0]				2		AC27
ddrc_dq[1]				4		AB27
ddrc_dq[2]				5		AC28
ddrc_dq[3]				7		AC31
ddrc_dq[4]				8		AA28
ddrc_dq[5]				10		AB30
ddrc_dq[6]				11		AB31
ddrc_dq[7]				13		AB32
ddrc_dq[8]				54		Y31
ddrc_dq[9]				56		Y30
ddrc_dq[10]				57		Y29
ddrc_dq[11]				59		Y28
ddrc_dq[12]				60		W30
ddrc_dq[13]				62		W29
ddrc_dq[14]				63		W28
ddrc_dq[15]				65		W27
ddrc_ldm				20		AA30
ddrc_ldqs				16		AA29
ddrc_udm				47		W32
ddrc_udqs				51		W31

Table 26. DDR-I (A - D) Pin Out						
		DDR-I Devices A - D				
Signal Name	Shared Pins	Device A	Device B	Device C	Device D	Stratix Pin Number
ddrd_cke					44	AE27
ddrd_csn					24	AH32
ddrd_dq[0]					2	AF32
ddrd_dq[1]					4	AG32
ddrd_dq[2]					5	AG31
ddrd_dq[3]					7	AF31
ddrd_dq[4]					8	AF30
ddrd_dq[5]					10	AG29
ddrd_dq[6]					11	AF29
ddrd_dq[7]					13	AF28
ddrd_dq[8]					54	AD32
ddrd_dq[9]					56	AE32
ddrd_dq[10]					57	AE31
ddrd_dq[11]					59	AD31
ddrd_dq[12]					60	AD30
ddrd_dq[13]					62	AD29
ddrd_dq[14]					63	AE29
ddrd_dq[15]					65	AE28
ddrd_ldm					20	AG28
ddrd_ldqs					16	AG30
ddrd_udm					47	AD28
ddrd_udqs					51	AE30
vref	49					
vss	34,48,66					
vssq	6,12,52,58,64					
vdd	1,18,33					
vddq	3,9,15,55,61					
nc	14,17,25,43,53					

DDR-I DIMM Memory Interface

The DDR-I module (DIMM) (part number Micron MT9VDDT3272AG-40B or Samsung M381L3223ETM-CCC), connected to banks 7 and 8 of the Stratix device, support 200 MHz double data rate (DDR). It is a 32 Meg x 72 (256MB) and is available in a 184-pin DIMM package.

Like the DDR-I x16 SDRAM the I/O standard for the DDR-I module is 2.5V SSTL_2 Class II. Its termination scheme is the same as well.

DDR-I DIMM Memory Connector Pinout

Table 27 shows the pinouts for the DDR-I DIMM connector on the SMB1 to the Stratix device.

Table 27. DDR-i DIMM Pinout		
Signal Name	**Pin Number (U27)**	**Stratix Pin Number (U20)**
DDRE_CK_P0	137	AM13
DDRE_CK_N0	138	AM14
DDRE_CK_P1	16	AK12
DDRE_CK_N1	17	AL12
DDRE_CK_P2	76	AL13
DDRE_CK_N2	75	AL14
DDRE_CKE	21	AF11
DDRE_CKE1	111	AE10
DDRE_WEn	63	AE23
DDRE_CASn	65	AE24
DDRE_RASn	154	AF23
DDRE_CSn0	157	AF24
DDRE_CSn1	158	AA13
DDRE_CSn2	71	AB12
DDRE_CSn3	163	AB14
DDRE_BA0	59	AF22
DDRE_BA1	52	AE22
DDRE_BA2	113	AJ12
DDRE_A0	48	AK14
DDRE_A1	43	AE14
DDRE_A2	41	AD14
DDRE_A3	130	AK13
DDRE_A4	37	AJ13
DDRE_A5	32	AG13
DDRE_A6	125	AH13
DDRE_A7	29	AE13
DDRE_A8	122	AF13
DDRE_A9	27	AF12
DDRE_A10	141	AJ15
DDRE_A11	118	AD12
DDRE_A12	115	AD11
DDRE_A13		AC13
DDRE_DQS0	5	AK5
DDRE_DQS1	14	AH7
DDRE_DQS2	25	AK8
DDRE_DQS3	36	AJ11
DDRE_DQS4	56	AJ22
DDRE_DQS5	67	AL26
DDRE_DQS6	78	AL27
DDRE_DQS7	86	AK28
DDRE_DQS8	47	AJ20

Table 27. DDR-i DIMM Pinout		
Signal Name	**Pin Number (U27)**	**Stratix Pin Number (U20)**
DDRE_DM0	97	AG9
DDRE_DM1	107	AG10
DDRE_DM2	119	AF10
DDRE_DM3	129	AM11
DDRE_DM4	149	AG21
DDRE_DM5	159	AG22
DDRE_DM6	169	AG23
DDRE_DM7	177	AG24
DDRE_DM8	140	AG20
DDRE_DQ0	2	AK4
DDRE_DQ1	4	AK3
DDRE_DQ2	6	AH5
DDRE_DQ3	8	AJ5
DDRE_DQ4	94	AJ4
DDRE_DQ5	95	AM4
DDRE_DQ6	98	AL4
DDRE_DQ7	99	AL3
DDRE_DQ8	12	AJ6
DDRE_DQ9	13	AK6
DDRE_DQ10	19	AL5
DDRE_DQ11	20	AK7
DDRE_DQ12	105	AM5
DDRE_DQ13	106	AJ7
DDRE_DQ14	109	AM6
DDRE_DQ15	110	AL6
DDRE_DQ16	23	AL7
DDRE_DQ17	24	AJ8
DDRE_DQ18	28	AM7
DDRE_DQ19	31	AH9
DDRE_DQ20	114	AM8
DDRE_DQ21	117	AK9
DDRE_DQ22	121	AJ9
DDRE_DQ23	123	AL8
DDRE_DQ24	33	AH11
DDRE_DQ25	35	AJ10
DDRE_DQ26	39	AL9
DDRE_DQ27	40	AM9
DDRE_DQ28	126	AK10
DDRE_DQ29	127	AL11
DDRE_DQ30	131	AK11
DDRE_DQ31	133	AL10

Table 27. DDR-i DIMM Pinout		
Signal Name	**Pin Number (U27)**	**Stratix Pin Number (U20)**
DDRE_DQ32	53	AL22
DDRE_DQ33	55	AK22
DDRE_DQ34	57	AL23
DDRE_DQ35	60	AK23
DDRE_DQ36	146	AM24
DDRE_DQ37	147	AH22
DDRE_DQ38	150	AL24
DDRE_DQ39	151	AJ23
DDRE_DQ40	61	AM26
DDRE_DQ41	64	AM25
DDRE_DQ42	68	AK24
DDRE_DQ43	69	AL25
DDRE_DQ44	153	AK25
DDRE_DQ45	155	AJ25
DDRE_DQ46	161	AJ24
DDRE_DQ47	162	AH24
DDRE_DQ48	72	AK26
DDRE_DQ49	73	AM28
DDRE_DQ50	79	AM27
DDRE_DQ51	80	AJ26
DDRE_DQ52	165	AK27
DDRE_DQ53	166	AL28
DDRE_DQ54	170	AJ27
DDRE_DQ55	171	AH26
DDRE_DQ56	83	AM29
DDRE_DQ57	84	AL29
DDRE_DQ58	87	AL30
DDRE_DQ59	88	AK29
DDRE_DQ60	174	AJ29
DDRE_DQ61	175	AJ28
DDRE_DQ62	178	AK30
DDRE_DQ63	179	AH28
DDRE_CB0	44	AM20
DDRE_CB1	45	AL20
DDRE_CB2	49	AK20
DDRE_CB3	51	AH20
DDRE_CB4	134	AL21
DDRE_CB5	135	AK21
DDRE_CB6	142	AJ21
DDRE_CB7	144	AM22
DDRE_SA0	181	N/A

Table 27. DDR-i DIMM Pinout		
Signal Name	**Pin Number (U27)**	**Stratix Pin Number (U20)**
DDRE_SA1	182	N/A
DDRE_SA2	183	N/A
DDRE_WP	90	N/A
DDRE_SCL	91	AE21
DDRE_SDA	92	AD21
VREF	1	N/A
NC	158	N/A
NC	71	N/A
NC	163	N/A
NC	167	N/A
NC	9	N/A
NC	10	N/A
NC	101	N/A
NC	102	N/A
NC	173	N/A
NC	103	N/A
VDD (2.6V_VDD)	7	N/A
VDD (2.6V_VDD)	38	N/A
VDD (2.6V_VDD)	46	N/A
VDD (2.6V_VDD)	70	N/A
VDD (2.6V_VDD)	85	N/A
VDD (2.6V_VDD)	108	N/A
VDD (2.6V_VDD)	120	N/A
VDD (2.6V_VDD)	148	N/A
VDD (2.6V_VDD)	168	N/A
VDDQ (2.6V_TERM)	15	N/A
VDDQ (2.6V_TERM)	22	N/A
VDDQ (2.6V_TERM)	30	N/A
VDDQ (2.6V_TERM)	54	N/A
VDDQ (2.6V_TERM)	62	N/A
VDDQ (2.6V_TERM)	77	N/A
VDDQ (2.6V_TERM)	96	N/A
VDDQ (2.6V_TERM)	104	N/A
VDDQ (2.6V_TERM)	112	N/A
VDDQ (2.6V_TERM)	128	N/A
VDDQ (2.6V_TERM)	136	N/A
VDDQ (2.6V_TERM)	143	N/A
VDDQ (2.6V_TERM)	156	N/A
VDDQ (2.6V_TERM)	164	N/A
VDDQ (2.6V_TERM)	172	N/A
VDDQ (2.6V_TERM)	180	N/A

Table 27. DDR-i DIMM Pinout		
Signal Name	**Pin Number (U27)**	**Stratix Pin Number (U20)**
VDDSPD	184	N/A
VDDID	82	N/A
VSS	3	N/A
VSS	11	N/A
VSS	18	N/A
VSS	26	N/A
VSS	34	N/A
VSS	42	N/A
VSS	50	N/A
VSS	58	N/A
VSS	66	N/A
VSS	74	N/A
VSS	81	N/A
VSS	89	N/A
VSS	93	N/A
VSS	100	N/A
VSS	116	N/A
VSS	124	N/A
VSS	132	N/A
VSS	139	N/A
VSS	145	N/A
VSS	152	N/A
VSS	160	N/A
VSS	176	N/A
DDRE_DLL_CLK_OUT	N/A	AJ19
DDRE_DLL_CLK_IN	N/A	AK19
DDRE_SMA_DLL_CLK	N/A	AM15
DDRE_FBCLK	N/A	AB28
DDRE_FBCLK_OUT	N/A	AL15

RLDRAM-II Separate Input/Output (SIO) Interface

The SMB1 contains one RLDRAM-II SIO x18 device (part number Micron MT49H16M18CFM-2.5) connected to bank 3 of the Stratix device and supports 400 MHz double data rate (DDR). The RLDRAM SIO device is in a 16 Meg x 18 configuration and is available in a 144-ball FBGA (11mm x 18.5mm) package.

The I/O standard for the RLDRAM-II SIO x18 is 1.8V HSTL1. (1.5V HSTL1 will also be possible by changing the adjustable voltage regulator resistors). This requires HSTL1 VTT (0.9V center-rail Voltage termination) on each line. Refer to the SMB1 Memory Termination Specification for the RLDRAM-II termination scheme.

This termination scheme allows for all types of characterization for the RLDRAM-II SIO device on the top bank of the Stratix device. By removing resistors or exchanging them for zero ohm values all HSTL class terminations can be tested to find the optimum configuration for RLDRAM-II SIO.

The Stratix device controls all of the signals that are routed to the RLDRAM-II SIO x18 device through the RLDRAM-II controller core. Table 28 shows the pinouts for the RLDRAM-II SIO connections to the Stratix device.

RLDRAM-II Separate Input/Output (SIO) Pinout

Table 28. RLDRAM-II SIO Pin Out

Signal Name	RLDRAM-II SIO Pins Number	Stratix Pin Number
rlds_a[0]	G12	D19
rlds_a[1]	G11	F19
rlds_a[2]	G10	G20
rlds_a[3]	H12	B20
rlds_a[4]	H11	C20
rlds_a[5]	E1	L18
rlds_a[6]	G2	K20
rlds_a[7]	G3	H20
rlds_a[8]	G1	L19
rlds_a[9]	H2	J21
rlds_a[10]	M12	F21
rlds_a[11]	M11	F22
rlds_a[12]	M12	G22
rlds_a[13]	L12	C21
rlds_a[14]	L11	D21
rlds_a[15]	P1	L24
rlds_a[16]	M2	K22
rlds_a[17]	M3	J22
rlds_a[18]	N1	L23
rlds_a[19]	N12	G23
rlds_a[20]	E12	A20
rlds_a[21]	E1	K18
rlds_a[22]	D1	H19
rlds_ba[0]	J11	E20
rlds_ba[1]	K11	F20
rlds_ba[2]	H1	L20
rlds_ck_n	K12	A18
rlds_ck_p	J12	B18
rlds_csn	L2	K21
rlds_d[0]	B11	D24
rlds_d[1]	C11	A25
rlds_d[2]	E11	C24
rlds_d[3]	F11	B25
rlds_d[4]	B2	C25
rlds_d[5]	C2	D25
rlds_d[6]	D2	A26
rlds_d[7]	E2	E24
rlds_d[8]	F2	F23

Table 28. RLDRAM-II SIO Pin Out		
Signal Name	**RLDRAM-II SIO Pins Number**	**Stratix Pin Number**
rlds_d[9]	N11	C26
rlds_d[10]	P11	A28
rlds_d[11]	R11	A27
rlds_d[12]	T11	D26
rlds_d[13]	U11	C27
rlds_d[14]	N2	B28
rlds_d[15]	P2	D27
rlds_d[16]	T2	B26
rlds_d[17]	U2	F24
rlds_dm	P12	G24
rlds_q[0]	B10	B22
rlds_q[1]	C10	C22
rlds_q[2]	E10	B23
rlds_q[3]	F10	C23
rlds_q[4]	B3	A24
rlds_q[5]	C3	E22
rlds_q[6]	D3	B24
rlds_q[7]	E3	D23
rlds_q[8]	F3	A22
rlds_q[9]	N10	A29
rlds_q[10]	P10	B29
rlds_q[11]	R10	B30
rlds_q[12]	T10	C29
rlds_q[13]	U10	D29
rlds_q[14]	N3	D28
rlds_q[15]	P3	C30
rlds_q[16]	T3	E28
rlds_q[17]	U3	E26
rlds_qk_n[0]	D10	D20
rlds_qk_n[1]	R3	C28
rlds_qk_p[0]	D11	D22
rlds_qk_p[1]	R2	B27
rlds_qvld	F12	B21
rlds_refn	L1	L21
rlds_wen	M1	L22
vss	A2,A4,A9,D12,H3,H4, H9,H10,L3,L4,L9,L10, R1,R12,V4,V9	
vssq	B4,B9,D4,D9,F4,F9,N4, N9,R4,R9,U4,U9	
vdd	B1,B12,G4,G9,J3,J4,J9, J10,K3,K4,K9,K10,M4, M9,U1,U12	
vddq	C4,C9,E4,E9,P4,P9,T4,T9	
vtt	C1,C12,T1,T12	
vext	A3,A10,V3,V10	

Table 28. RLDRAM-II SIO Pin Out		
Signal Name	RLDRAM-II SIO Pins Number	Stratix Pin Number
dnu	B11,C11,E11,F11,B2,C2, D2,E2,F2,N11,P11,R11, T11,U11,N2,P2,T2,U2	
zq	V2	
tms	A11	
tck	A12	
tdo	V11	
tdi	V12	

RLDRAM-II Combined Input/Output (CIO) Interface

The SMB1 contains two RLDRAM-II CIO x16 devices (part number Micron MT49H16M18FM-2.5) connected to bank 4 of the Stratix device and supports 400 MHz double data rate (DDR). The RLDRAM CIO device is in a 16 Meg x18 configuration and is available in a 144-ball FBGA (11mm x 18.5mm) package. Although the SMB1 is using the RLDRAM-II CIO x18 device, two pins per device will not be used (hence x16), so that these interfaces will fit into one bank.

Like the RLDRAM-II SIO x18 the I/O standard for the RLDRAM-II CIO x16 is 1.8V HSTL1. (1.5V HSTL1 will also be possible by changing the adjustable voltage regulator resistors). The termination scheme is the same for RLDRAM-II SIO as well.

Table 29 shows the pinouts for the RLDRAM-II CIO connections to the Stratix device.

RLDRAM-II Combined Input/Output (CIO) Pinout

Table 29. RLDRAM-II CIO Pin Out				
Signal Name	CIO Shared Pins Number	CIO 1 Pin Number	CIO 2 Pin Number	Stratix Pin Number
rldc_a[0]	G12			B12
rldc_a[1]	G11			C12
rldc_a[2]	G10			D12
rldc_a[3]	H12			A13
rldc_a[4]	H11			B13
rldc_a[5]	E1			K11
rldc_a[6]	G2			H11
rldc_a[7]	G3			H12
rldc_a[8]	G1			K12
rldc_a[9]	H2			F12
rldc_a[10]	M12			C14
rldc_a[11]	M11			E13
rldc_a[12]	M12			F13
rldc_a[13]	L12			A14
rldc_a[14]	L11			B14
rldc_a[15]	P1			J15
rldc_a[16]	M2			J14
rldc_a[17]	M3			H14

Table 29. RLDRAM-II CIO Pin Out				
Signal Name	CIO Shared Pins Number	CIO 1 Pin Number	CIO 2 Pin Number	Stratix Pin Number
rldc_a[18]	N1			K15
rldc_a[19]	N12			C15
rldc_a[20]	E12			A11
rldc_a[21]	E1			K10
rldc_a[22]	D1			K9
rldc_ba[0]	J11			C13
rldc_ba[1]	K11			D13
rldc_ba[2]	H1			G13
rldc_ck_out				F11
rldc_csn		L2		H13
rldc_dm		P12		F8
rldc_dq[0]		B10		D5
rldc_dq[1]		C10		C3
rldc_dq[2]		E10		E5
rldc_dq[3]		F10		C4
rldc_dq[4]		B3		D4
rldc_dq[5]		C3		A4
rldc_dq[6]		D3		B4
rldc_dq[7]		E3		B3
rldc_dq[8]		N10		D6
rldc_dq[9]		P10		C6
rldc_dq[10]		R10		B5
rldc_dq[11]		T10		C7
rldc_dq[12]		U10		A5
rldc_dq[13]		N3		D7
rldc_dq[14]		P3		A6
rldc_dq[15]		T3		B6
rldc_qk_p[0]		D11		C5
rldc_qk_p[1]		R2		E7
rldc_qk_n[0]		D10		
rldc_qk_n[1]		R3		
rldc_ck_p		J12		
rldc_ck_n		K12		
rldc_dk_p		K1		
rldc_dk_n		K2		
rldc_qvld		F12		F7
rldc_refclk_n				A17
rldc_refclk_p				B17
rldc_refn	L1			K13
rldc_wen	M1			K14
rldc2_csn			L2	J13
rldc2_dm			P12	F10
rldc2_dq[0]			B10	B7
rldc2_dq[1]			C10	D8
rldc2_dq[2]			E10	B8
rldc2_dq[3]			F10	E9

Table 29. RLDRAM-II CIO Pin Out				
Signal Name	CIO Shared Pins Number	CIO 1 Pin Number	CIO 2 Pin Number	Stratix Pin Number
rldc2_dq[4]			B3	A8
rldc2_dq[5]			C3	C9
rldc2_dq[6]			D3	C8
rldc2_dq[7]			E3	D9
rldc2_dq[8]			N10	E11
rldc2_dq[9]			P10	B9
rldc2_dq[10]			R10	D10
rldc2_dq[11]			T10	C10
rldc2_dq[12]			U10	A9
rldc2_dq[13]			N3	B11
rldc2_dq[14]			P3	C11
rldc2_dq[15]			T3	B10
rldc2_ck_p			J12	
rldc2_ck_n			K12	
rldc2_dk_p			K1	
rldc2_dk_n			K2	
rldc2_qk_p[0]			D11	A7
rldc2_qk_p[1]			R2	D11
rldc2_qk_n[0]			D10	
rldc2_qk_n[1]			R3	
rldc2_qvld			F12	F9
vss	A2,A4,A9,D12,H3,H4, H9,H10,L3,L4,L9,L10, R1,R12,V4,V9			
vssq	B4,B9,D4,D9,F4,F9,N4, N9,R4,R9,U4,U9			
vdd	B1,B12,G4,G9,J3,J4,J9, J10,K3,K4,K9,K10,M4, M9,U1,U12			
vddq	C4,C9,E4,E9,P4,P9,T4,T9			
vtt	C1,C12,T1,T12			
vext	A3,A10,V3,V10			
dnu	B11,C11,E11,F11,B2,C2, D2,E2,F2,N11,P11,R11, T11,U11,N2,P2,T2,U2			
zq	V2			
tms	A11			
tck	A12			
tdo	V11			
tdi	V12			

Stratix Pinout

Table 30 shows the Stratix device pinouts alphabetical by both signal name and pin number.

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
1.5v_int	AD16		A2	gnd
1.5v_int	AF16		A3	vcc_s_io
1.5v_int	AJ3		A4	rldc_dq[5]
1.5v_int	AJ30		A5	rldc_dq[12]
1.5v_int	D3		A6	rldc_dq[14]
1.5v_int	D30		A7	rldc2_qk_p[0]
1.5v_int	H16		A8	rldc2_dq[4]
1.5v_int	J16		A9	rldc2_dq[12]
1.5v_int	M12		A10	gnd
1.5v_int	M14		A11	rldc_a[20]
1.5v_int	M19		A12	vcc_s_io
1.5v_int	M21		A13	rldc_a[3]
1.5v_int	N13		A14	rldc_a[13]
1.5v_int	N15		A15	nc
1.5v_int	N18		A16	rld_fbclk_n_out
1.5v_int	N20		A17	rldc_refclk_n
1.5v_int	P12		A18	rlds_ck_n
1.5v_int	P14		A19	rld_dll_clk_in
1.5v_int	P16		A20	rlds_a[20]
1.5v_int	P17		A21	vcc_s_io
1.5v_int	P19		A22	rlds_q[8]
1.5v_int	P21		A23	gnd
1.5v_int	R13		A24	rlds_q[4]
1.5v_int	R15		A25	rlds_d[1]
1.5v_int	R18		A26	rlds_d[6]
1.5v_int	R20		A27	rlds_d[11]
1.5v_int	R22		A28	rlds_d[10]
1.5v_int	T14		A29	rlds_q[9]
1.5v_int	T16		A30	vcc_s_io
1.5v_int	T17		A31	gnd
1.5v_int	T19		B1	gnd
1.5v_int	T9		B2	gnd
1.5v_int	U14		B3	rldc_dq[7]
1.5v_int	U16		B4	rldc_dq[6]
1.5v_int	U17		B5	rldc_dq[10]
1.5v_int	U19		B6	rldc_dq[15]
1.5v_int	U24		B7	rldc2_dq[0]
1.5v_int	V11		B8	rldc2_dq[2]
1.5v_int	V13		B9	rldc2_dq[9]
1.5v_int	V15		B10	rldc2_dq[15]
1.5v_int	V18		B11	rldc2_dq[13]
1.5v_int	V20		B12	rldc_a[0]
1.5v_int	W14		B13	rldc_a[4]
1.5v_int	W16		B14	rldc_a[14]
1.5v_int	W17		B15	nc
1.5v_int	W19		B16	rld_fbclk_p_out
1.5v_int	Y13		B17	rldc_refclk_p
1.5v_int	Y15		B18	rlds_ck_p

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
1.5v_int	Y18		B19	rld_dll_clk_out
1.5v_int	Y20		B20	rlds_a[3]
1.5v_pll	AG16		B21	rlds_qvld
1.5v_pll	AG17		B22	rlds_q[0]
1.5v_pll	AJ2		B23	rlds_q[2]
1.5v_pll	AJ31		B24	rlds_q[6]
1.5v_pll	D2		B25	rlds_d[3]
1.5v_pll	D31		B26	rlds_d[16]
1.5v_pll	E16		B27	rlds_qk_p[1]
1.5v_pll	G17		B28	rlds_d[14]
1.5v_pll	T25		B29	rlds_q[10]
1.5v_pll	T8		B30	rlds_q[11]
1.5v_pll	U25		B31	gnd
1.5v_pll	U8		B32	gnd
3.3v_s_clk	AB17		C1	3.3v_s_io
3.3v_s_clk	AE17		C2	3.3v_s_io
3.3v_s_io	AA1		C3	rldc_dq[1]
3.3v_s_io	AF5		C4	rldc_dq[3]
3.3v_s_io	AF6		C5	rldc_qk_p[0]
3.3v_s_io	AK1		C6	rldc_dq[9]
3.3v_s_io	AK2		C7	rldc_dq[11]
3.3v_s_io	C1		C8	rldc2_dq[6]
3.3v_s_io	C2		C9	rldc2_dq[5]
3.3v_s_io	M1		C10	rldc2_dq[11]
3.3v_s_io	T10		C11	rldc2_dq[14]
3.3v_s_io	U10		C12	rldc_a[1]
ck_to_scruz	AL18		C13	rldc_ba[0]
clk_from_scruz	AB5		C14	rldc_a[10]
clk1_out_s	U31		C15	rldc_a[19]
clk2_out_s[1]	T29		C16	config_d3
clk2_out_s[2]	AM19		C17	nc
clk2_out_s[3]	C19		C18	nc
clk2_out_s[4]	AK15		C19	clk2_out_s[3]
clkout_n	AM16		C20	rlds_a[4]
clkout_p	AL16		C21	rlds_a[13]
config__ry_byn	AA19		C22	rlds_q[1]
config_cen	AF18		C23	rlds_q[3]
config_ceon	AH15		C24	rlds_d[2]
config_cs	AG19		C25	rlds_d[4]
config_csn	AC19		C26	rlds_d[9]
config_d0	E14		C27	rlds_d[13]
config_d1	F14		C28	rlds_qk_n[1]
config_d2	F15		C29	rlds_q[12]
config_d3	C16		C30	rlds_q[15]
config_d4	G19		C31	vcc_s_io
config_d5	J19		C32	vcc_s_io
config_d6	K19		D1	gnd_pll
config_d7	J20		D2	1.5v_pll

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
config_dclk	E19		D3	1.5v_int
config_rsn	AB18		D4	rldc_dq[4]
config_wsn	D14		D5	rldc_dq[0]
cpld_user[0]	AF8		D6	rldc_dq[8]
cpld_user[1]	AF7		D7	rldc_dq[13]
crc_error	AF20		D8	rldc2_dq[1]
ddr_fbclk	T27		D9	rldc2_dq[7]
ddr_fbclk_r	R27		D10	rldc2_dq[10]
ddra_a[0]	V29		D11	rldc2_qk_p[1]
ddra_a[1]	V30		D12	rldc_a[2]
ddra_a[10]	V28		D13	rldc_ba[1]
ddra_a[11]	R29		D14	config_wsn
ddra_a[12]	R28		D15	rld_sma_dll_clk
ddra_a[2]	V31		D16	jtag_stratix_tdi
ddra_a[3]	V32		D17	gnd
ddra_a[4]	T32		D18	nc
ddra_a[5]	R32		D19	rlds_a[0]
ddra_a[6]	T31		D20	rlds_qk_n[0]
ddra_a[7]	R31		D21	rlds_a[14]
ddra_a[8]	R30		D22	rlds_qk_p[0]
ddra_a[9]	T28		D23	rlds_q[7]
ddra_ba[0]	U27		D24	rlds_d[0]
ddra_ba[1]	U28		D25	rlds_d[5]
ddra_casn	V27		D26	rlds_d[12]
ddra_ck_n	M28		D27	rlds_d[15]
ddra_ck_p	N27		D28	rlds_q[14]
ddra_cke	G32		D29	rlds_q[13]
ddra_csn	K31		D30	1.5v_int
ddra_dq[0]	H31		D31	1.5v_pll
ddra_dq[1]	J28		D32	gnd_pll
ddra_dq[10]	F29		E1	fse_a[3]
ddra_dq[11]	E31		E2	fse_a[2]
ddra_dq[12]	F30		E3	gnd_pll
ddra_dq[13]	F31		E4	fse_a[1]
ddra_dq[14]	E29		E5	rldc_dq[2]
ddra_dq[15]	F28		E6	vref
ddra_dq[2]	J30		E7	rldc_qk_p[1]
ddra_dq[3]	J29		E8	vref
ddra_dq[4]	H30		E9	rldc2_dq[3]
ddra_dq[5]	H29		E10	vref
ddra_dq[6]	H28		E11	rldc2_dq[8]
ddra_dq[7]	J31		E12	vref
ddra_dq[8]	F32		E13	rldc_a[11]
ddra_dq[9]	E32		E14	config_d0
ddra_ldm	J32		E15	jtag_tms
ddra_ldqs	H32		E16	1.5v_pll
ddra_rasn	W26		E17	gnd_pll
ddra_udm	G31		E18	s_tempdiodep

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
ddra_udqs	G30		E19	config_dclk
ddra_wen	V26		E20	rlds_ba[0]
ddrb_cke	M31		E21	vref
ddrb_csn	P32		E22	rlds_q[5]
ddrb_dq[0]	N28		E23	vref
ddrb_dq[1]	N29		E24	rlds_d[7]
ddrb_dq[10]	L30		E25	vref
ddrb_dq[11]	K30		E26	rlds_q[17]
ddrb_dq[12]	K29		E27	vref
ddrb_dq[13]	K28		E28	rlds_q[16]
ddrb_dq[14]	L27		E29	ddra_dq[14]
ddrb_dq[15]	K27		E20	gnd_pll
ddrb_dq[2]	N30		E31	ddra_dq[11]
ddrb_dq[3]	N31		E32	ddra_dq[9]
ddrb_dq[4]	P27		F1	fse_a[8]
ddrb_dq[5]	P28		F2	fse_a[9]
ddrb_dq[6]	P29		F3	fse_a[4]
ddrb_dq[7]	P30		F4	fse_a[5]
ddrb_dq[8]	L32		F5	fse_a[0]
ddrb_dq[9]	L31		F6	vref
ddrb_ldm	N32		F7	rldc_qvld
ddrb_ldqs	P31		F8	rldc_dm
ddrb_udm	M30		F9	rldc2_qvld
ddrb_udqs	M29		F10	rldc2_dm
ddrc_cke	Y32		F11	rldc_ck_out
ddrc_csn	AA31		F12	rldc_a[9]
ddrc_dq[0]	AC27		F13	rldc_a[12]
ddrc_dq[1]	AB27		F14	config_d1
ddrc_dq[10]	Y29		F15	config_d2
ddrc_dq[11]	Y28		F16	jtag_conn_tdi
ddrc_dq[12]	W30		F17	gnd_pll
ddrc_dq[13]	W29		F18	s_tempdioden
ddrc_dq[14]	W28		F19	rlds_a[1]
ddrc_dq[15]	W27		F20	rlds_ba[1]
ddrc_dq[2]	AC28		F21	rlds_a[10]
ddrc_dq[3]	AC31		F22	rlds_a[11]
ddrc_dq[4]	AA28		F23	rlds_d[8]
ddrc_dq[5]	AB30		F24	rlds_d[17]
ddrc_dq[6]	AB31		F25	gnd
ddrc_dq[7]	AB32		F26	gnd
ddrc_dq[8]	Y31		F27	vref
ddrc_dq[9]	Y30		F28	ddra_dq[15]
ddrc_ldm	AA30		F29	ddra_dq[10]
ddrc_ldqs	AA29		F30	ddra_dq[12]
ddrc_udm	W32		F31	ddra_dq[13]
ddrc_udqs	W31		F32	ddra_dq[8]
ddrd_cke	AE27		G1	fse_a[12]
ddrd_csn	AH32		G2	fse_a[13]

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
ddrd_dq[0]	AF32		G3	fse_a[6]
ddrd_dq[1]	AG32		G4	fse_a[7]
ddrd_dq[10]	AE31		G5	fse_d[3]
ddrd_dq[11]	AD31		G6	fse_d[2]
ddrd_dq[12]	AD30		G7	fse_d[0]
ddrd_dq[13]	AD29		G8	fse_d[1]
ddrd_dq[14]	AE29		G9	vcc_s_io
ddrd_dq[15]	AE28		G10	gnd
ddrd_dq[2]	AG31		G11	ddrupdnt_out
ddrd_dq[3]	AF31		G12	ddrupdnt_in
ddrd_dq[4]	AF30		G13	rldc_ba[2]
ddrd_dq[5]	AG29		G14	jtag_tck
ddrd_dq[6]	AF29		G15	jtag_trstn
ddrd_dq[7]	AF28		G16	ep1s_status
ddrd_dq[8]	AD32		G17	1.5v_pll
ddrd_dq[9]	AE32		G18	ep1s_conf_done
ddrd_ldm	AG28		G19	config_d4
ddrd_ldqs	AG30		G20	rlds_a[2]
ddrd_udm	AD28		G21	vcc_s_io
ddrd_udqs	AE30		G22	rlds_a[12]
ddre_a[0]	AK14		G23	rlds_a[19]
ddre_a[1]	AE14		G24	rlds_dm
ddre_a[10]	AJ15		G25	gnd
ddre_a[11]	AD12		G26	vcc_s_io
ddre_a[12]	AD11		G27	vcc_s_io
ddre_a[13]	AC13		G28	gnd
ddre_a[2]	AD14		G29	nc
ddre_a[3]	AK13		G30	ddra_udqs
ddre_a[4]	AJ13		G31	ddra_udm
ddre_a[5]	AG13		G32	ddra_cke
ddre_a[6]	AH13		H1	fse_a[14]
ddre_a[7]	AE13		H2	fse_a[15]
ddre_a[8]	AF13		H3	fse_a[10]
ddre_a[9]	AF12		H4	fse_a[11]
ddre_ba[0]	AF22		H5	fse_d[6]
ddre_ba[1]	AE22		H6	fse_d[7]
ddre_ba[2]	AJ12		H7	fse_d[5]
ddre_casn	AE24		H8	fse_d[4]
ddre_cb[0]	AM20		H9	vcc_s_io
ddre_cb[1]	AL20		H10	gnd
ddre_cb[2]	AK20		H11	rldc_a[6]
ddre_cb[3]	AH20		H12	rldc_a[7]
ddre_cb[4]	AL21		H13	rldc_csn
ddre_cb[5]	AK21		H14	rldc_a[17]
ddre_cb[6]	AJ21		H15	gnd_pll
ddre_cb[7]	AM22		H16	1.5v_int
ddre_ck_n[0]	AM14		H17	vcc_s_io
ddre_ck_n[1]	AL12		H18	gnd

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
ddre_ck_n[2]	AL14		H19	rlds_a[22]
ddre_ck_p[0]	AM13		H20	rlds_a[7]
ddre_ck_p[1]	AK12		H21	nc
ddre_ck_p[2]	AL13		H22	vcc_s_io
ddre_cke	AF11		H23	gnd
ddre_cke1	AE10		H24	gnd
ddre_csn[0]	AF24		H25	nc
ddre_csn[1]	AA13		H26	nc
ddre_csn[2]	AB12		H27	gnd
ddre_csn[3]	AB14		H28	ddra_dq[6]
ddre_dll_clk_in	AK19		H29	ddra_dq[5]
ddre_dll_clk_out	AJ19		H30	ddra_dq[4]
ddre_dm[0]	AG9		H31	ddra_dq[0]
ddre_dm[1]	AG10		H32	ddra_ldqs
ddre_dm[2]	AF10		J1	fse_a[21]
ddre_dm[3]	AM11		J2	fse_a[20]
ddre_dm[4]	AG21		J3	fse_a[16]
ddre_dm[5]	AG22		J4	fse_a[17]
ddre_dm[6]	AG23		J5	fse_d[10]
ddre_dm[7]	AG24		J6	fse_d[11]
ddre_dm[8]	AG20		J7	fse_d[8]
ddre_dq[0]	AK4		J8	fse_d[9]
ddre_dq[1]	AK3		J9	vcc_s_io
ddre_dq[10]	AL5		J10	gnd
ddre_dq[11]	AK7		J11	enddrt_in
ddre_dq[12]	AM5		J12	enddrt_out
ddre_dq[13]	AJ7		J13	rldc2_csn
ddre_dq[14]	AM6		J14	rldc_a[16]
ddre_dq[15]	AL6		J15	rldc_a[15]
ddre_dq[16]	AL7		J16	1.5v_int
ddre_dq[17]	AJ8		J17	gnd
ddre_dq[18]	AM7		J18	ep1s_configN
ddre_dq[19]	AH9		J19	config_d5
ddre_dq[2]	AH5		J20	config_d7
ddre_dq[20]	AM8		J21	rlds_a[9]
ddre_dq[21]	AK9		J22	rlds_a[17]
ddre_dq[22]	AJ9		J23	nc
ddre_dq[23]	AL8		J24	vcc_s_io
ddre_dq[24]	AH11		J25	nc
ddre_dq[25]	AJ10		J26	nc
ddre_dq[26]	AL9		J27	vcc_s_io
ddre_dq[27]	AM9		J28	ddra_dq[1]
ddre_dq[28]	AK10		J29	ddra_dq[3]
ddre_dq[29]	AL11		J30	ddra_dq[2]
ddre_dq[3]	AJ5		J31	ddra_dq[7]
ddre_dq[30]	AK11		J32	ddra_ldm
ddre_dq[31]	AL10		K1	gnd
ddre_dq[32]	AL22		K2	fse_a[23]

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
ddre_dq[33]	AK22		K3	fse_a[19]
ddre_dq[34]	AL23		K4	fse_a[18]
ddre_dq[35]	AK23		K5	fse_d[14]
ddre_dq[36]	AM24		K6	fse_d[15]
ddre_dq[37]	AH22		K7	fse_d[13]
ddre_dq[38]	AL24		K8	fse_d[12]
ddre_dq[39]	AJ23		K9	rldc_a[22]
ddre_dq[4]	AJ4		K10	rldc_a[21]
ddre_dq[40]	AM26		K11	rldc_a[5]
ddre_dq[41]	AM25		K12	rldc_a[8]
ddre_dq[42]	AK24		K13	rldc_refn
ddre_dq[43]	AL25		K14	rldc_wen
ddre_dq[44]	AK25		K15	rldc_a[18]
ddre_dq[45]	AJ25		K16	vcc_s_io
ddre_dq[46]	AJ24		K17	vcc_s_io
ddre_dq[47]	AH24		K18	rlds_a[21]
ddre_dq[48]	AK26		K19	config_d6
ddre_dq[49]	AM28		K20	rlds_a[6]
ddre_dq[5]	AM4		K21	rlds_csn
ddre_dq[50]	AM27		K22	rlds_a[16]
ddre_dq[51]	AJ26		K23	vcc_s_io
ddre_dq[52]	AK27		K24	gnd
ddre_dq[53]	AL28		K25	vcc_s_io
ddre_dq[54]	AJ27		K26	gnd
ddre_dq[55]	AH26		K27	ddrb_dq[15]
ddre_dq[56]	AM29		K28	ddrb_dq[13]
ddre_dq[57]	AL29		K29	ddrb_dq[12]
ddre_dq[58]	AL30		K30	ddrb_dq[11]
ddre_dq[59]	AK29		K31	ddra_csn
ddre_dq[6]	AL4		K32	gnd
ddre_dq[60]	AJ29		L1	fse_a[22]
ddre_dq[61]	AJ28		L2	fse_a[26]
ddre_dq[62]	AK30		L3	flash_resetn
ddre_dq[63]	AH28		L4	rld_buf_fbclk_p
ddre_dq[7]	AL3		L5	rld_buf_fbclk_n
ddre_dq[8]	AJ6		L6	fse_d[16]
ddre_dq[9]	AK6		L7	fse_d[17]
ddre_dqs[0]	AK5		L8	vref
ddre_dqs[1]	AH7		L9	vcc_s_io
ddre_dqs[2]	AK8		L10	gnd
ddre_dqs[3]	AJ11		L11	gnd
ddre_dqs[4]	AJ22		L12	gnd
ddre_dqs[5]	AL26		L13	nc
ddre_dqs[6]	AL27		L14	vcc_s_io
ddre_dqs[7]	AK28		L15	vcc_s_io
ddre_dqs[8]	AJ20		L16	gnd_pll
ddre_fbclk	AB28		L17	vcc_s_io
ddre_fbclk_out	AL15		L18	rlds_a[5]

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
ddre_rasn	AF23		L19	rlds_a[8]
ddre_scl	AE21		L20	rlds_ba[2]
ddre_sda	AD21		L21	rlds_refn
ddre_sma_dll_clk	AM15		L22	rlds_wen
ddre_wen	AE23		L23	rlds_a[18]
ddrupdnb_in	AG11		L24	rlds_a[15]
ddrupdnb_out	AG12		L25	vref
ddrupdnt_in	G12		L26	gnd
ddrupdnt_out	G11		L27	ddrb_dq[14]
dig_1_a	AC5		L28	rld_fbclk_n_in
dig_1_b	AC8		L29	rld_fbclk_p_in
dig_1_c	AC7		L30	ddrb_dq[10]
dig_1_d	AB6		L31	ddrb_dq[9]
dig_1_dp	AA8		L32	ddrb_dq[8]
dig_1_e	AB7		M1	3.3v_s_io
dig_1_f	AA7		M2	nc
dig_1_g	AA6		M3	flash_cen
dig_2_a	AE7		M4	fse_a[24]
dig_2_b	AD5		M5	fse_a[25]
dig_2_c	AD6		M6	fse_d[18]
dig_2_d	AE5		M7	fse_d[19]
dig_2_dp	AC6		M8	fse_d[20]
dig_2_e	AE6		M9	fse_d[21]
dig_2_f	AD7		M10	vcc_s_io
dig_2_g	AD8		M11	gnd
dip[0]	AB19		M12	1.5v_int
dip[1]	AD20		M13	gnd
dip[10]	AC21		M14	1.5v_int
dip[11]	AB20		M15	gnd
dip[12]	AB24		M16	gnd
dip[13]	AC24		M17	gnd
dip[14]	AC23		M18	gnd
dip[15]	AD24		M19	1.5v_int
dip[2]	AE20		M20	gnd
dip[3]	AD19		M21	1.5v_int
dip[4]	AJ18		M22	vcc_s_io
dip[5]	AH18		M23	gnd
dip[6]	AK18		M24	gnd
dip[7]	AA21		M25	vcc_s_io
dip[8]	AB21		M26	vcc_s_io
dip[9]	AD22		M27	nc
enddrb_in	AE12		M28	ddra_ck_n
enddrb_out	AE11		M29	ddrb_udqs
enddrt_in	J11		M30	ddrb_udm
enddrt_out	J12		M31	ddrb_cke
enet_adsn	W12		M32	vcc_s_io
enet_aen	W11		N1	flash_rdy_bsyn
enet_ben[0]	Y11		N2	sram_ben[0]

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
enet_ben[1]	Y12		N3	flash_oen
enet_ben[2]	AB10		N4	flash_wen
enet_ben[3]	AA11		N5	fse_d[24]
enet_cyclen	W8		N6	fse_d[25]
enet_datacsn	W7		N7	fse_d[28]
enet_intrq0	V8		N8	fse_d[29]
enet_iochrdy	V7		N9	fse_d[23]
enet_iorn	V5		N10	fse_d[22]
enet_iown	V6		N11	s_smb_data
enet_lclk	V9		N12	gnd
enet_ldevn	V10		N13	1.5v_int
enet_rdyrtnn	W9		N14	gnd
enet_srdyn	R1		N15	1.5v_int
enet_vlbusn	R2		N16	gnd
enet_w_rn	Y10		N17	gnd
ep1s_conf_done	G18		N18	1.5v_int
ep1s_confign	J18		N19	gnd
ep1s_init_done	AE15		N20	1.5v_int
ep1s_status	G16		N21	gnd
flash_cen	M3		N22	gnd
flash_oen	N3		N23	nc
flash_rdy_bsyn	N1		N24	nc
flash_resetn	L3		N25	nc
flash_wen	N4		N26	nc
fse_a[0]	F5		N27	ddra_ck_p
fse_a[1]	E4		N28	ddrb_dq[0]
fse_a[10]	H3		N29	ddrb_dq[1]
fse_a[11]	H4		N30	ddrb_dq[2]
fse_a[12]	G1		N31	ddrb_dq[3]
fse_a[13]	G2		N32	ddrb_ldm
fse_a[14]	H1		P1	sram_ben[3]
fse_a[15]	H2		P2	sram_csn
fse_a[16]	J3		P3	sram_ben[1]
fse_a[17]	J4		P4	sram_ben[2]
fse_a[18]	K4		P5	fse_d[31]
fse_a[19]	K3		P6	fse_d[30]
fse_a[2]	E2		P7	max_led[4]
fse_a[20]	J2		P8	max_led[5]
fse_a[21]	J1		P9	fse_d[26]
fse_a[22]	L1		P10	fse_d[27]
fse_a[23]	K2		P11	s_smb_clk
fse_a[24]	M4		P12	1.5v_int
fse_a[25]	M5		P13	gnd
fse_a[26]	L2		P14	1.5v_int
fse_a[3]	E1		P15	gnd
fse_a[4]	F3		P16	1.5v_int
fse_a[5]	F4		P17	1.5v_int
fse_a[6]	G3		P18	gnd

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
fse_a[7]	G4		P19	1.5v_int
fse_a[8]	F1		P20	gnd
fse_a[9]	F2		P21	1.5v_int
fse_d[0]	G7		P22	vcc_s_io
fse_d[1]	G8		P23	gnd
fse_d[10]	J5		P24	vcc_s_io
fse_d[11]	J6		P25	nc
fse_d[12]	K8		P26	nc
fse_d[13]	K7		P27	ddrb_dq[4]
fse_d[14]	K5		P28	ddrb_dq[5]
fse_d[15]	K6		P29	ddrb_dq[6]
fse_d[16]	L6		P30	ddrb_dq[7]
fse_d[17]	L7		P31	ddrb_ldqs
fse_d[18]	M6		P32	ddrb_csn
fse_d[19]	M7		R1	enet_srdyn
fse_d[2]	G6		R2	enet_vlbusn
fse_d[20]	M8		R3	sram_oen
fse_d[21]	M9		R4	sram_wen
fse_d[22]	N10		R5	max_led[2]
fse_d[23]	N9		R6	max_led[3]
fse_d[24]	N5		R7	max_led[6]
fse_d[25]	N6		R8	max_led[7]
fse_d[26]	P9		R9	max_led[1]
fse_d[27]	P10		R10	max_led[0]
fse_d[28]	N7		R11	scruz_cardseln
fse_d[29]	N8		R12	vref
fse_d[3]	G5		R13	1.5v_int
fse_d[30]	P6		R14	gnd
fse_d[31]	P5		R15	1.5v_int
fse_d[4]	H8		R16	gnd
fse_d[5]	H7		R17	gnd
fse_d[6]	H5		R18	1.5v_int
fse_d[7]	H6		R19	gnd
fse_d[8]	J7		R20	1.5v_int
fse_d[9]	J8		R21	
gnd	A10		R22	1.5v_int
gnd	A2		R23	gnd
gnd	A23		R24	vcc_s_io
gnd	A31		R25	nc
gnd	AA16		R26	nc
gnd	AA17		R27	ddr_fbclk_r
gnd	AA18		R28	ddra_a[12]
gnd	AA27		R29	ddra_a[11]
gnd	AB22		R30	ddra_a[8]
gnd	AB26		R31	ddra_a[7]
gnd	AC1		R32	ddra_a[5]
gnd	AC18		T1	s_alertn
gnd	AC22		T2	s_overtempn

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
gnd	AC25		T3	sma_clk_n
gnd	AC32		T4	sma_clk_p
gnd	AD10		T5	nc
gnd	AD17		T6	gnd
gnd	AD23		T7	gnd_pll
gnd	AD27		T8	1.5v_pll
gnd	AE9		T9	1.5v_int
gnd	AF17		T10	3.3v_s_io
gnd	AG7		T11	ref_lock
gnd	AH4		T12	gnd
gnd	AL1		T13	gnd
gnd	AL2		T14	1.5v_int
gnd	AL31		T15	gnd
gnd	AL32		T16	1.5v_int
gnd	AM10		T17	1.5v_int
gnd	AM2		T18	gnd
gnd	AM23		T19	1.5v_int
gnd	AM31		T20	gnd
gnd	B1		T21	gnd
gnd	B2		T22	gnd_pll
gnd	B31		T23	vcc_s_io
gnd	B32		T24	gnd_pll
gnd	D17		T25	1.5v_pll
gnd	F25		T26	gnd_pll
gnd	F26		T27	ddr_fbclk
gnd	G10		T28	ddra_a[9]
gnd	G25		T29	clk2_out_s[1]
gnd	G28		T30	gnd
gnd	H10		T31	ddra_a[6]
gnd	H18		T32	ddra_a[4]
gnd	H23		U1	nc
gnd	H24		U2	gnd
gnd	H27		U3	nc
gnd	J10		U4	gnd
gnd	J17		U5	proto1_io[39]
gnd	K1		U6	proto1_io[38]
gnd	K24		U7	gnd_pll
gnd	K26		U8	1.5v_pll
gnd	K32		U9	gnd_pll
gnd	L10		U10	3.3v_s_io
gnd	L11		U11	gnd_pll
gnd	L12		U12	gnd
gnd	L26		U13	gnd
gnd	M11		U14	1.5v_int
gnd	M13		U15	gnd
gnd	M15		U16	1.5v_int
gnd	M16		U17	1.5v_int
gnd	M17		U18	gnd

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
gnd	M18		U19	1.5v_int
gnd	M20		U20	gnd
gnd	M23		U21	gnd
gnd	M24		U22	vrefio_loopin
gnd	N12		U23	vcc_s_io
gnd	N14		U24	1.5v_int
gnd	N16		U25	1.5v_pll
gnd	N17		U26	gnd_pll
gnd	N19		U27	ddra_ba[0]
gnd	N21		U28	ddra_ba[1]
gnd	N22		U29	nc
gnd	P13		U30	nc
gnd	P15		U31	clk1_out_s
gnd	P18		U32	nc
gnd	P20		V1	proto1_io[36]
gnd	P23		V2	proto1_io[37]
gnd	R14		V3	proto1_io[34]
gnd	R16		V4	proto1_io[35]
gnd	R17		V5	enet_iorn
gnd	R19		V6	enet_iown
gnd	R23		V7	enet_iochrdy
gnd	T12		V8	enet_intrq0
gnd	T13		V9	enet_lclk
gnd	T15		V10	enet_ldevn
gnd	T18		V11	1.5v_int
gnd	T20		V12	nc
gnd	T21		V13	1.5v_int
gnd	T30		V14	gnd
gnd	T6		V15	1.5v_int
gnd	U12		V16	gnd
gnd	U13		V17	gnd
gnd	U15		V18	1.5v_int
gnd	U18		V19	gnd
gnd	U2		V20	1.5v_int
gnd	U20		V21	vref
gnd	U21		V22	vrefio_smain
gnd	U4		V23	vcc_s_io
gnd	V14		V24	gnd
gnd	V16		V25	nc
gnd	V17		V26	ddra_wen
gnd	V19		V27	ddra_casn
gnd	V24		V28	ddra_a[10]
gnd	W13		V29	ddra_a[0]
gnd	W15		V30	ddra_a[1]
gnd	W18		V31	ddra_a[2]
gnd	W20		V32	ddra_a[3]
gnd	W23		W1	proto1_io[32]
gnd	W25		W2	proto1_io[33]

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
gnd	Y14		W3	proto1_io[30]
gnd	Y16		W4	proto1_io[31]
gnd	Y17		W5	rs232a_rts
gnd	Y19		W6	rs232a_rxd
gnd	Y21		W7	enet_datacsn
gnd	Y23		W8	enet_cyclen
gnd	Y26		W9	enet_rdyrtnn
gnd_pll	AB16		W10	nc
gnd_pll	AE16		W11	enet_aen
gnd_pll	AH16		W12	enet_adsn
gnd_pll	AH17		W13	gnd
gnd_pll	AH3		W14	1.5v_int
gnd_pll	AH30		W15	gnd
gnd_pll	AJ1		W16	1.5v_int
gnd_pll	AJ32		W17	1.5v_int
gnd_pll	D1		W18	gnd
gnd_pll	D32		W19	1.5v_int
gnd_pll	E17		W20	gnd
gnd_pll	E3		W21	vrefio_loopout
gnd_pll	E30		W22	vrefio_smaout
gnd_pll	F17		W23	gnd
gnd_pll	H15		W24	vcc_s_io
gnd_pll	L16		W25	gnd
gnd_pll	T22		W26	ddra_rasn
gnd_pll	T24		W27	ddrc_dq[15]
gnd_pll	T26		W28	ddrc_dq[14]
gnd_pll	T7		W29	ddrc_dq[13]
gnd_pll	U11		W30	ddrc_dq[12]
gnd_pll	U26		W31	ddrc_udqs
gnd_pll	U7		W32	ddrc_udm
gnd_pll	U9		Y1	proto1_io[28]
jtag_conn_tdi	F16		Y2	proto1_io[29]
jtag_stratix_tdi	D16		Y3	proto1_io[26]
jtag_tck	G14		Y4	proto1_io[27]
jtag_tms	E15		Y5	rs232b_rts
jtag_trstn	G15		Y6	rs232b_rxd
max_led[0]	R10		Y7	rs232a_cts
max_led[1]	R9		Y8	rs232b_txd
max_led[2]	R5		Y9	rs232a_txd
max_led[3]	R6		Y10	enet_w_rn
max_led[4]	P7		Y11	enet_ben[0]
max_led[5]	P8		Y12	enet_ben[1]
max_led[6]	R7		Y13	1.5v_int
max_led[7]	R8		Y14	gnd
msel0	AG18		Y15	1.5v_int
msel1	AE18		Y16	gnd
msel2	AE19		Y17	gnd
nc	A15		Y18	1.5v_int

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
nc	AA12		Y19	gnd
nc	AA14		Y20	1.5v_int
nc	AA15		Y21	gnd
nc	AA22		Y22	vcc_s_io
nc	AA24		Y23	gnd
nc	AA25		Y24	vcc_s_io
nc	AB11		Y25	vcc_s_io
nc	AB13		Y26	gnd
nc	AB15		Y27	vcc_s_io
nc	AB23		Y28	ddrc_dq[11]
nc	AB29		Y29	ddrc_dq[10]
nc	AB4		Y30	ddrc_dq[9]
nc	AB9		Y31	ddrc_dq[8]
nc	AC10		Y32	ddrc_cke
nc	AC11		AA1	3.3v_s_io
nc	AC12		AA2	proto1_io[24]
nc	AC14		AA3	proto1_io[25]
nc	AC15		AA4	proto1_io[21]
nc	AC29		AA5	proto1_io[20]
nc	AC30		AA6	dig_1_g
nc	AC9		AA7	dig_1_f
nc	AD25		AA8	dig_1_dp
nc	AE26		AA9	rs232b_cts
nc	AF25		AA10	vref
nc	AF26		AA11	enet_ben[3]
nc	AF27		AA12	nc
nc	AG25		AA13	ddre_csn[1]
nc	AG26		AA14	nc
nc	AG27		AA15	nc
nc	AH29		AA16	gnd
nc	AH31		AA17	gnd
nc	AJ16		AA18	gnd
nc	AJ17		AA19	config__ry_byn
nc	AK16		AA20	spgm2
nc	AK17		AA21	dip[7]
nc	AL19		AA22	nc
nc	AM18		AA23	vref
nc	B15		AA24	nc
nc	C17		AA25	nc
nc	C18		AA26	vcc_s_io
nc	D18		AA27	gnd
nc	G29		AA28	ddrc_dq[4]
nc	H21		AA29	ddrc_ldqs
nc	H25		AA30	ddrc_ldm
nc	H26		AA31	ddrc_csn
nc	J23		AA32	vcc_s_io
nc	J25		AB1	proto1_io[18]
nc	J26		AB2	proto1_io[22]

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
nc	L13		AB3	proto1_io[23]
nc	M2		AB4	nc
nc	M27		AB5	clk_from_scruz
nc	N23		AB6	dig_1_d
nc	N24		AB7	dig_1_e
nc	N25		AB8	vref
nc	N26		AB9	nc
nc	P25		AB10	enet_ben[2]
nc	P26		AB11	nc
nc	R25		AB12	ddre_csn[2]
nc	R26		AB13	nc
nc	T5		AB14	ddre_csn[3]
nc	U1		AB15	nc
nc	U29		AB16	gnd_pll
nc	U3		AB17	3.3v_s_clk
nc	U30		AB18	config_rsn
nc	U32		AB19	dip[0]
nc	V12		AB20	dip[11]
nc	V25		AB21	dip[8]
nc	W10		AB22	gnd
nio_pullup	AF15		AB23	nc
pb[0]	AG8		AB24	dip[12]
pb[1]	AH2		AB25	vref
pb[2]	AH1		AB26	gnd
pb_dev_clrn	AH14		AB27	ddrc_dq[1]
porsel	AG15		AB28	ddre_fbclk
proto1_io[0]	AG3		AB29	nc
proto1_io[1]	AG4		AB30	ddrc_dq[5]
proto1_io[10]	AE1		AB31	ddrc_dq[6]
proto1_io[11]	AE2		AB32	ddrc_dq[7]
proto1_io[12]	AC4		AC1	gnd
proto1_io[13]	AC3		AC2	proto1_io[19]
proto1_io[14]	AD4		AC3	proto1_io[13]
proto1_io[15]	AD3		AC4	proto1_io[12]
proto1_io[16]	AD1		AC5	dig_1_a
proto1_io[17]	AD2		AC6	dig_2_dp
proto1_io[18]	AB1		AC7	dig_1_c
proto1_io[19]	AC2		AC8	dig_1_b
proto1_io[2]	AG2		AC9	nc
proto1_io[20]	AA5		AC10	nc
proto1_io[21]	AA4		AC11	nc
proto1_io[22]	AB2		AC12	nc
proto1_io[23]	AB3		AC13	ddre_a[13]
proto1_io[24]	AA2		AC14	nc
proto1_io[25]	AA3		AC15	nc
proto1_io[26]	Y3		AC16	vcc_s_io
proto1_io[27]	Y4		AC17	vcc_s_io
proto1_io[28]	Y1		AC18	gnd

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
proto1_io[29]	Y2		AC19	config_csn
proto1_io[3]	AG1		AC20	vcc_s_io
proto1_io[30]	W3		AC21	dip[10]
proto1_io[31]	W4		AC22	gnd
proto1_io[32]	W1		AC23	dip[14]
proto1_io[33]	W2		AC24	dip[13]
proto1_io[34]	V3		AC25	gnd
proto1_io[35]	V4		AC26	vcc_s_io
proto1_io[36]	V1		AC27	ddrc_dq[0]
proto1_io[37]	V2		AC28	ddrc_dq[2]
proto1_io[38]	U6		AC29	nc
proto1_io[39]	U5		AC30	nc
proto1_io[4]	AF3		AC31	ddrc_dq[3]
proto1_io[40]	AE8		AC32	gnd
proto1_io[5]	AF4		AD1	proto1_io[16]
proto1_io[6]	AF1		AD2	proto1_io[17]
proto1_io[7]	AF2		AD3	proto1_io[15]
proto1_io[8]	AE3		AD4	proto1_io[14]
proto1_io[9]	AE4		AD5	dig_2_b
ref_lock	T11		AD6	dig_2_c
rld_buf_fbclk_n	L5		AD7	dig_2_f
rld_buf_fbclk_p	L4		AD8	dig_2_g
rld_dll_clk_in	A19		AD9	vcc_s_io
rld_dll_clk_out	B19		AD10	gnd
rld_fbclk_n_in	L28		AD11	ddre_a[12]
rld_fbclk_n_out	A16		AD12	ddre_a[11]
rld_fbclk_p_in	L29		AD13	vcc_s_io
rld_fbclk_p_out	B16		AD14	ddre_a[2]
rld_sma_dll_clk	D15		AD15	vcc_s_io
rldc_a[0]	B12		AD16	1.5v_int
rldc_a[1]	C12		AD17	gnd
rldc_a[10]	C14		AD18	spgm0
rldc_a[11]	E13		AD19	dip[3]
rldc_a[12]	F13		AD20	dip[1]
rldc_a[13]	A14		AD21	ddre_sda
rldc_a[14]	B14		AD22	dip[9]
rldc_a[15]	J15		AD23	gnd
rldc_a[16]	J14		AD24	dip[15]
rldc_a[17]	H14		AD25	nc
rldc_a[18]	K15		AD26	vcc_s_io
rldc_a[19]	C15		AD27	gnd
rldc_a[2]	D12		AD28	ddrd_udm
rldc_a[20]	A11		AD29	ddrd_dq[13]
rldc_a[21]	K10		AD30	ddrd_dq[12]
rldc_a[22]	K9		AD31	ddrd_dq[11]
rldc_a[3]	A13		AD32	ddrd_dq[8]
rldc_a[4]	B13		AE1	proto1_io[10]
rldc_a[5]	K11		AE2	proto1_io[11]

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
rldc_a[6]	H11		AE3	proto1_io[8]
rldc_a[7]	H12		AE4	proto1_io[9]
rldc_a[8]	K12		AE5	dig_2_d
rldc_a[9]	F12		AE6	dig_2_e
rldc_ba[0]	C13		AE7	dig_2_a
rldc_ba[1]	D13		AE8	proto1_io[40]
rldc_ba[2]	G13		AE9	gnd
rldc_ck_out	F11		AE10	ddre_cke1
rldc_csn	H13		AE11	enddrb_out
rldc_dm	F8		AE12	enddrb_in
rldc_dq[0]	D5		AE13	ddre_a[7]
rldc_dq[1]	C3		AE14	ddre_a[1]
rldc_dq[10]	B5		AE15	ep1s_init_done
rldc_dq[11]	C7		AE16	gnd_pll
rldc_dq[12]	A5		AE17	3.3v_s_clk
rldc_dq[13]	D7		AE18	msel1
rldc_dq[14]	A6		AE19	msel2
rldc_dq[15]	B6		AE20	dip[2]
rldc_dq[2]	E5		AE21	ddre_scl
rldc_dq[3]	C4		AE22	ddre_ba[1]
rldc_dq[4]	D4		AE23	ddre_wen
rldc_dq[5]	A4		AE24	ddre_casn
rldc_dq[6]	B4		AE25	vcc_s_io
rldc_dq[7]	B3		AE26	nc
rldc_dq[8]	D6		AE27	ddrd_cke
rldc_dq[9]	C6		AE28	ddrd_dq[15]
rldc_qk_p[0]	C5		AE29	ddrd_dq[14]
rldc_qk_p[1]	E7		AE30	ddrd_udqs
rldc_qvld	F7		AE31	ddrd_dq[10]
rldc_refclk_n	A17		AE32	ddrd_dq[9]
rldc_refclk_p	B17		AF1	proto1_io[6]
rldc_refn	K13		AF2	proto1_io[7]
rldc_wen	K14		AF3	proto1_io[4]
rldc2_csn	J13		AF4	proto1_io[5]
rldc2_dm	F10		AF5	3.3v_s_io
rldc2_dq[0]	B7		AF6	3.3v_s_io
rldc2_dq[1]	D8		AF7	cpld_user[1]
rldc2_dq[10]	D10		AF8	cpld_user[0]
rldc2_dq[11]	C10		AF9	vcc_s_io
rldc2_dq[12]	A9		AF10	ddre_dm[2]
rldc2_dq[13]	B11		AF11	ddre_cke
rldc2_dq[14]	C11		AF12	ddre_a[9]
rldc2_dq[15]	B10		AF13	ddre_a[8]
rldc2_dq[2]	B8		AF14	ru_n_lu
rldc2_dq[3]	E9		AF15	nio_pullup
rldc2_dq[4]	A8		AF16	1.5v_int
rldc2_dq[5]	C9		AF17	gnd
rldc2_dq[6]	C8		AF18	config_cen

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
rldc2_dq[7]	D9		AF19	s_pll_ena
rldc2_dq[8]	E11		AF20	crc_error
rldc2_dq[9]	B9		AF21	vcc_s_io
rldc2_qk_p[0]	A7		AF22	ddre_ba[0]
rldc2_qk_p[1]	D11		AF23	ddre_rasn
rldc2_qvld	F9		AF24	ddre_csn[0]
rlds_a[0]	D19		AF25	nc
rlds_a[1]	F19		AF26	nc
rlds_a[10]	F21		AF27	nc
rlds_a[11]	F22		AF28	ddrd_dq[7]
rlds_a[12]	G22		AF29	ddrd_dq[6]
rlds_a[13]	C21		AF30	ddrd_dq[4]
rlds_a[14]	D21		AF31	ddrd_dq[3]
rlds_a[15]	L24		AF32	ddrd_dq[0]
rlds_a[16]	K22		AG1	proto1_io[3]
rlds_a[17]	J22		AG2	proto1_io[2]
rlds_a[18]	L23		AG3	proto1_io[0]
rlds_a[19]	G23		AG4	proto1_io[1]
rlds_a[2]	G20		AG5	sys_resetn
rlds_a[20]	A20		AG6	vref
rlds_a[21]	K18		AG7	gnd
rlds_a[22]	H19		AG8	pb[0]
rlds_a[3]	B20		AG9	ddre_dm[0]
rlds_a[4]	C20		AG10	ddre_dm[1]
rlds_a[5]	L18		AG11	ddrupdnb_in
rlds_a[6]	K20		AG12	ddrupdnb_out
rlds_a[7]	H20		AG13	ddre_a[5]
rlds_a[8]	L19		AG14	spgm1
rlds_a[9]	J21		AG15	porsel
rlds_ba[0]	E20		AG16	1.5v_pll
rlds_ba[1]	F20		AG17	1.5v_pll
rlds_ba[2]	L20		AG18	msel0
rlds_ck_n	A18		AG19	config_cs
rlds_ck_p	B18		AG20	ddre_dm[8]
rlds_csn	K21		AG21	ddre_dm[4]
rlds_d[0]	D24		AG22	ddre_dm[5]
rlds_d[1]	A25		AG23	ddre_dm[6]
rlds_d[10]	A28		AG24	ddre_dm[7]
rlds_d[11]	A27		AG25	nc
rlds_d[12]	D26		AG26	nc
rlds_d[13]	C27		AG27	nc
rlds_d[14]	B28		AG28	ddrd_ldm
rlds_d[15]	D27		AG29	ddrd_dq[5]
rlds_d[16]	B26		AG30	ddrd_ldqs
rlds_d[17]	F24		AG31	ddrd_dq[2]
rlds_d[2]	C24		AG32	ddrd_dq[1]
rlds_d[3]	B25		AH1	pb[2]
rlds_d[4]	C25		AH2	pb[1]

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
rlds_d[5]	D25		AH3	gnd_pll
rlds_d[6]	A26		AH4	gnd
rlds_d[7]	E24		AH5	ddre_dq[2]
rlds_d[8]	F23		AH6	vref
rlds_d[9]	C26		AH7	ddre_dqs[1]
rlds_dm	G24		AH8	vref
rlds_q[0]	B22		AH9	ddre_dq[19]
rlds_q[1]	C22		AH10	vref
rlds_q[10]	B29		AH11	ddre_dq[24]
rlds_q[11]	B30		AH12	vref
rlds_q[12]	C29		AH13	ddre_a[6]
rlds_q[13]	D29		AH14	pb_dev_clrn
rlds_q[14]	D28		AH15	config_ceon
rlds_q[15]	C30		AH16	gnd_pll
rlds_q[16]	E28		AH17	gnd_pll
rlds_q[17]	E26		AH18	dip[5]
rlds_q[2]	B23		AH19	vcc_s_io
rlds_q[3]	C23		AH20	ddre_cb[3]
rlds_q[4]	A24		AH21	vref
rlds_q[5]	E22		AH22	ddre_dq[37]
rlds_q[6]	B24		AH23	vref
rlds_q[7]	D23		AH24	ddre_dq[47]
rlds_q[8]	A22		AH25	vref
rlds_q[9]	A29		AH26	ddre_dq[55]
rlds_qk_n[0]	D20		AH27	vref
rlds_qk_n[1]	C28		AH28	ddre_dq[63]
rlds_qk_p[0]	D22		AH29	nc
rlds_qk_p[1]	B27		AH30	gnd_pll
rlds_qvld	B21		AH31	nc
rlds_refn	L21		AH32	ddrd_csn
rlds_wen	L22		AJ1	gnd_pll
rs232a_cts	Y7		AJ2	1.5v_pll
rs232a_rts	W5		AJ3	1.5v_int
rs232a_rxd	W6		AJ4	ddre_dq[4]
rs232a_txd	Y9		AJ5	ddre_dq[3]
rs232b_cts	AA9		AJ6	ddre_dq[8]
rs232b_rts	Y5		AJ7	ddre_dq[13]
rs232b_rxd	Y6		AJ8	ddre_dq[17]
rs232b_txd	Y8		AJ9	ddre_dq[22]
ru_n_lu	AF14		AJ10	ddre_dq[25]
s_alertn	T1		AJ11	ddre_dqs[3]
s_overtempn	T2		AJ12	ddre_ba[2]
s_pll_ena	AF19		AJ13	ddre_a[4]
s_smb_clk	P11		AJ14	vcc_sel
s_smb_data	N11		AJ15	ddre_a[10]
s_tempdioden	F18		AJ16	nc
s_tempdiodep	E18		AJ17	nc
scruz_cardseln	R11		AJ18	dip[4]

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
sma_clk_n	T3		AJ19	ddre_dll_clk_out
sma_clk_p	T4		AJ20	ddre_dqs[8]
sma_fb_n	AM17		AJ21	ddre_cb[6]
sma_fb_p	AL17		AJ22	ddre_dqs[4]
spgm0	AD18		AJ23	ddre_dq[39]
spgm1	AG14		AJ24	ddre_dq[46]
spgm2	AA20		AJ25	ddre_dq[45]
sram_ben[0]	N2		AJ26	ddre_dq[51]
sram_ben[1]	P3		AJ27	ddre_dq[54]
sram_ben[2]	P4		AJ28	ddre_dq[61]
sram_ben[3]	P1		AJ29	ddre_dq[60]
sram_csn	P2		AJ30	1.5v_int
sram_oen	R3		AJ31	1.5v_pll
sram_wen	R4		AJ32	gnd_pll
sys_resetn	AG5		AK1	3.3v_s_io
vcc_s_io	A12		AK2	3.3v_s_io
vcc_s_io	A21		AK3	ddre_dq[1]
vcc_s_io	A3		AK4	ddre_dq[0]
vcc_s_io	A30		AK5	ddre_dqs[0]
vcc_s_io	AA26		AK6	ddre_dq[9]
vcc_s_io	AA32		AK7	ddre_dq[11]
vcc_s_io	AC16		AK8	ddre_dqs[2]
vcc_s_io	AC17		AK9	ddre_dq[21]
vcc_s_io	AC20		AK10	ddre_dq[28]
vcc_s_io	AC26		AK11	ddre_dq[30]
vcc_s_io	AD13		AK12	ddre_ck_p[1]
vcc_s_io	AD15		AK13	ddre_a[3]
vcc_s_io	AD26		AK14	ddre_a[0]
vcc_s_io	AD9		AK15	clk2_out_s[4]
vcc_s_io	AE25		AK16	nc
vcc_s_io	AF21		AK17	nc
vcc_s_io	AF9		AK18	dip[6]
vcc_s_io	AH19		AK19	ddre_dll_clk_in
vcc_s_io	AK31		AK20	ddre_cb[2]
vcc_s_io	AK32		AK21	ddre_cb[5]
vcc_s_io	AM12		AK22	ddre_dq[33]
vcc_s_io	AM21		AK23	ddre_dq[35]
vcc_s_io	AM3		AK24	ddre_dq[42]
vcc_s_io	AM30		AK25	ddre_dq[44]
vcc_s_io	C31		AK26	ddre_dq[48]
vcc_s_io	C32		AK27	ddre_dq[52]
vcc_s_io	G21		AK28	ddre_dqs[7]
vcc_s_io	G26		AK29	ddre_dq[59]
vcc_s_io	G27		AK30	ddre_dq[62]
vcc_s_io	G9		AK31	vcc_s_io
vcc_s_io	H17		AK32	vcc_s_io
vcc_s_io	H22		AL1	gnd
vcc_s_io	H9		AL2	gnd

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	Pin Number		Pin Number	Signal Name
vcc_s_io	J24		AL3	ddre_dq[7]
vcc_s_io	J27		AL4	ddre_dq[6]
vcc_s_io	J9		AL5	ddre_dq[10]
vcc_s_io	K16		AL6	ddre_dq[15]
vcc_s_io	K17		AL7	ddre_dq[16]
vcc_s_io	K23		AL8	ddre_dq[23]
vcc_s_io	K25		AL9	ddre_dq[26]
vcc_s_io	L14		AL10	ddre_dq[31]
vcc_s_io	L15		AL11	ddre_dq[29]
vcc_s_io	L17		AL12	ddre_ck_n[1]
vcc_s_io	L9		AL13	ddre_ck_p[2]
vcc_s_io	M10		AL14	ddre_ck_n[2]
vcc_s_io	M22		AL15	ddre_fbclk_out
vcc_s_io	M25		AL16	clkout_p
vcc_s_io	M26		AL17	sma_fb_p
vcc_s_io	M32		AL18	ck_to_scruz
vcc_s_io	P22		AL19	nc
vcc_s_io	P24		AL20	ddre_cb[1]
vcc_s_io	R24		AL21	ddre_cb[4]
vcc_s_io	T23		AL22	ddre_dq[32]
vcc_s_io	U23		AL23	ddre_dq[34]
vcc_s_io	V23		AL24	ddre_dq[38]
vcc_s_io	W24		AL25	ddre_dq[43]
vcc_s_io	Y22		AL26	ddre_dqs[5]
vcc_s_io	Y24		AL27	ddre_dqs[6]
vcc_s_io	Y25		AL28	ddre_dq[53]
vcc_s_io	Y27		AL29	ddre_dq[57]
vcc_sel	AJ14		AL30	ddre_dq[58]
vref	AA10		AL31	gnd
vref	AA23		AL32	gnd
vref	AB25		AM2	gnd
vref	AB8		AM3	vcc_s_io
vref	AG6		AM4	ddre_dq[5]
vref	AH10		AM5	ddre_dq[12]
vref	AH12		AM6	ddre_dq[14]
vref	AH21		AM7	ddre_dq[18]
vref	AH23		AM8	ddre_dq[20]
vref	AH25		AM9	ddre_dq[27]
vref	AH27		AM10	gnd
vref	AH6		AM11	ddre_dm[3]
vref	AH8		AM12	vcc_s_io
vref	E10		AM13	ddre_ck_p[0]
vref	E12		AM14	ddre_ck_n[0]
vref	E21		AM15	ddre_sma_dll_clk
vref	E23		AM16	clkout_n
vref	E25		AM17	sma_fb_n
vref	E27		AM18	nc
vref	E6		AM19	clk2_out_s[2]

Table 30. Stratix SMB1 Pin Out				
Alphabetical by Signal Name			Alphabetical by Pin Name	
Signal Name	**Pin Number**		**Pin Number**	**Signal Name**
vref	E8		AM20	ddre_cb[0]
vref	F27		AM21	vcc_s_io
vref	F6		AM22	ddre_cb[7]
vref	L25		AM23	gnd
vref	L8		AM24	ddre_dq[36]
vref	R12		AM25	ddre_dq[41]
vref	R21		AM26	ddre_dq[40]
vref	V21		AM27	ddre_dq[50]
vrefio_loopin	U22		AM28	ddre_dq[49]
vrefio_loopout	W21		AM29	ddre_dq[56]
vrefio_smain	V22		AM30	vcc_s_io
vrefio_smaout	W22		AM31	gnd