The Programmable Solutions Company®

Arria II GX™ FPGA Development Kit HSMC Loopback Tests

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1 Introduction

This document is intended to provide the user of the Arria II GX FPGA Development Kit with a basic introduction to the board, and a procedure to control the different hardware and software settings. Test designs for the various interfaces on the Arria II GX FPGA Development Kit are described below, and contain a functional block diagrams and production test instructions.

Many of the test designs described below use the Arria II GX Board Test System (BTS). The BTS uses several IP cores to simplify verification and debug of the various interfaces of the board, using a common test platform which is reusable, scalable, and modular. For example, all test designs using BTS support the following design methodology:

1) All push buttons are metastabilized and debounced.
2) All phase compensation FIFO's read and write pointers are initialized after their read and write clocks are phase locked. For example, TX_DIGITALRESET is pulsed after the PLL_LOCKED signal asserts, and the RX_DIGITALRESET signal is pulsed after the RX_FREQLOCKED asserts.
3) Signals crossing clock domains are metastabilized.
4) PCS functions are implemented either in the ALTGX PCS or ALTLVDS, or in the FPGA fabric using a BTS soft IP core if that function is not available for a particular protocol in the MegaCore.

The BTS supports asynchronous board to board testing, and contains parameterizable IP cores including a PRBS Pattern Generator, PRBS Pattern Comparator, Phase Compensation FIFOs, Transmitter Channel to Channel Skew Inserter, Endian Converters, Word Aligner, Byte Order, Channel Bonder, Sync Detector, Error Detector, and various other modules. All test designs using BTS have the BTS IP cores included in the QAR file, they are located in the local /bts folder.

1.1 HSMC Interface Tests

The HSMC Interface tests send multiple high-speed serial data streams through the HSMC loopback connectors. For the transceiver portion of each HSMC interface, 4 transceiver channels of pseudo-random data are serialized, pre-emphasized, and then transmitted out of the Arria II GX device at around 3.75 Gbps. The transmitter PLL uses a 100 MHz reference clock. The high-speed serial data is then looped back through an external HSMC Loopback Card back to the Arria II GX device. The data is then equalized, retimed, deserialized, word aligned, channel bonded, and then the 4 bonded channels are compared against a receive side PRBS generator inside the Arria II GX FPGA fabric. A functional

block diagram of the x4 3.75 Gbps transceiver section of the HSMC Loopback Test Design is shown in Figure 1.

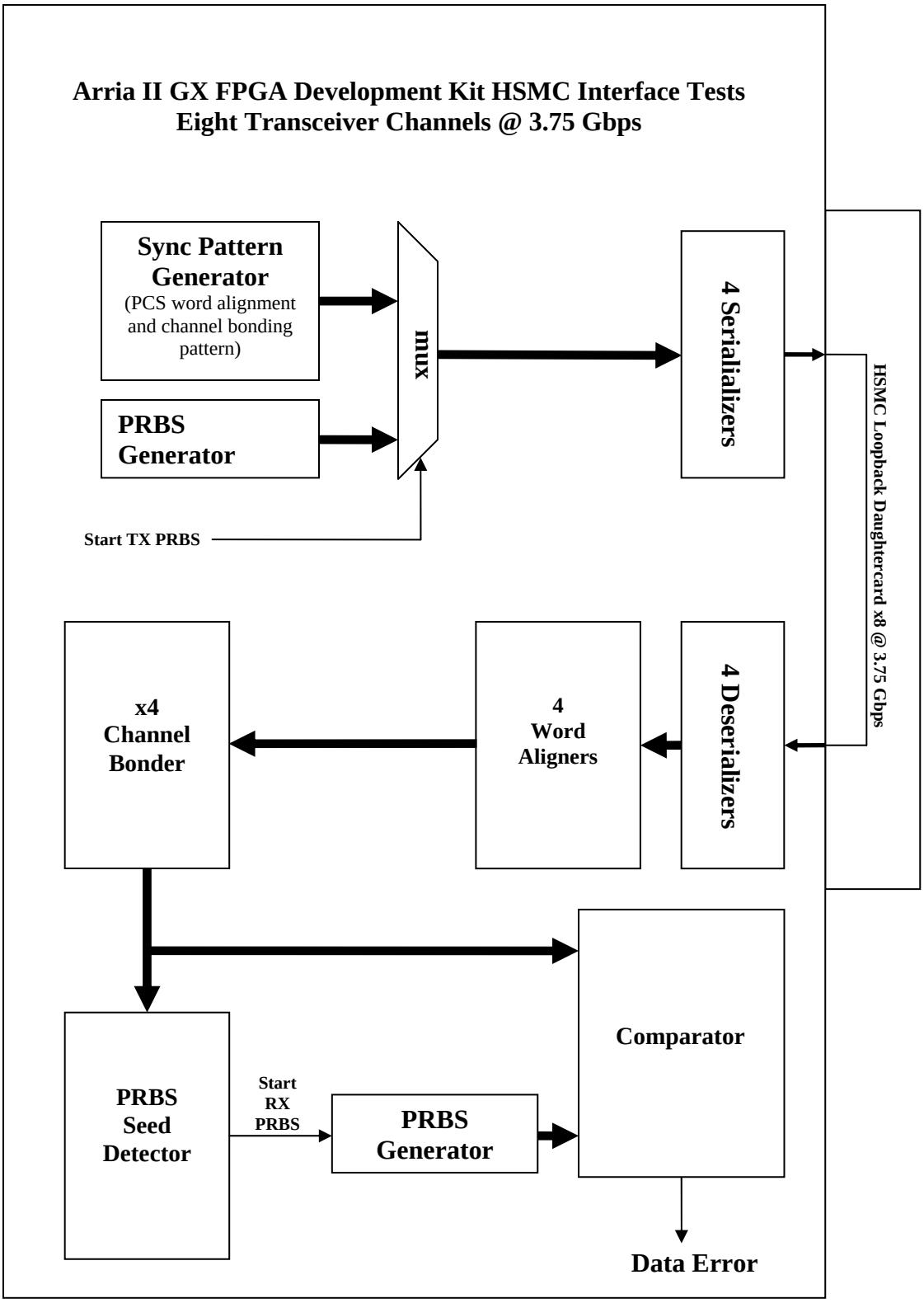
Arria II GX FPGA Development Kit HSMC Interface Tests
Eight Transceiver Channels @ 3.75 Gbps
Sync Pattern Generator
(PCS word alignment and channel bonding pattern)
PRBS Generator
mux
Start TX PRBS
4 Serializers
HSMC Loopback Daughtercard x8 @ 3.75 Gbps
x4 Channel Bonder
4 Word Aligners
4 Deserializers
PRBS Seed Detector
Start RX PRBS
PRBS Generator
Comparator
Data Error

Figure 1

Simultaneously to the test running four 3.75 Gbps transceivers on the HSMC interface, the source synchronous SERDES are tested by looping back 17 LVDS channels (16 data plus 1 control) running at 1 Gbps. The transmitter PLL uses a 125 MHz reference clock. 17 channels of pseudo-random data are serialized and transmitted out of the Arria II GX device, and are then looped through the HSMC Loopback Card back to the Arria II GX device. The 17 LVDS receivers are then DPA locked, deserialized, word aligned, channel bonded, and then compared against a receive side PRBS generator. A functional block diagram of the SPI4.2 section of the HSMC test design is shown in Figure 2. Low speed status channels and the extra clock are also looped back and tested.

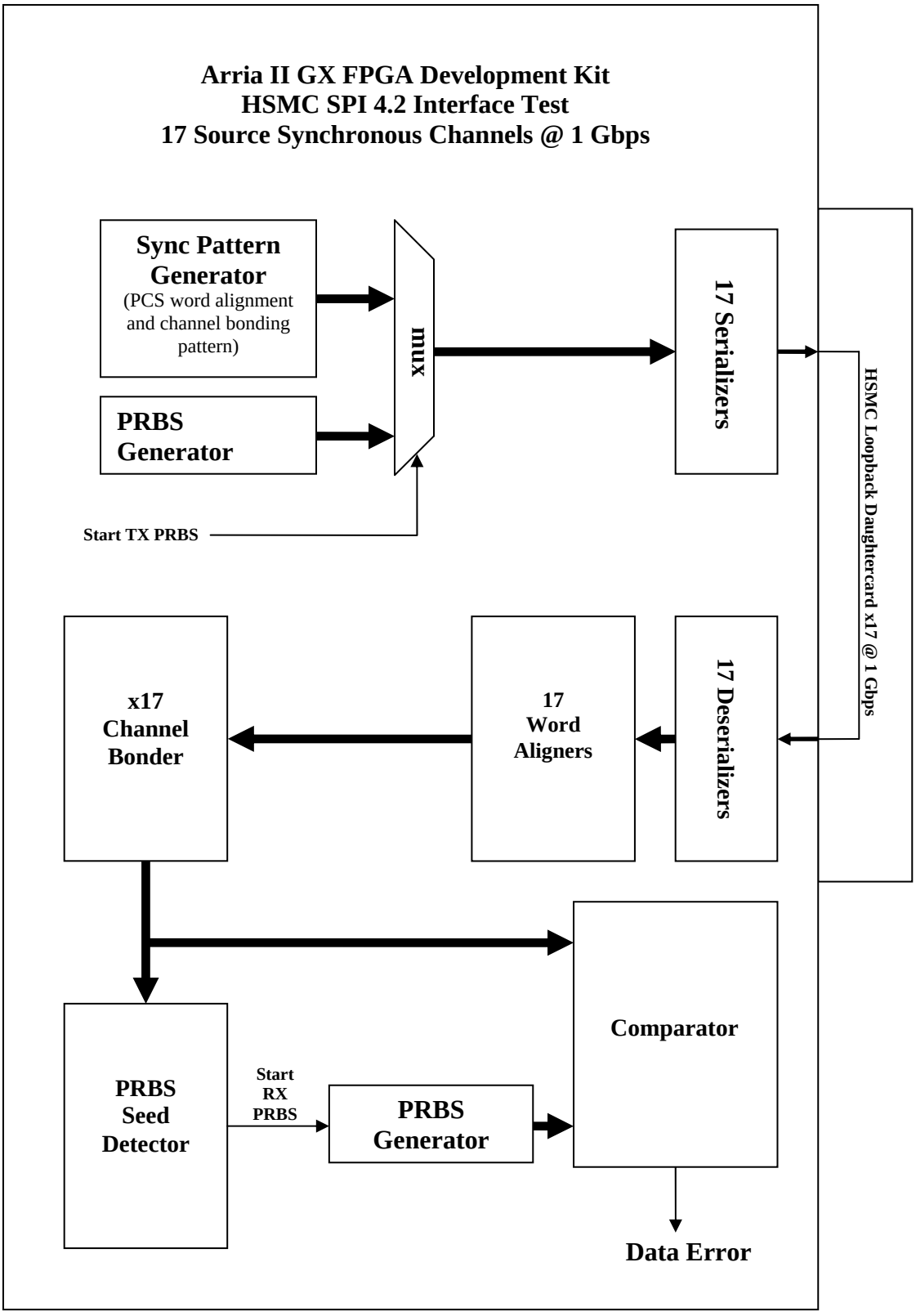
Arria II GX FPGA Development Kit
HSMC SPI 4.2 Interface Test
17 Source Synchronous Channels @ 1 Gbps
Sync Pattern Generator
(PCS word alignment and channel bonding pattern)
PRBS Generator
mux
Start TX PRBS
17 Serializers
HSMC Loopback Daughtercard x17 @ 1 Gbps
17 Deserializers
17 Word Aligners
x17 Channel Bonder
Comparator
PRBS Seed Detector
Start RX PRBS
PRBS Generator
Data Error

Figure 2

Pushbutton, Dip Switch, and LED Definitions

LED indicators combine transceiver, source synchronous and low speed interface test results. Different tests are enabled by the User Dipswitch (abbreviated user_dipsw below):

FPGA_RST	Resets the Board Test System
PB0	1st press: Enable Comma Detect 2nd press: Enable Channel Bond 3rd press: Start transmitting PRBS data 4th press: Create an error in the TX data stream
PB1	Initially LED results are for XCVRs, LVDS SERDES, and Parallel Loopback. 1st press: Test XCVRs only 2nd press: Test LVDS only 3rd press: Test Parallel only
USER_DIP[0]	HSMA Transceivers, Source Synchronous, and Parallel Loopback
USER_DIP[1]	HSMB Transceivers, Source Synchronous, and Parallel Loopback HSMB is disabled until A2GX260 silicon is available
USER_DIP[2]	PCIe Edge Connector
USER_DIP[3]	HSMA & HSMB Parallel Clock Phase Control: 0=0 degrees 1=180 degrees Disabled for NIOS designs
LED0	PLLs are locked.
LED1	Pattern Sync Acquired (Word aligned, Channel Bonded, 1st PRBS Data Received).
LED2	Test Complete
LED2	Error
HSMA_TX	HSMA TX PLLs Locked
HSMA_RX	HSMA RX PLLs Locked
HSMB_TX	HSMB TX PLLs Locked (Disabled until A2GX260 silicon is available)
HSMB_RX	HSMB RX PLLs Locked (Disabled until A2GX260 silicon is available)

To run the HSMC Loopback Tests, perform the following steps:

1) Set SW4[1:8]=[00000011], where 1=”ON” silk screen on the SW4 mini dipswitch.

2) Plug in the HSMA loopback card.
3) Set USER_DIP[0:3]=[1000] (0=ON on the dipswitch silk screen)
4) Plug in the USB cable from the PC to the board's USB Embedded Blaster input. You can also usse a USB Blaster cable between the PC's USB and the JTAG connector on the board.
5) Power on the board.
6) Using the Quartus Programmer, program the hsmc_loopback.sof into the Arria IV GX FPGA Development Kit.

NOTE If you can't autodetect the board, make certain HSMA, HSMB and PCIe are not in the JTAG CHAIN by using the J9 JTAG CHAIN jumpers.

7) Press and release the FPGA_RST pushbutton. LEDs {pcie_led_x1, pcie_led_x4,pcie_led_x8} will display the "heartbeat pattern" indicating the Arria II GX test design is running, and HSMA_TX & HSMA_RX should also illuminate. Also the HSMA_PRSTN LED illuminates whenever the loopback card is installed.
8) Press and release PB0. (RX enable comma detect)
9) Press and release PB0. (RX channel bond)
10) Press and release PB0.(RX start transmitting PRBS data)
11) Confirm LEDS 0, 1 and 2 illuminate, and LED 3 is not illuminated.
12) Press and release PB0 (create tx error)
13) Confirm LED3 is illuminated.

NOTE: If the test does not pass, try repeating steps 6-12 for the 180 degree phase of the forwarded clock vs parallel data by setting USER_DIP[3] = 1.