DDR2 SODIMM Test Setup Information:

- Arria II GX FPGA Development Board (PCIe) - DDR3 SODIMM x64Test
- Arria II GX Device EP2AGX125EF35
- DDR2 200-pin SODIMM (J7)
    - Micron Part Number: MT41J64M16LA-15E
    - Size: 1Gb (128Meg x 8)
    - Max Memory Speed: 400MHz (800Mb/sec)
- Quartus II Version 9.0 SP2
- MegaWizard: DDR and DDR2 SDRAM High-Performance Controller V9.0
- The clock source is the 100MHz on-board oscillator (CLKIN_BOT_P/ CLKIN_BOT_N)
- DDR2 SDRAM Test Frequency: 300MHz
- Local Interface Clock Frequency: Half-Rate Mode (150MHz)
- Memory Width: 64-bit running in x9 mode
- DDR2 SDRAM On-Die Termination : ON

Test Status Information:

- LED2 indicates test completed. This LED will appear to always be on, but toggles high when the test completes.
- LED3 indicates that an error occurred when illuminated and will remain on until the Error-Control -> Clear button is pressed in the GUI.
- The Clear button will reset the test and clear any errors.

The DDR3 SDRAM controller used in this demonstration was created using the Altera® :DDR and DDR2 SDRAM High-Performance Controller V9.0 MegaWizard. The memory data-bus is 64-bits wide, running at 300MHz. With a half-rate mode the controller and user interface logic run at half the speed of the memory clock interface.