

Arria-II GX PCIe board BTS System Installation and Use

Introduction

The BTS System is a demonstration of several tests that can be run from a Graphical User Interface. Included with this package is an external power monitor that can be used with an external USB Blaster to examine power usage of the FPGA running any given design. This document can be used for either the Arria-II GX PCIe Development Kit.

Requirements

- Full installation of either the
 - Quartus II 9.0 sp2 or Quartus Programmer 9.0 sp2
- For the BTS Demo
 - The Development Board, Power Supply and USB Cable all plugged together as they are at the end of going through the User Guide for the kit
- MAX-II should be ver8 or above

Installation:

1. Quartus II 9.0sp2 or Quartus Programmer 9.0sp2 is required. The latest Quartus II is available from Altera.com.
2. Locate BTS application where does not contain white space in its full path. For example, Desktop may contains white space, so please do not locate program at desktop.

Uninstalling:

1. Delete the installation files and folder
2. No registration change needed.

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Setting up the board for the BTS System

The system should be set up as it was at the end of the processes outlined in the Kit User Guide as shown in figure 1-1



Figure 1-1-1

Dipswitch setting

User need to set JTAG chain to be able to see MAX-II device in it.
In order to access MAX-II device, user need to set dipswitch on the back of the board.

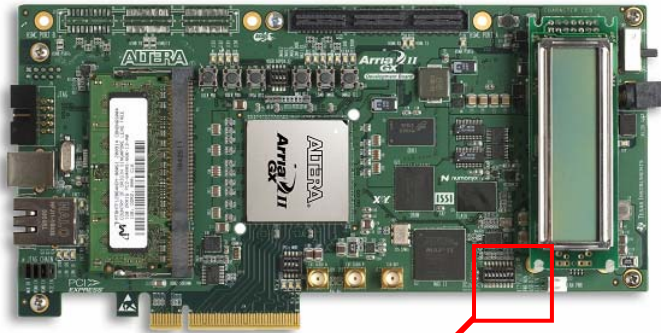
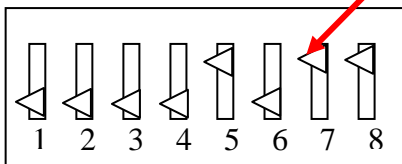


Figure1-1-2
SW4



Other dipswitches don't affect to this Power Monitor Tool.

Opening the BTS Graphical User Interface

To load the Graphical User Interface, browse to where the BTS section was installed and double click on BoardTestSystem.exe. You should see something similar to Figure 1-2.

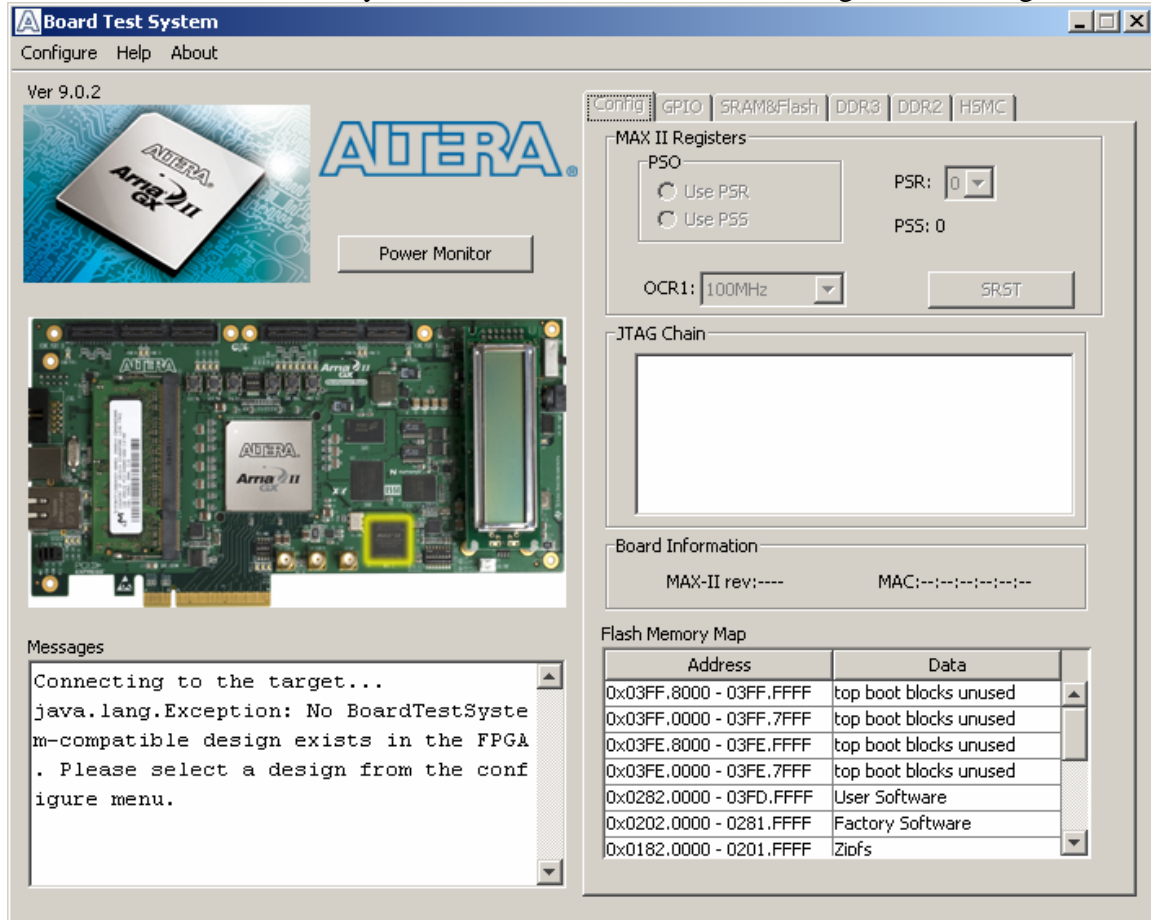


Figure 1-2

With no FPGA design or without BTS design in FPGA, GUI will tell “Program could not find a system in FPGA. Please reconfigure” or “java.lang.Exception: Could not find configured device EP2AGX125” as you can see in the above figure 1-2.

Programming the FPGA with the BTS design

From the menu bar select "Configure" menu as shown in Figure 1-3

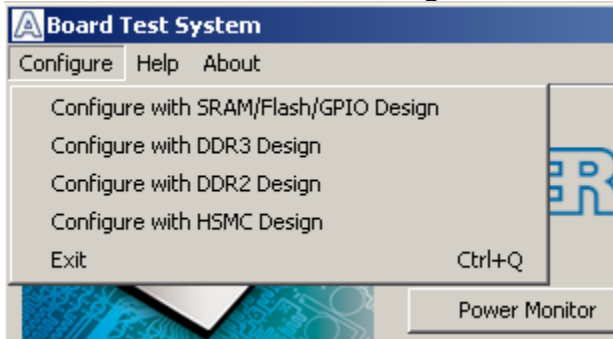


Figure 1-3

Select project to configure.

The following window will pop-up as in Figure 1-4.

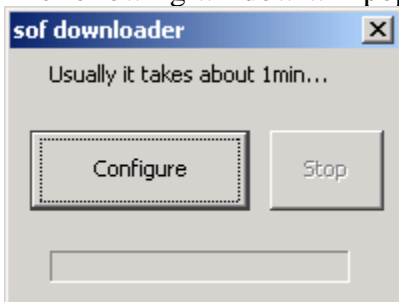


Figure 1-4

Click on the "Configure" button to start downloading. It will take about 60sec to download and configure the FPGA.

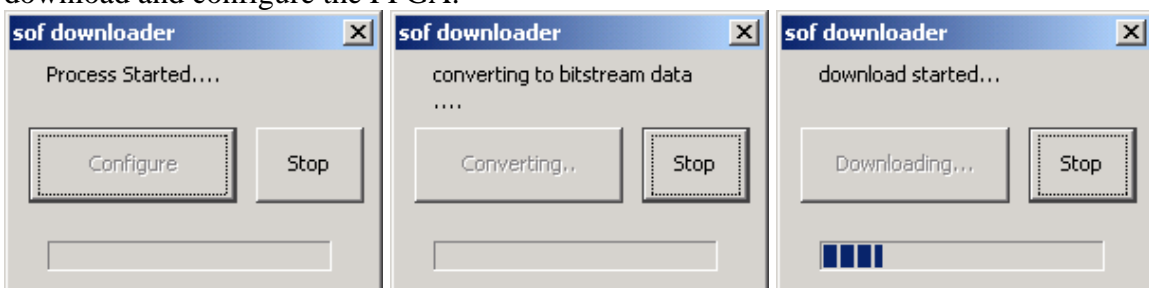


Figure 1-5

First, downloader will convert sof file to bitstream, then download the bitstream data to FPGA. Once the download started, the progress bar will show the current status. After finishing download, the button says Connecting.. and change to Close. Now all configuration process is done. Close the pop-up window.

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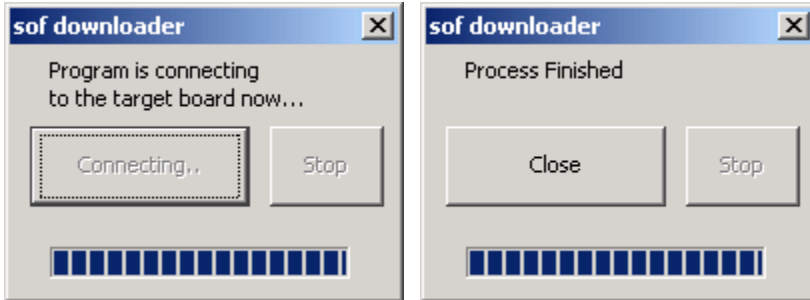


Figure 1-6

The GUI program and board are synchronized and ready to use. You should be able to see the information window displaying Detected “Projec name” similar to Figure 1-7 as well as JTAG Chain list in right window. In this picture, GPIO, SRAM, Flash project has detected in the FPGA.

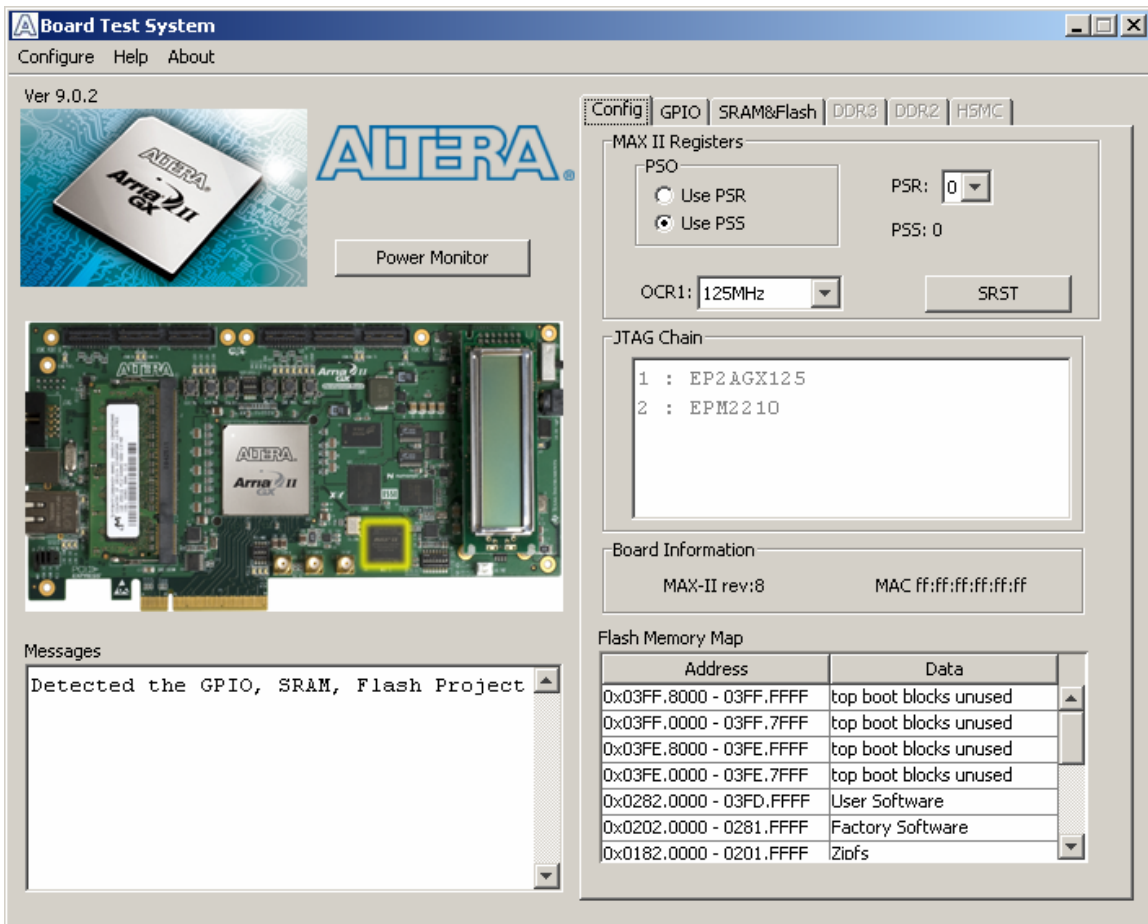
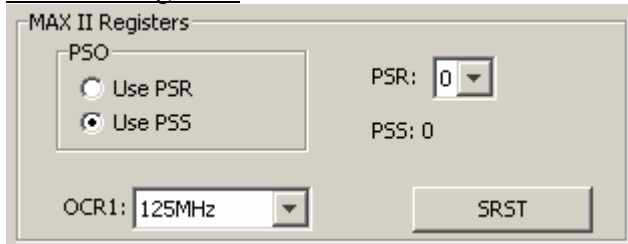


Figure 1-7

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The Config Tab

MAX-II Registers



User can see the current registers and can control it from GUI.

User can set SRST, PSR, PSO.

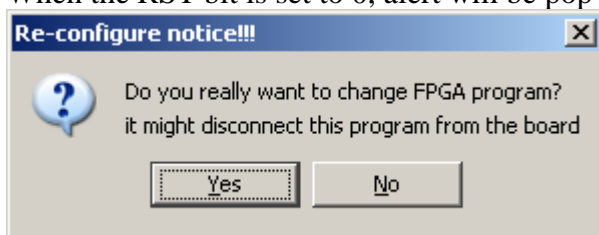
SRST : W only Software Reset 0: reconfigure request

PSR : R/W Page Select Register 0 – 7 pages to load from Flash

PSO : R/W Page Select Override 0: register setting 1: rotary switch setting

PSS : R only Page Select Switch 0 – 15 this is the value from rotary switch

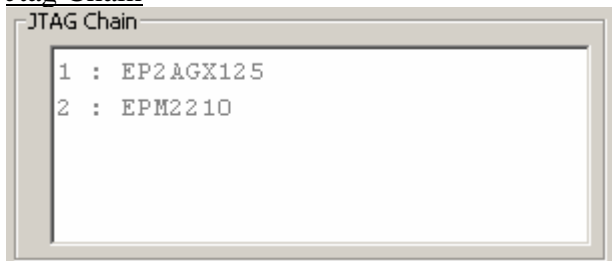
When the RST bit is set to 0, alert will be pop up.



This is because if you change the program, you will lose the connection to the board.

This GUI only can go with specific FPGA program.

Jtag Chain

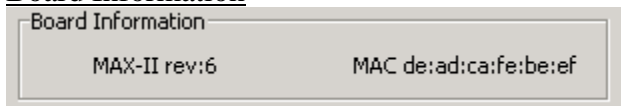


All the device in a JTAG Chain will be displayed in here.

The Stratix-IV device is always on the top. By changing JTAG dipswitch, SW4,

EPM2210 can be disappeared.

Board Information



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MAX-II rev : this is a version information of MAX-II device.

MAC : this is the MAC address assigned to this board. The information is in Flash device.

Flash Memory Map

Flash memory map

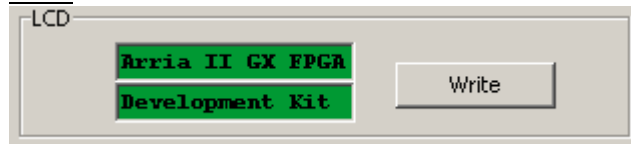
| Address | Data |
|-------------------------|------------------------|
| 0x03FF.FFFF - 03FF.8000 | top boot blocks unused |
| 0x03FF.7FFF - 03FF.0000 | top boot blocks unused |
| 0x03FE.FFFF - 03FE.8000 | top boot blocks unused |
| 0x03FD.7FFF - 03FD.0000 | top boot blocks unused |
| 0x0282.0000 - 03FC.FFFF | User Software |

This map is currently hard coded.

It may be read from Flash

The GPIO Tab

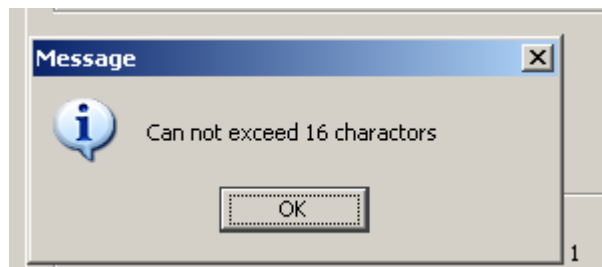
LCD



Read and Write function for the 16x2 character LCD display.

User can change it from GUI and reflect it to LCD display.

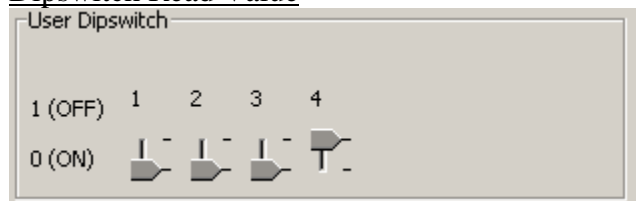
If something is already there, user can read it from LCD display and show it in GUI.



User can enter up to 16 characters for each line.

If it exceed, you'll alert.

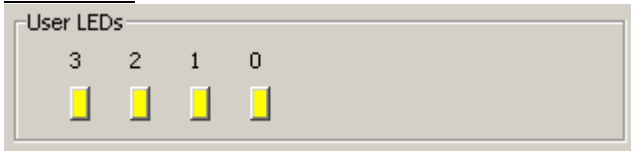
Dipswitch Read Value



GUI reads User Dipswitch data constantly.

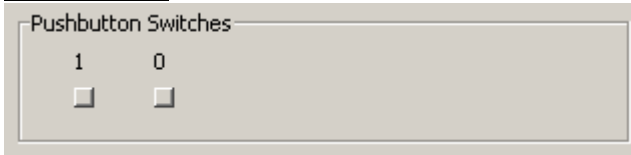
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User LED



Displays current user LED status.
Also, user can control LED by pressing button.
Yellow is turning on, light gray is turning off.

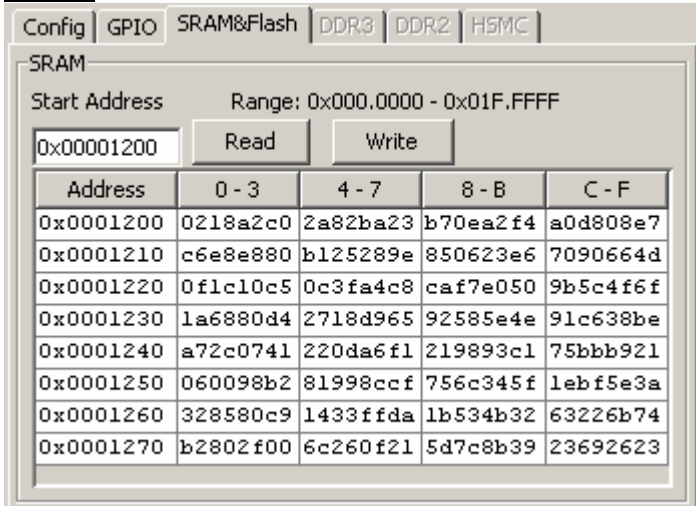
Push buttons



Displays user push button status.
If button is pushed, the GUI button will be dent.

The SRAM&FLASH Tab

SRAM

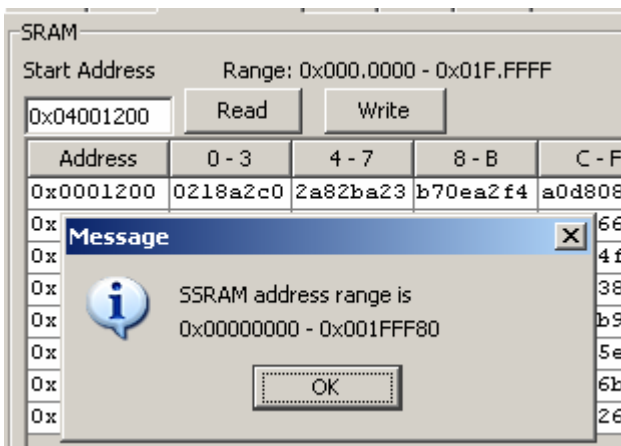


User can read and write to SRAM.

Also, user can specify the start address to read/write.

User can change table. When the modification finishes, hit Write button to write data into SRAM.

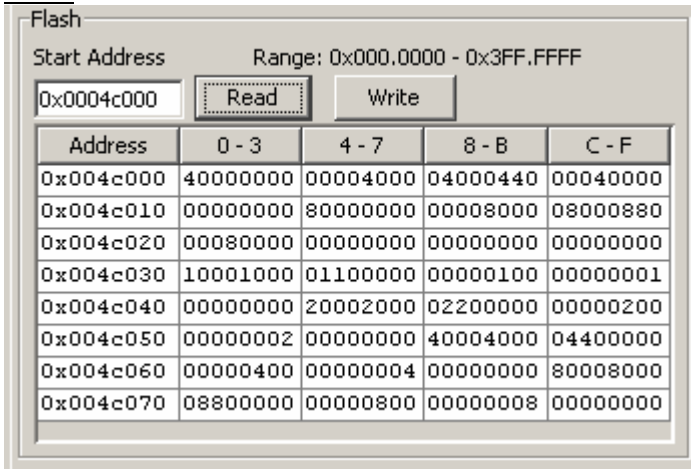
The address range is currently 0x00000000 to 0x001FFF80



If the address is out of range, alert will pop up.

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Flash



User can read Flash data.

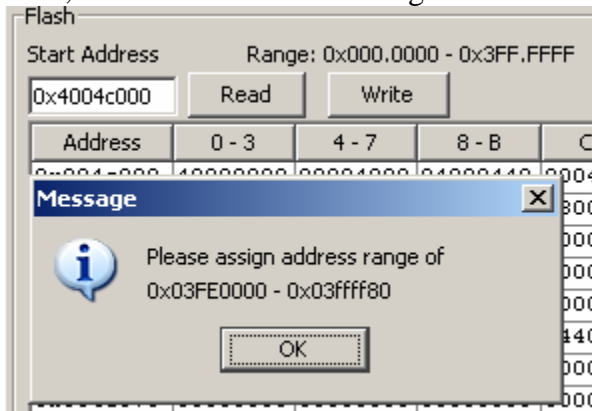
Currently write function is not yet implemented.

The Flash address range is 0x00000000 – 0x3FFFF80



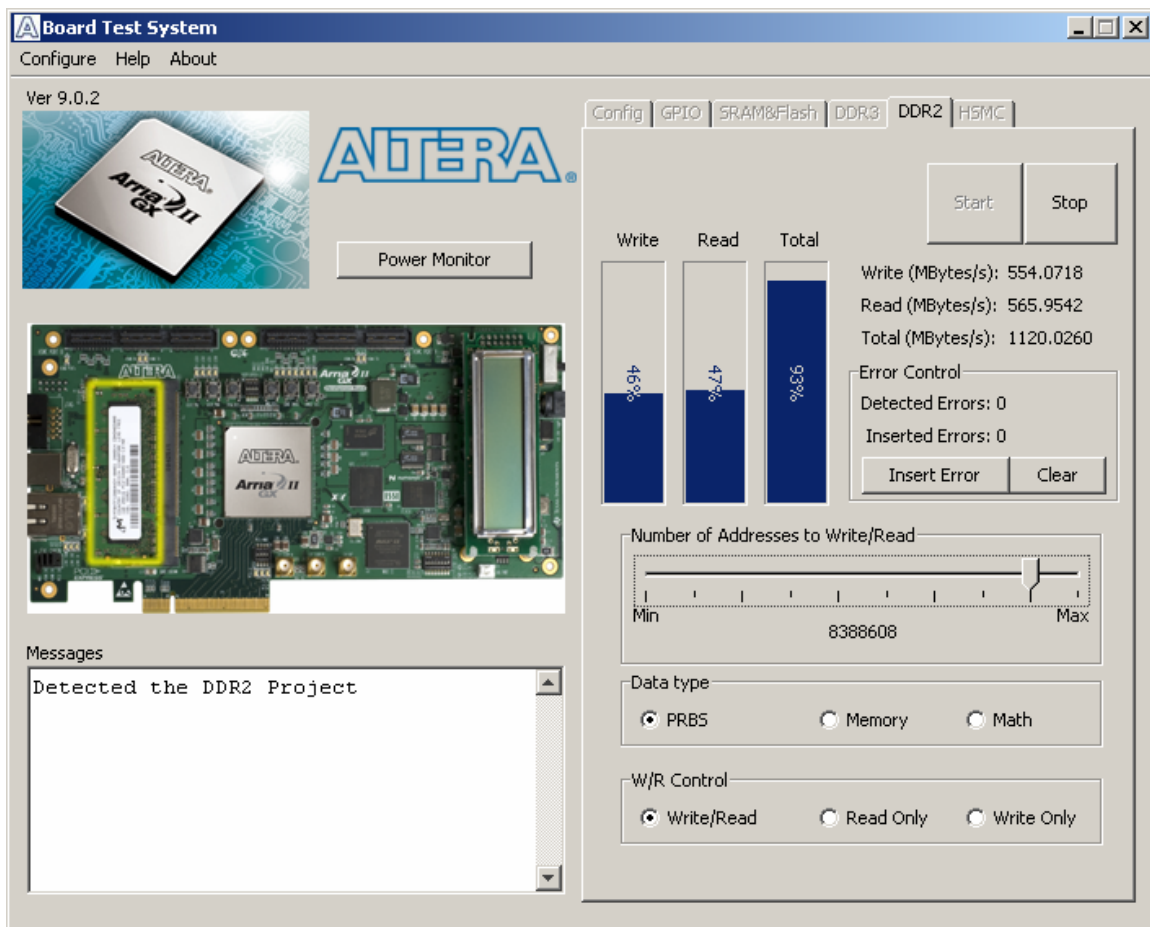
If the specified address is out of range, alert will pop up.

Also, flash writable address range is from 0x03FE0000 to 0x03FFFF80



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The DDR2 Tab



Start button will start test process. Tx, Rx or both progress bar will go up and show the percentage to maximum possible performance.

Tx counter and Rx counter or both should display the Mega-Transaction per second that the current transaction performance.

Stop button will stop test process.

Error Section

Insert Error button will insert 1 word error at a time. User can check how many errors has inserted by user by checking Inserted error counter. The Detected error counter is actually detected errors at hardware.

Clear button will clear both Detected error and inserted error counters.

Data Size slider will enable user to select size of data to transmit at a time.

User can select from size of 2 to 524288.

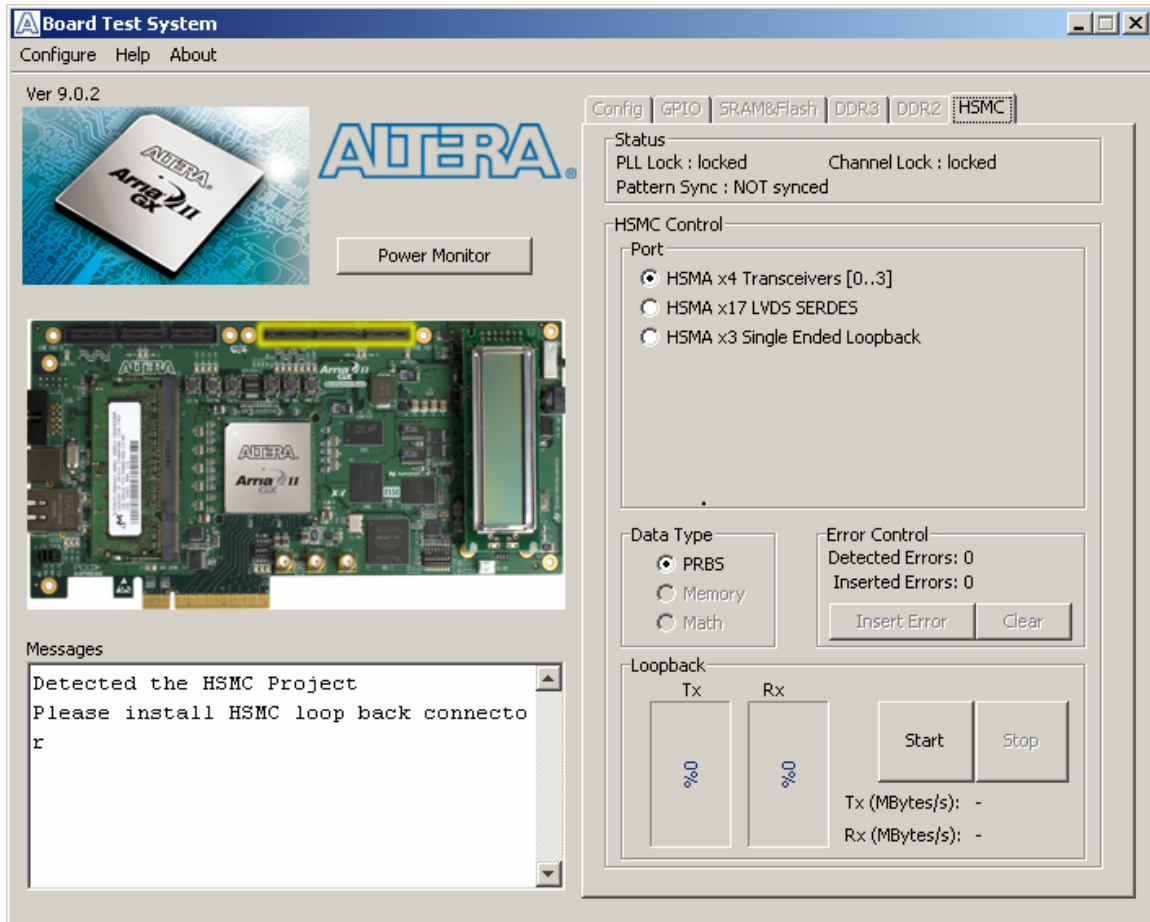
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Data Type Section

User can select data type from

- PRBS
- Memory
- Math

The HSMC Tab



Status Section

- PLL Lock Status
- Channel Lock Status
- Pattern Sync Status

Port Section

0. HSMC x4 Transceivers [0..3]
1. HSMC x17 LVDS SERDES
2. HSMC x3 Single Ended Loopback

Data Type Section

- PRBS
- ~~Memory~~
- ~~Math~~

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Error Control Section

Insert Error button will insert 1 word error at a time. User can check how many errors has inserted by user by checking Inserted error counter. The Detected error counter is actually detected errors at hardware.

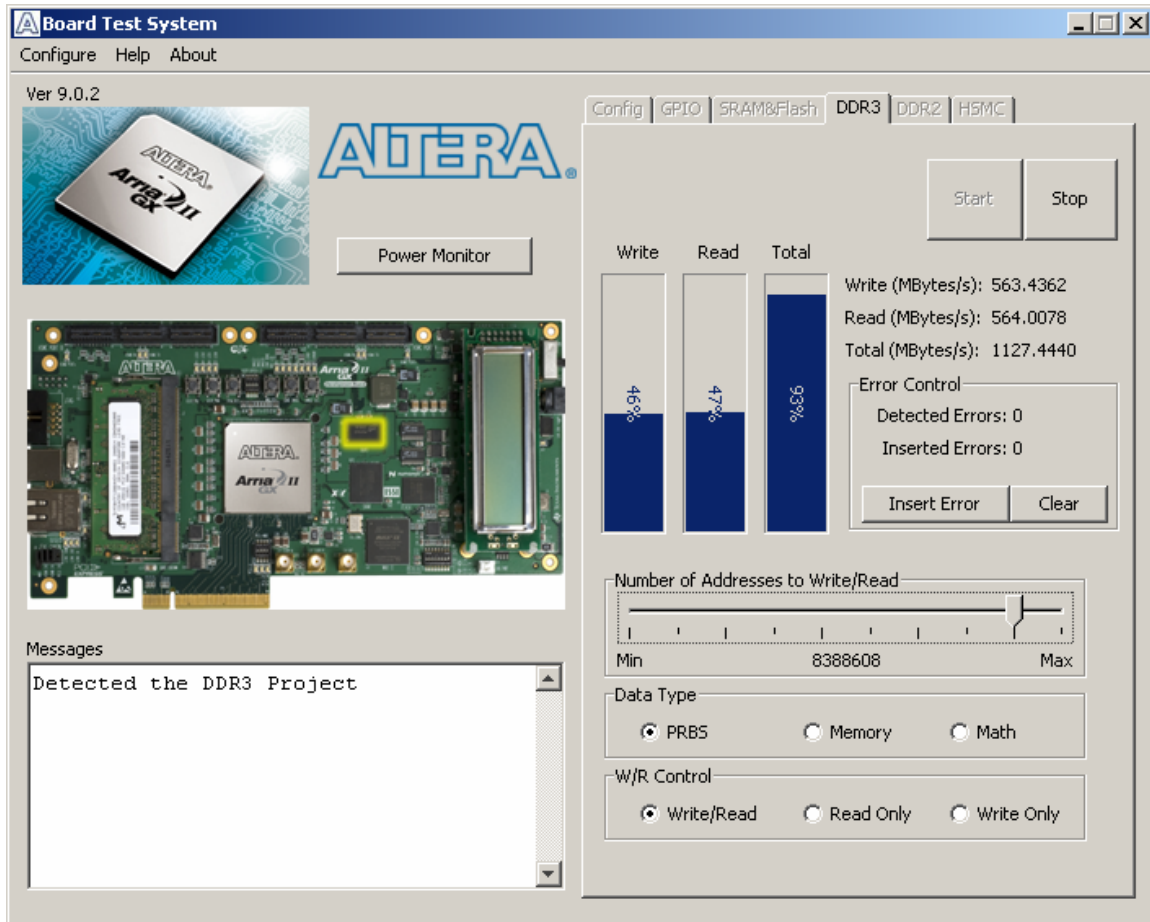
LoopBack Section

Start button will start test process. Tx, Rx or both progress bar will go up and show the percentage to maximum possible performance.

Tx counter and Rx counter or both should display the Mega-Transaction per second that the current transaction performance.

Stop button will stop test process.

The DDR3 Tab



Performance Section

Start button will start test process. Tx, Rx or both progress bar will go up and show the percentage to maximum possible performance.

Tx counter and Rx counter or both should display the Mega-Transaction per second that the current transaction performance.

Stop button will stop test process.

Error Control Section

Insert Error button will insert 1 word error at a time. User can check how many errors has inserted by user by checking Inserted error counter. The Detected error counter is actually detected errors at hardware.

Data Size slider

It will enable user to select size of data to transmit at a time.

User can select from size of 2 to 524288.

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Data Type Section

- PRBS
- Memory
- Math

R/W Control

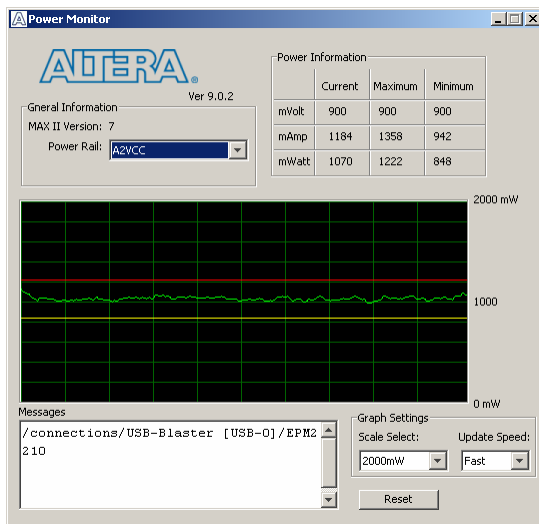
- Write after Read
- Read only
- Write only

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The External Tool



User can start Stand alone Power Tool from this GUI.

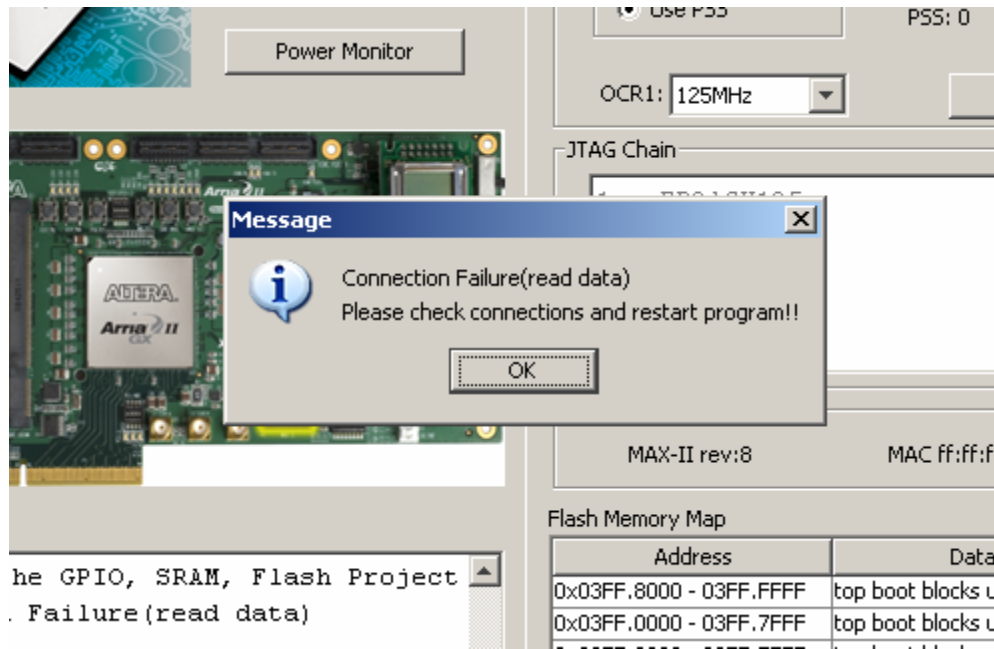


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The Connection error

When user change FPGA program or hit CPU_Reset button, the connection between GUI and the target board will be lost.

In this case, following alert will be pop up.



User need to closer or restart GUI.

Known Issues:

When you hit CPU RESET button, or Config button, program will stack and will no response.

If this happens you will not be able to close window at all.

In this case, open task manager, go to process tab. Find "javaw" process, and terminate it.