

FPGA Package Top View

Notes:

- FPGA Schematic Symbol Breakdown:
 - (A) Banks 3A
 - (B) Banks 3B (EP2AGX260)
 - (C) Banks 4A,4B
 - (D) Banks 5A
 - (E) Banks 5B (EP2AGX260)
 - (F) Banks 6A
 - (G) Banks 6B (EP2AGX260)
 - (H) Banks 7A,7B
 - (I) Bank 8A
 - (J) Clocks
 - (K) Configuration
 - (L) Power
 - (M) IO Power
 - (N) GND1
 - (O) Transceivers
 - (P) Transceiver Power
- Board can support the EP2AGX125EF35 and EP2AGX260EF35 devices.

Symbol	Pin Type
	User I/O
	User Assigned I/O
	Fitter Assigned I/O
	Unbonded Pad
	Reserved Pin
	DEV_OE
	DEV_CLR
	DIFF_n
	DIFF_p
	DQ
	DQS
	DQSB
	CQ#
	Other PLL
	Other Dual Purpose
	CLK_n
	CLK_p
	GX_X*n
	GX_X*p
	MSEL0
	MSEL1
	MSEL2
	MSEL3
	CONF_DONE
	DCLK
	nCE
	nCONFIG
	DATA0
	TDI
	TCK
	TMS
	TDO
	nSTATUS
	nIO_PLLUP
	Other Dedicated Programming
	VREF
	VCCP/VCCR/VCC
	VCCA
	VCCIO
	GND
	RREF
	No Connect

BANK 6B
(EP2AGX260 only)
VCCIO = 2.5V
HSMC Port B

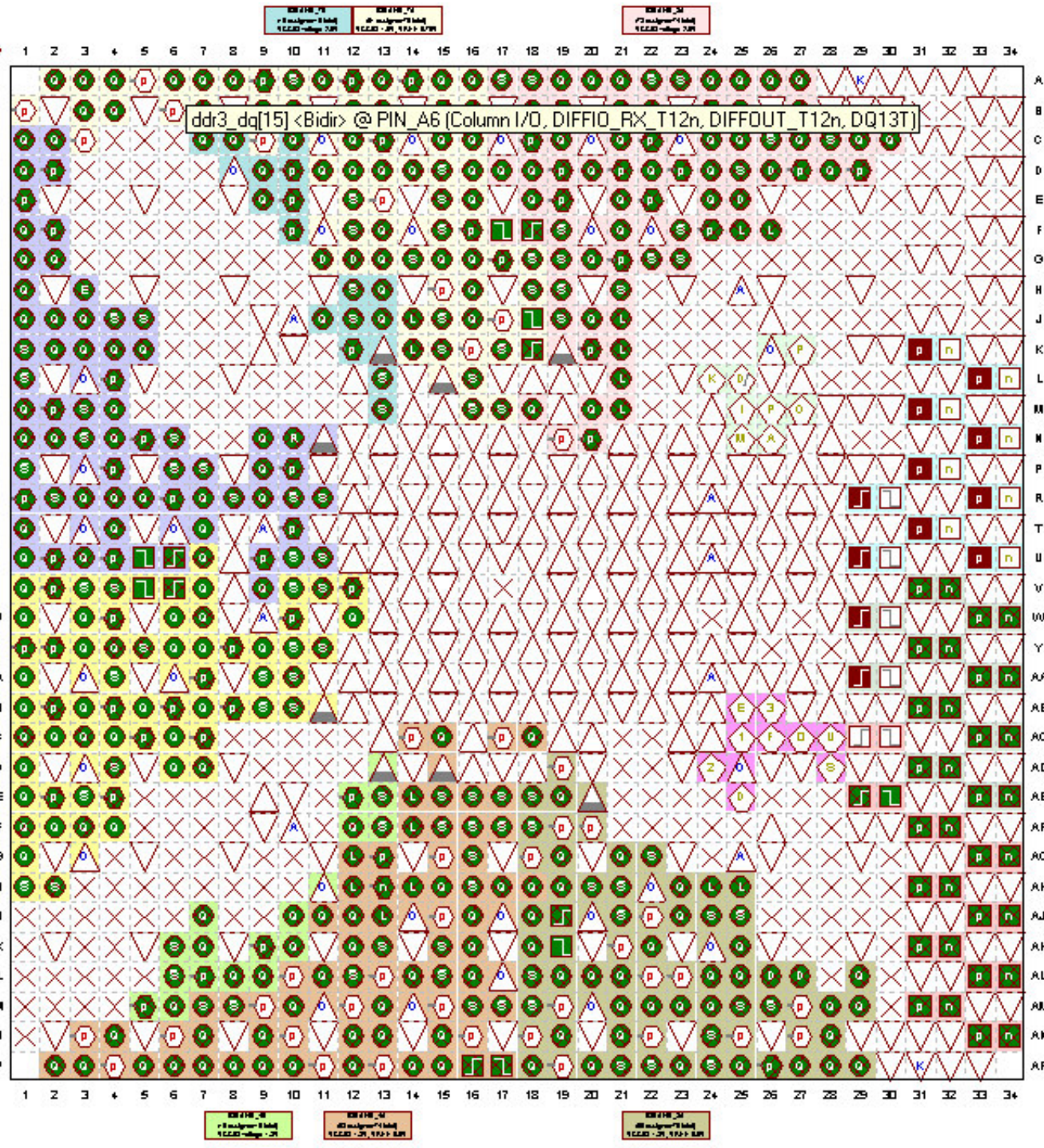
BANK 6A
VCCIO = 2.5V
HSMC Port A,
Flash Control, FSM Address,
LCD, DIP Switch, LEDs,
PCIe Control

BANK 5A
VCCIO = 2.5V
HSMC Port A

BANK 5B
(EP2AGX260 only)
VCCIO = 2.5V
HSMC Port B

BANK 7A
VCCIO = 1.5V
DDR3 Device (128MB)

BANK 7B, 8A
VCCIO = 2.5V
ENET, FSM Bus, SSRAM



XCVR BANK QR3 (EP2AGX260 only)
HSMC Port B x4

XCVR BANK QR2
HSMC Port A x4

XCVR BANKS QL0, QL1
PCI Express x8
PCIe REFCLK

BANK 4B
VCCIO = 1.8V
DDR2 SODIMM x64
Push-buttons

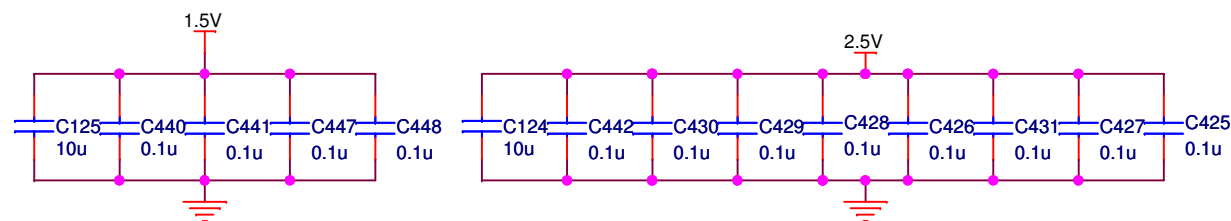
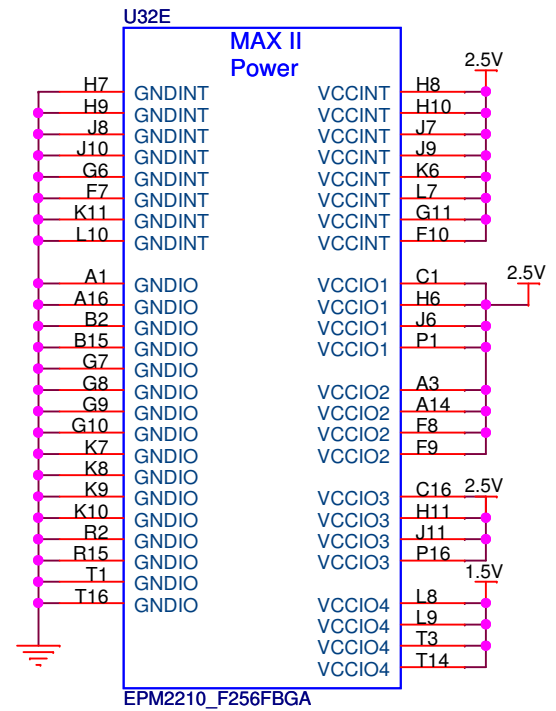
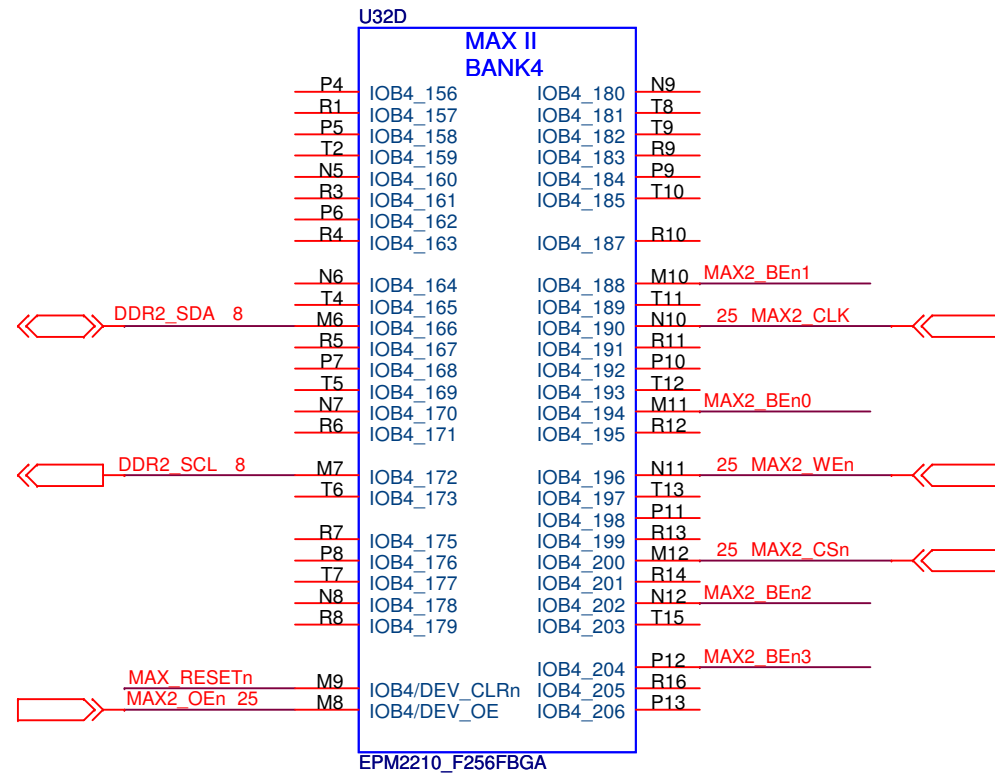
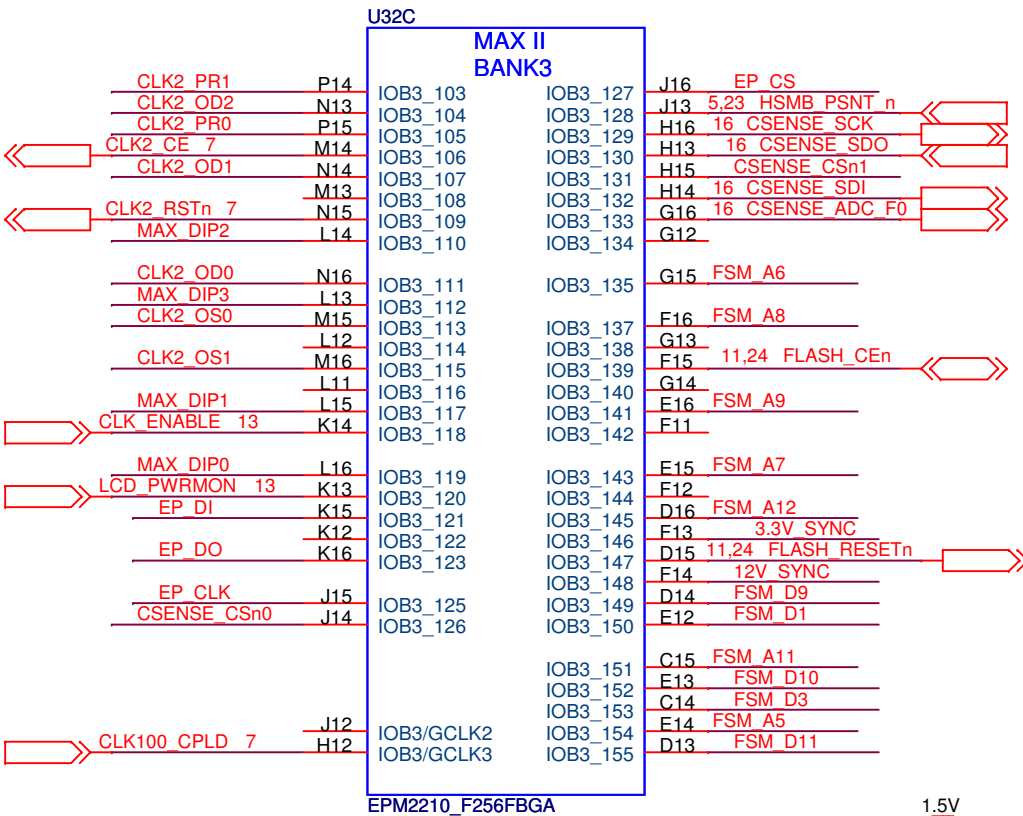
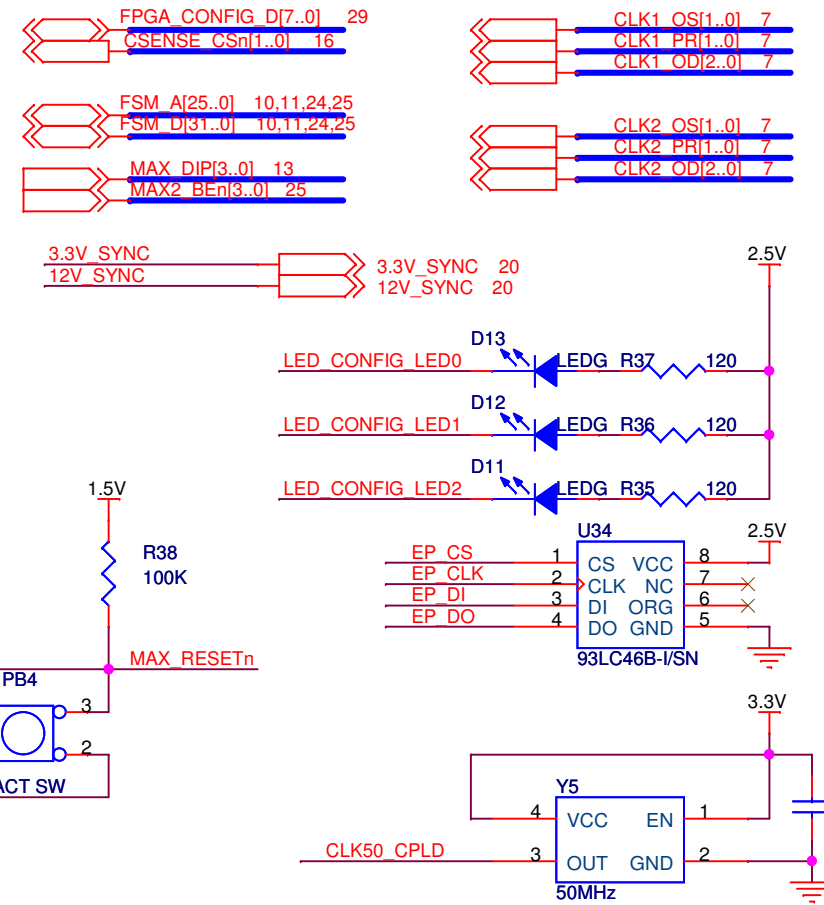
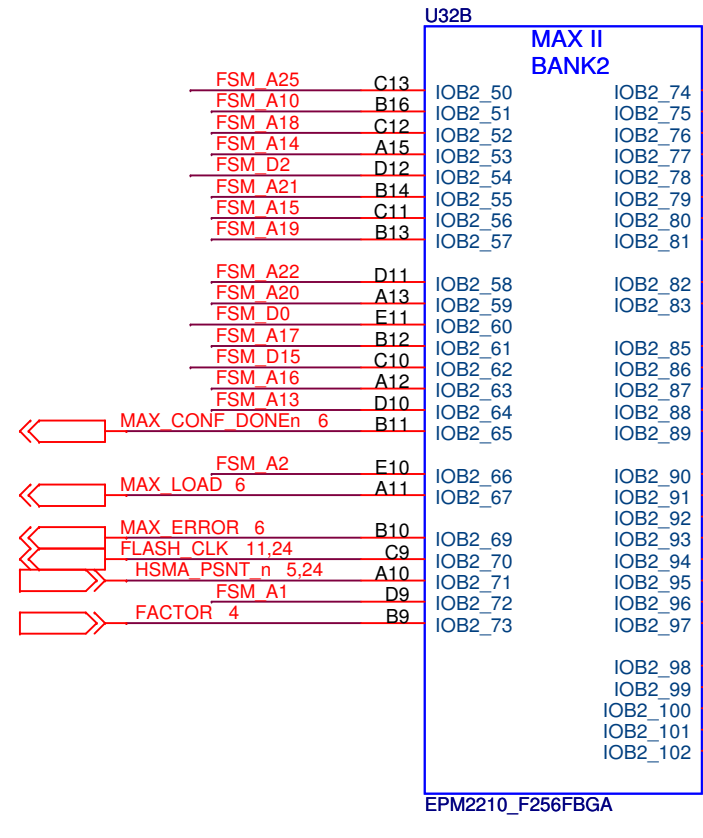
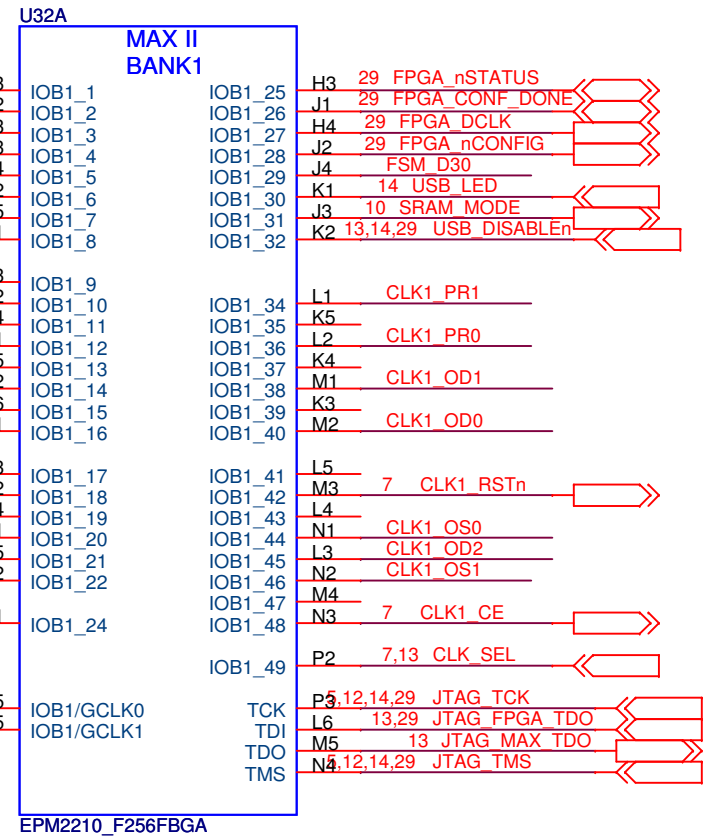
BANK 4A & 3A
VCCIO = 1.8V
DDR2 SODIMM x64

BANK 3B
(EP2AGX260 only)
VCCIO = 2.5V
HSMC Port B



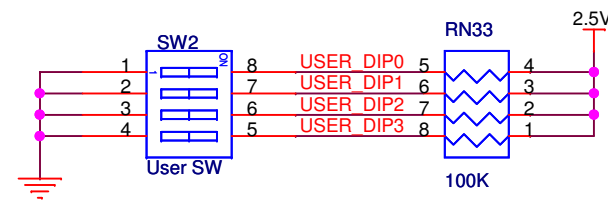
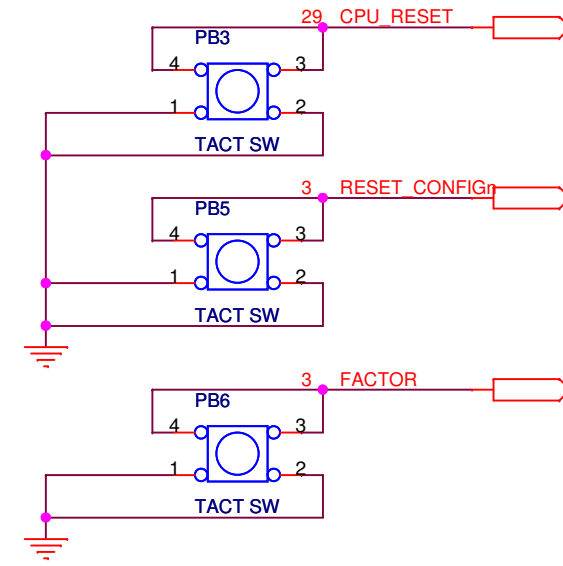
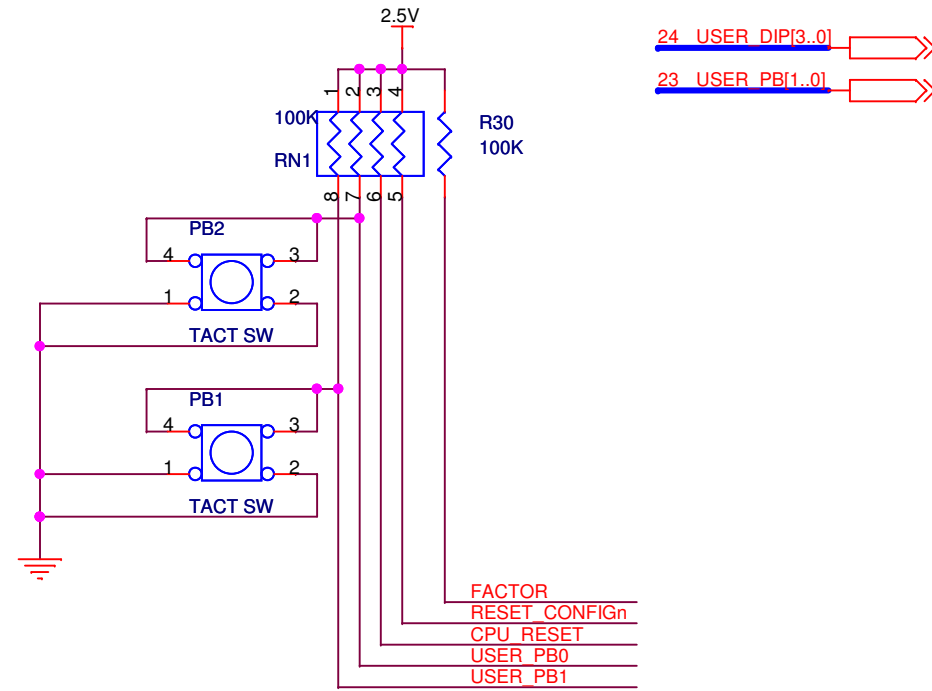
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MAX II EPM2210

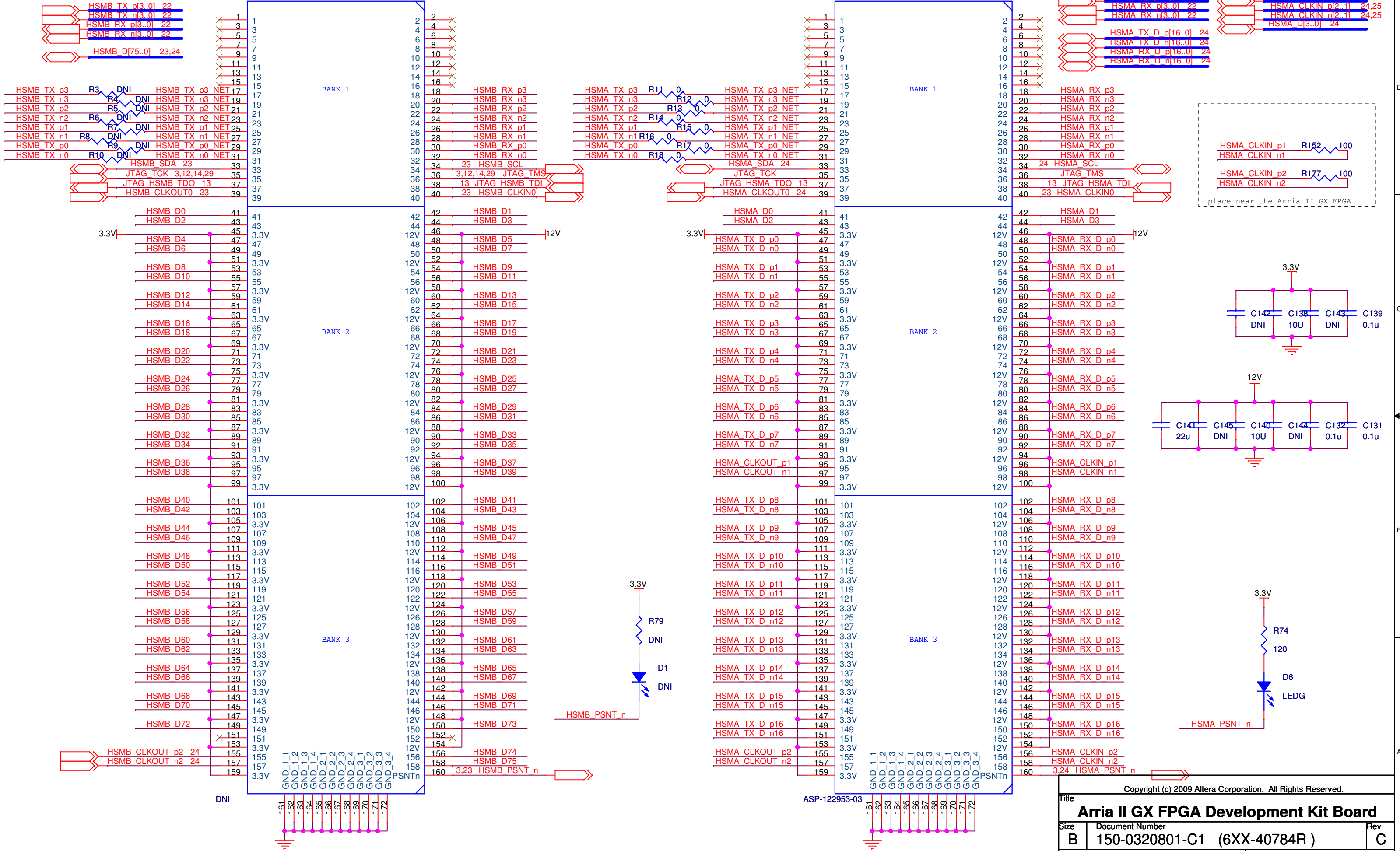


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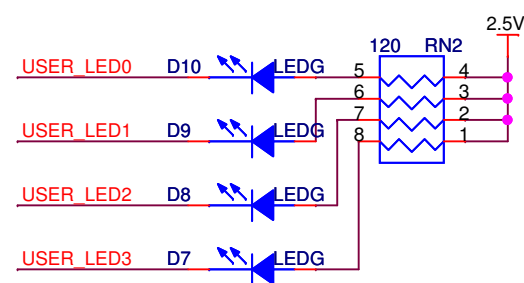
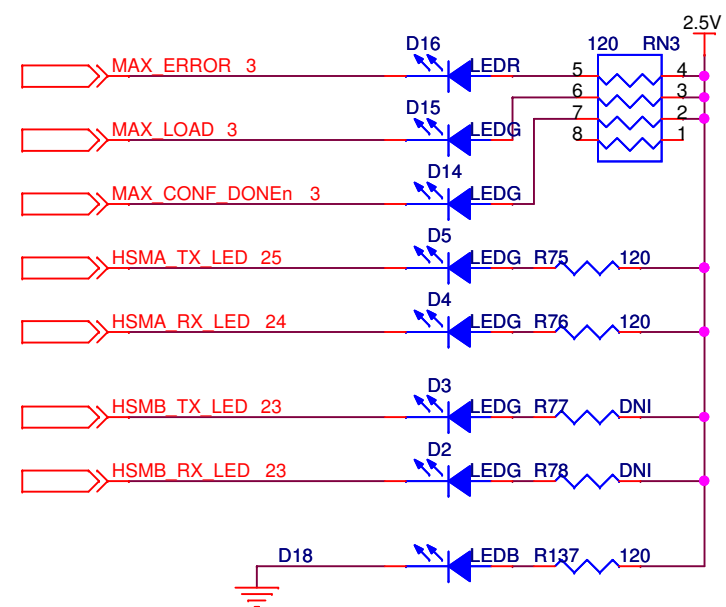
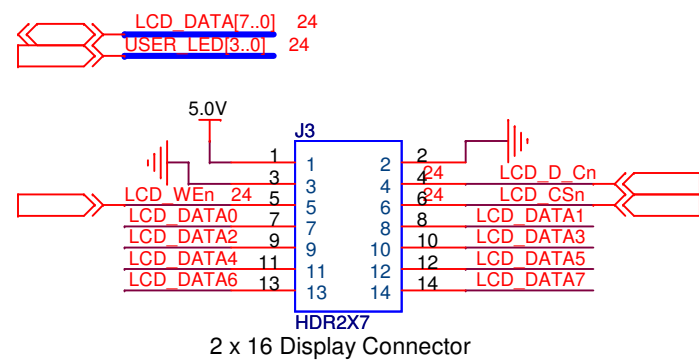
Buttons & Switches



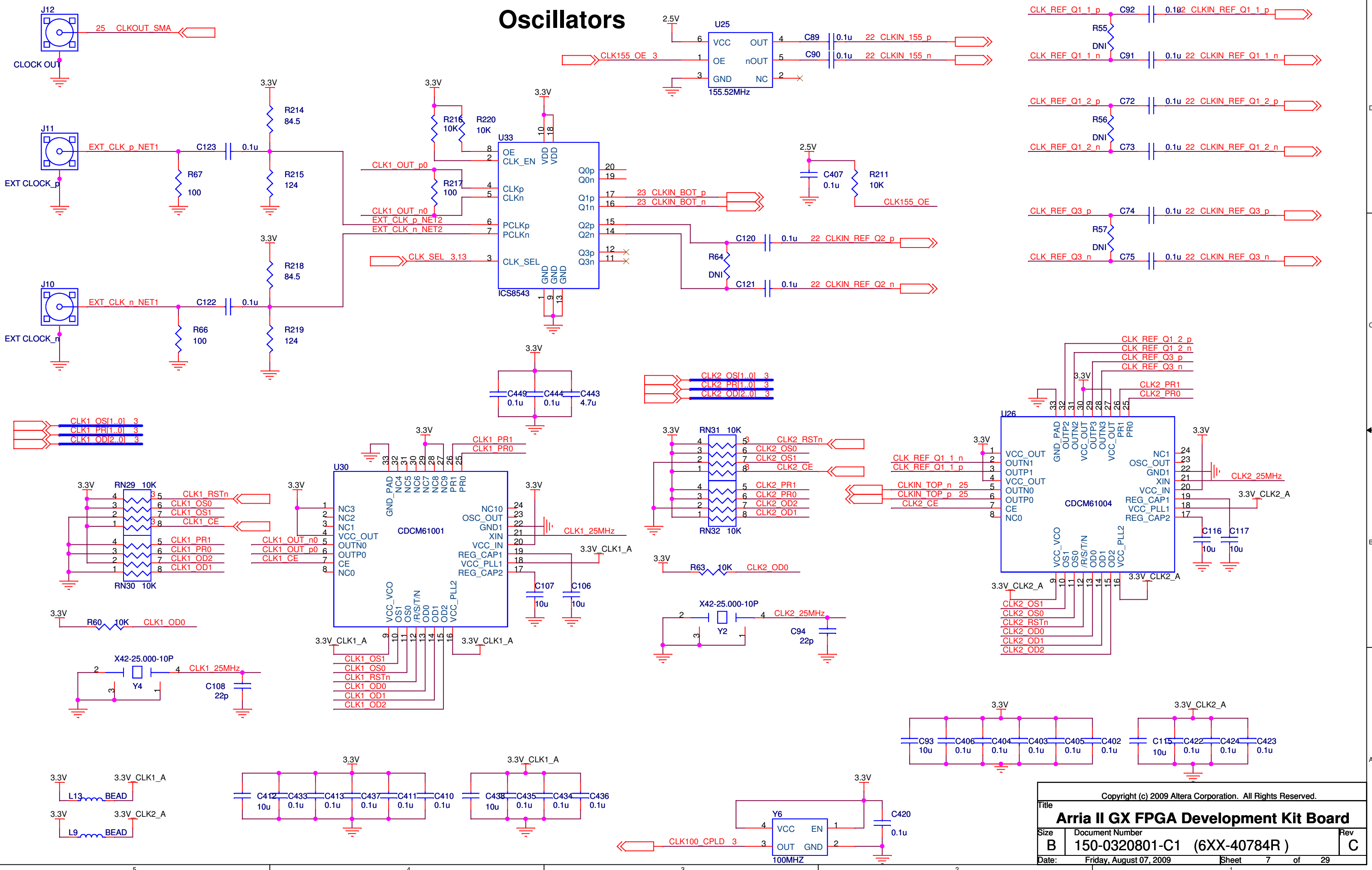
HSMC Port A & Port B



LCD & LEDs

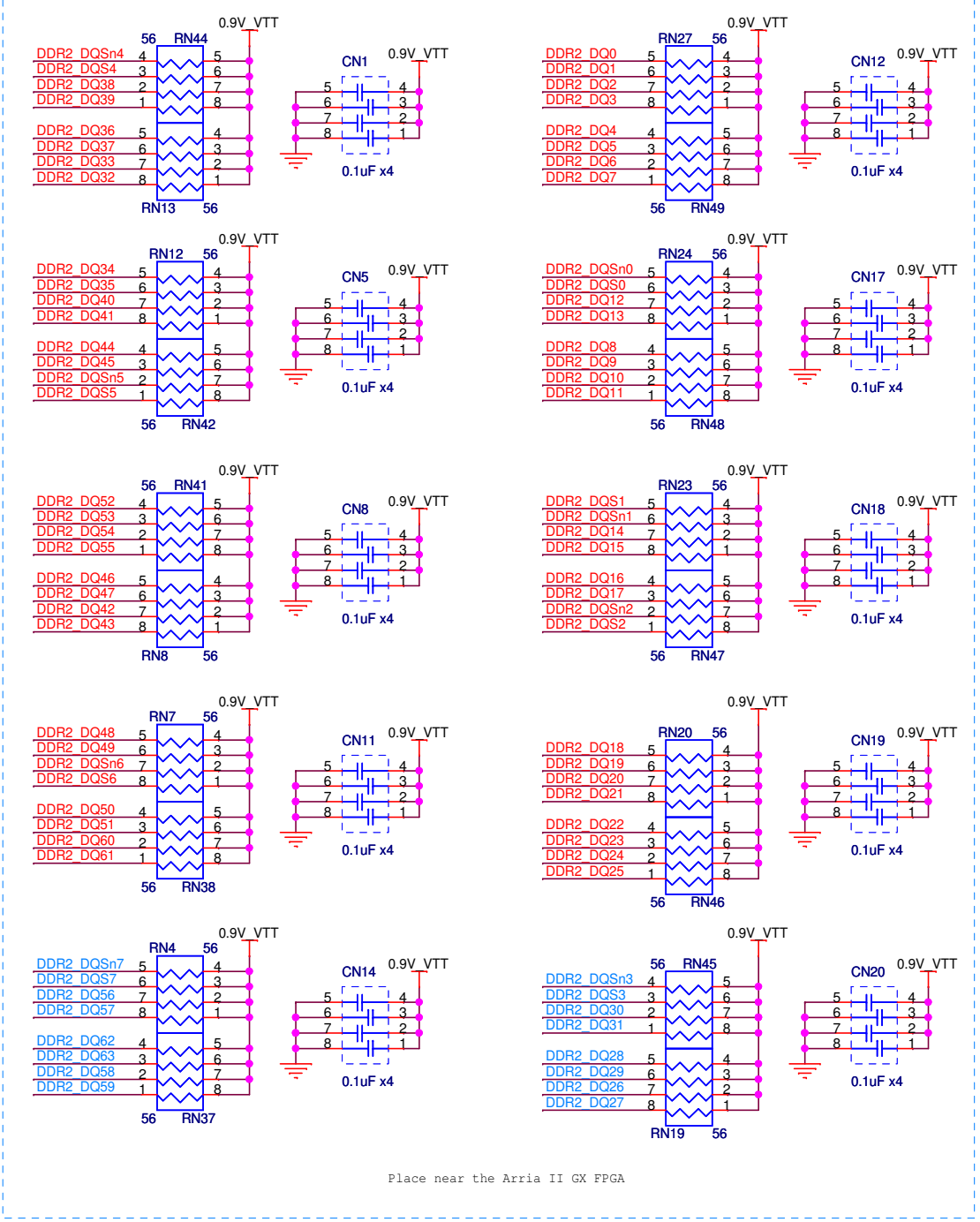


Oscillators

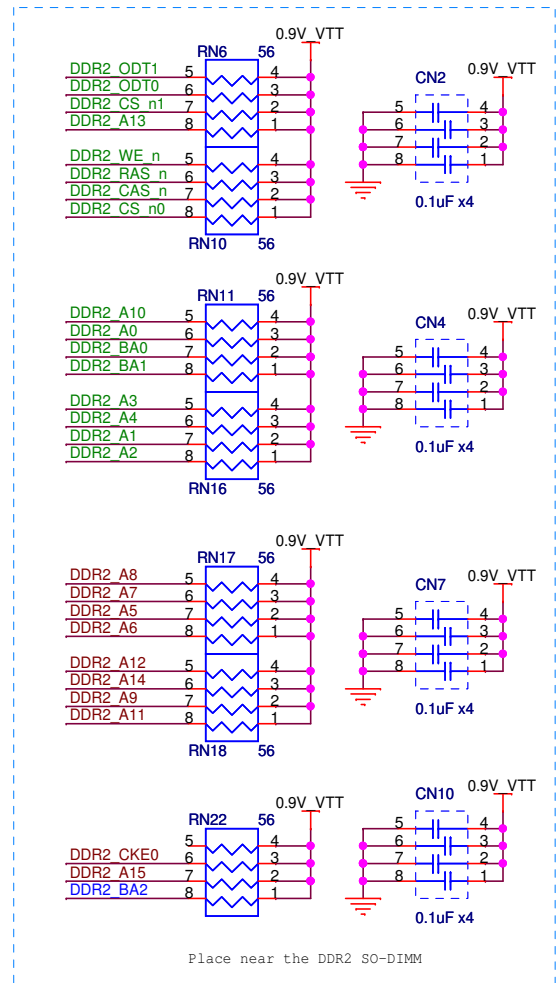
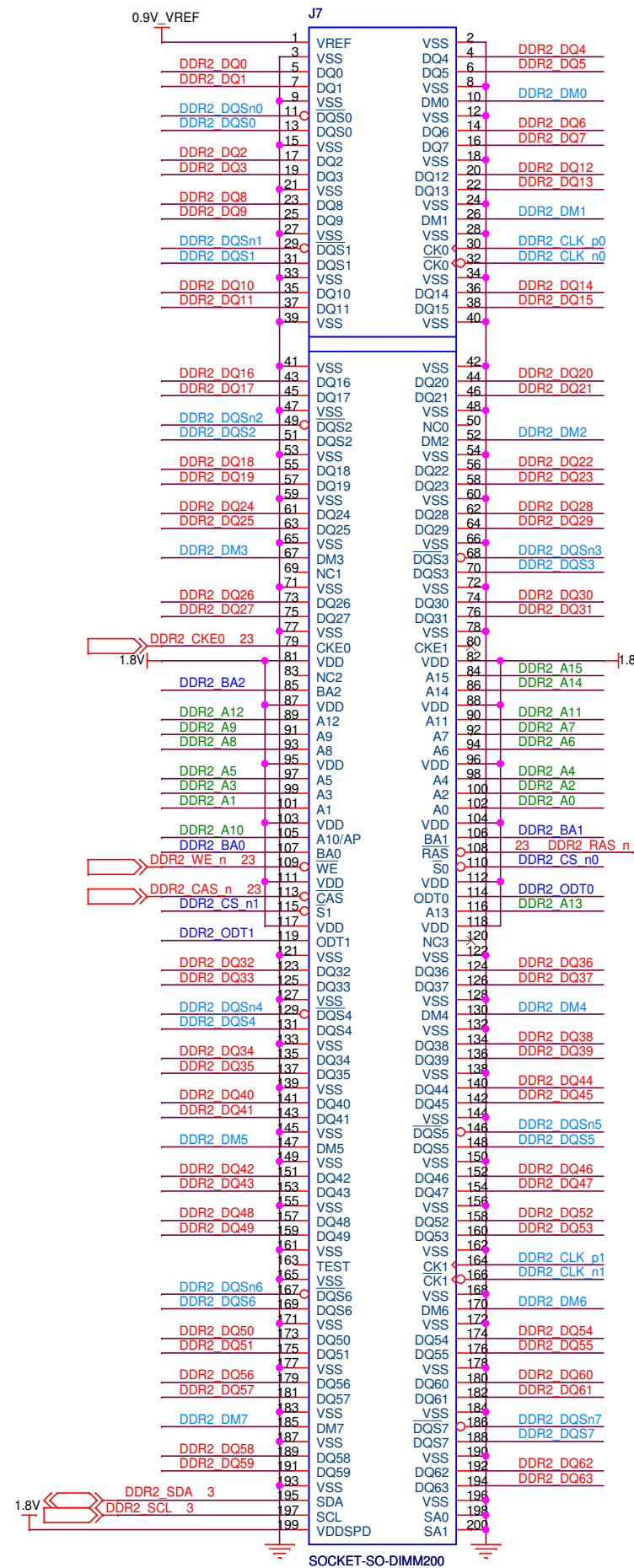
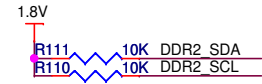


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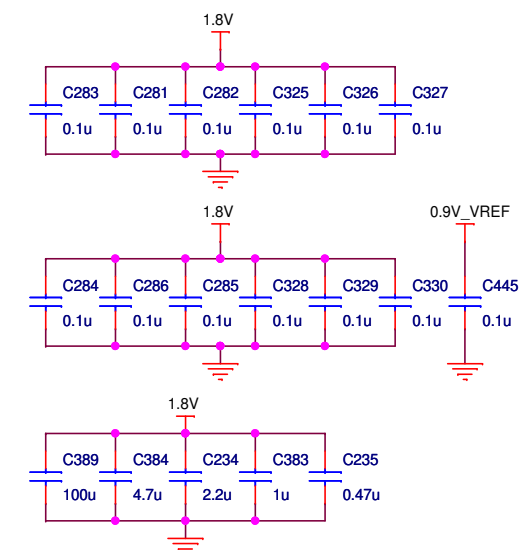
DDR2 SO-DIMM



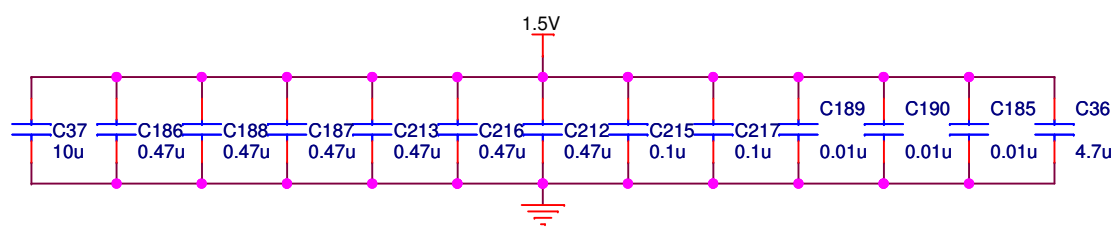
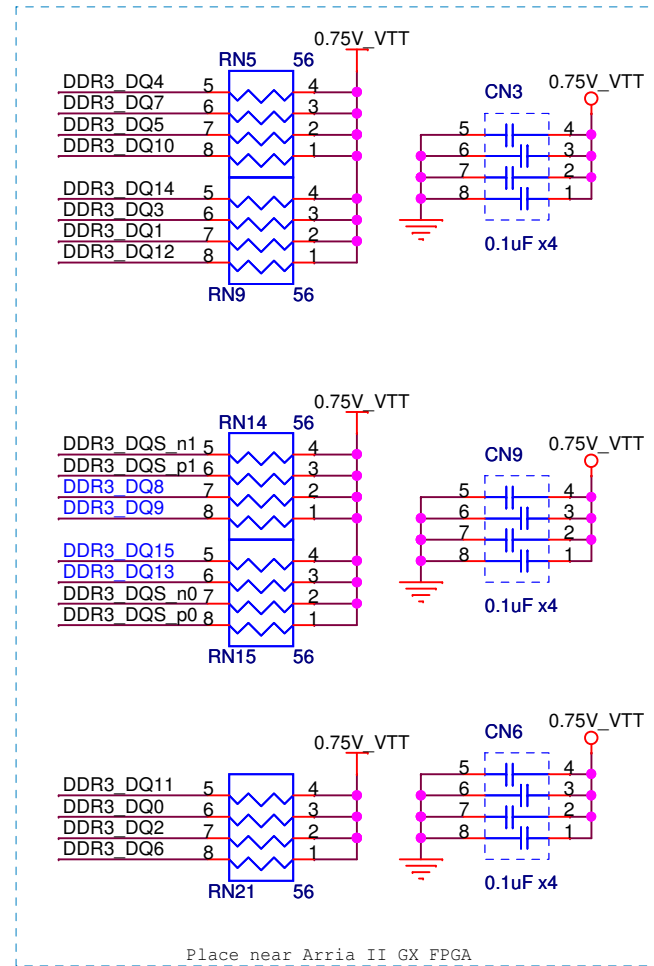
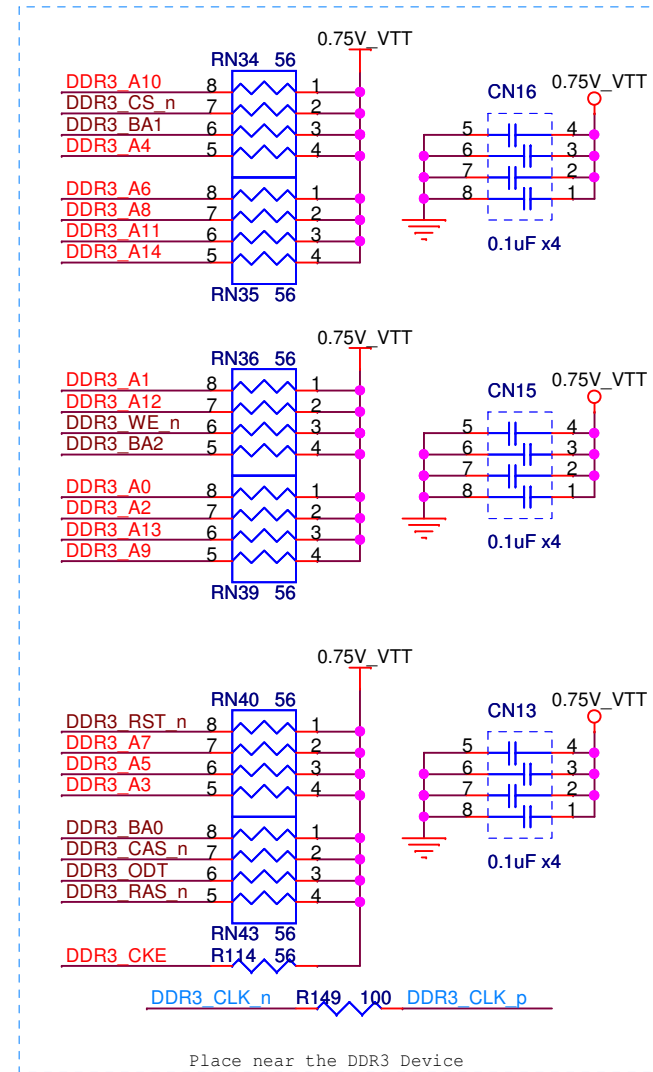
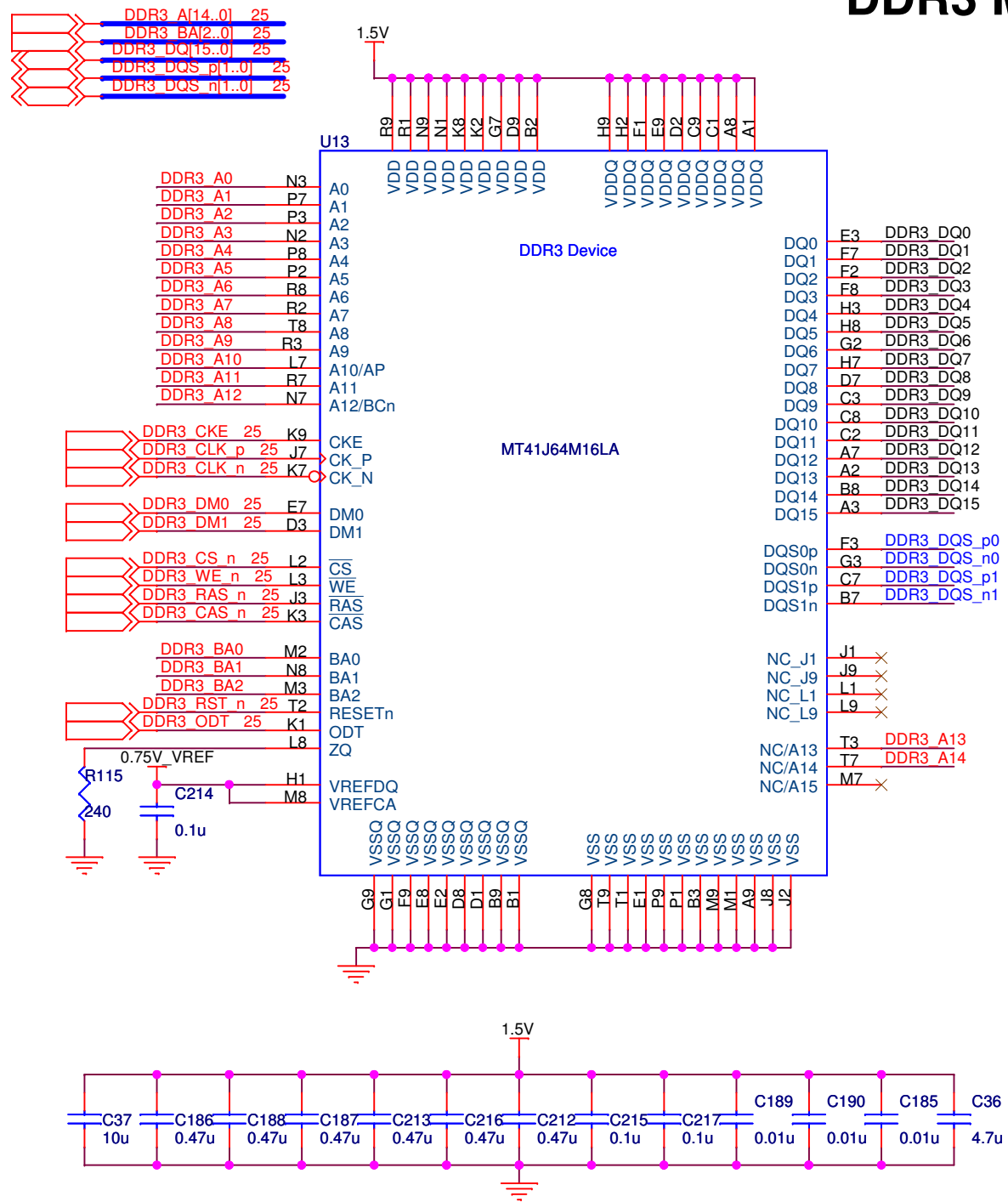
Place near the Arria II GX FPGA



Place near the DDR2 SO-DIMM



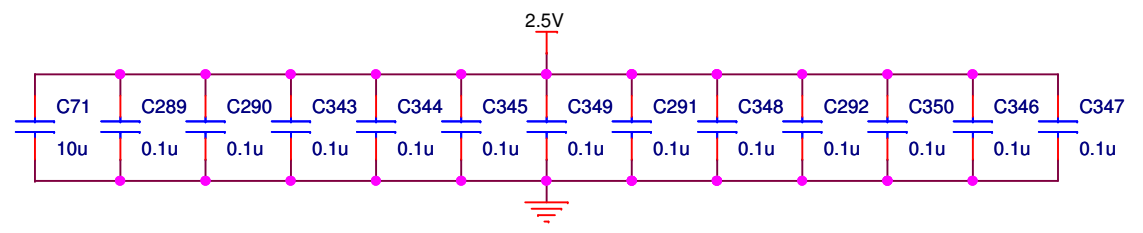
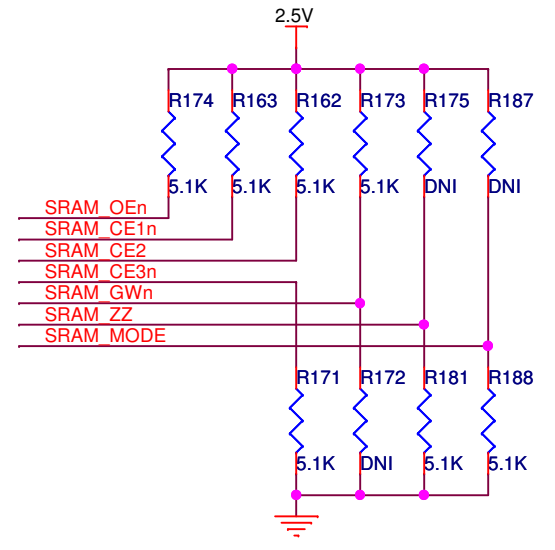
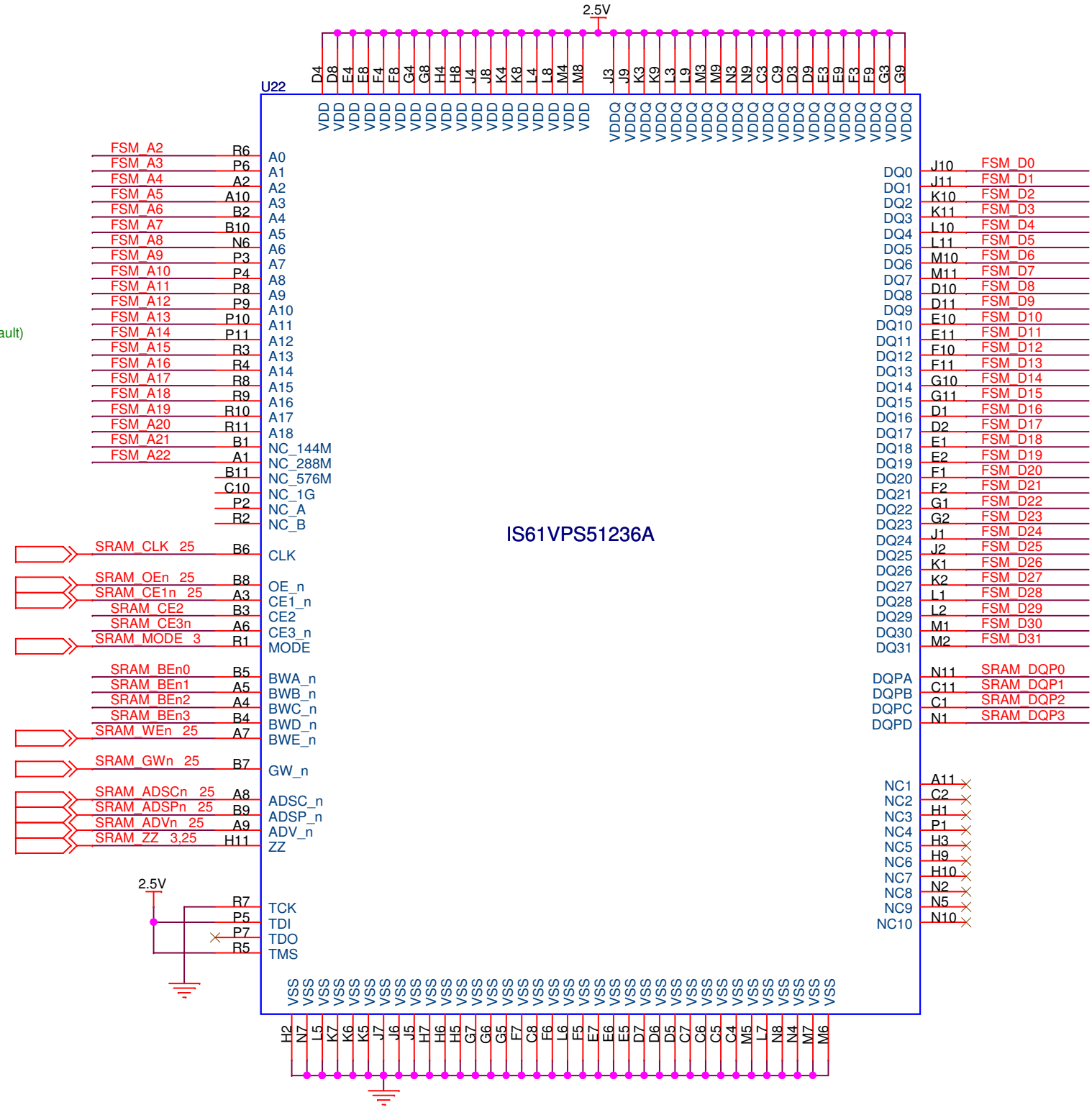
DDR3 Memory Device



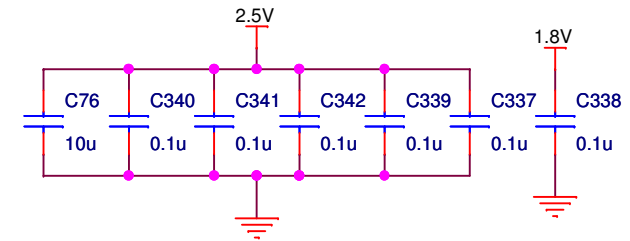
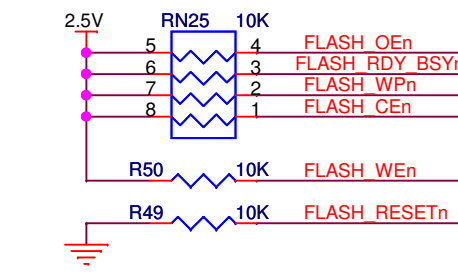
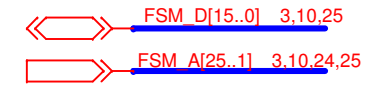
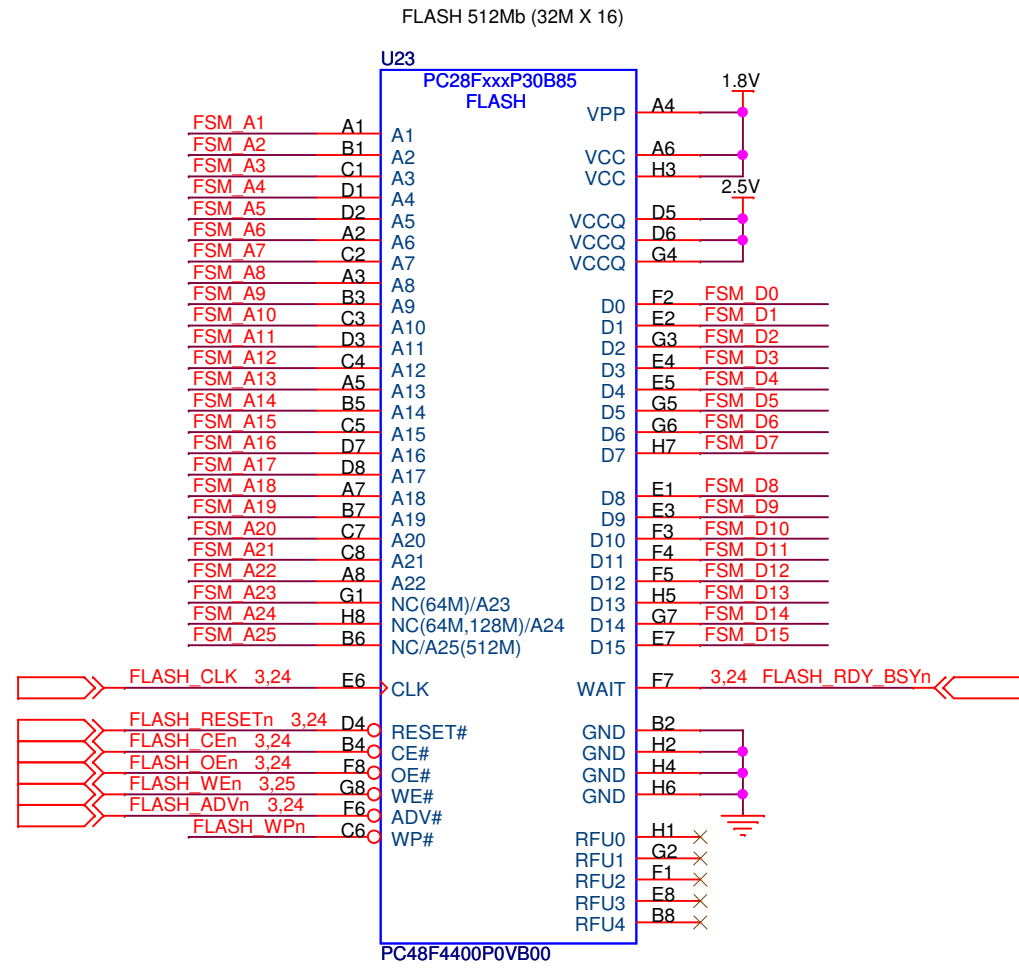
SSRAM

FSM D[31..0] 3,11,24,25
 SRAM DQP[3..0] 24,25
 FSM A[22..2] 3,11,24,25
 SRAM BEn[3..0] 25

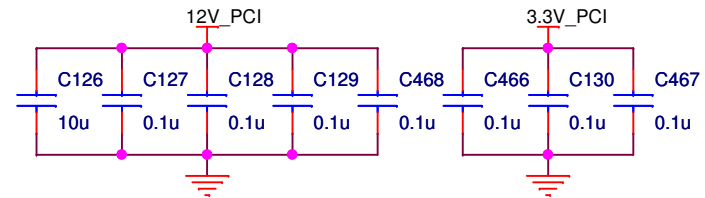
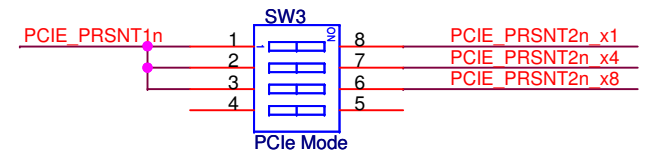
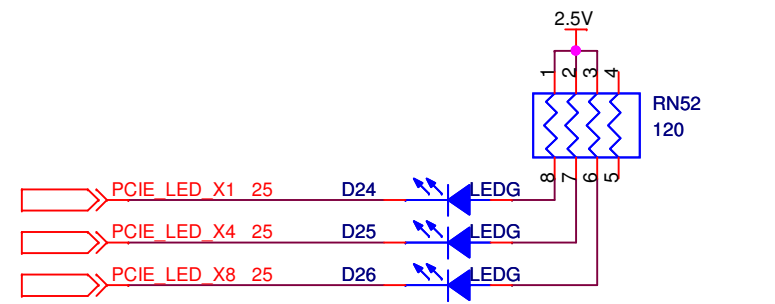
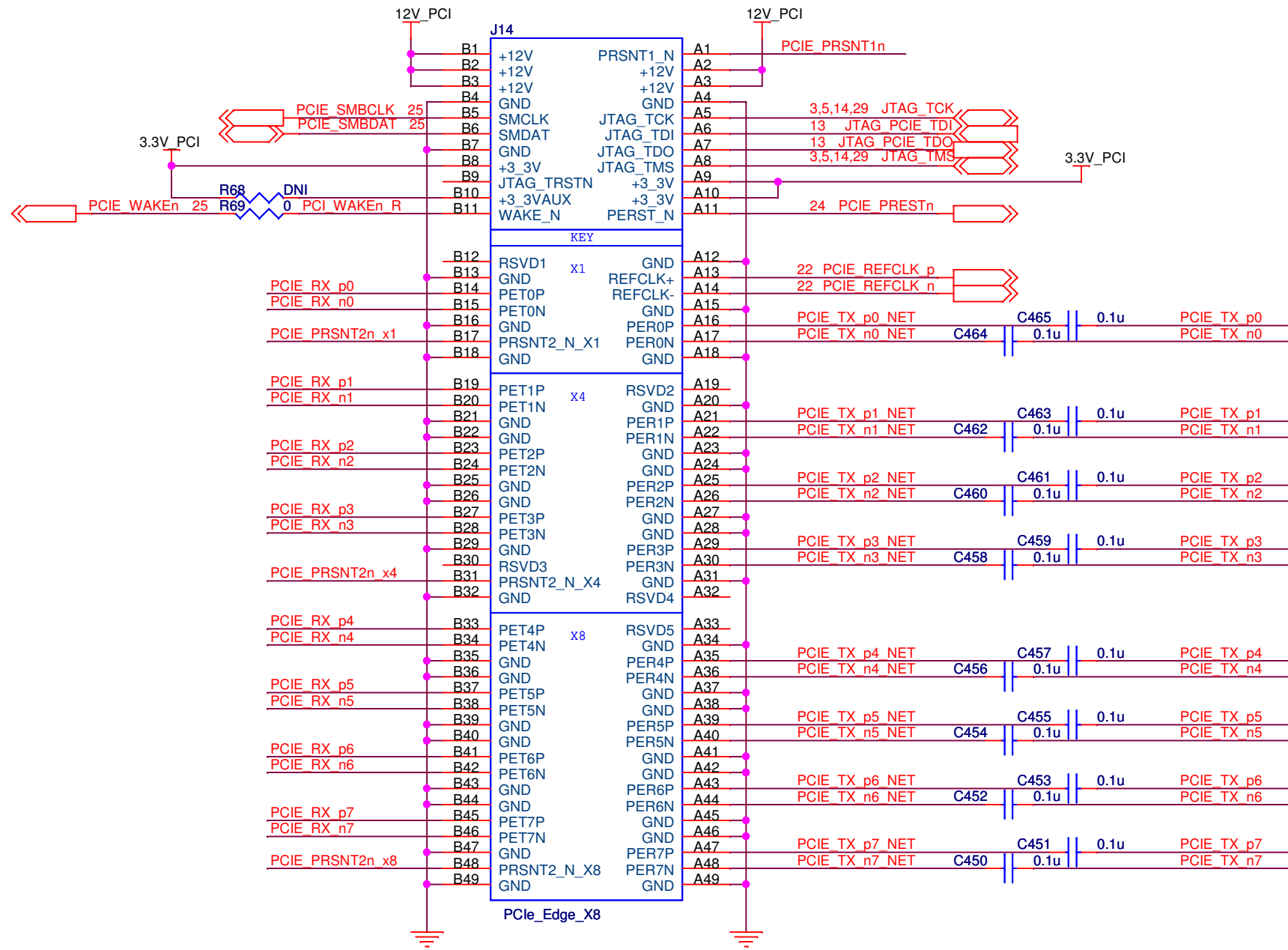
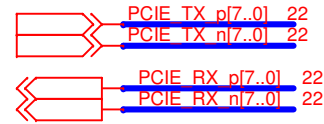
NOTE:
 SSRAM 256Kx36
 SSRAM 512Kx36 (Default)
 SSRAM 1Mx36
 SSRAM 2Mx36



Sync Flash



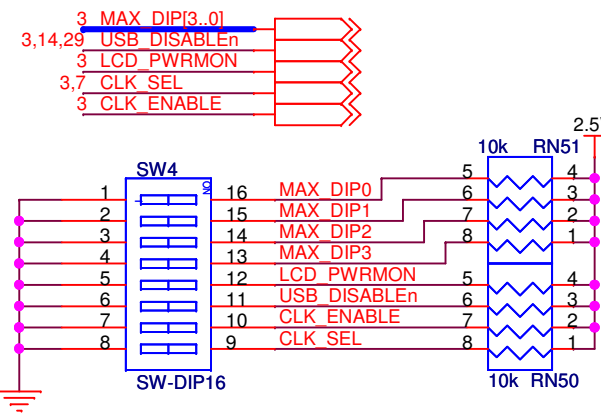
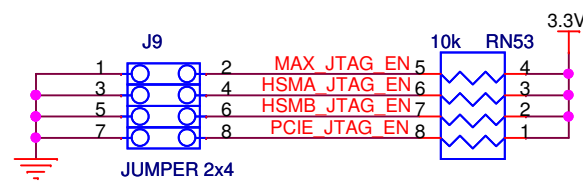
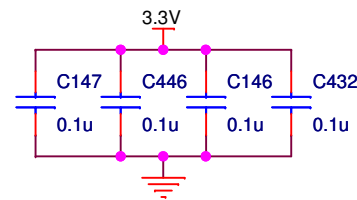
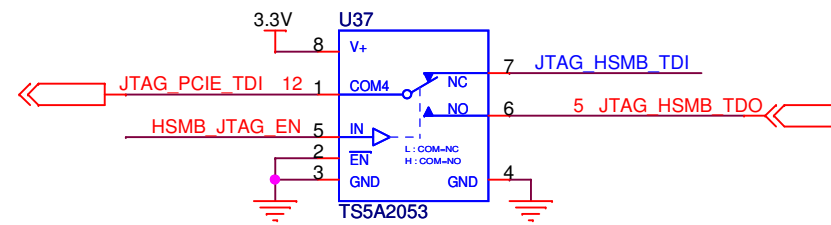
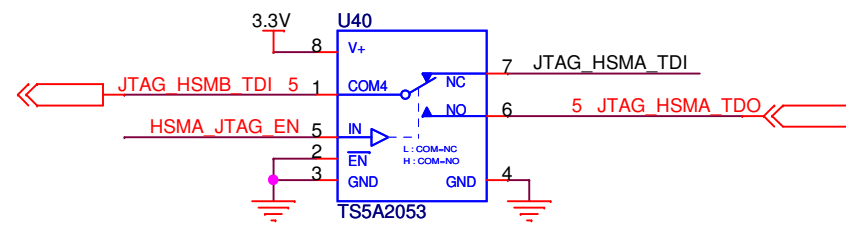
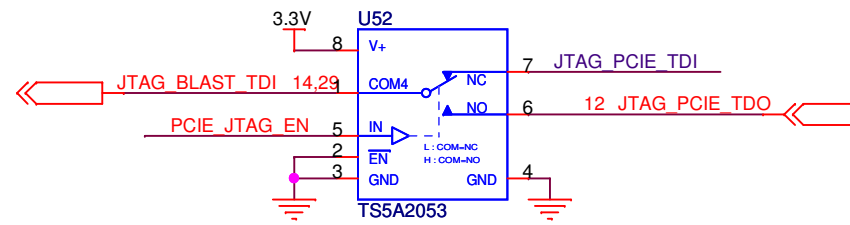
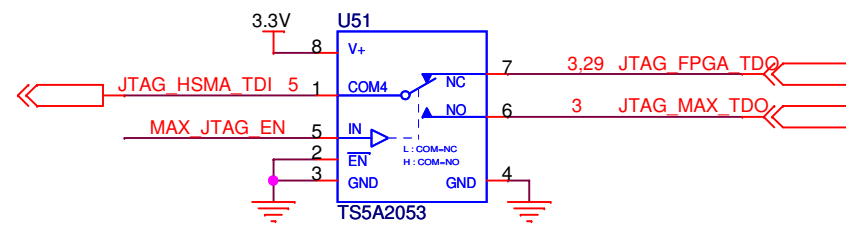
PCIe x8 Edge Connector



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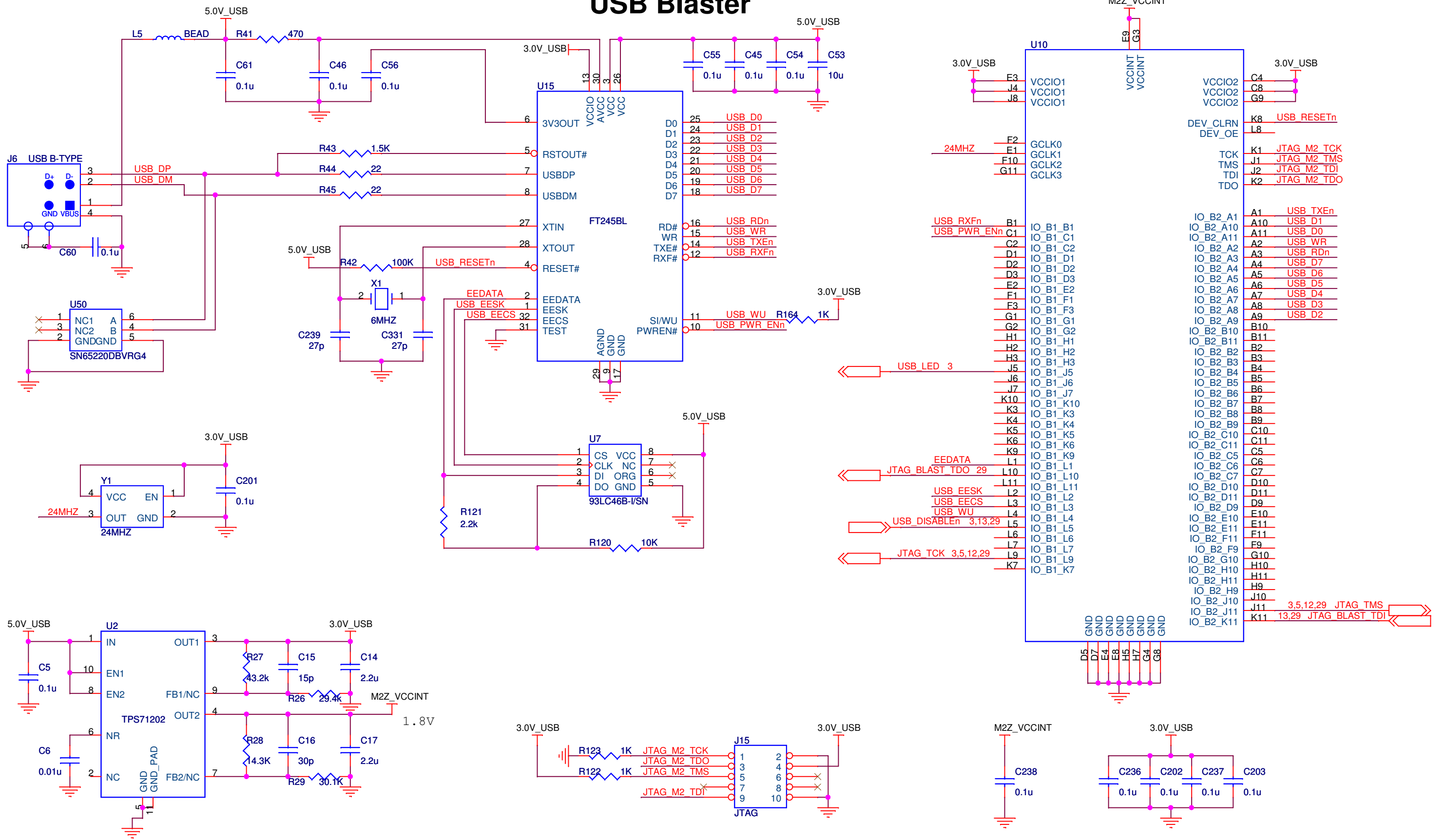
JTAG Control & Setting



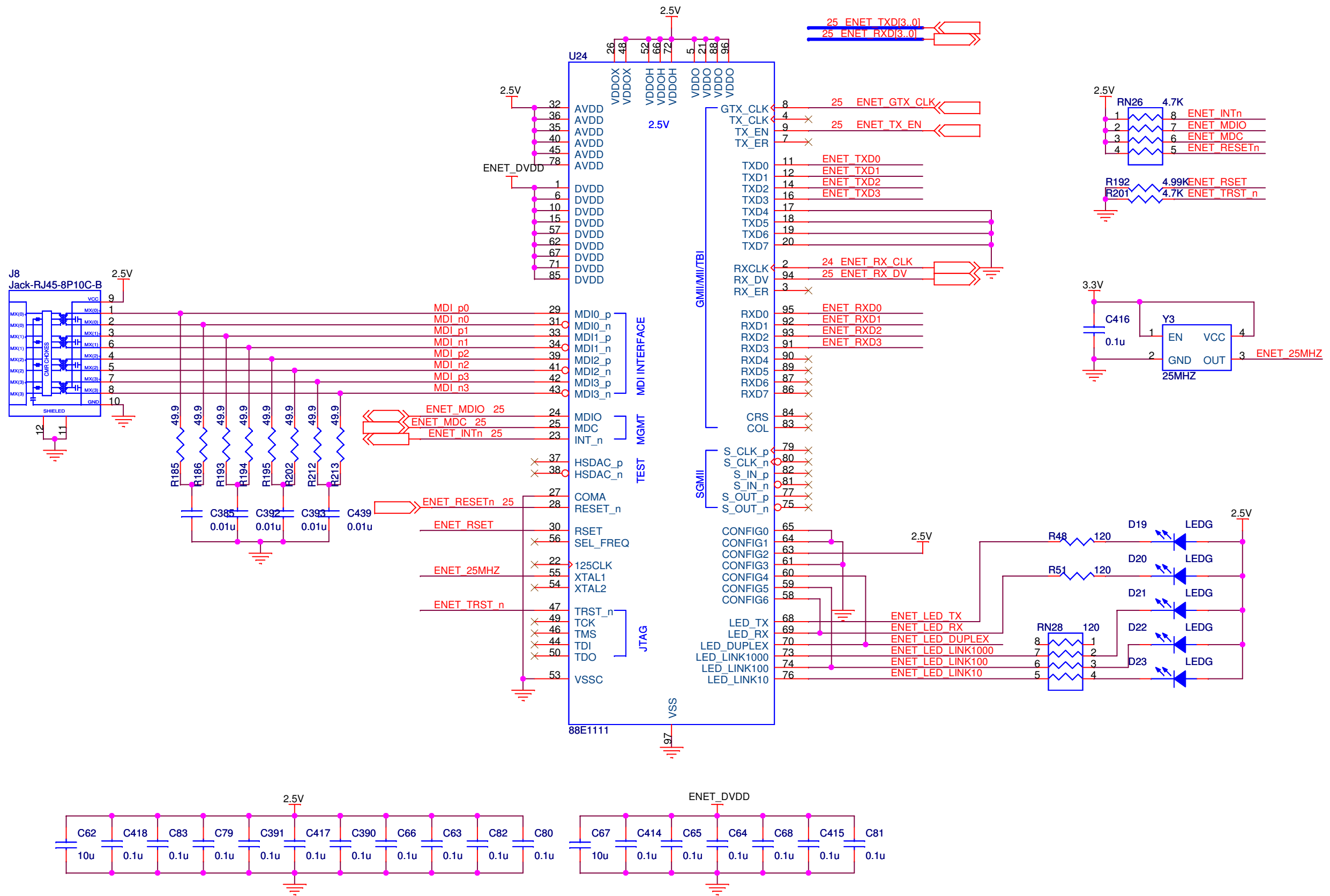
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USB Blaster

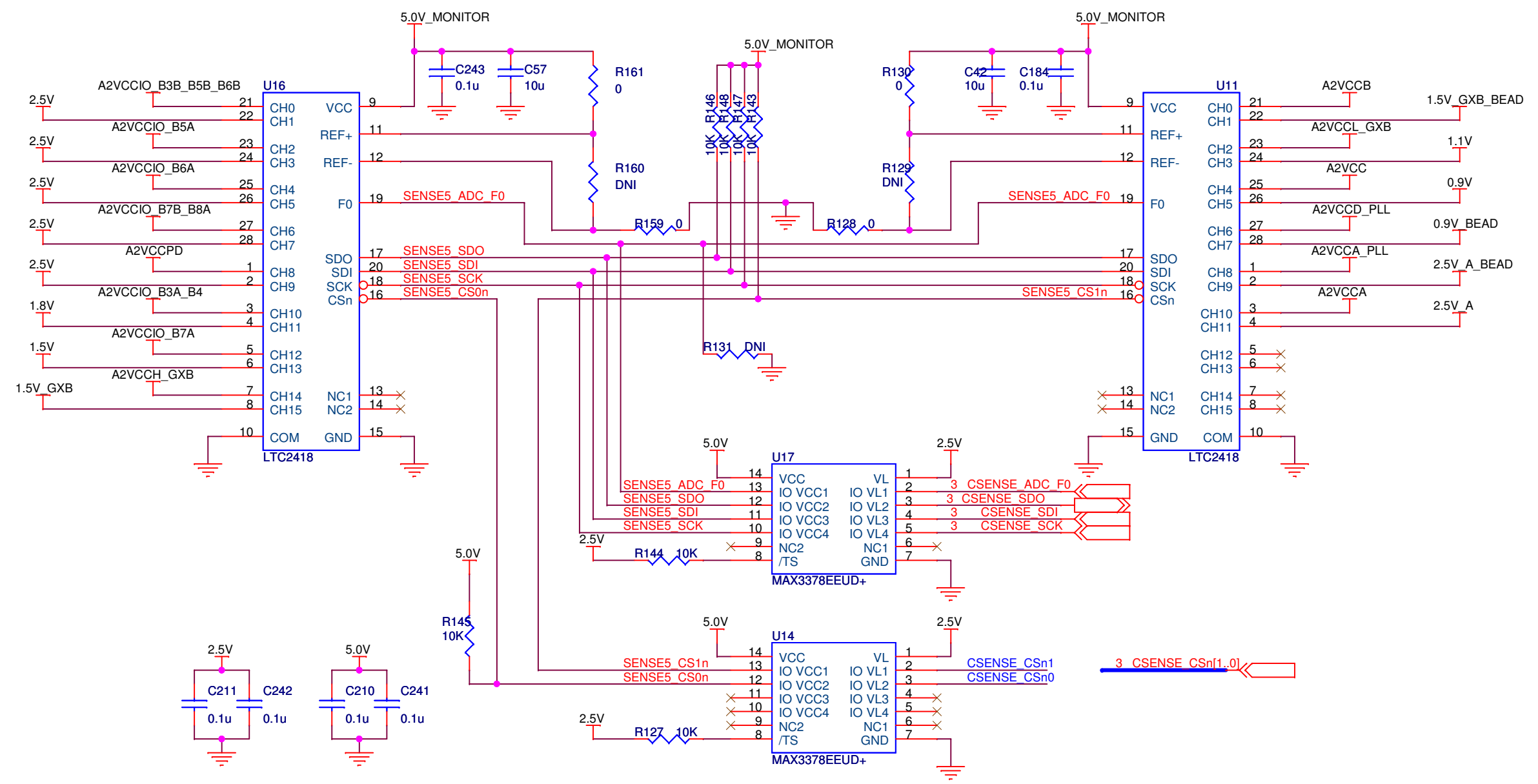


Ethernet



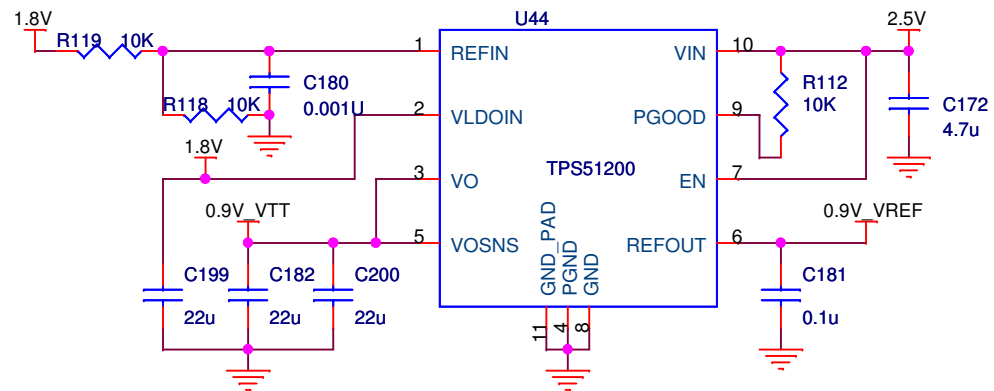
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Power Monitor

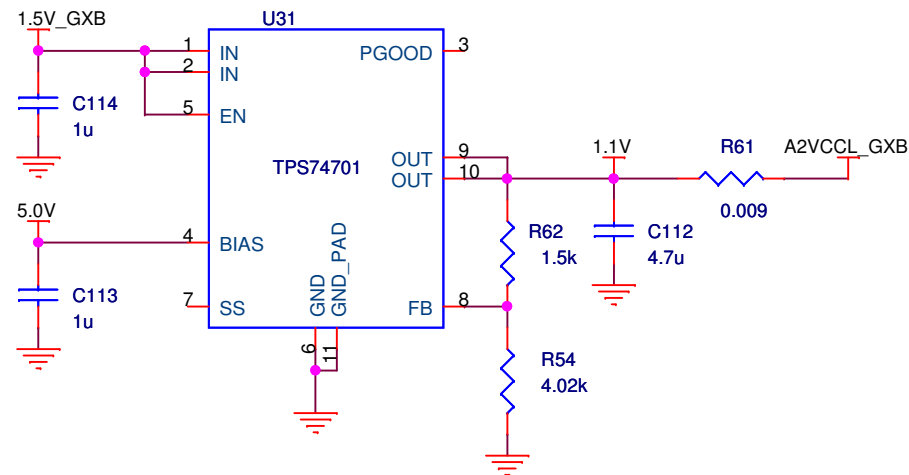


1.1V, 1.0V, VTT & VREF

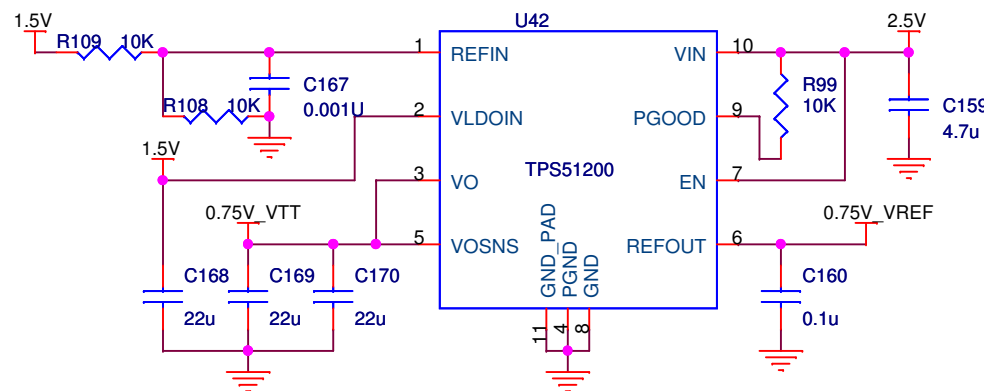
DDR2 VTT, VREF



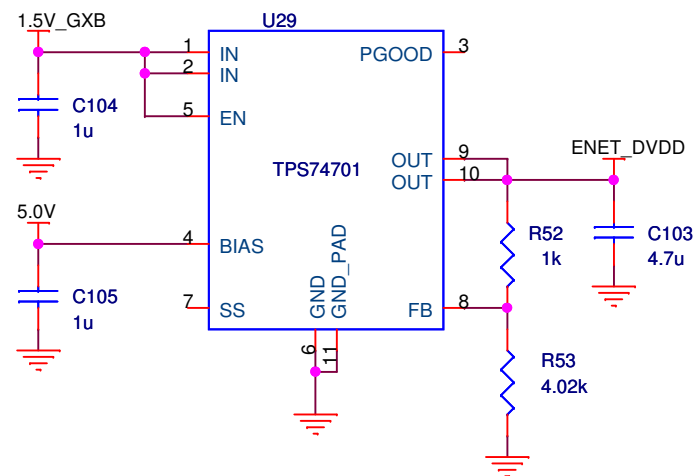
1.1V/500mA



DDR3 VTT, VREF

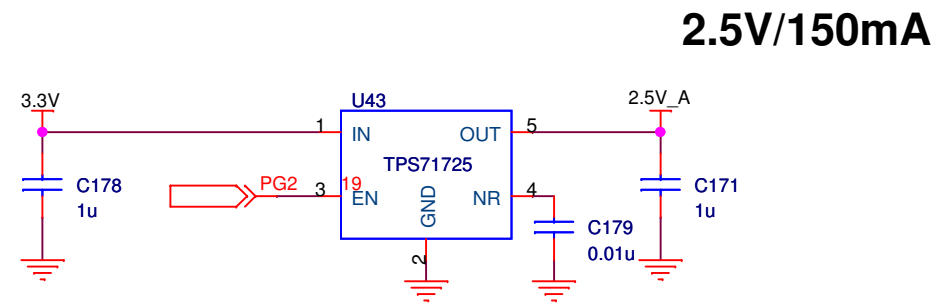
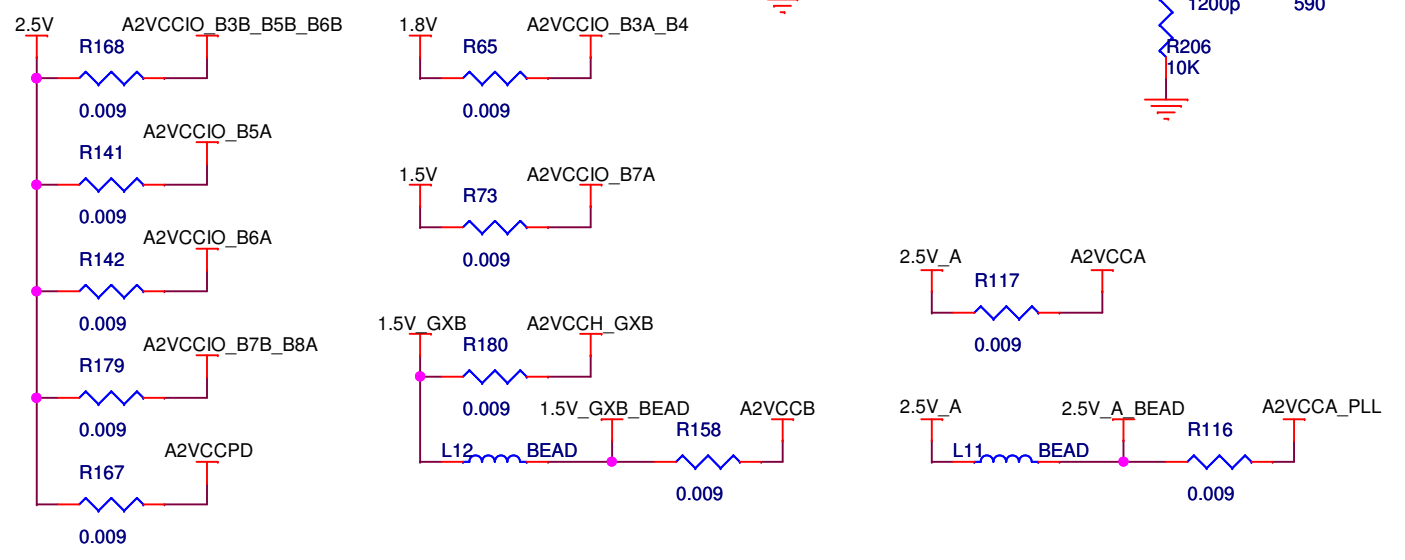
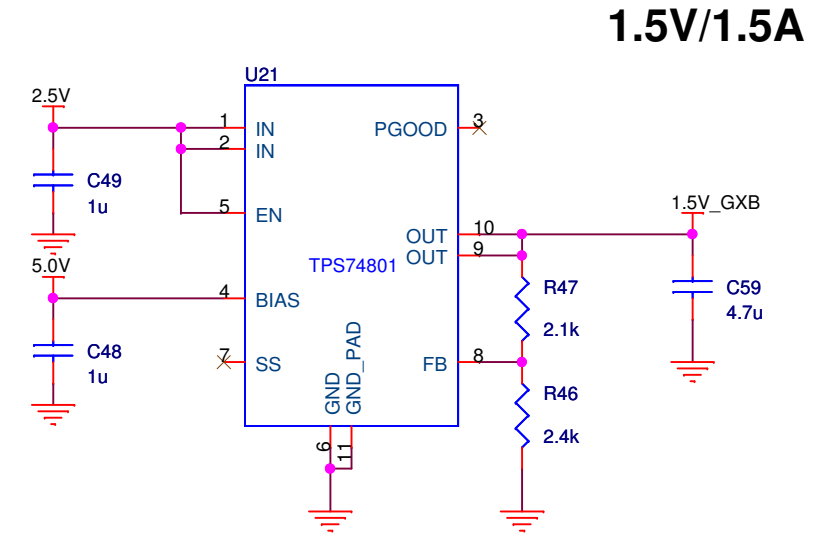
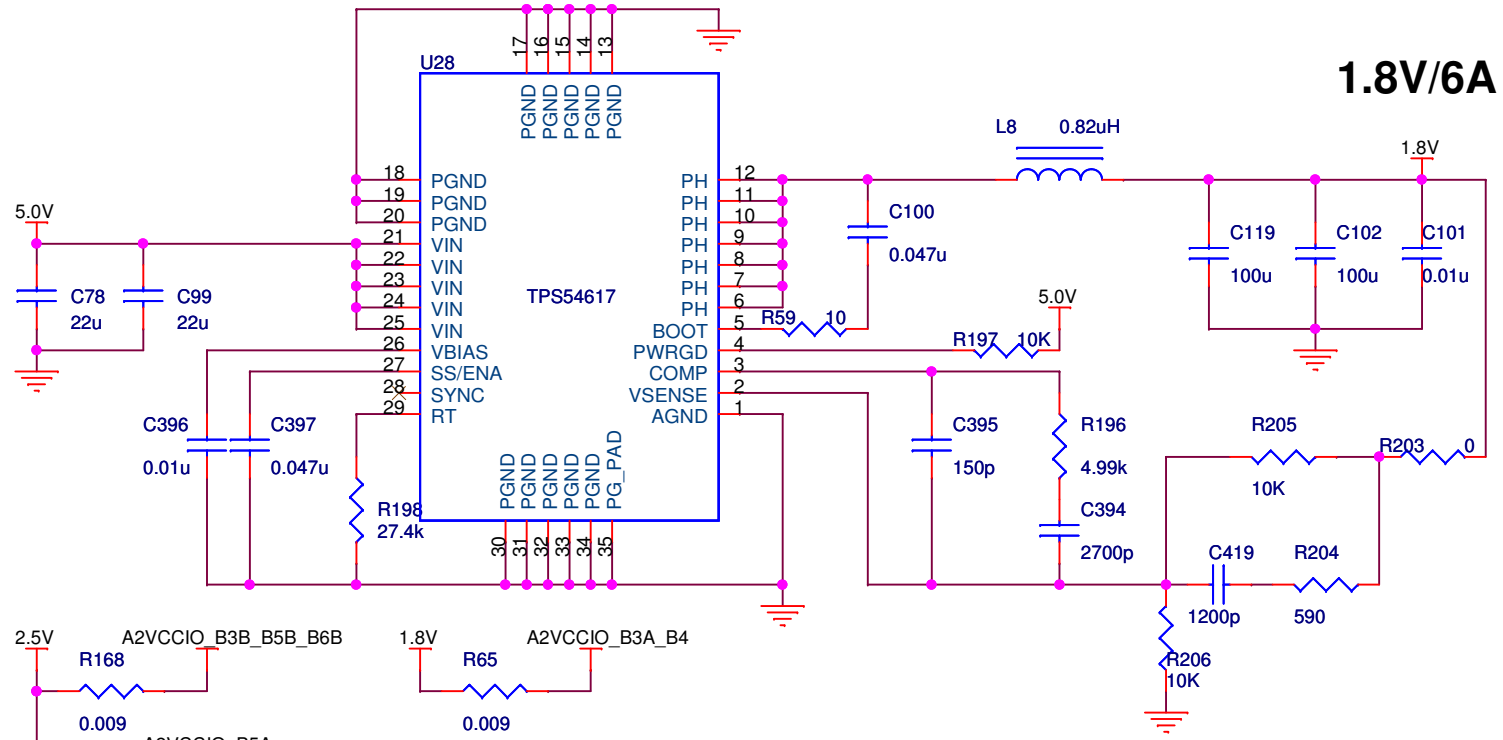
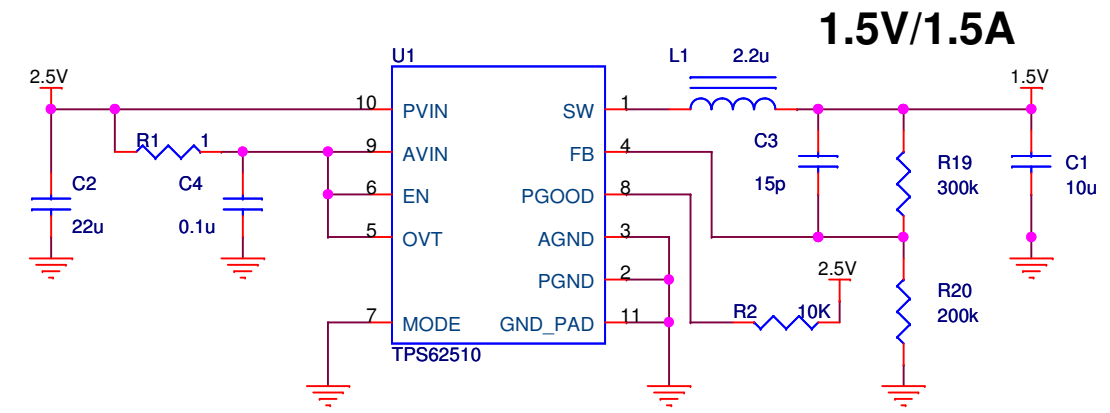
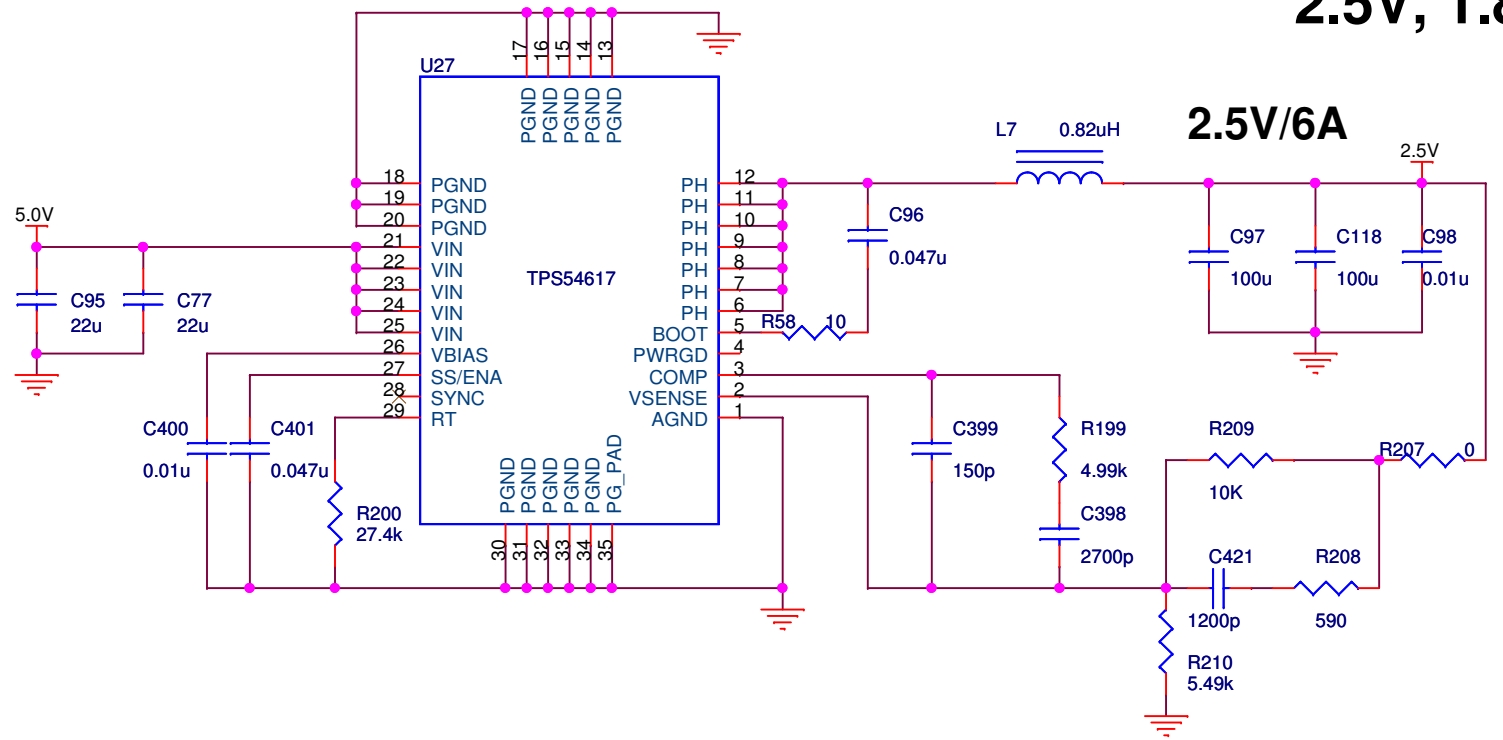


1.0V/500mA



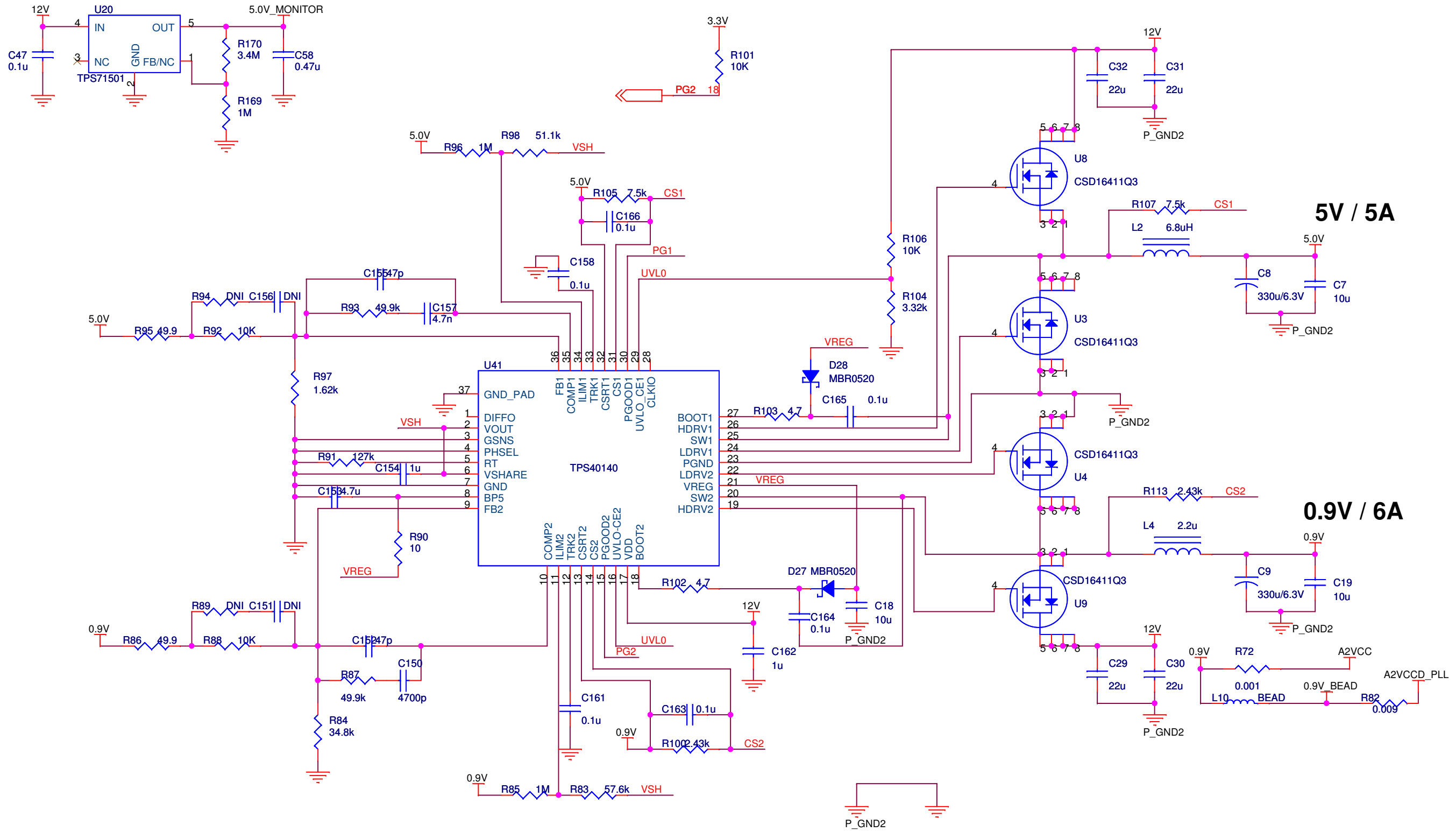
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2.5V, 1.8V & 1.5V



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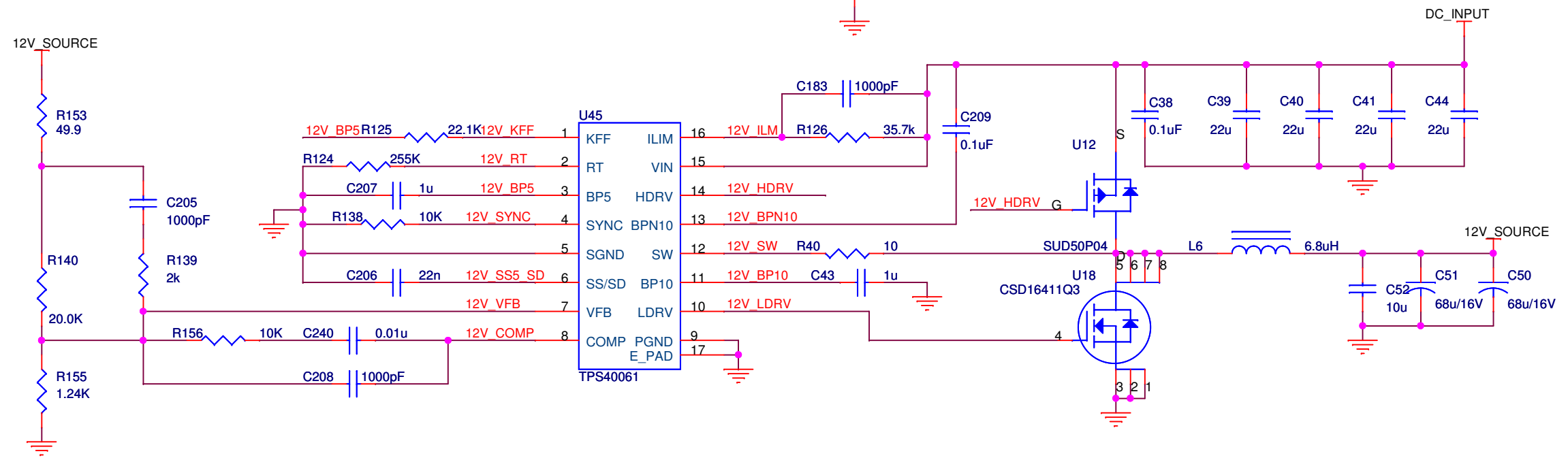
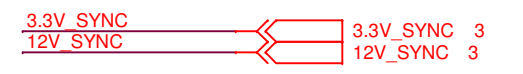
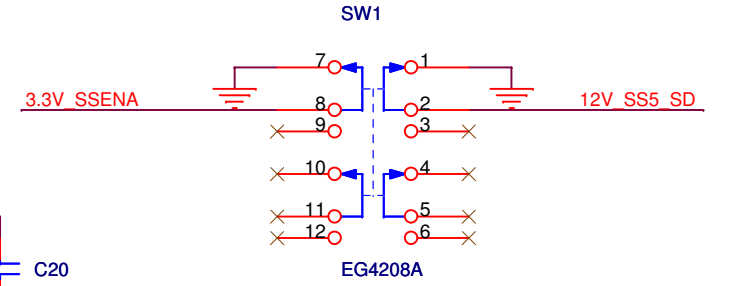
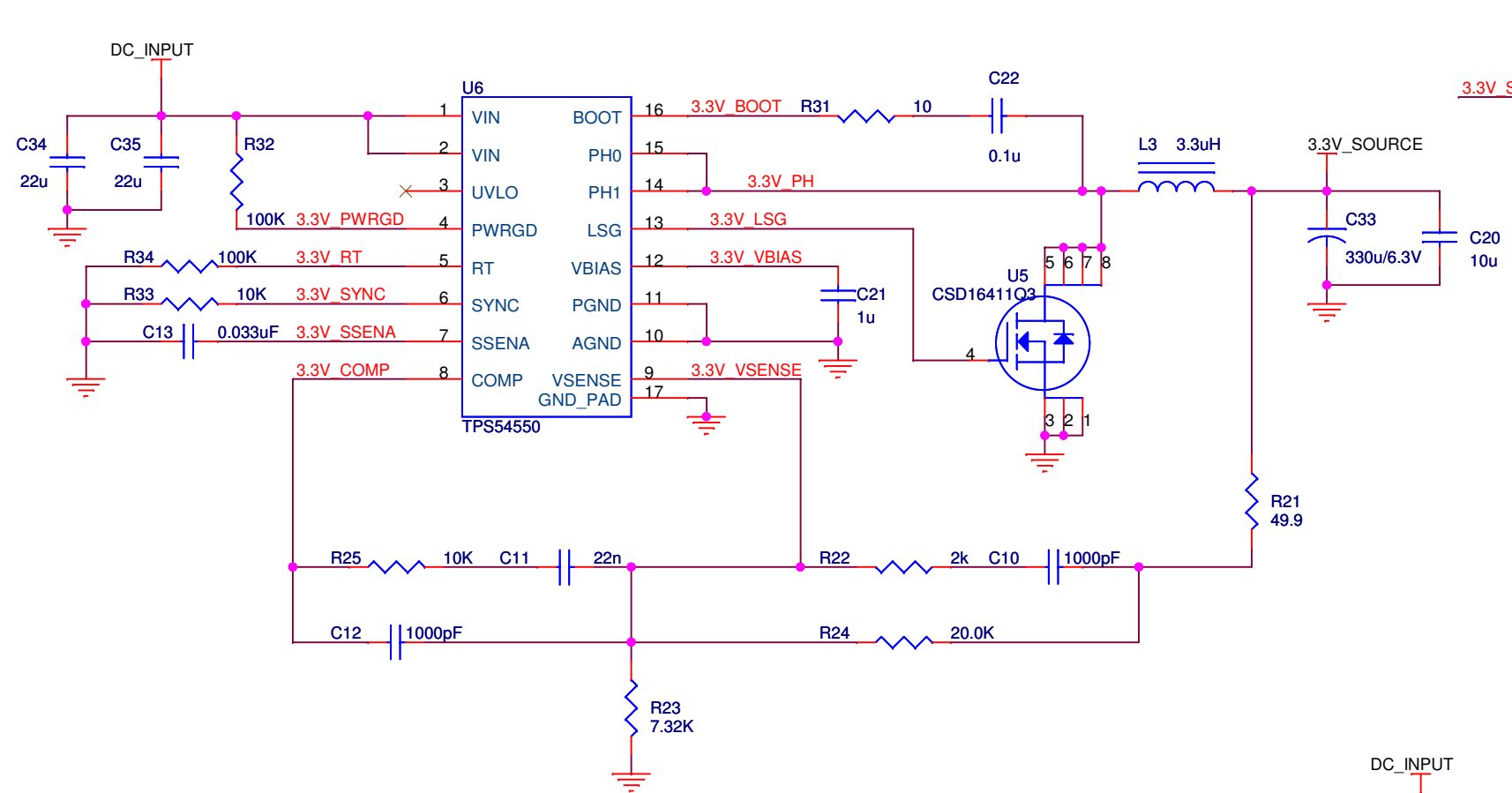
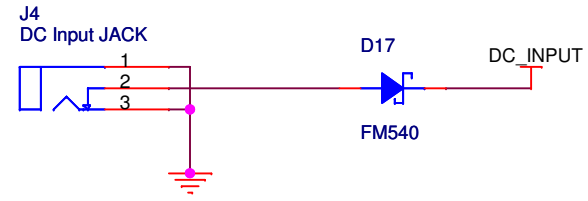
5V & 0.9V Dual Output



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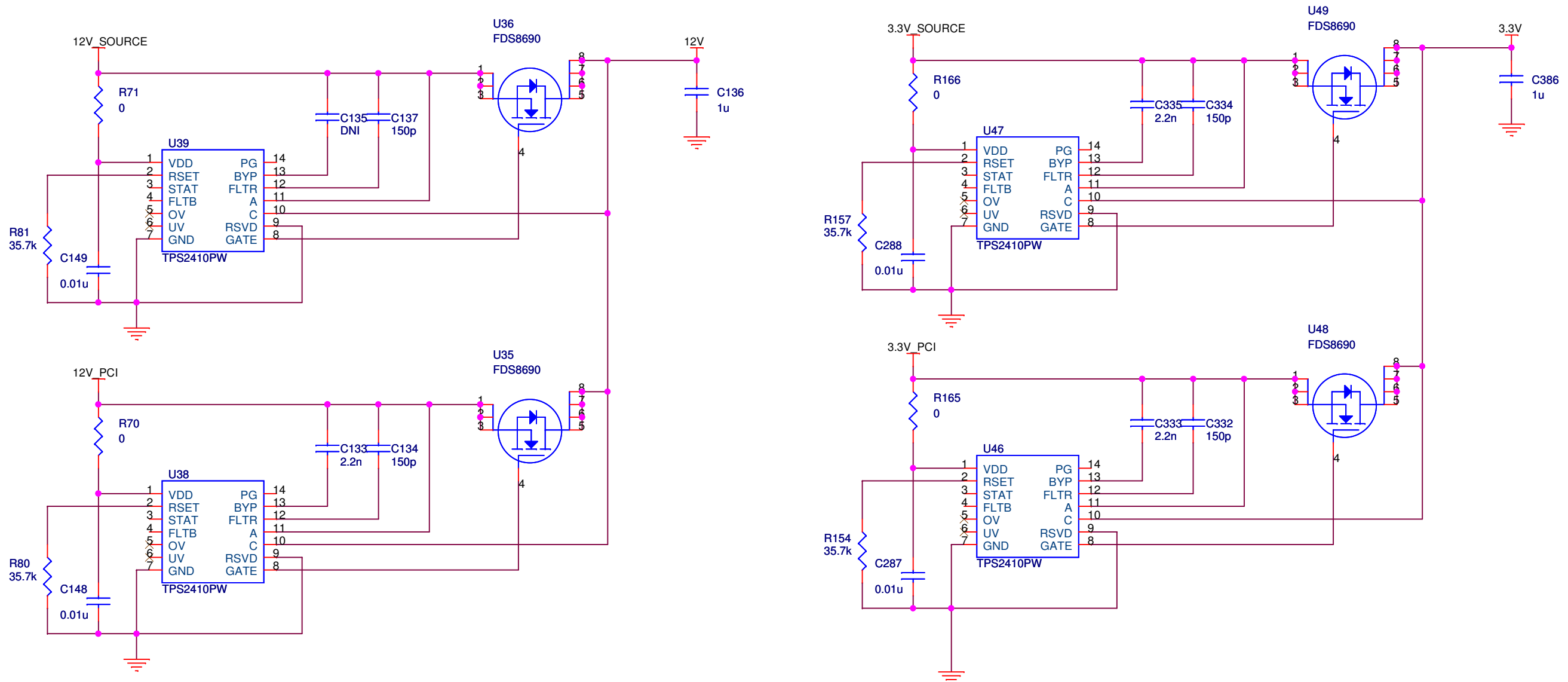
DC IN to 12V & 3.3V

14V ~ 20V DC Input



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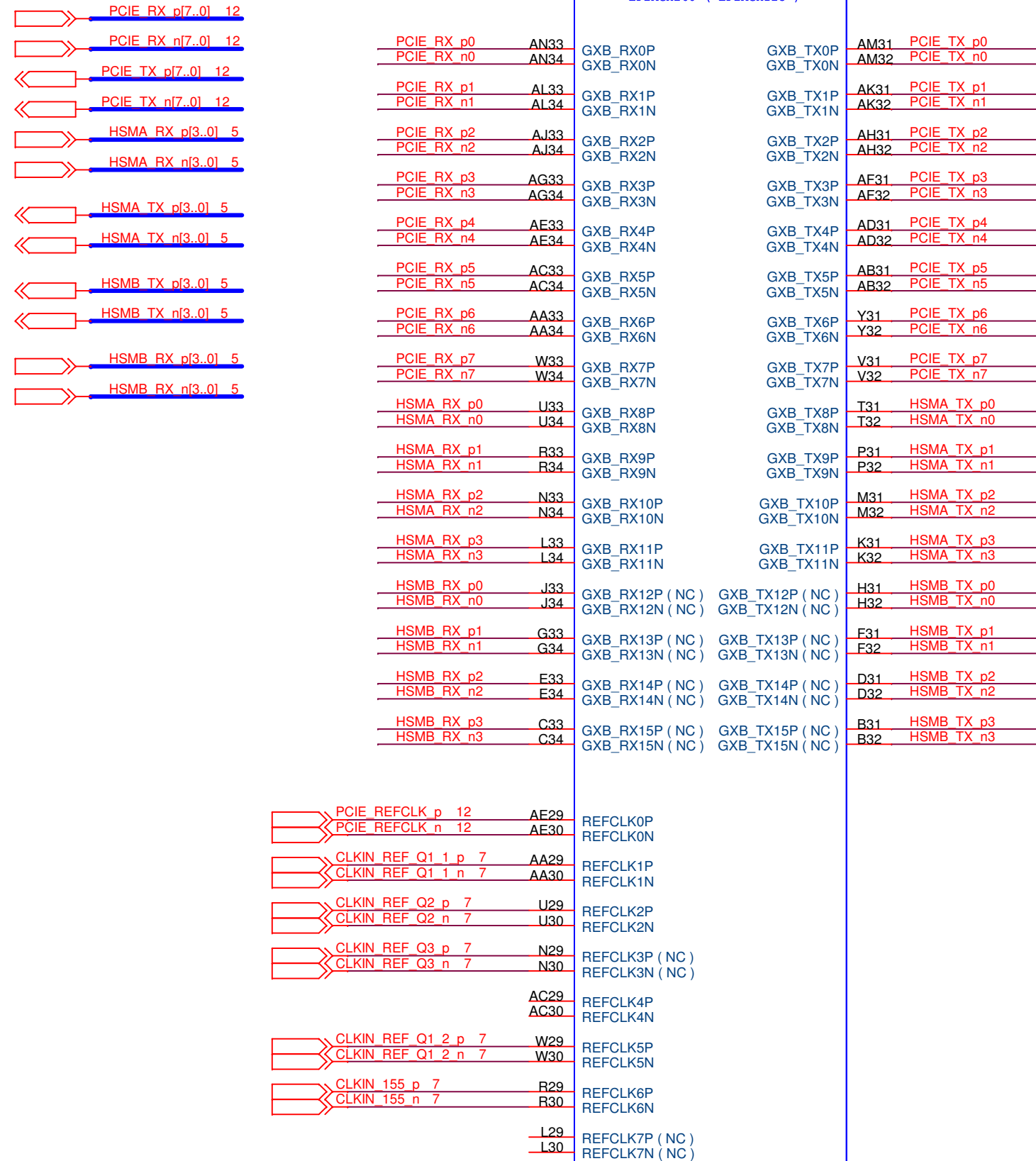
Power MUX



BANK QL

U19A

Arria II GX Bank QL
EP2AGX260 (EP2AGX125)



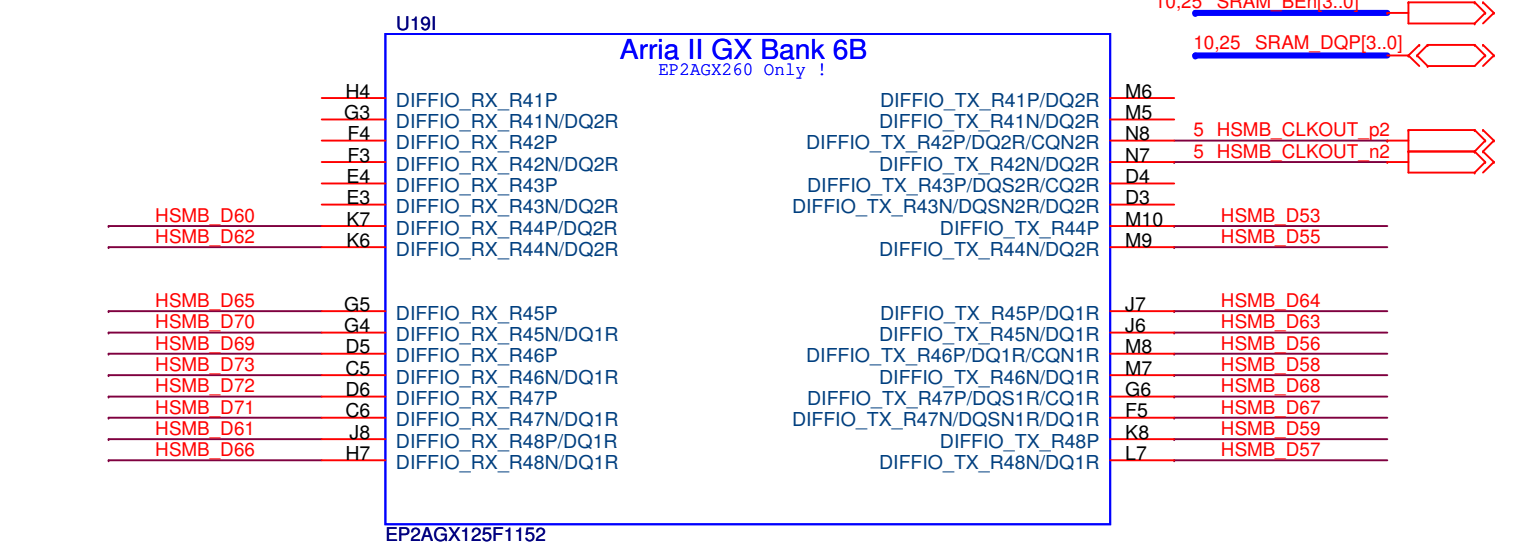
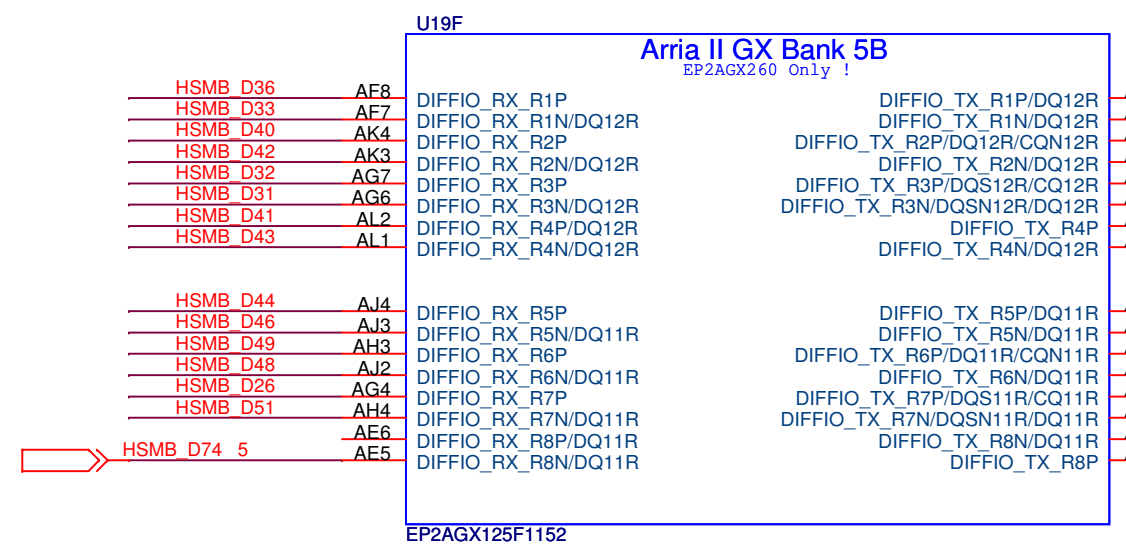
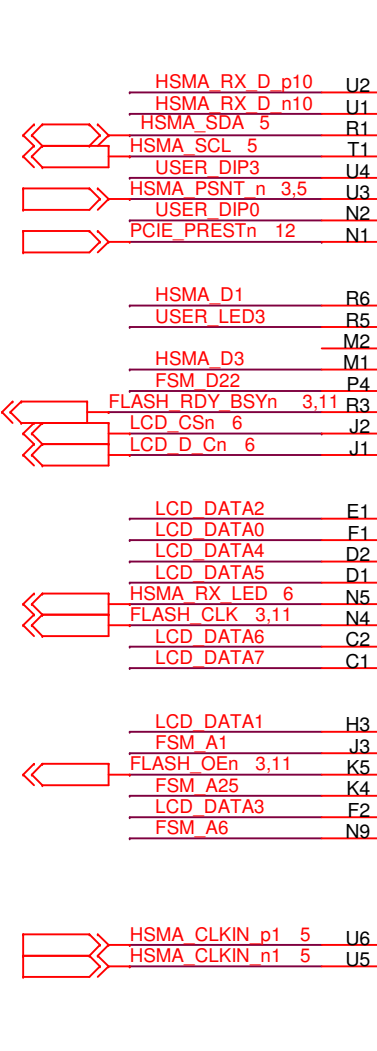
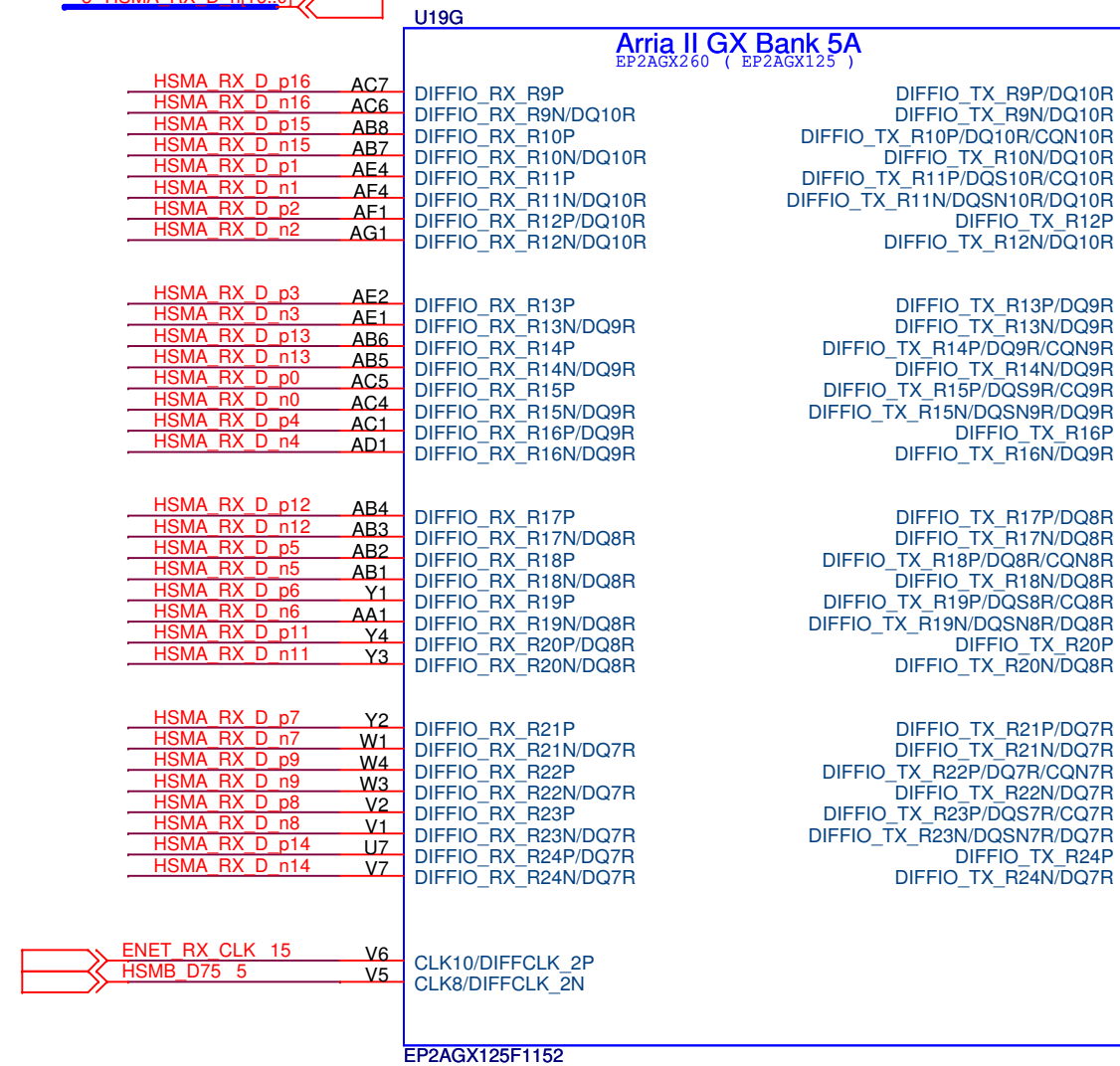
EP2AGX125F1152

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BANK5 & BANK6

5 HSMA RX D p[16..0] ←
5 HSMA RX D n[16..0] ←

5 HSMA CLKOUT p[2..1] →
5 HSMA CLKOUT n[2..1] →

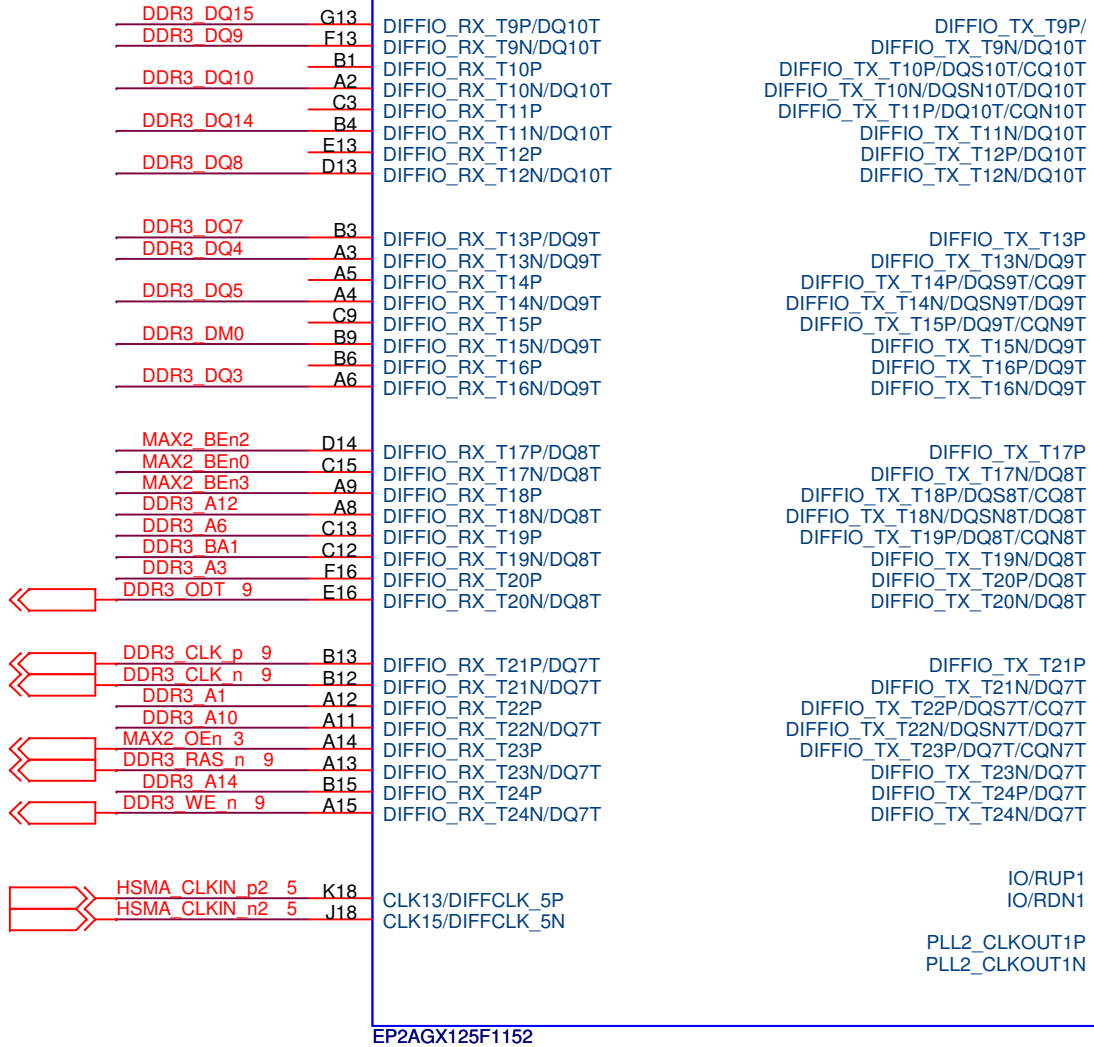


BANK7 & BANK8

U19K

Arria II GX Bank 7A

EP2AGX260 (EP2AGX125)

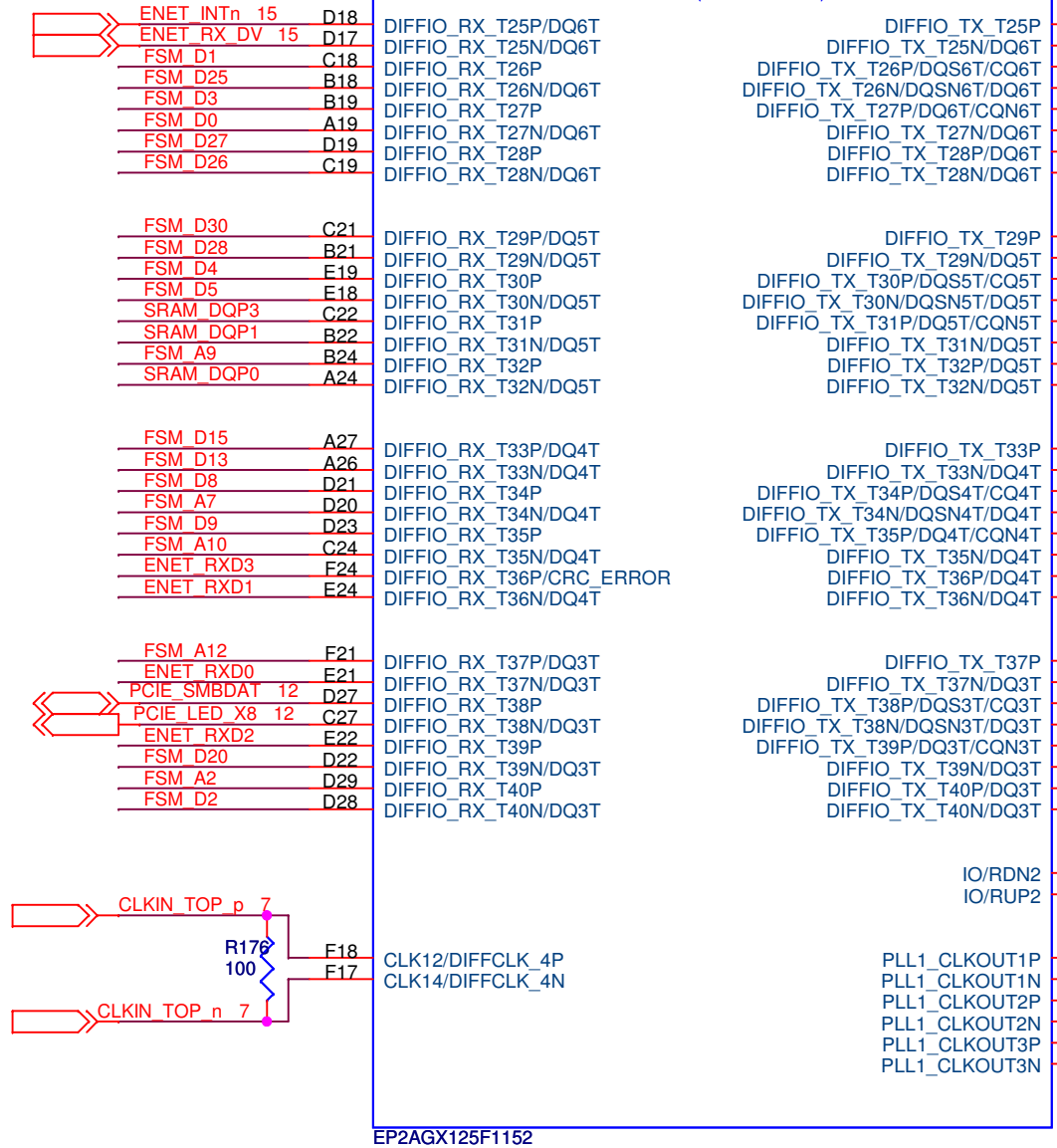


EP2AGX125F1152

U19L

Arria II GX Bank 8A

EP2AGX260 (EP2AGX125)

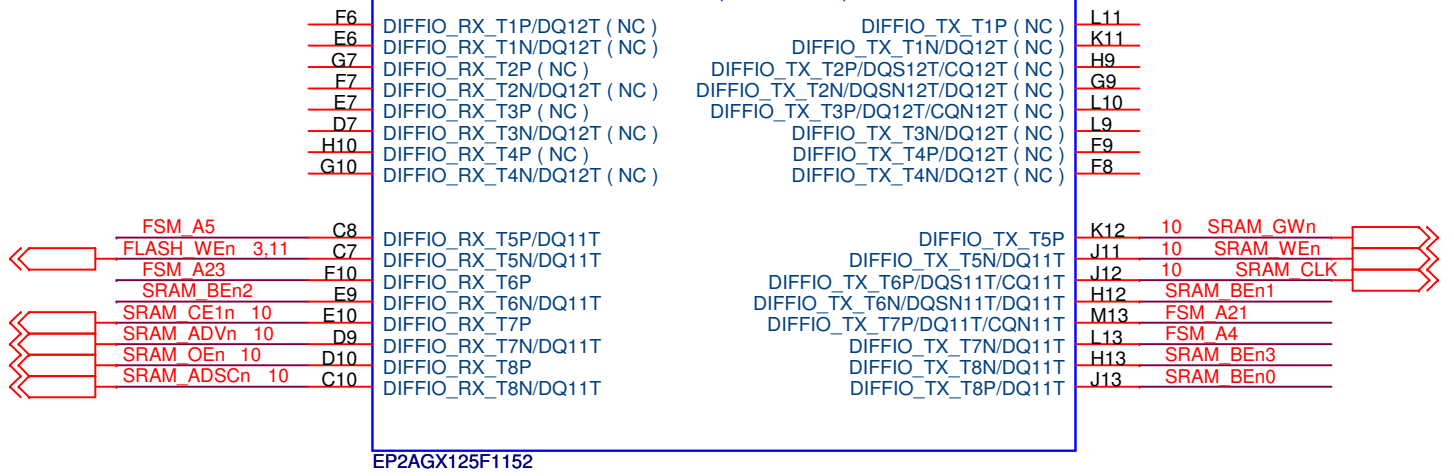


EP2AGX125F1152

U19J

Arria II GX Bank 7B

EP2AGX260 (EP2AGX125)

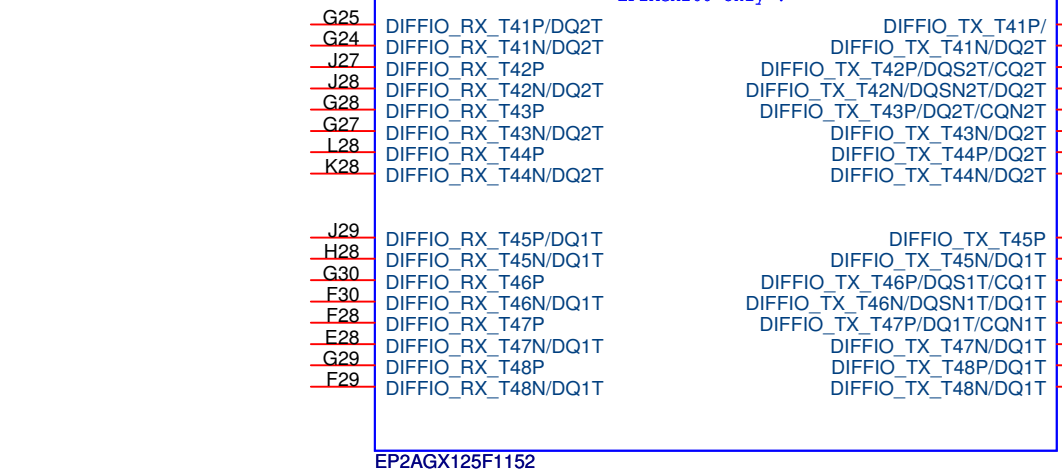


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U19M

Arria II GX Bank 8B

EP2AGX260 Only !



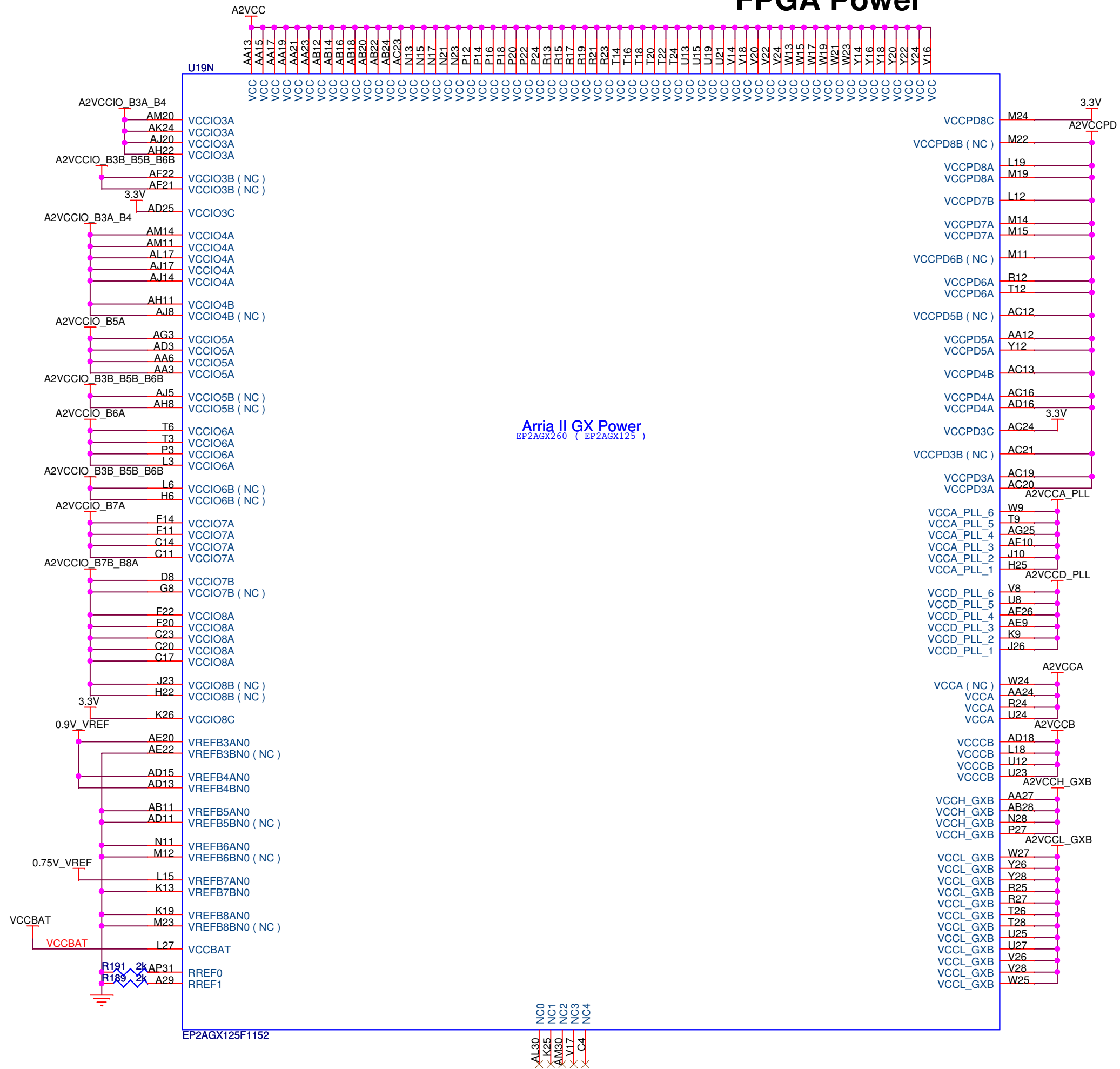
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FPGA Power



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FPGA Ground

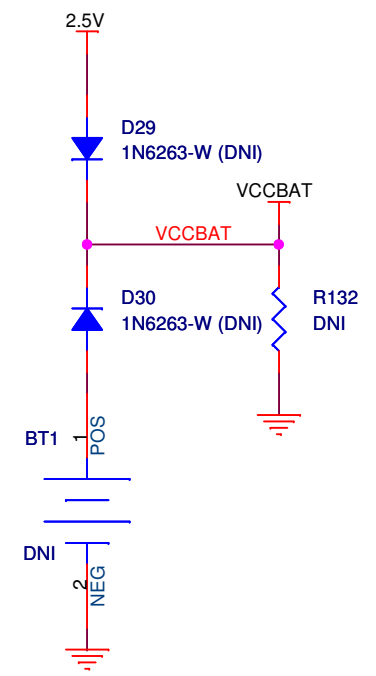
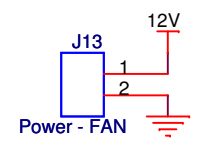
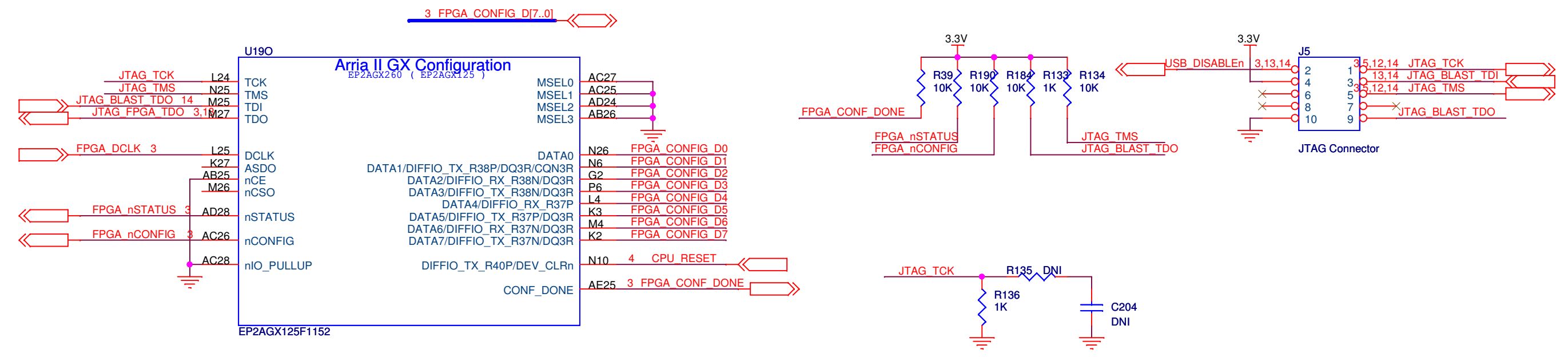


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FPGA Decoupling



FPGA Configuration



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