DE5a-Net Board

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Title: DE5a-Net Board

Size: B | Document Number: Cover Page | Rev: C

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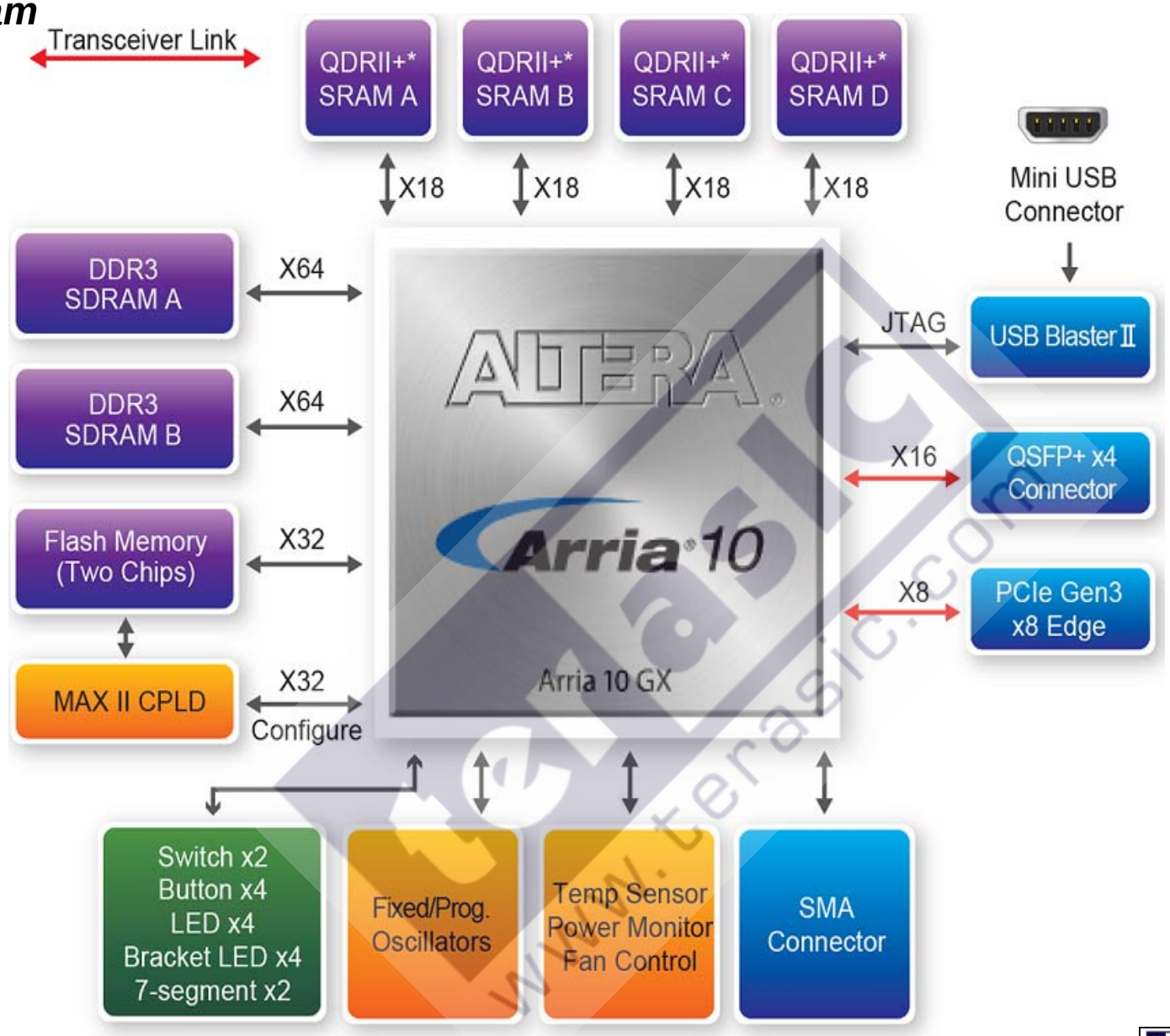
Block Diagram



*Cypress QDRII+ SRAM or functional compatible SRAMS provided by GSI (SigmaQuad-II+) and ISSI (QUADP).

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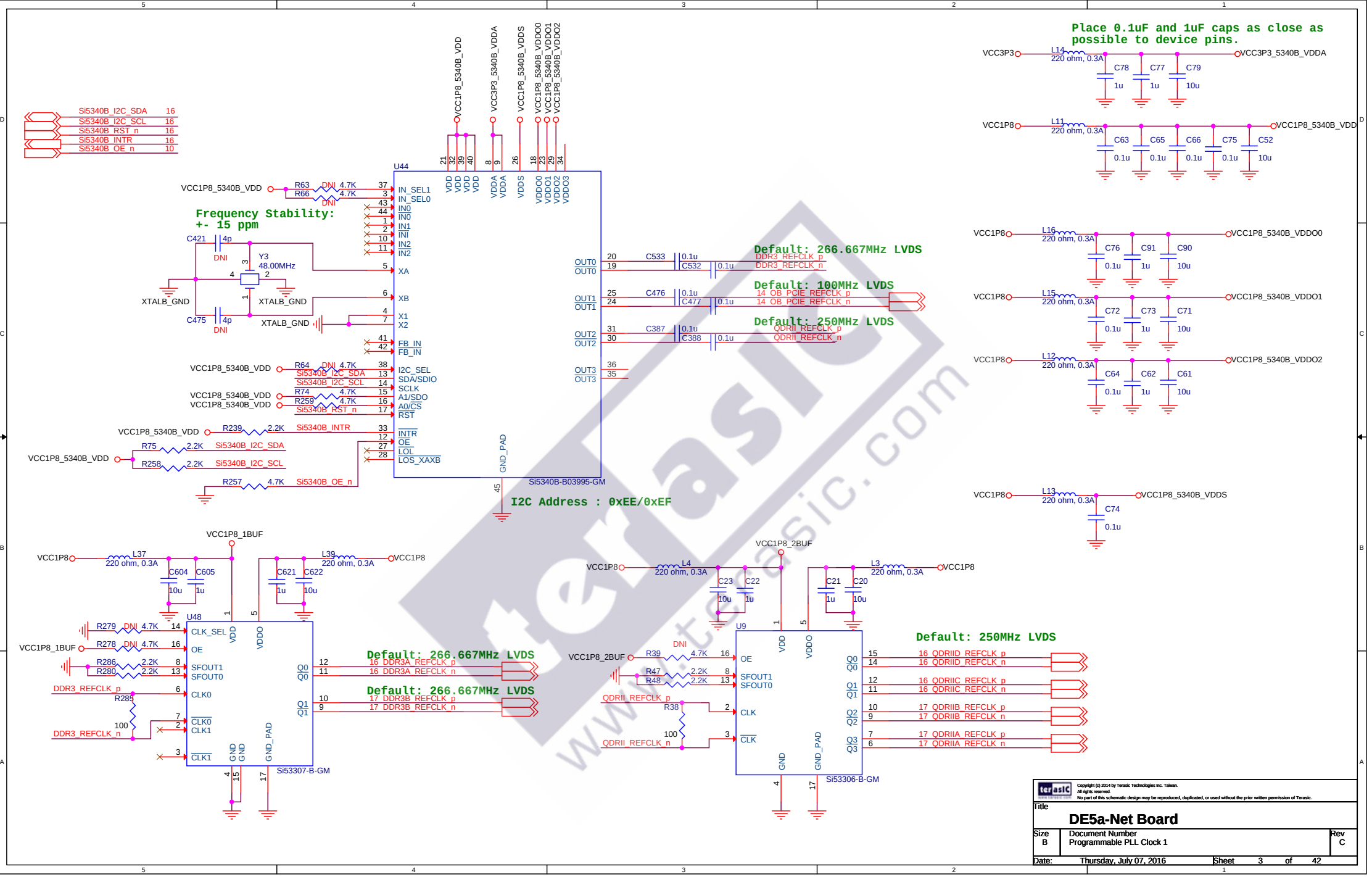
Title	DE5a-Net Board	
Size B	Document Number Block Diagram	Rev C
Date: Friday, June 03, 2016	Sheet 2 of 42	


Place 0.1uF and 1uF caps as close as possible to device pins.
Frequency Stability: +- 15 ppm
Default: 266.667MHz LVDS
Default: 100MHz LVDS
Default: 250MHz LVDS
I2C Address : 0xEE/0xEF
U44
Si5340B-B03995-GM
U48
Si53307-B-GM
U9
Si53306-B-GM
Y3 48.00MHz
VCC1P8_5340B_VDD
VCC3P3_5340B_VDDA
VCC1P8_5340B_VDDS
VCC1P8_5340B_VDDO0
VCC1P8_5340B_VDDO1
VCC1P8_5340B_VDDO2
VCC3P3_5340B_VDDA
VCC1P8_5340B_VDDO0
VCC1P8_5340B_VDDO1
VCC1P8_5340B_VDDO2
VCC1P8_5340B_VDDS
VCC1P8_1BUF
VCC1P8_2BUF
XTALB_GND
Si5340B_I2C_SDA
Si5340B_I2C_SCL
Si5340B_RST_n
Si5340B_INTR
Si5340B_OE_n
DDR3_REFCLK_p
DDR3_REFCLK_n
QDRII_REFCLK_p
QDRII_REFCLK_n
16_DDR3A_REFCLK_p
16_DDR3A_REFCLK_n
17_DDR3B_REFCLK_p
17_DDR3B_REFCLK_n
14_OB_PCIE_REFCLK_p
14_OB_PCIE_REFCLK_n
16_QDRIID_REFCLK_p
16_QDRIID_REFCLK_n
16_QDRIIC_REFCLK_p
16_QDRIIC_REFCLK_n
17_QDRIIB_REFCLK_p
17_QDRIIB_REFCLK_n
17_QDRIIA_REFCLK_p
17_QDRIIA_REFCLK_n
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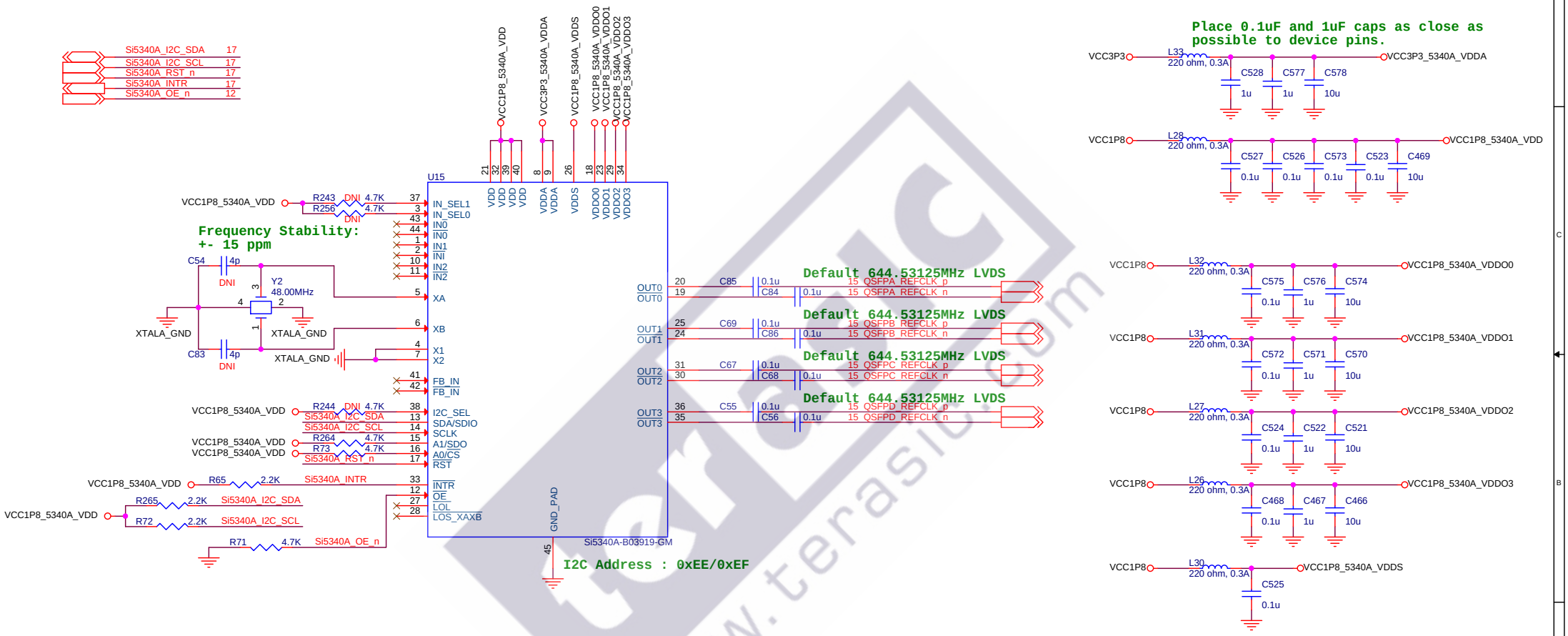
Title
DE5a-Net Board
Size B
Document Number
Programmable PLL Clock 1
Rev C
Date: Thursday, July 07, 2016
Sheet 3 of 42



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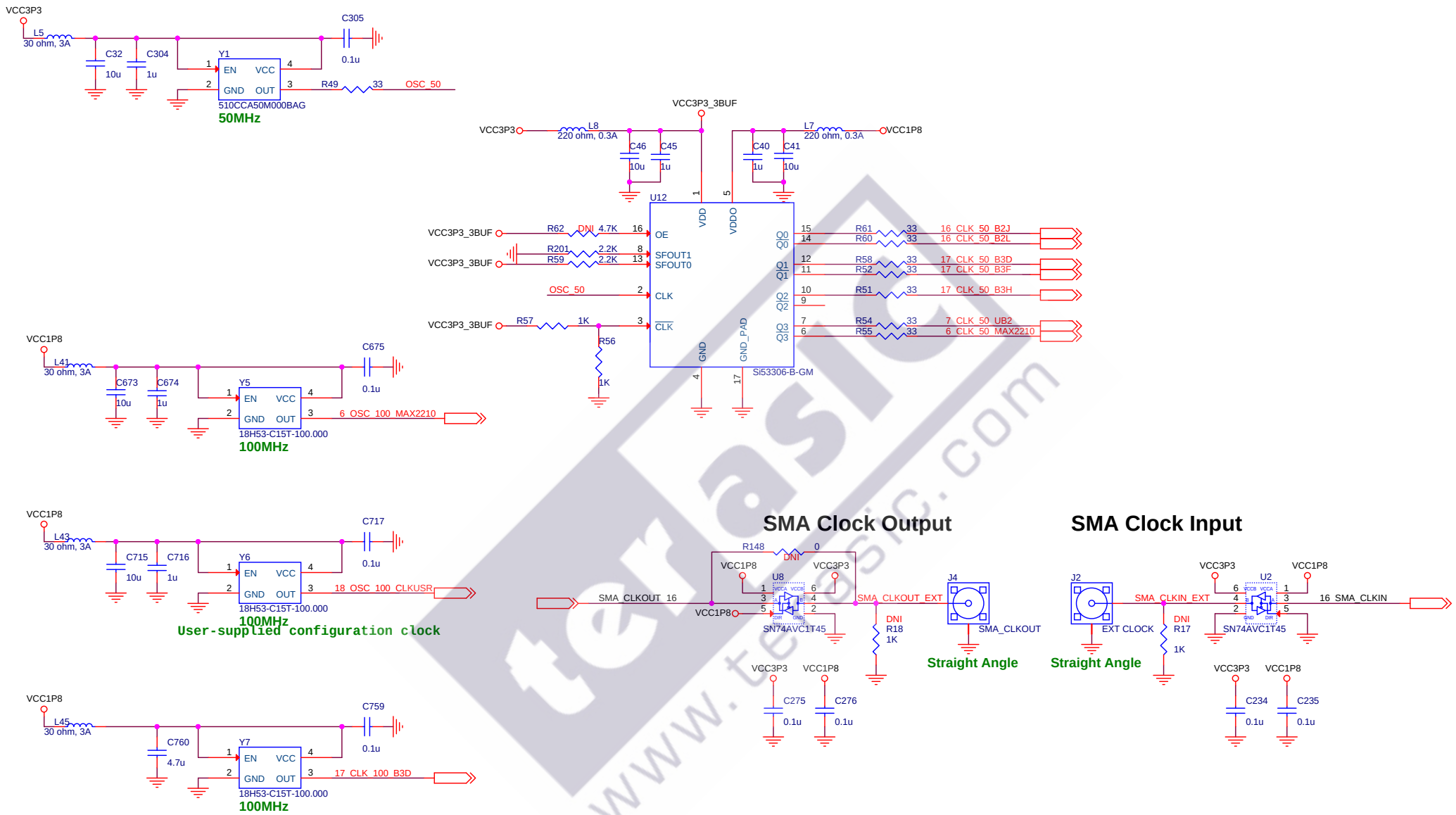
Title
DE5a-Net Board

Size	Document Number	Rev
B	Programmable PLL Clock 2	C

Date: Thursday, July 07, 2016 Sheet 4 of 42



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Title
DE5a-Net Board

Size	Document Number	Rev
B	Singled-ended Clock and SMA Clock	C

Date: Thursday, May 26, 2016 Sheet 5 of 42

FPGA FPP Configuration

FPGA_DCLK 18,28
FPGA_nCONFIG 18
FPGA_nSTATUS 18
FPGA_CONF_DONE 18
MSEL[2..0] 18
FPGA_CONFIG_D[31..0] 18

FLASH Bus and Control

FLASH_A[26..1] 11,13,28
FLASH_D[31..0] 11,28
FLASH_CLK 13,28
FLASH_RESET_n 13,28
FLASH_OE_n 13,28
FLASH_WE_n 13,28
FLASH_ADV_n 13,28
FLASH_CE_n[1..0] 13,28
FLASH_RDY_BSY_n[1..0] 11,13,28

Reserved IO for MAX V and MAX II

M5M2_R_IO[3..0] 7

Reserved IO for MAX V and Arria 10

M5A10_R_CLK 17
M5A10_R_IO[31..0] 13,17

MAX5 Interface

CPU_RESET_n 18,35
CLK_50_MAX2210 5
OSC_100_MAX2210 5

Configuration CvP with PCIe

FPGA_PR_DONE 18
FPGA_PR_REQUEST 18
FPGA_PR_READY 18
FPGA_PR_ERROR 18
FPGA_CvP_CONFIG_DONE 18

JTAG Control for MAX2

FACTORY_LOAD 18
FACTORY_REQUEST 7
FACTORY_STATUS 7

MAX V JTAG Interface

M5_JTAG_TCK 7
M5_JTAG_TMS 7
M5_JTAG_TDI 7
M5_JTAG_TDO 7

U47A — Bank = 1.8V — MAX V BANK1 — 5M2210ZF256

Pin	Signal	Pin	Signal
D3	FPGA_CONFIG_D2	J4	FPGA_CONFIG_D28
C2	FPGA_CONFIG_D3	K1	FPGA_CONFIG_D24
C3	FPGA_CONFIG_D4	J3	FPGA_CONFIG_D29
E3	FPGA_CONFIG_D7	K2	FPGA_CONFIG_D21
D2	FPGA_CONFIG_D26	K5	FPGA_CONFIG_D31
E4	FPGA_CONFIG_D6	L1	FPGA_CONFIG_D14
D1	FPGA_CONFIG_D0	L2	FPGA_CONFIG_D25
E5	FPGA_CONFIG_D22	K3	FPGA_CONFIG_D30
F3	FPGA_CONFIG_D5	M1	
E1	FPGA_CONFIG_D1	M2	FPGA_CONFIG_D15
F4	FPGA_CONFIG_D12	L4	FPGA_CvP_CONFIG_DONE
F2	FPGA_CONFIG_D11	L3	FPGA_PR_READY
F1	FPGA_CONFIG_D10	N1	FPGA_PR_ERROR
F6	FPGA_CONFIG_D23	M4	FPGA_PR_REQUEST
G2	FPGA_CONFIG_D13	N2	FPGA_PR_DONE
G3	FPGA_CONFIG_D9	M3	
G1	FPGA_CONFIG_D8	N3	FPGA_nSTATUS
G4	FPGA_CONFIG_D16	P2	FPGA_DCLK
H2	FPGA_CONFIG_D18		
G5	FPGA_CONFIG_D27	E2	FPGA_CONF_DONE
H3	FPGA_CONFIG_D19	F5	FPGA_nCONFIG
J1	FPGA_CONFIG_D20	H1	
H4	FPGA_CONFIG_D17	K4	
J2		L5	
H5	OSC_100_MAX2210	P3	M5_JTAG_TCK
J5		L6	M5_JTAG_TDI
		M5	M5_JTAG_TDO
		N4	M5_JTAG_TMS

U47B — Bank = 1.8V — MAX V BANK2 — 5M2210ZF256

Pin	Signal	Pin	Signal
D4	M5A10_R_IO0	E10	MAX_CONF_DONEn
B1	M5A10_R_IO1	A11	MAX_LOAD
C5	M5A10_R_IO2	B11	MAX_ERROR
C4	M5A10_R_IO3	A12	BOOT_PAGE
B4	M5A10_R_IO4	E11	M5A10_R_IO24
D6	M5A10_R_IO5	B12	M5A10_R_IO25
E6	M5A10_R_IO6	C11	M5A10_R_IO26
B5	M5A10_R_IO7	B13	M5A10_R_IO27
A5	M5A10_R_IO8	D12	M5A10_R_IO28
D7	M5A10_R_IO9	B14	M5A10_R_IO29
B6	M5A10_R_IO10	C13	M5A10_R_IO30
E7	M5A10_R_IO11	B16	M5A10_R_IO31
C8	M5A10_R_IO12		
B7	M5A10_R_IO13		
D8	M5A10_R_IO14	A13	
A7	M5A10_R_IO15	A15	
B8	M5A10_R_IO16	A2	
A8	M5A10_R_IO17	A4	
A9	M5A10_R_IO18	A6	
E9	M5A10_R_IO19	B10	M5M2_R_IO0
B9	M5A10_R_IO20	B3	M5M2_R_IO1
D9	M5A10_R_IO21	C10	M5M2_R_IO2
A10	M5A10_R_IO22	C12	M5M2_R_IO3
C9	M5A10_R_IO23	C6	
		C7	
		D10	
		D11	
		D5	
		E8	

U47C — Bank = 1.8V — MAX V BANK3 — 5M2210ZF256

Pin	Signal	Pin	Signal
E14	FLASH_A11	J14	FLASH_D4
C14	FLASH_A13	J15	FLASH_D20
C15	FLASH_A25	K16	FLASH_D14
E13	FLASH_A5	K13	FLASH_D29
E12	FLASH_A10	K15	FLASH_D12
D15	FLASH_A14	K14	FLASH_D27
F14	FLASH_A23	L16	FLASH_D6
D16	FLASH_A15	L11	FLASH_D22
F13	FLASH_A7	L15	FLASH_D7
E15	FLASH_A8	L12	FLASH_D10
E16	FLASH_A12	M16	FLASH_D26
F15	FLASH_A18	L13	FLASH_D13
G14	FLASH_A4	M15	FLASH_D18
F16	FLASH_A22	L14	FLASH_D5
G13	FLASH_A3	N16	FLASH_D16
G15	FLASH_A19	M13	FLASH_D2
G12	FLASH_A2	N15	FLASH_D17
G16	FLASH_A26	N14	FLASH_D11
H14	FLASH_A17	P15	FLASH_D24
H15	FLASH_A21	P14	FLASH_D3
H13	FLASH_A16		
H16	FLASH_A20	D13	FLASH_D30
J13	FLASH_A24	D14	FLASH_D23
J16	FLASH_D21	F11	FLASH_D31
		F12	FLASH_D15
		K12	FLASH_D28
		M14	FLASH_D19
J12	M5A10_R_CLK	N13	FLASH_D25
H12	CLK_50_MAX2210		

U47D — Bank = 1.8V — MAX V BANK4 — 5M2210ZF256

Pin	Signal	Pin	Signal
R1	FLASH_D1	M10	
P4	FLASH_D9	R10	
T2	FLASH_D8	N10	
P5	FLASH_D0	T11	
R3	FLASH_A6	P10	
N5		R11	
P6	FLASH_A1	T12	
N6	FLASH_A9	N11	
R5	FLASH_RESET_n	T13	
M6	FLASH_ADV_n	R13	
T5	FLASH_CE_n1	R12	FACTORY_LOAD
P7	FLASH_CLK	P11	CPU_RESET_n
R6	FLASH_WE_n	N12	
N7	FLASH_OE_n	R14	
M7	FLASH_RDY_BSY_n0	P12	
R7	FACTORY_STATUS	T15	FACTORY_LOAD
P8	FLASH_RDY_BSY_n1	R16	
T7	FLASH_CE_n0	P13	MSEL0
N8		M11	
R8		M12	MSEL1
T8		N9	MSEL2
T9		R4	
R9		T10	
P9	FACTORY_REQUEST	T4	
M9	MAX_RESET_n		
M8			

U47E — MAX V Power — 5M2210ZF256

Pin	Signal	Pin	Signal
F7	GNDINT	F10	VCCINT
G6	GNDINT	G11	VCCINT
H7	GNDINT	H10	VCCINT
H9	GNDINT	H8	VCCINT
J10	GNDINT	J7	VCCINT
J8	GNDINT	J9	VCCINT
K11	GNDINT	K6	VCCINT
L10	GNDINT	L7	VCCINT
A1	GNDIO	C1	VCCIO1
A16	GNDIO	H6	VCCIO1
B15	GNDIO	J6	VCCIO1
B2	GNDIO	P1	VCCIO1
G10	GNDIO		
G7	GNDIO	A14	VCCIO2
G8	GNDIO	A3	VCCIO2
G9	GNDIO	F8	VCCIO2
K10	GNDIO	F9	VCCIO2
K7	GNDIO		
K8	GNDIO	C16	VCCIO3
K9	GNDIO	H11	VCCIO3
R15	GNDIO	J11	VCCIO3
R2	GNDIO	P16	VCCIO3
T1	GNDIO		
T16	GNDIO	L8	VCCIO4
T6	GNDIO	L9	VCCIO4
		T14	VCCIO4
		T3	VCCIO4

VCC1P8

VCCINT

C121	C115	C119	C120	C114	C123	C112	C116
0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V

VCC1P8

VCCIO: 1.8V

C124	C122	C113	C133	C97	C99	C117	C135	C118	C134	C111	C98
0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V	0.1u 25V

VCC3P1_CPLDLED

Signal	Diode	Resistor
MAX_CONF_DONEn	D16 LEDG	R357 22
MAX_LOAD	D15 LEDY	R358 22
MAX_ERROR	D17 LEDR	R356 22
BOOT_PAGE	D19 LEDG	R355 22

VCC1P8

R342 10K

MAX_RST

MAX_RESET_n
PB5
TACT SW
C713 0.1u

VCC3P3

D24 1N4148WT-7
D23 1N4148WT-7

VCC3P1_CPLDLED

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Title: **DE5a-Net Board**

Size	Document Number	Rev
B	5M2210 System Controller	C

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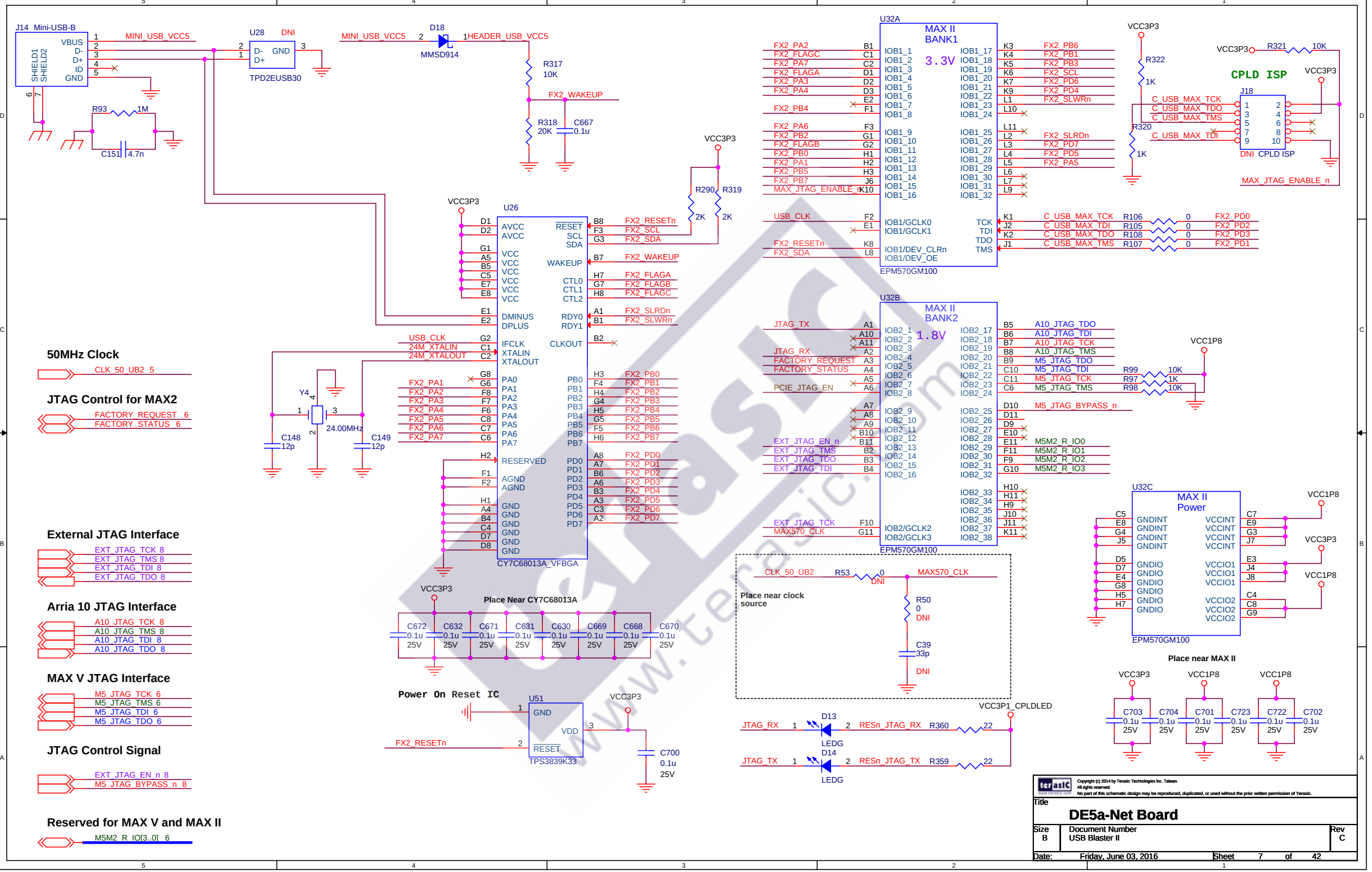

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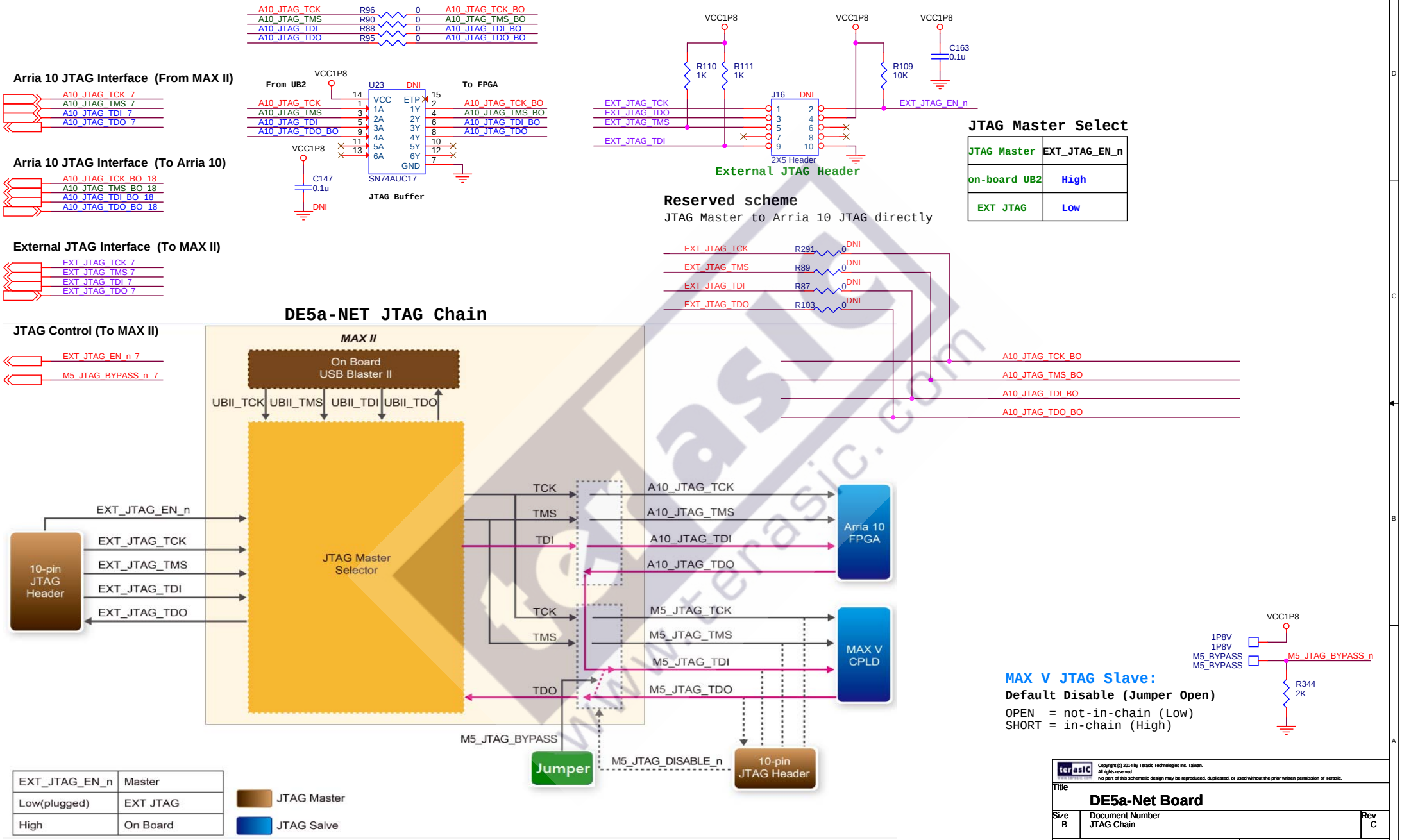
A10_JTAG_TCK
A10_JTAG_TMS
A10_JTAG_TDI
A10_JTAG_TDO
R96 0 A10_JTAG_TCK_BO
R90 0 A10_JTAG_TMS_BO
R88 0 A10_JTAG_TDI_BO
R95 0 A10_JTAG_TDO_BO
Arria 10 JTAG Interface (From MAX II)
A10_JTAG_TCK_7
A10_JTAG_TMS_7
A10_JTAG_TDI_7
A10_JTAG_TDO_7
VCC1P8
From UB2
U23 DNI
To FPGA
VCC
ETP
1A 1Y
2A 2Y
3A 3Y
4A 4Y
5A 5Y
6A 6Y
GND
SN74AUC17
A10_JTAG_TCK_BO
A10_JTAG_TMS_BO
A10_JTAG_TDI_BO
A10_JTAG_TDO
C147 0.1u
DNI
JTAG Buffer
Arria 10 JTAG Interface (To Arria 10)
A10_JTAG_TCK_BO_18
A10_JTAG_TMS_BO_18
A10_JTAG_TDI_BO_18
A10_JTAG_TDO_BO_18
External JTAG Interface (To MAX II)
EXT_JTAG_TCK_7
EXT_JTAG_TMS_7
EXT_JTAG_TDI_7
EXT_JTAG_TDO_7
JTAG Control (To MAX II)
EXT_JTAG_EN_n_7
M5_JTAG_BYPASS_n_7
R110 1K
R111 1K
R109 10K
C163 0.1u
J16 DNI
EXT_JTAG_TCK
EXT_JTAG_TDO
EXT_JTAG_TMS
EXT_JTAG_TDI
EXT_JTAG_EN_n
2X5 Header
External JTAG Header
JTAG Master Select
JTAG Master | EXT_JTAG_EN_n
on-board UB2 | High
EXT JTAG | Low
Reserved scheme
JTAG Master to Arria 10 JTAG directly
R291 0 DNI
R89 0 DNI
R87 0 DNI
R103 0 DNI
A10_JTAG_TCK_BO
A10_JTAG_TMS_BO
A10_JTAG_TDI_BO
A10_JTAG_TDO_BO
DE5a-NET JTAG Chain
MAX II
On Board USB Blaster II
UBII_TCK UBII_TMS UBII_TDI UBII_TDO
JTAG Master Selector
10-pin JTAG Header
EXT_JTAG_EN_n
EXT_JTAG_TCK
EXT_JTAG_TMS
EXT_JTAG_TDI
EXT_JTAG_TDO
TCK
TMS
TDI
TDO
A10_JTAG_TCK
A10_JTAG_TMS
A10_JTAG_TDI
A10_JTAG_TDO
Arria 10 FPGA
M5_JTAG_TCK
M5_JTAG_TMS
M5_JTAG_TDI
M5_JTAG_TDO
MAX V CPLD
M5_JTAG_BYPASS
Jumper
M5_JTAG_DISABLE_n
10-pin JTAG Header
EXT_JTAG_EN_n | Master
Low(plugged) | EXT JTAG
High | On Board
JTAG Master
JTAG Salve
VCC1P8
1P8V
1P8V
M5_BYPASS
M5_BYPASS
M5_JTAG_BYPASS_n
R344 2K
MAX V JTAG Slave:
Default Disable (Jumper Open)
OPEN = not-in-chain (Low)
SHORT = in-chain (High)
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Title
DE5a-Net Board
Size B
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JTAG Chain
Rev C
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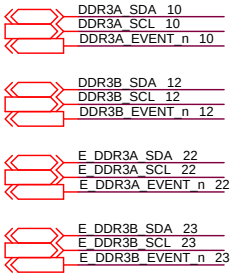
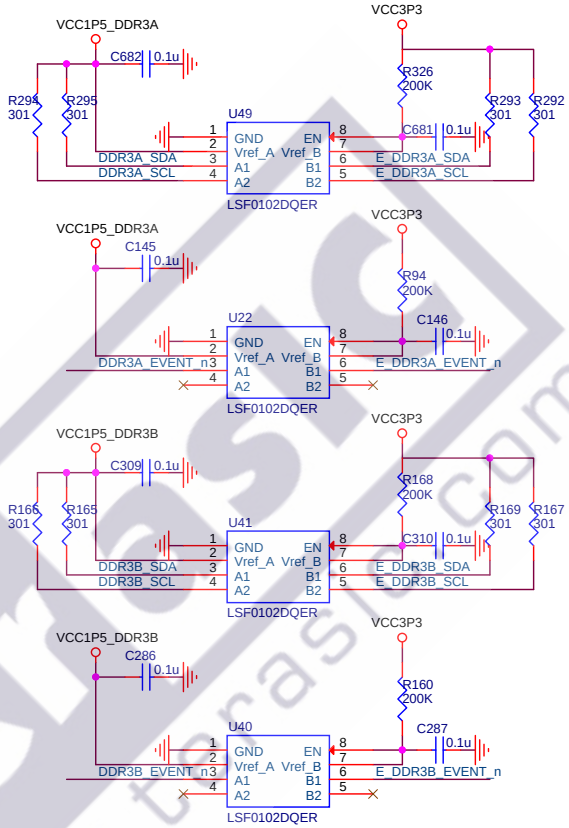
SO-DIMM1/2 SPD Interface





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Title
DE5a-Net Board

Size	Document Number	Rev
B	Level Shift	C

Date: Tuesday, May 24, 2016 Sheet 9 of 42

DDR3 DO-DIMM A

DDR3A_CK[1..0] 22
DDR3A_CK_n[1..0] 22
DDR3A_BA[2..0] 22
DDR3A_ODT[1..0] 22
DDR3A_CS_n[1..0] 22

DDR3A_DQ[63..0] 16,22
DDR3A_DQS[7..0] 16,22
DDR3A_DQS_n[7..0] 16,22

DDR3A_A[15..0] 16,22
DDR3A_DM[7..0] 16,22
DDR3A_CKE[1..0] 22

DDR3A_WE_n 22
DDR3A_CAS_n 22
DDR3A_RAS_n 22
DDR3A_RESET_n 22

DDR3A_SDA 9
DDR3A_SCL 9
DDR3A_EVENT_n 9

User Interface

SW[1..0] 35

User Interface 7'Seg

HEX1_D[6..0] 35
HEX1_DP 35

FAN Control Interface

FAN_I2C_SCL 34
FAN_I2C_SDA 34
FAN_ALERT_n 34

Clock Generator Interface

Si5340B_OE_n 3

U16-26

ARRIA 10 BANK 2G

VCCIO = 1.5V

HEX1_D0	AM33	LVDS2G_1P/DQ20,46		AY32	DDR3A_A8
HEX1_D1	AN33	LVDS2G_1N/DQ20,47		AY33	DDR3A_A9
HEX1_D2	AM32	LVDS2G_2P/DQ20,44	LVDS2G_14P/DQ22,20		
HEX1_D3	AN32	LVDS2G_2N/DQ20,45	LVDS2G_14N/DQ22,21		
HEX1_D4	AN31	LVDS2G_3P/DQ20,42			
HEX1_D5	AP31	LVDS2G_3N/DQ20,43			
HEX1_D6	AK32	LVDS2G_4P/DQS20/CQ20,40	LVDS2G_16P/DQS22/CQ22,16	BA37	DDR3A_A4
HEX1_DP	AK31	LVDS2G_4N/DQSN20/CQN20,41	LVDS2G_16N/DQSN22/CQN22,17	BB37	DDR3A_A5
FAN_I2C_SCL	AJ33	LVDS2G_5P/DQ20,38	LVDS2G_17P/DQ22,14	AV31	DDR3A_A2
FAN_I2C_SDA	AK33	LVDS2G_5N/DQ20,39	LVDS2G_17N/DQ22,15	AW31	DDR3A_A3
FAN_ALERT_n	AL32	LVDS2G_6P/DQ20,36 DQS10	DQS11 LVDS2G_18P/DQ22,12	AW34	DDR3A_A0
Si5340B_OE_n	AL31	LVDS2G_6N/DQ20,37 DQSn10	DQSn11 LVDS2G_18N/DQ22,13	AY34	DDR3A_A1
DDR3A_BA1	AP33			BA35	DDR3A_CK1
DDR3A_BA2	AR33	LVDS2G_7P/DQ21,34	LVDS2G_19P/DQ23,10	BA36	DDR3A_CK_n1
DDR3A_CAS_n	AR31	LVDS2G_7N/DQ21,35	LVDS2G_19N/DQ23,11	BA34	DDR3A_CK0
DDR3A_BA0	AR32	LVDS2G_8P/DQ21,32	LVDS2G_20P/DQ23,08	BB35	DDR3A_CK_n0
DDR3A_A15	AU32	LVDS2G_8N/DQ21,33	LVDS2G_20N/DQ23,09	BD33	DDR3A_CKE0
DDR3A_RAS_n	AV32	LVDS2G_9P/DQ21,30	LVDS2G_21P/DQ23,06	BD34	DDR3A_CKE1
		LVDS2G_9N/DQ21,31	LVDS2G_21N/DQ23,07	BC32	DDR3A_ODT0
			LVDS2G_22P/DQS23/CQ23,04	BC33	DDR3A_ODT1
			LVDS2G_22N/DQSN23/CQN23,05	BB33	DDR3A_CS_n0
	AU33	RZQ_2G/LVDS2G_11P/DQ21,26	LVDS2G_23P/DQ23,02	BB34	DDR3A_CS_n1
DDR3A_A12	AU34	LVDS2G_11N/DQ21,27	LVDS2G_23N/DQ23,03	BC35	DDR3A_WE_n
			LVDS2G_24P/DQ23,00	BD35	DDR3A_RESET_n
			LVDS2G_24N/DQ23,01		

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ARRIA 10 BANK 2F

VCCIO = 1.5V

DDR3A_DQ36	AN30	LVDS2F_1P/DQ24,46		BA32	DDR3A_DQ41
DDR3A_DM4	AP30	LVDS2F_1N/DQ24,47		BB32	DDR3A_DQ40
DDR3A_DQ35	AN28	LVDS2F_2P/DQ24,44	LVDS2F_14P/DQ26,20		
DDR3A_DQ34	AP28	LVDS2F_2N/DQ24,45	LVDS2F_14N/DQ26,21		
DDR3A_DQ38	AM28	LVDS2F_3P/DQ24,42			
DDR3A_DQ39	AM29	LVDS2F_3N/DQ24,43			
DDR3A_DQS4	AP29	LVDS2F_4P/DQS24/CQ24,40	LVDS2F_16P/DQS26/CQ26,16	BA29	DDR3A_DQS5
DDR3A_DQS_n4	AR29	LVDS2F_4N/DQSN24/CQN24,41	LVDS2F_16N/DQSN26/CQN26,17	BA30	DDR3A_DQS_n5
DDR3A_DQ32	AL30	LVDS2F_5P/DQ24,38	LVDS2F_17P/DQ26,14	BB30	DDR3A_DQ42
DDR3A_DQ33	AM30	LVDS2F_5N/DQ24,39	LVDS2F_17N/DQ26,15	BC31	DDR3A_DQ43
SW1	AM27	LVDS2F_6P/DQ24,36 DQS12	DQS13 LVDS2F_18P/DQ26,12	AY28	SW0
DDR3A_DQ37	AN27	LVDS2F_6N/DQ24,37 DQSn12	DQSn13 LVDS2F_18N/DQ26,13	AY29	DDR3A_DQ44
DDR3A_DQ58	AT30	LVDS2F_7P/DQ25,34	LVDS2F_19P/DQ27,10	BD30	DDR3A_DQ49
DDR3A_DM7	AU30	LVDS2F_7N/DQ25,35	LVDS2F_19N/DQ27,11	BD31	DDR3A_DM6
DDR3A_DQ62	AT29	LVDS2F_8P/DQ25,32	LVDS2F_20P/DQ27,08	BB28	DDR3A_DQ51
DDR3A_DQ60	AU29	LVDS2F_8N/DQ25,33	LVDS2F_20N/DQ27,09	BB29	DDR3A_DQ50
DDR3A_DQ59	AR28	LVDS2F_9P/DQ25,30	LVDS2F_21P/DQ27,06	BB27	DDR3A_DQ55
DDR3A_DQ63	AR27	LVDS2F_9N/DQ25,31	LVDS2F_21N/DQ27,07	BC27	DDR3A_DQ54
			LVDS2F_22P/DQS27/CQ27,04	BA26	DDR3A_DQS6
			LVDS2F_22N/DQSN27/CQN27,05	BA27	DDR3A_DQS_n6
RZQ_DDR3_A	AU28	RZQ_2F/LVDS2F_11P/DQ25,26	LVDS2F_23P/DQ27,02	BC30	DDR3A_DQ48
DDR3A_DQ61	AV28	LVDS2F_11N/DQ25,27	LVDS2F_23N/DQ27,03	BD29	DDR3A_DQ53
			LVDS2F_24P/DQ27,00	BC28	
			LVDS2F_24N/DQ27,01	BD28	DDR3A_DQ52

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ARRIA 10 BANK 2H

VCCIO = 1.5V

DDR3A_DQ7	AH36	LVDS2H_1P/DQ16,46		AL36	DDR3A_DQ14
DDR3A_DQ4	AH35	LVDS2H_1N/DQ16,47		AM37	DDR3A_DQ12
DDR3A_DQ5	AJ35	LVDS2H_2P/DQ16,44	LVDS2H_14P/DQ18,20		
DDR3A_DQ6	AJ36	LVDS2H_2N/DQ16,45	LVDS2H_14N/DQ18,21		
DDR3A_DQ2	AJ34	LVDS2H_3P/DQ16,42			
DDR3A_DM0	AK34	LVDS2H_3N/DQ16,43			
DDR3A_DQS0	AK37	LVDS2H_4P/DQS16/CQ16,40	LVDS2H_16P/DQS18/CQ18,16	AL34	DDR3A_DQS1
DDR3A_DQS_n0	AL37	LVDS2H_4N/DQSN16/CQN16,41	LVDS2H_16N/DQSN18/CQN18,17	AM34	DDR3A_DQS_n1
DDR3A_DQ0	AH32	LVDS2H_5P/DQ16,38	LVDS2H_17P/DQ18,14	AK36	DDR3A_DQ15
DDR3A_DQ1	AH33	LVDS2H_5N/DQ16,39	LVDS2H_17N/DQ18,15	AL35	DDR3A_DQ11
DDR3A_SDA	AG34	LVDS2H_6P/DQ16,36 DQS8/CQ8	DQS9/CQ9 LVDS2H_18P/DQ18,12	AR34	DDR3A_EVENT_n
DDR3A_DQ3	AG35	LVDS2H_6N/DQ16,37 DQSn8/CQn8	DQSn9/CQn9 LVDS2H_18N/DQ18,13	AT34	DDR3A_DQ13
DDR3A_DQ27	AN37	LVDS2H_7P/DQ17,34	LVDS2H_19P/DQ19,10	AT36	DDR3A_DQ17
DDR3A_DQ26	AN38	LVDS2H_7N/DQ17,35	LVDS2H_19N/DQ19,11	AT37	DDR3A_DM2
DDR3A_DQ29	AM39	LVDS2H_8P/DQ17,32	LVDS2H_20P/DQ19,08	AU37	DDR3A_DQ18
DDR3A_DQ28	AM38	LVDS2H_8N/DQ17,33	LVDS2H_20N/DQ19,09	AV37	DDR3A_DQ19
DDR3A_DQ25	AN36	LVDS2H_9P/DQ17,30	LVDS2H_21P/DQ19,06	AT39	DDR3A_DQ22
DDR3A_DM3	AP36	LVDS2H_9N/DQ17,31	LVDS2H_21N/DQ19,07	AU39	DDR3A_DQ23
			LVDS2H_22P/DQS19/CQ19,04	AU38	DDR3A_DQS2
			LVDS2H_22N/DQSN19/CQN19,05	AV38	DDR3A_DQS_n2
	AP39	RZQ_2H/LVDS2H_11P/DQ17,26	LVDS2H_23P/DQ19,02	AV35	DDR3A_DQ20
DDR3A_DQ31	AR39	LVDS2H_11N/DQ17,27	LVDS2H_23N/DQ19,03	AV36	DDR3A_DQ21
			LVDS2H_24P/DQ19,00	AT35	DDR3A_SCL
			LVDS2H_24N/DQ19,01	AU35	DDR3A_DQ16

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Title
DE5a-Net Board

Size	Document Number	Rev
B	FPGA Bank 2F, 2G, 2H	C

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QDRII+ PORT C

QDRIIC_Q[17..0] 16,26
QDRIIC_D[17..0] 16,26
QDRIIC_A[21..0] 16,26
QDRIIC_BWS_n[1..0] 16,26
QDRIIC_WPS_n 26
QDRIIC_RPS_n 26
QDRIIC_K_p 26
QDRIIC_K_n 26
QDRIIC_CQ_p 26
QDRIIC_CQ_n 26
QDRIIC_ODT 26
QDRIIC_DOFF_n 26
QDRIIC_QVLD 26

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QDRII+ PORT D

QDRIID_Q[17..0] 16,27
QDRIID_D[17..0] 16,27
QDRIID_A[21..0] 16,27
QDRIID_BWS_n[1..0] 27
QDRIID_WPS_n 27
QDRIID_RPS_n 27
QDRIID_K_p 27
QDRIID_K_n 27
QDRIID_CQ_p 27
QDRIID_CQ_n 27
QDRIID_QVLD 27
QDRIID_ODT 27
QDRIID_DOFF_n 27

TI TPS40422 Interface

TPS40422_CLK 38
TPS40422_DATA 38

FLASH Bus

FLASH_A[26..1] 6,13,28
FLASH_D[31..0] 6,28

FLASH control signal

FLASH_CLK 6,13,28
FLASH_RESET_n 6,13,28
FLASH_OE_n 6,13,28
FLASH_WE_n 6,13,28
FLASH_ADV_n 6,13,28
FLASH_CE_n[1..0] 6,13,28
FLASH_RDY_BSY_n[1..0] 6,13,28

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ARRIA 10 BANK 2I

VCCIO = 1.8V

FLASH_D9	B34	LVDS2I_1P/DQ12,46	
FLASH_D0	B35	LVDS2I_1N/DQ12,47	
FLASH_D2	C35	LVDS2I_2P/DQ12,44	LVDS2I_14P/DQ14,20
FLASH_D8	C36	LVDS2I_2N/DQ12,45	LVDS2I_14N/DQ14,21
FLASH_D4	C32	LVDS2I_3P/DQ12,42	
FLASH_D3	C33	LVDS2I_3N/DQ12,43	
FLASH_D10	A34	LVDS2I_4P/DQS12/CQ12,40	LVDS2I_16P/DQS14/CQ14,16
FLASH_D1	A35	LVDS2I_4N/DQSN12/CQN12,41	LVDS2I_16N/DQSN14/CQN14,17
FLASH_D11	B33	LVDS2I_5P/DQ12,38	LVDS2I_17P/DQ14,14
FLASH_D12	B32	LVDS2I_5N/DQ12,39	LVDS2I_17N/DQ14,15
FLASH_D5	A32	LVDS2I_6P/DQ12,36 DQS6/CQ6	DQS7/CQ7 LVDS2I_18P/DQ14,12
FLASH_D13	A31	LVDS2I_6N/DQ12,37 DQSn6/CQn6	DQSn7/CQn7 LVDS2I_18N/DQ14,13
QDRIIC_A21	J26	LVDS2I_7P/DQ13,34	LVDS2I_19P/DQ15,10
FLASH_A1	H26	LVDS2I_7N/DQ13,35	LVDS2I_19N/DQ15,11
QDRIIC_A19	J25	LVDS2I_8P/DQ13,32	LVDS2I_20P/DQ15,08
QDRIIC_A20	H25	LVDS2I_8N/DQ13,33	LVDS2I_20N/DQ15,09
QDRIIC_A17	G25	LVDS2I_9P/DQ13,30	LVDS2I_21P/DQ15,06
QDRIIC_A18	F25	LVDS2I_9N/DQ13,31	LVDS2I_21N/DQ15,07
			LVDS2I_22P/DQS15/CQ15,04
			LVDS2I_22N/DQSN15/CQN15,05
RZQ_QDRII_C	L24	RZQ_2I/LVDS2I_11P/DQ13,26	LVDS2I_23P/DQ15,02
QDRIIC_A14	L25	LVDS2I_11N/DQ13,27	LVDS2I_23N/DQ15,03
			LVDS2I_24P/DQ15,00
			LVDS2I_24N/DQ15,01

B29	QDRIIC_A10
B30	QDRIIC_A11
B27	QDRIIC_A6
B28	QDRIIC_A7
A29	QDRIIC_A4
A30	QDRIIC_A5
A26	QDRIIC_A2
A27	QDRIIC_A3
D25	QDRIIC_A0
D26	QDRIIC_A1
C25	FLASH_D15
C26	FLASH_D6
F26	QDRIIC_WPS_n
E26	QDRIIC_RPS_n
E24	FLASH_D14
D24	QDRIIC_DOFF_n
A24	TPS40422_CLK
A25	TPS40422_DATA
B24	FLASH_D7
B25	QDRIIC_ODT

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ARRIA 10 BANK 2K

VCCIO = 1.8V

FLASH_D20	H36	LVDS2K_1P/DQ4,46	
FLASH_D30	H35	LVDS2K_1N/DQ4,47	
FLASH_D16	K33	LVDS2K_2P/DQ4,44	LVDS2K_14P/DQ6,20
FLASH_D31	J33	LVDS2K_2N/DQ4,45	LVDS2K_14N/DQ6,21
FLASH_D26	K34	LVDS2K_3P/DQ4,42	
FLASH_D22	J34	LVDS2K_3N/DQ4,43	
FLASH_D25	J38	LVDS2K_4P/DQS4/CQ4,40	LVDS2K_16P/DQS6/CQ6,16
FLASH_D17	J39	LVDS2K_4N/DQSN4/CQN4,41	LVDS2K_16N/DQSN6/CQN6,17
FLASH_D28	H37	LVDS2K_5P/DQ4,38	LVDS2K_17P/DQ6,14
FLASH_D27	H38	LVDS2K_5N/DQ4,39	LVDS2K_17N/DQ6,15
FLASH_D19	J35	LVDS2K_6P/DQ4,36 DQS2/CQ2	DQS3/CQ3 LVDS2K_18P/DQ6,12
FLASH_D24	J36	LVDS2K_6N/DQ4,37 DQSn2/CQn2	DQSn3/CQn3 LVDS2K_18N/DQ6,13
QDRIID_A21	L35	LVDS2K_7P/DQ5,34	LVDS2K_19P/DQ7,10
FLASH_RDY_BSY_n1	L36	LVDS2K_7N/DQ5,35	LVDS2K_19N/DQ7,11
QDRIID_A19	L39	LVDS2K_8P/DQ5,32	LVDS2K_20P/DQ7,08
QDRIID_A20	K39	LVDS2K_8N/DQ5,33	LVDS2K_20N/DQ7,09
QDRIID_A17	N33	LVDS2K_9P/DQ5,30	LVDS2K_21P/DQ7,06
QDRIID_A18	M33	LVDS2K_9N/DQ5,31	LVDS2K_21N/DQ7,07
			LVDS2K_22P/DQS7/CQ7,04
			LVDS2K_22N/DQSN7/CQN7,05
RZQ_QDRII_D	K37	RZQ_2K/LVDS2K_11P/DQ5,26	LVDS2K_23P/DQ7,02
QDRIID_A14	K38	LVDS2K_11N/DQ5,27	LVDS2K_23N/DQ7,03
			LVDS2K_24P/DQ7,00
			LVDS2K_24N/DQ7,01

N32	QDRIID_A10
M32	QDRIID_A11
R34	QDRIID_A6
R33	QDRIID_A7
L32	QDRIID_A4
K32	QDRIID_A5
P34	QDRIID_A2
P33	QDRIID_A3
Y32	QDRIID_A0
W33	QDRIID_A1
AB32	FLASH_D21
AA31	FLASH_D23
V32	QDRIID_WPS_n
V33	QDRIID_RPS_n
Y31	FLASH_D29
W31	QDRIID_DOFF_n
U33	
U32	
AA32	FLASH_D18
Y33	QDRIID_ODT

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ARRIA 10 BANK 2J

VCCIO = 1.8V

QDRIIC_D11	AD34	LVDS2J_1P/DQ8,46	
QDRIIC_BWS_n1	AD35	LVDS2J_1N/DQ8,47	
QDRIIC_D15	AE31	LVDS2J_2P/DQ8,44	LVDS2J_14P/DQ10,20
QDRIIC_D14	AE32	LVDS2J_2N/DQ8,45	LVDS2J_14N/DQ10,21
QDRIIC_D9	AF36	LVDS2J_3P/DQ8,42	
QDRIIC_D10	AE36	LVDS2J_3N/DQ8,43	
QDRIIC_D17	AF31	LVDS2J_4P/DQS8/CQ8,40	LVDS2J_16P/DQS10/CQ10,16
QDRIIC_D16	AF32	LVDS2J_4N/DQSN8/CQN8,41	LVDS2J_16N/DQSN10/CQN10,17
QDRIIC_D13	AE33	LVDS2J_5P/DQ8,38	LVDS2J_17P/DQ10,14
QDRIIC_D12	AE34	LVDS2J_5N/DQ8,39	LVDS2J_17N/DQ10,15
QDRIIC_K_p	AF34	LVDS2J_6P/DQ8,36 DQS4/CQ4	DQS5/CQ5 LVDS2J_18P/DQ10,12
QDRIIC_K_n	AF35	LVDS2J_6N/DQ8,37 DQSn4/CQn4	DQSn5/CQn5 LVDS2J_18N/DQ10,13
QDRIIC_D6	W34	LVDS2J_7P/DQ9,34	LVDS2J_19P/DQ11,10
QDRIIC_D5	Y34	LVDS2J_7N/DQ9,35	LVDS2J_19N/DQ11,11
QDRIIC_D3	AB34	LVDS2J_8P/DQ9,32	LVDS2J_20P/DQ11,08
QDRIIC_D7	AC35	LVDS2J_8N/DQ9,33	LVDS2J_20N/DQ11,09
QDRIIC_D2	AB33	LVDS2J_9P/DQ9,30	LVDS2J_21P/DQ11,06
QDRIIC_D4	AA34	LVDS2J_9N/DQ9,31	LVDS2J_21N/DQ11,07
			LVDS2J_22P/DQS11/CQ11,04
			LVDS2J_22N/DQSN11/CQN11,05
QDRIIC_D0	AD33	RZQ_2J/LVDS2J_11P/DQ9,26	LVDS2J_23P/DQ11,02
QDRIIC_D1	AC33	LVDS2J_11N/DQ9,27	LVDS2J_23N/DQ11,03
			LVDS2J_24P/DQ11,00
			LVDS2J_24N/DQ11,01

U35	QDRIIC_Q15
T35	QDRIIC_Q14
W35	QDRIIC_Q17
V35	QDRIIC_Q16
U34	QDRIIC_QVLD
T34	QDRIIC_Q12
AD36	QDRIIC_CQ_p
AC36	QDRIIC_CQ_n
N35	QDRIIC_Q13
M35	QDRIIC_Q11
N36	QDRIIC_Q3
M37	QDRIIC_Q10
M39	QDRIIC_Q6
M38	QDRIIC_Q5
N38	QDRIIC_Q7
N37	QDRIIC_Q4
T36	QDRIIC_Q0
R36	QDRIIC_Q1
P35	QDRIIC_Q2
P36	QDRIIC_Q8

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ARRIA 10 BANK 2L

VCCIO = 1.8V

QDRIID_D9	E33	LVDS2L_1P/DQ0,46	
QDRIID_D4	D33	LVDS2L_1N/DQ0,47	
QDRIID_D6	G30	LVDS2L_2P/DQ0,44	LVDS2L_14P/DQ2,20
QDRIID_BWS_n0	F30	LVDS2L_2N/DQ0,45	LVDS2L_14N/DQ2,21
QDRIID_D7	H30	LVDS2L_3P/DQ0,42	
QDRIID_D8	G29	LVDS2L_3N/DQ0,43	
QDRIID_D1	F34	LVDS2L_4P/DQS0/CQ0,40	LVDS2L_16P/DQS2/CQ2,16
QDRIID_D13	E34	LVDS2L_4N/DQSN0/CQN0,41	LVDS2L_16N/DQSN2/CQN2,17
QDRIID_D5	F31	LVDS2L_5P/DQ0,38	LVDS2L_17P/DQ2,14
QDRIID_BWS_n1	E31	LVDS2L_5N/DQ0,39	LVDS2L_17N/DQ2,15
QDRIID_K_p	F32	LVDS2L_6P/DQ0,36 DQS0/CQ0	DQS1/CQ1 LVDS2L_18P/DQ2,12
QDRIID_K_n	E32	LVDS2L_6N/DQ0,37 DQSn0/CQn0	DQSn1/CQn1 LVDS2L_18N/DQ2,13
QDRIID_D14	D36	LVDS2L_7P/DQ1,34	LVDS2L_19P/DQ3,10
QDRIID_D15	C37	LVDS2L_7N/DQ1,35	LVDS2L_19N/DQ3,11
QDRIID_D16	D35	LVDS2L_8P/DQ1,32	LVDS2L_20P/DQ3,08
QDRIID_D17	D34	LVDS2L_8N/DQ1,33	LVDS2L_20N/DQ3,09
QDRIID_D10	G39	LVDS2L_9P/DQ1,30	LVDS2L_21P/DQ3,06
QDRIID_D2	F39	LVDS2L_9N/DQ1,31	LVDS2L_21N/DQ3,07
			LVDS2L_22P/DQS3/CQ3,04
			LVDS2L_22N/DQSN3/CQN3,05
QDRIID_D12	F37	RZQ_2L/LVDS2L_11P/DQ1,26	LVDS2L_23P/DQ3,02
QDRIID_D11	E37	LVDS2L_11N/DQ1,27	LVDS2L_23N/DQ3,03
			LVDS2L_24P/DQ3,00
			LVDS2L_24N/DQ3,01

K31	QDRIID_Q13
J31	QDRIID_Q12
G34	QDRIID_Q9
G33	QDRIID_Q10
L31	QDRIID_Q11
L30	QDRIID_Q14
G35	QDRIID_CQ_p
F35	QDRIID_CQ_n
M28	QDRIID_Q16
M29	QDRIID_Q15
P28	QDRIID_QVLD
N28	QDRIID_Q17
L29	QDRIID_Q0
K29	QDRIID_Q2
J30	QDRIID_Q5
J29	QDRIID_Q3
N30	QDRIID_Q1
M30	QDRIID_Q4
P31	QDRIID_Q7
N31	QDRIID_Q6

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Title
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Size	Document Number	Rev
B	FPGA Bank 2I, 2J, 2K, 2L	C

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DDR3 DO-DIMM B

DDR3B_CK[1..0] 23
DDR3B_CK_n[1..0] 23
DDR3B_BA[2..0] 23
DDR3B_ODT[1..0] 23
DDR3B_CS_n[1..0] 23

DDR3B_DQ[63..0] 17,23
DDR3B_DQS[7..0] 17,23
DDR3B_DQS_n[7..0] 17,23

DDR3B_A[15..0] 17,23
DDR3B_DM[7..0] 17,23
DDR3B_CKE[1..0] 23

DDR3B_WE_n 23
DDR3B_CAS_n 23
DDR3B_RAS_n 23
DDR3B_RESET_n 23

DDR3B_SDA 9
DDR3B_SCL 9
DDR3B_EVENT_n 9

User Interface

BUTTON[3..0] 35

User Interface 7'Seg

HEX0_D[6..0] 35
HEX0_DP 35

RS-422 Interface

RS422_RE_n 35
RS422_DIN 35

RS422_DOUT 35
RS422_DE 35

Clock Generator Interface

Si5340A_OE_n 4

FPGA Temperature Control and Monitor

TEMP_I2C_SCL 34
TEMP_I2C_SDA 34
TEMP_OVERT_n 34
TEMP_INT_n 34

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ARRIA 10 BANK 3C

VCCIO = 1.5V

DDR3B_DQ24	AN11	LVDS3C_1P/DQ52,46			
DDR3B_DQ25	AP11	LVDS3C_1N/DQ52,47			
DDR3B_DQ27	AR11	LVDS3C_2P/DQ52,44	LVDS3C_14P/DQ54,20	AE12	DDR3B_DQ47
DDR3B_DM3	AT11	LVDS3C_2N/DQ52,45	LVDS3C_14N/DQ54,21	AF12	DDR3B_DQ46
DDR3B_DQ31	AR12	LVDS3C_3P/DQ52,42			
DDR3B_DQ29	AT12	LVDS3C_3N/DQ52,43			
DDR3B_DQS3	AT10	LVDS3C_4P/DQS52/CQ52,40	LVDS3C_16P/DQS54/CQ54,16	AG12	DDR3B_DQS5
DDR3B_DQS_n3	AU10	LVDS3C_4N/DQSN52/CQN52,41	LVDS3C_16N/DQSN54/CQN54,17	AH12	DDR3B_DQS_n5
DDR3B_DQ28	AR8	LVDS3C_5P/DQ52,38	LVDS3C_17P/DQ54,14	AH13	DDR3B_DQ43
DDR3B_DQ26	AR7	LVDS3C_5N/DQ52,39	LVDS3C_17N/DQ54,15	AG13	DDR3B_DQ42
DDR3B_SDA	AP9	LVDS3C_6P/DQ52,36	LVDS3C_18P/DQ54,12	AJ13	BUTTON0
DDR3B_DQ30	AP8	LVDS3C_6N/DQ52,37	LVDS3C_18N/DQ54,13	AK13	DDR3B_DQ41
DDR3B_DQ39	AP10	LVDS3C_7P/DQ53,34	LVDS3C_19P/DQ55,10	AG14	DDR3B_DQ61
DDR3B_DM4	AN10	LVDS3C_7N/DQ53,35	LVDS3C_19N/DQ55,11	AF14	DDR3B_DM7
DDR3B_DQ32	AU8	LVDS3C_8P/DQ53,32	LVDS3C_20P/DQ55,08	AD14	DDR3B_DQ63
DDR3B_DQ36	AU7	LVDS3C_8N/DQ53,33	LVDS3C_20N/DQ55,09	AD13	DDR3B_DQ59
DDR3B_DQ34	AU9	LVDS3C_9P/DQ53,30	LVDS3C_21P/DQ55,06	AB14	DDR3B_DQ62
DDR3B_DQ33	AV8	LVDS3C_9N/DQ53,31	LVDS3C_21N/DQ55,07	AB13	DDR3B_DQ58
			LVDS3C_22P/DQS55/CQ55,04	AC13	DDR3B_DQS7
			LVDS3C_22N/DQSN55/CQN55,05	AB12	DDR3B_DQS_n7
BUTTON3	AR9	RZQ_3C/LVDS3C_11P/DQ53,26	LVDS3C_23P/DQ55,02	AC12	DDR3B_DQ57
DDR3B_DQ38	AT9	LVDS3C_11N/DQ53,27	LVDS3C_23N/DQ55,03	AC11	DDR3B_DQ56
			LVDS3C_24P/DQ55,00	AE13	BUTTON1
			LVDS3C_24N/DQ55,01	AE14	DDR3B_DQ60

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ARRIA 10 BANK 3A

VCCIO = 1.5V

DDR3B_DQ1	AU19	LVDS3A_1P/DQ60,46			
DDR3B_DM0	AT19	LVDS3A_1N/DQ60,47			
DDR3B_DQ4	AM20	LVDS3A_2P/DQ60,44	LVDS3A_14P/DQ62,20	AW16	DDR3B_DQ14
DDR3B_DQ3	AM19	LVDS3A_2N/DQ60,45	LVDS3A_14N/DQ62,21	AY16	DDR3B_DQ10
DDR3B_DQ2	AP19	LVDS3A_3P/DQ60,42			
DDR3B_DQ0	AR19	LVDS3A_3N/DQ60,43			
DDR3B_DQS0	AV18	LVDS3A_4P/DQS60/CQ60,40	LVDS3A_16P/DQS62/CQ62,16	BA15	DDR3B_DQS1
DDR3B_DQS_n0	AU18	LVDS3A_4N/DQSN60/CQN60,41	LVDS3A_16N/DQSN62/CQN62,17	BA16	DDR3B_DQS_n1
DDR3B_DQ7	AM17	LVDS3A_5P/DQ60,38	LVDS3A_17P/DQ62,14	AU15	DDR3B_DQ15
DDR3B_DQ6	AM18	LVDS3A_5N/DQ60,39	LVDS3A_17N/DQ62,15	AV15	DDR3B_DQ11
DDR3B_EVENT_n	AP18	LVDS3A_6P/DQ60,36	LVDS3A_18P/DQ62,12	AV16	BUTTON2
DDR3B_DQ5	AR18	LVDS3A_6N/DQ60,37	LVDS3A_18N/DQ62,13	AV17	DDR3B_DQ13
DDR3B_DQ22	BC16	LVDS3A_7P/DQ61,34	LVDS3A_19P/DQ63,10	AT17	DDR3B_DQ53
DDR3B_DM2	BC17	LVDS3A_7N/DQ61,35	LVDS3A_19N/DQ63,11	AU17	DDR3B_DM6
DDR3B_DQ18	BD15	LVDS3A_8P/DQ61,32	LVDS3A_20P/DQ63,08	AR16	DDR3B_DQ51
DDR3B_DQ17	BD16	LVDS3A_8N/DQ61,33	LVDS3A_20N/DQ63,09	AR17	DDR3B_DQ55
DDR3B_DQ21	BC18	LVDS3A_9P/DQ61,30	LVDS3A_21P/DQ63,06	AN15	DDR3B_DQ49
DDR3B_DQ20	BD18	LVDS3A_9N/DQ61,31	LVDS3A_21N/DQ63,07	AM15	DDR3B_DQ48
			LVDS3A_22P/DQS63/CQ63,04	AT15	DDR3B_DQS6
			LVDS3A_22N/DQSN63/CQN63,05	AT16	DDR3B_DQS_n6
RZQ_DDR3_B	BB15	RZQ_3A/LVDS3A_11P/DQ61,26	LVDS3A_23P/DQ63,02	AN16	DDR3B_DQ50
DDR3B_DQ19	BC15	LVDS3A_11N/DQ61,27	LVDS3A_23N/DQ63,03	AN17	DDR3B_DQ54
			LVDS3A_24P/DQ63,00	AP16	DDR3B_SCL
			LVDS3A_24N/DQ63,01	AP15	DDR3B_DQ52

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ARRIA 10 BANK 3D

VCCIO = 1.8V

QSFPA_MOD_SEL_n	AC10	LVDS3D_1P/DQ48,46			
QSFPA_INTERRUPT_n	AB9	LVDS3D_1N/DQ48,47			
QSFPA_SCL	AA10	LVDS3D_2P/DQ48,44	LVDS3D_14P/DQ50,20	AL9	QSFPC_MOD_SEL_n
QSFPA_SDA	Y9	LVDS3D_2N/DQ48,45	LVDS3D_14N/DQ50,21	AM9	RS422_DIN
QSFPA_RST_n	AA9	LVDS3D_3P/DQ48,42			
QSFPA_LP_MODE	AB10	LVDS3D_3N/DQ48,43			
QSFPA_MOD_PRS_n	AG10	LVDS3D_4P/DQS48/CQ48,40	LVDS3D_16P/DQS50/CQ50,16	AP6	QSFPB_MOD_SEL_n
LED_BRACKET0	AF10	LVDS3D_4N/DQSN48/CQN48,41	LVDS3D_16N/DQSN50/CQN50,17	AR6	QSFPB_RST_n
	AG9	LVDS3D_5P/DQ48,38	LVDS3D_17P/DQ50,14	AL10	QSFPB_MOD_PRS_n
LED_BRACKET1	AF9	LVDS3D_5N/DQ48,39	LVDS3D_17N/DQ50,15	AM10	QSFPB_LP_MODE
	AE9	LVDS3D_6P/DQ48,36	LVDS3D_18P/DQ50,12	AM8	QSFPB_SDA
RS422_RE_n	AD9	LVDS3D_6N/DQ48,37	LVDS3D_18N/DQ50,13	AM7	QSFPB_SCL
QSFPC_RST_n	AJ9	LVDS3D_7P/DQ49,34	LVDS3D_19P/DQ51,10	W14	RS422_DOUT
QSFPB_INTERRUPT_n	AK9	LVDS3D_7N/DQ49,35	LVDS3D_19N/DQ51,11	W13	QSFPD_INTERRUPT_n
QSFPC_MOD_PRS_n	AD10	LVDS3D_8P/DQ49,32	LVDS3D_20P/DQ51,08	Y11	QSFPD_RST_n
QSFPC_INTERRUPT_n	AD11	LVDS3D_8N/DQ49,33	LVDS3D_20N/DQ51,09	AA11	QSFPD_MOD_SEL_n
QSFPC_SDA	AK11	LVDS3D_9P/DQ49,30	LVDS3D_21P/DQ51,06	W9	QSFPD_SCL
QSFPC_SCL	AL11	LVDS3D_9N/DQ49,31	LVDS3D_21N/DQ51,07	W10	QSFPD_SDA
			LVDS3D_22P/DQS51/CQ51,04	AA12	QSFPD_LP_MODE
			LVDS3D_22N/DQSN51/CQN51,05	Y12	QSFPD_MOD_PRS_n
QSFPC_LP_MODE	AH10	RZQ_3D/LVDS3D_11P/DQ49,26	LVDS3D_23P/DQ51,02	Y13	LED_BRACKET2
Si5340A_OE_n	AJ10	LVDS3D_11N/DQ49,27	LVDS3D_23N/DQ51,03	Y14	RS422_DE
			LVDS3D_24P/DQ51,00	W11	LED_BRACKET3
			LVDS3D_24N/DQ51,01	V10	

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ARRIA 10 BANK 3B

VCCIO = 1.5V

HEX0_D0	AV10	LVDS3B_1P/DQ56,46			
HEX0_D1	AV11	LVDS3B_1N/DQ56,47			
HEX0_D2	AW8	LVDS3B_2P/DQ56,44	LVDS3B_14P/DQ58,20	AU13	DDR3B_A8
HEX0_D3	AY8	LVDS3B_2N/DQ56,45	LVDS3B_14N/DQ58,21	AV13	DDR3B_A9
HEX0_D4	AY9	LVDS3B_3P/DQ56,42			
HEX0_D5	BA9	LVDS3B_3N/DQ56,43			
HEX0_D6	AW10	LVDS3B_4P/DQS56/CQ56,40	LVDS3B_16P/DQS58/CQ58,16	AY14	DDR3B_A4
HEX0_DP	AW9	LVDS3B_4N/DQSN56/CQN56,41	LVDS3B_16N/DQSN58/CQN58,17	BA14	DDR3B_A5
TEMP_I2C_SCL	AU12	LVDS3B_5P/DQ56,38	LVDS3B_17P/DQ58,14	AW13	DDR3B_A2
TEMP_I2C_SDA	AV12	LVDS3B_5N/DQ56,39	LVDS3B_17N/DQ58,15	AY13	DDR3B_A3
TEMP_OVERT_n	AW11	LVDS3B_6P/DQ56,36	LVDS3B_18P/DQ58,12	AW15	DDR3B_A0
TEMP_INT_n	AY12	LVDS3B_6N/DQ56,37	LVDS3B_18N/DQ58,13	AW14	DDR3B_A1
DDR3B_BA1	AP13	LVDS3B_7P/DQ57,34	LVDS3B_19P/DQ59,10	BB9	DDR3B_CK1
DDR3B_BA2	AR13	LVDS3B_7N/DQ57,35	LVDS3B_19N/DQ59,11	BB8	DDR3B_CK_n1
DDR3B_CAS_n	AT14	LVDS3B_8P/DQ57,32	LVDS3B_20P/DQ59,08	BA10	DDR3B_CK0
DDR3B_BA0	AU14	LVDS3B_8N/DQ57,33	LVDS3B_20N/DQ59,09	BB10	DDR3B_CK_n0
DDR3B_A15	AL14	LVDS3B_9P/DQ57,30	LVDS3B_21P/DQ59,06	BC10	DDR3B_CKE0
DDR3B_RAS_n	AM14	LVDS3B_9N/DQ57,31	LVDS3B_21N/DQ59,07	BD10	DDR3B_CKE1
			LVDS3B_22P/DQS59/CQ59,04	BC11	DDR3B_ODT0
			LVDS3B_22N/DQSN59/CQN59,05	BD11	DDR3B_ODT1
DDR3B_A12	AJ14	RZQ_3B/LVDS3B_11P/DQ57,26	LVDS3B_23P/DQ59,02	BC13	DDR3B_CS_n0
	AK14	LVDS3B_11N/DQ57,27	LVDS3B_23N/DQ59,03	BC12	DDR3B_CS_n1
			LVDS3B_24P/DQ59,00	BB14	DDR3B_WE_n
			LVDS3B_24N/DQ59,01	BB13	DDR3B_RESET_n

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QSFP Port A Control Interface

QSFPA_MOD_SEL_n 29
QSFPA_RST_n 29
QSFPA_SCL 29
QSFPA_SDA 29
QSFPA_LP_MODE 29
QSFPA_INTERRUPT_n 29
QSFPA_MOD_PRS_n 29

LED_BRACKET[3..0] 35

QSFP Port B Control Interface

QSFPB_MOD_SEL_n 30
QSFPB_RST_n 30
QSFPB_SCL 30
QSFPB_SDA 30
QSFPB_LP_MODE 30
QSFPB_INTERRUPT_n 30
QSFPB_MOD_PRS_n 30

QSFP Port C Control Interface

QSFPC_MOD_SEL_n 31
QSFPC_RST_n 31
QSFPC_SCL 31
QSFPC_SDA 31
QSFPC_LP_MODE 31
QSFPC_INTERRUPT_n 31
QSFPC_MOD_PRS_n 31

QSFP Port D Control Interface

QSFPD_MOD_SEL_n 32
QSFPD_RST_n 32
QSFPD_SCL 32
QSFPD_SDA 32
QSFPD_LP_MODE 32
QSFPD_INTERRUPT_n 32
QSFPD_MOD_PRS_n 32

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Title
DE5a-Net Board

Size	Document Number	Rev
B	FPGA Bank 3A, 3B, 3C, 3D	C

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QDRII+ PORT A

QDRIIA_Q[17..0] 17,24
QDRIIA_D[17..0] 17,24
QDRIIA_A[21..0] 17,24
QDRIIA_BWS_n[1..0] 24
QDRIIA_WPS_n 24
QDRIIA_RPS_n 24
QDRIIA_K_p 24
QDRIIA_K_n 24
QDRIIA_CQ_p 24
QDRIIA_CQ_n 24
QDRIIA_ODT 24
QDRIIA_DOFF_n 24
QDRIIA_QVLD 24

QDRII+ PORT B

QDRIIB_Q[17..0] 17,25
QDRIIB_D[17..0] 17,25
QDRIIB_A[21..0] 17,25
QDRIIB_BWS_n[1..0] 25
QDRIIB_WPS_n 25
QDRIIB_RPS_n 25
QDRIIB_K_p 25
QDRIIB_K_n 25
QDRIIB_CQ_p 25
QDRIIB_CQ_n 25
QDRIIB_QVLD 25
QDRIIB_ODT 25
QDRIIB_DOFF_n 25

System MAX-V Interface

M5A10_R_IO[31..0] 6,17

User Interface LED

LED[3..0] 35

FLASH Bus

FLASH_A[26..1] 6,11,28
FLASH_D[31..0] 6,11,28

FLASH control signal

FLASH_CLK 6,28
FLASH_RESET_n 6,28
FLASH_OE_n 6,28
FLASH_WE_n 6,28
FLASH_ADV_n 6,28
FLASH_CE_n[1..0] 6,28
FLASH_RDY_BSY_n[1..0] 6,11,28

U16-31 — ARRIA 10 BANK 3E

VCCIO = 1.8V

FLASH_A16	K11	LVDS3E_1P/DQ44,46	
FLASH_A10	J11	LVDS3E_1N/DQ44,47	
FLASH_A19	F6	LVDS3E_2P/DQ44,44	LVDS3E_14P/DQ46,20
FLASH_A25	F7	LVDS3E_2N/DQ44,45	LVDS3E_14N/DQ46,21
FLASH_ADV_n	H7	LVDS3E_3P/DQ44,42	
FLASH_A18	G7	LVDS3E_3N/DQ44,43	
FLASH_A8	J10	LVDS3E_4P/DQS44/CQ44,40	LVDS3E_16P/DQS46/CQ46,16
FLASH_CE_n0	H10	LVDS3E_4N/DQSN44/CQN44,41	LVDS3E_16N/DQSN46/CQN46,17
FLASH_A14	G9	LVDS3E_5P/DQ44,38	LVDS3E_17P/DQ46,14
FLASH_A13	G8	LVDS3E_5N/DQ44,39	LVDS3E_17N/DQ46,15
FLASH_RDY_BSY_n0	J8	LVDS3E_6P/DQ44,36 DQS22	DQS23 LVDS3E_18P/DQ46,12
FLASH_A11	H8	LVDS3E_6N/DQ44,37 DQSn22	DQSn23 LVDS3E_18N/DQ46,13
QDRIIA_A21	J6	LVDS3E_7P/DQ45,34	LVDS3E_19P/DQ47,10
FLASH_A22	H6	LVDS3E_7N/DQ45,35	LVDS3E_19N/DQ47,11
QDRIIA_A19	L6	LVDS3E_8P/DQ45,32	LVDS3E_20P/DQ47,08
QDRIIA_A20	K6	LVDS3E_8N/DQ45,33	LVDS3E_20N/DQ47,09
QDRIIA_A17	K8	LVDS3E_9P/DQ45,30	LVDS3E_21P/DQ47,06
QDRIIA_A18	J9	LVDS3E_9N/DQ45,31	LVDS3E_21N/DQ47,07
			LVDS3E_22P/DQS47/CQ47,04
			LVDS3E_22N/DQSN47/CQN47,05
RZQ_QDRII_A	L11	RZQ_3E/LVDS3E_11P/DQ45,26	LVDS3E_23P/DQ47,02
QDRIIA_A14	L10	LVDS3E_11N/DQ45,27	LVDS3E_23N/DQ47,03
			LVDS3E_24P/DQ47,00
			LVDS3E_24N/DQ47,01

P10	QDRIIA_A10
P9	QDRIIA_A11
M9	QDRIIA_A6
M8	QDRIIA_A7
P11	QDRIIA_A4
N11	QDRIIA_A5
N10	QDRIIA_A2
M10	QDRIIA_A3
V12	QDRIIA_A0
V13	QDRIIA_A1
U12	FLASH_A24
T12	FLASH_A23
U8	QDRIIA_WPS_n
U9	QDRIIA_RPS_n
T9	FLASH_CLK
R9	QDRIIA_DOFF_n
T11	LED0
R11	LED1
U10	FLASH_WE_n
T10	QDRIIA_ODT

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U16-29 — ARRIA 10 BANK 3G

VCCIO = 1.8V

FLASH_OE_n	C16	LVDS3G_1P/DQ36,46	
FLASH_RESET_n	C17	LVDS3G_1N/DQ36,47	
FLASH_A9	B17	LVDS3G_2P/DQ36,44	LVDS3G_14P/DQ38,20
FLASH_A5	B18	LVDS3G_2N/DQ36,45	LVDS3G_14N/DQ38,21
FLASH_A6	E18	LVDS3G_3P/DQ36,42	
FLASH_A7	D18	LVDS3G_3N/DQ36,43	
FLASH_A15	A16	LVDS3G_4P/DQS36/CQ36,40	LVDS3G_16P/DQS38/CQ38,16
FLASH_A12	A17	LVDS3G_4N/DQSN36/CQN36,41	LVDS3G_16N/DQSN38/CQN38,17
FLASH_A20	A15	LVDS3G_5P/DQ36,38	LVDS3G_17P/DQ38,14
FLASH_A21	A14	LVDS3G_5N/DQ36,39	LVDS3G_17N/DQ38,15
FLASH_A17	B15	LVDS3G_6P/DQ36,36 DQS18	DQS19 LVDS3G_18P/DQ38,12
FLASH_A26	B14	LVDS3G_6N/DQ36,37 DQSn18	DQSn19 LVDS3G_18N/DQ38,13
QDRIIB_A21	K18	LVDS3G_7P/DQ37,34	LVDS3G_19P/DQ39,10
FLASH_A2	J18	LVDS3G_7N/DQ37,35	LVDS3G_19N/DQ39,11
QDRIIB_A19	H17	LVDS3G_8P/DQ37,32	LVDS3G_20P/DQ39,08
QDRIIB_A20	H18	LVDS3G_8N/DQ37,33	LVDS3G_20N/DQ39,09
QDRIIB_A17	L17	LVDS3G_9P/DQ37,30	LVDS3G_21P/DQ39,06
QDRIIB_A18	K17	LVDS3G_9N/DQ37,31	LVDS3G_21N/DQ39,07
			LVDS3G_22P/DQS39/CQ39,04
			LVDS3G_22N/DQSN39/CQN39,05
RZQ_QDRII_B	F17	RZQ_3G/LVDS3G_11P/DQ37,26	LVDS3G_23P/DQ39,02
QDRIIB_A14	E17	LVDS3G_11N/DQ37,27	LVDS3G_23N/DQ39,03
			LVDS3G_24P/DQ39,00
			LVDS3G_24N/DQ39,01

H15	QDRIIB_A10
G15	QDRIIB_A11
D15	QDRIIB_A6
C15	QDRIIB_A7
G14	QDRIIB_A4
F14	QDRIIB_A5
E14	QDRIIB_A2
D14	QDRIIB_A3
L16	QDRIIB_A0
L15	QDRIIB_A1
P15	FLASH_A4
N16	FLASH_CE_n1
K16	QDRIIB_WPS_n
J16	QDRIIB_RPS_n
J15	M5A10_R_IO7
H16	QDRIIB_DOFF_n
N15	LED2
M15	LED3
N17	FLASH_A3
M17	QDRIIB_ODT

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U16-30 — ARRIA 10 BANK 3F

VCCIO = 1.8V

QDRIIA_D11	B12	LVDS3F_1P/DQ40,46	
QDRIIA_BWS_n1	B13	LVDS3F_1N/DQ40,47	
QDRIIA_D14	A11	LVDS3F_2P/DQ40,44	LVDS3F_14P/DQ42,20
QDRIIA_D12	A12	LVDS3F_2N/DQ40,45	LVDS3F_14N/DQ42,21
QDRIIA_D17	B10	LVDS3F_3P/DQ40,42	
QDRIIA_D15	A10	LVDS3F_3N/DQ40,43	
QDRIIA_D10	C12	LVDS3F_4P/DQS40/CQ40,40	LVDS3F_16P/DQS42/CQ42,16
QDRIIA_D9	C13	LVDS3F_4N/DQSN40/CQN40,41	LVDS3F_16N/DQSN42/CQN42,17
QDRIIA_D16	E13	LVDS3F_5P/DQ40,38	LVDS3F_17P/DQ42,14
QDRIIA_D13	D13	LVDS3F_5N/DQ40,39	LVDS3F_17N/DQ42,15
QDRIIA_K_p	F12	LVDS3F_6P/DQ40,36 DQS20	DQS21 LVDS3F_18P/DQ42,12
QDRIIA_K_n	E12	LVDS3F_6N/DQ40,37 DQSn20	DQSn21 LVDS3F_18N/DQ42,13
QDRIIA_D7	C10	LVDS3F_7P/DQ41,34	LVDS3F_19P/DQ43,10
QDRIIA_BWS_n0	C11	LVDS3F_7N/DQ41,35	LVDS3F_19N/DQ43,11
QDRIIA_D3	E11	LVDS3F_8P/DQ41,32	LVDS3F_20P/DQ43,08
QDRIIA_D8	D11	LVDS3F_8N/DQ41,33	LVDS3F_20N/DQ43,09
QDRIIA_D1	E9	LVDS3F_9P/DQ41,30	LVDS3F_21P/DQ43,06
QDRIIA_D0	E8	LVDS3F_9N/DQ41,31	LVDS3F_21N/DQ43,07
			LVDS3F_22P/DQS43/CQ43,04
			LVDS3F_22N/DQSN43/CQN43,05
QDRIIA_D2	D8	RZQ_3F/LVDS3F_11P/DQ41,26	LVDS3F_23P/DQ43,02
QDRIIA_D5	C8	LVDS3F_11N/DQ41,27	LVDS3F_23N/DQ43,03
			LVDS3F_24P/DQ43,00
			LVDS3F_24N/DQ43,01

L14	QDRIIA_Q14
K14	QDRIIA_Q12
H12	QDRIIA_Q9
H11	QDRIIA_Q10
K13	QDRIIA_Q13
J14	QDRIIA_Q11
J13	QDRIIA_CQ_p
H13	QDRIIA_CQ_n
P13	QDRIIA_Q16
N13	QDRIIA_Q15
R12	QDRIIA_Q0
R13	QDRIIA_Q17
N12	QDRIIA_Q2
M12	QDRIIA_Q4
L12	QDRIIA_Q6
K12	QDRIIA_Q7
M14	QDRIIA_Q5
M13	QDRIIA_Q3
T14	QDRIIA_QVLD
R14	QDRIIA_Q1

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VCCIO = 1.8V

QDRIIB_D14	K19	LVDS3H_1P/DQ32,46	
QDRIIB_D15	J19	LVDS3H_1N/DQ32,47	
QDRIIB_D17	M19	LVDS3H_2P/DQ32,44	LVDS3H_14P/DQ34,20
QDRIIB_D12	L19	LVDS3H_2N/DQ32,45	LVDS3H_14N/DQ34,21
QDRIIB_D11	N20	LVDS3H_3P/DQ32,42	
QDRIIB_D16	M20	LVDS3H_3N/DQ32,43	
QDRIIB_D13	L21	LVDS3H_4P/DQS32/CQ32,40	LVDS3H_16P/DQS34/CQ34,16
QDRIIB_D9	L20	LVDS3H_4N/DQSN32/CQN32,41	LVDS3H_16N/DQSN34/CQN34,17
QDRIIB_D10	J20	LVDS3H_5P/DQ32,38	LVDS3H_17P/DQ34,14
QDRIIB_BWS_n1	H20	LVDS3H_5N/DQ32,39	LVDS3H_17N/DQ34,15
QDRIIB_K_p	K21	LVDS3H_6P/DQ32,36 DQS16	DQS17 LVDS3H_18P/DQ34,12
QDRIIB_K_n	J21	LVDS3H_6N/DQ32,37 DQSn16	DQSn17 LVDS3H_18N/DQ34,13
QDRIIB_BWS_n0	G20	LVDS3H_7P/DQ33,34	LVDS3H_19P/DQ35,10
QDRIIB_D0	G19	LVDS3H_7N/DQ33,35	LVDS3H_19N/DQ35,11
QDRIIB_D8	F20	LVDS3H_8P/DQ33,32	LVDS3H_20P/DQ35,08
QDRIIB_D1	F19	LVDS3H_8N/DQ33,33	LVDS3H_20N/DQ35,09
QDRIIB_D4	C18	LVDS3H_9P/DQ33,30	LVDS3H_21P/DQ35,06
QDRIIB_D5	B19	LVDS3H_9N/DQ33,31	LVDS3H_21N/DQ35,07
			LVDS3H_22P/DQS35/CQ35,04
			LVDS3H_22N/DQSN35/CQN35,05
QDRIIB_D7	C20	RZQ_3H/LVDS3H_11P/DQ33,26	LVDS3H_23P/DQ35,02
QDRIIB_D6	B20	LVDS3H_11N/DQ33,27	LVDS3H_23N/DQ35,03
			LVDS3H_24P/DQ35,00
			LVDS3H_24N/DQ35,01

A22	QDRIIB_Q9
A21	QDRIIB_Q13
C22	QDRIIB_Q11
C21	QDRIIB_Q14
B23	QDRIIB_Q12
B22	QDRIIB_Q10
D23	QDRIIB_CQ_p
C23	QDRIIB_CQ_n
G22	QDRIIB_Q17
F22	QDRIIB_Q16
E23	QDRIIB_Q8
E22	QDRIIB_Q15
H22	QDRIIB_Q5
H21	QDRIIB_Q4
L22	QDRIIB_Q0
K22	QDRIIB_QVLD
H23	QDRIIB_Q3
G23	QDRIIB_Q6
K23	QDRIIB_Q1
J23	QDRIIB_Q2

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Title: **DE5a-Net Board**

Size	Document Number	Rev
B	FPGA Bank 3E, 3F, 3G, 3H	C

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PCIe Transceiver

PCIE_TX_p[7..0] 33
PCIE_TX_n[7..0] 33
PCIE_RX_p[7..0] 33
PCIE_RX_n[7..0] 33
PCIE_REFCLK_p 33
PCIE_REFCLK_n 33
OB_PCIE_REFCLK_p 3
OB_PCIE_REFCLK_n 3

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ARRIA 10 Transceiver BANK 1C

	BB40	GXBL1C_RX_CH0P,GXBL1C_REFCLK0P	GXBL1C_TX_CH0P	BD40	
	BB39	GXBL1C_RX_CH0N,GXBL1C_REFCLK0N	GXBL1C_TX_CH0N	BD39	
	AY40	GXBL1C_RX_CH1P,GXBL1C_REFCLK1P	GXBL1C_TX_CH1P	BC42	
	AY39	GXBL1C_RX_CH1N,GXBL1C_REFCLK1N	GXBL1C_TX_CH1N	BC41	
	BA42	GXBL1C_RX_CH2P,GXBL1C_REFCLK2P	GXBL1C_TX_CH2P	BB44	
	BA41	GXBL1C_RX_CH2N,GXBL1C_REFCLK2N	GXBL1C_TX_CH2N	BB43	
	AW42	GXBL1C_RX_CH3P,GXBL1C_REFCLK3P	GXBL1C_TX_CH3P	AY44	
	AW41	GXBL1C_RX_CH3N,GXBL1C_REFCLK3N	GXBL1C_TX_CH3N	AY43	
PCIE_RX_p0	AU42	GXBL1C_RX_CH4P,GXBL1C_REFCLK4P	GXBL1C_TX_CH4P	AV44	PCIE_TX_p0
PCIE_RX_n0	AU41	GXBL1C_RX_CH4N,GXBL1C_REFCLK4N	GXBL1C_TX_CH4N	AV43	PCIE_TX_n0
PCIE_RX_p1	AR42	GXBL1C_RX_CH5P,GXBL1C_REFCLK5P	GXBL1C_TX_CH5P	AT44	PCIE_TX_p1
PCIE_RX_n1	AR41	GXBL1C_RX_CH5N,GXBL1C_REFCLK5N	GXBL1C_TX_CH5N	AT43	PCIE_TX_n1
PCIE_REFCLK_p	AH40	REFCLK_GXBL1C_CHTP			
PCIE_REFCLK_n	AH39	REFCLK_GXBL1C_CHTN			
OB_PCIE_REFCLK_p	AK40	REFCLK_GXBL1C_CHBP			
OB_PCIE_REFCLK_n	AK39	REFCLK_GXBL1C_CHBN			

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ARRIA 10 Transceiver BANK 1E

	AA42	GXBL1E_RX_CH0P,GXBL1E_REFCLK0P	GXBL1E_TX_CH0P	AB44	
	AA41	GXBL1E_RX_CH0N,GXBL1E_REFCLK0N	GXBL1E_TX_CH0N	AB43	
	W42	GXBL1E_RX_CH1P,GXBL1E_REFCLK1P	GXBL1E_TX_CH1P	Y44	
	W41	GXBL1E_RX_CH1N,GXBL1E_REFCLK1N	GXBL1E_TX_CH1N	Y43	
	U42	GXBL1E_RX_CH2P,GXBL1E_REFCLK2P	GXBL1E_TX_CH2P	V44	
	U41	GXBL1E_RX_CH2N,GXBL1E_REFCLK2N	GXBL1E_TX_CH2N	V43	
	R42	GXBL1E_RX_CH3P,GXBL1E_REFCLK3P	GXBL1E_TX_CH3P	T44	
	R41	GXBL1E_RX_CH3N,GXBL1E_REFCLK3N	GXBL1E_TX_CH3N	T43	
	N42	GXBL1E_RX_CH4P,GXBL1E_REFCLK4P	GXBL1E_TX_CH4P	P44	
	N41	GXBL1E_RX_CH4N,GXBL1E_REFCLK4N	GXBL1E_TX_CH4N	P43	
	L42	GXBL1E_RX_CH5P,GXBL1E_REFCLK5P	GXBL1E_TX_CH5P	M44	
	L41	GXBL1E_RX_CH5N,GXBL1E_REFCLK5N	GXBL1E_TX_CH5N	M43	
	Y40	REFCLK_GXBL1E_CHTP			
	Y39	REFCLK_GXBL1E_CHTN			
	AB40	REFCLK_GXBL1E_CHBP			
R253 10K	AB39	REFCLK_GXBL1E_CHBN			

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ARRIA 10 Transceiver BANK 1D

PCIE_RX_p2	AN42	GXBL1D_RX_CH0P,GXBL1D_REFCLK0P	GXBL1D_TX_CH0P	AP44	PCIE_TX_p2
PCIE_RX_n2	AN41	GXBL1D_RX_CH0N,GXBL1D_REFCLK0N	GXBL1D_TX_CH0N	AP43	PCIE_TX_n2
PCIE_RX_p3	AL42	GXBL1D_RX_CH1P,GXBL1D_REFCLK1P	GXBL1D_TX_CH1P	AM44	PCIE_TX_p3
PCIE_RX_n3	AL41	GXBL1D_RX_CH1N,GXBL1D_REFCLK1N	GXBL1D_TX_CH1N	AM43	PCIE_TX_n3
PCIE_RX_p4	AJ42	GXBL1D_RX_CH2P,GXBL1D_REFCLK2P	GXBL1D_TX_CH2P	AK44	PCIE_TX_p4
PCIE_RX_n4	AJ41	GXBL1D_RX_CH2N,GXBL1D_REFCLK2N	GXBL1D_TX_CH2N	AK43	PCIE_TX_n4
PCIE_RX_p5	AG42	GXBL1D_RX_CH3P,GXBL1D_REFCLK3P	GXBL1D_TX_CH3P	AH44	PCIE_TX_p5
PCIE_RX_n5	AG41	GXBL1D_RX_CH3N,GXBL1D_REFCLK3N	GXBL1D_TX_CH3N	AH43	PCIE_TX_n5
PCIE_RX_p6	AE42	GXBL1D_RX_CH4P,GXBL1D_REFCLK4P	GXBL1D_TX_CH4P	AF44	PCIE_TX_p6
PCIE_RX_n6	AE41	GXBL1D_RX_CH4N,GXBL1D_REFCLK4N	GXBL1D_TX_CH4N	AF43	PCIE_TX_n6
PCIE_RX_p7	AC42	GXBL1D_RX_CH5P,GXBL1D_REFCLK5P	GXBL1D_TX_CH5P	AD44	PCIE_TX_p7
PCIE_RX_n7	AC41	GXBL1D_RX_CH5N,GXBL1D_REFCLK5N	GXBL1D_TX_CH5N	AD43	PCIE_TX_n7
	AD40	REFCLK_GXBL1D_CHTP			
R254 10K	AD39	REFCLK_GXBL1D_CHTN			
	AF40	REFCLK_GXBL1D_CHBP			
R260 10K	AF39	REFCLK_GXBL1D_CHBN			

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ARRIA 10 Transceiver BANK 1F

	J42	GXBL1F_RX_CH0P,GXBL1F_REFCLK0P	GXBL1F_TX_CH0P	K44	
	J41	GXBL1F_RX_CH0N,GXBL1F_REFCLK0N	GXBL1F_TX_CH0N	K43	
	G42	GXBL1F_RX_CH1P,GXBL1F_REFCLK1P	GXBL1F_TX_CH1P	H44	
	G41	GXBL1F_RX_CH1N,GXBL1F_REFCLK1N	GXBL1F_TX_CH1N	H43	
	E42	GXBL1F_RX_CH2P,GXBL1F_REFCLK2P	GXBL1F_TX_CH2P	F44	
	E41	GXBL1F_RX_CH2N,GXBL1F_REFCLK2N	GXBL1F_TX_CH2N	F43	
	D40	GXBL1F_RX_CH3P,GXBL1F_REFCLK3P	GXBL1F_TX_CH3P	D44	
	D39	GXBL1F_RX_CH3N,GXBL1F_REFCLK3N	GXBL1F_TX_CH3N	D43	
	C42	GXBL1F_RX_CH4P,GXBL1F_REFCLK4P	GXBL1F_TX_CH4P	B44	
	C41	GXBL1F_RX_CH4N,GXBL1F_REFCLK4N	GXBL1F_TX_CH4N	B43	
	B40	GXBL1F_RX_CH5P,GXBL1F_REFCLK5P	GXBL1F_TX_CH5P	A42	
	B39	GXBL1F_RX_CH5N,GXBL1F_REFCLK5N	GXBL1F_TX_CH5N	A41	
	T40	REFCLK_GXBL1F_CHTP			
R240 10K	T39	REFCLK_GXBL1F_CHTN			
	V40	REFCLK_GXBL1F_CHBP			
R241 10K	V39	REFCLK_GXBL1F_CHBN			

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Title: **DE5a-Net Board**

Size	Document Number	Rev
B	FPGA GXB 1C, 1D, 1E, 1F	C

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QSFP Transceivers

QSFPA_TX_P[3:0]_29
QSFPA_TX_N[3:0]_29
QSFPA_RX_P[3:0]_29
QSFPA_RX_N[3:0]_29
QSFPA_REFCLK_p_4
QSFPA_REFCLK_n_4

QSFP Port B Transceivers

QSFPB_TX_P[3:0]_30
QSFPB_TX_N[3:0]_30
QSFPB_RX_P[3:0]_30
QSFPB_RX_N[3:0]_30
QSFPB_REFCLK_p_4
QSFPB_REFCLK_n_4

QSFP Port C Transceivers

QSFPC_TX_P[3:0]_31
QSFPC_TX_N[3:0]_31
QSFPC_RX_P[3:0]_31
QSFPC_RX_N[3:0]_31
QSFPC_REFCLK_p_4
QSFPC_REFCLK_n_4

QSFP Port D Transceivers

QSFPD_TX_P[3:0]_32
QSFPD_TX_N[3:0]_32
QSFPD_RX_P[3:0]_32
QSFPD_RX_N[3:0]_32
QSFPD_REFCLK_p_4
QSFPD_REFCLK_n_4

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ARRIA 10 Transceiver BANK 4F

QSFPD_RX_P0	J3	GXBR4F_RX_CH0P,GXBR4F_REFCLK0P	GXBR4F_TX_CH0P	K1	QSFPD_TX_P0
QSFPD_RX_N0	J4	GXBR4F_RX_CH0N,GXBR4F_REFCLK0N	GXBR4F_TX_CH0N	K2	QSFPD_TX_N0
QSFPD_RX_P1	G3	GXBR4F_RX_CH1P,GXBR4F_REFCLK1P	GXBR4F_TX_CH1P	H1	QSFPD_TX_P1
QSFPD_RX_N1	G4	GXBR4F_RX_CH1N,GXBR4F_REFCLK1N	GXBR4F_TX_CH1N	H2	QSFPD_TX_N1
QSFPD_RX_P2	E3	GXBR4F_RX_CH2P,GXBR4F_REFCLK2P	GXBR4F_TX_CH2P	F1	QSFPD_TX_P2
QSFPD_RX_N2	E4	GXBR4F_RX_CH2N,GXBR4F_REFCLK2N	GXBR4F_TX_CH2N	F2	QSFPD_TX_N2
QSFPD_RX_P3	D5	GXBR4F_RX_CH3P,GXBR4F_REFCLK3P	GXBR4F_TX_CH3P	D1	QSFPD_TX_P3
QSFPD_RX_N3	D6	GXBR4F_RX_CH3N,GXBR4F_REFCLK3N	GXBR4F_TX_CH3N	D2	QSFPD_TX_N3
	C3	GXBR4F_RX_CH4P,GXBR4F_REFCLK4P	GXBR4F_TX_CH4P	B1	
	C4	GXBR4F_RX_CH4N,GXBR4F_REFCLK4N	GXBR4F_TX_CH4N	B2	
	B5	GXBR4F_RX_CH5P,GXBR4F_REFCLK5P	GXBR4F_TX_CH5P	A3	
	B6	GXBR4F_RX_CH5N,GXBR4F_REFCLK5N	GXBR4F_TX_CH5N	A4	
QSFPD_REFCLK_p	T5	REFCLK_GXBR4F_CHTP			
QSFPD_REFCLK_n	T6	REFCLK_GXBR4F_CHTN			
R242 10K	V5	REFCLK_GXBR4F_CHBP			
	V6	REFCLK_GXBR4F_CHBN			

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ARRIA 10 Transceiver BANK 4D

QSFPB_RX_P0	AN3	GXBR4D_RX_CH0P,GXBR4D_REFCLK0P	GXBR4D_TX_CH0P	AP1	QSFPB_TX_P0
QSFPB_RX_N0	AN4	GXBR4D_RX_CH0N,GXBR4D_REFCLK0N	GXBR4D_TX_CH0N	AP2	QSFPB_TX_N0
QSFPB_RX_P1	AL3	GXBR4D_RX_CH1P,GXBR4D_REFCLK1P	GXBR4D_TX_CH1P	AM1	QSFPB_TX_P1
QSFPB_RX_N1	AL4	GXBR4D_RX_CH1N,GXBR4D_REFCLK1N	GXBR4D_TX_CH1N	AM2	QSFPB_TX_N1
QSFPB_RX_P2	AJ3	GXBR4D_RX_CH2P,GXBR4D_REFCLK2P	GXBR4D_TX_CH2P	AK1	QSFPB_TX_P2
QSFPB_RX_N2	AJ4	GXBR4D_RX_CH2N,GXBR4D_REFCLK2N	GXBR4D_TX_CH2N	AK2	QSFPB_TX_N2
QSFPB_RX_P3	AG3	GXBR4D_RX_CH3P,GXBR4D_REFCLK3P	GXBR4D_TX_CH3P	AH1	QSFPB_TX_P3
QSFPB_RX_N3	AG4	GXBR4D_RX_CH3N,GXBR4D_REFCLK3N	GXBR4D_TX_CH3N	AH2	QSFPB_TX_N3
	AE3	GXBR4D_RX_CH4P,GXBR4D_REFCLK4P	GXBR4D_TX_CH4P	AF1	
	AE4	GXBR4D_RX_CH4N,GXBR4D_REFCLK4N	GXBR4D_TX_CH4N	AF2	
	AC3	GXBR4D_RX_CH5P,GXBR4D_REFCLK5P	GXBR4D_TX_CH5P	AD1	
	AC4	GXBR4D_RX_CH5N,GXBR4D_REFCLK5N	GXBR4D_TX_CH5N	AD2	
QSFPB_REFCLK_p	AD5	REFCLK_GXBR4D_CHTP			
QSFPB_REFCLK_n	AD6	REFCLK_GXBR4D_CHTN			
R262 10K	AF5	REFCLK_GXBR4D_CHBP			
	AF6	REFCLK_GXBR4D_CHBN			

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ARRIA 10 Transceiver BANK 4E

QSFPC_RX_P0	AA3	GXBR4E_RX_CH0P,GXBR4E_REFCLK0P	GXBR4E_TX_CH0P	AB1	QSFPC_TX_P0
QSFPC_RX_N0	AA4	GXBR4E_RX_CH0N,GXBR4E_REFCLK0N	GXBR4E_TX_CH0N	AB2	QSFPC_TX_N0
QSFPC_RX_P1	W3	GXBR4E_RX_CH1P,GXBR4E_REFCLK1P	GXBR4E_TX_CH1P	Y1	QSFPC_TX_P1
QSFPC_RX_N1	W4	GXBR4E_RX_CH1N,GXBR4E_REFCLK1N	GXBR4E_TX_CH1N	Y2	QSFPC_TX_N1
QSFPC_RX_P2	U3	GXBR4E_RX_CH2P,GXBR4E_REFCLK2P	GXBR4E_TX_CH2P	V1	QSFPC_TX_P2
QSFPC_RX_N2	U4	GXBR4E_RX_CH2N,GXBR4E_REFCLK2N	GXBR4E_TX_CH2N	V2	QSFPC_TX_N2
QSFPC_RX_P3	R3	GXBR4E_RX_CH3P,GXBR4E_REFCLK3P	GXBR4E_TX_CH3P	T1	QSFPC_TX_P3
QSFPC_RX_N3	R4	GXBR4E_RX_CH3N,GXBR4E_REFCLK3N	GXBR4E_TX_CH3N	T2	QSFPC_TX_N3
	N3	GXBR4E_RX_CH4P,GXBR4E_REFCLK4P	GXBR4E_TX_CH4P	P1	
	N4	GXBR4E_RX_CH4N,GXBR4E_REFCLK4N	GXBR4E_TX_CH4N	P2	
	L3	GXBR4E_RX_CH5P,GXBR4E_REFCLK5P	GXBR4E_TX_CH5P	M1	
	L4	GXBR4E_RX_CH5N,GXBR4E_REFCLK5N	GXBR4E_TX_CH5N	M2	
QSFPC_REFCLK_p	Y5	REFCLK_GXBR4E_CHTP			
QSFPC_REFCLK_n	Y6	REFCLK_GXBR4E_CHTN			
R255 10K	AB5	REFCLK_GXBR4E_CHBP			
	AB6	REFCLK_GXBR4E_CHBN			

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ARRIA 10 Transceiver BANK 4C

QSFPA_RX_P0	BB5	GXBR4C_RX_CH0P,GXBR4C_REFCLK0P	GXBR4C_TX_CH0P	BD5	QSFPA_TX_P0
QSFPA_RX_N0	BB6	GXBR4C_RX_CH0N,GXBR4C_REFCLK0N	GXBR4C_TX_CH0N	BD6	QSFPA_TX_N0
QSFPA_RX_P1	AY5	GXBR4C_RX_CH1P,GXBR4C_REFCLK1P	GXBR4C_TX_CH1P	BC3	QSFPA_TX_P1
QSFPA_RX_N1	AY6	GXBR4C_RX_CH1N,GXBR4C_REFCLK1N	GXBR4C_TX_CH1N	BC4	QSFPA_TX_N1
QSFPA_RX_P2	BA3	GXBR4C_RX_CH2P,GXBR4C_REFCLK2P	GXBR4C_TX_CH2P	BB1	QSFPA_TX_P2
QSFPA_RX_N2	BA4	GXBR4C_RX_CH2N,GXBR4C_REFCLK2N	GXBR4C_TX_CH2N	BB2	QSFPA_TX_N2
QSFPA_RX_P3	AW3	GXBR4C_RX_CH3P,GXBR4C_REFCLK3P	GXBR4C_TX_CH3P	AY1	QSFPA_TX_P3
QSFPA_RX_N3	AW4	GXBR4C_RX_CH3N,GXBR4C_REFCLK3N	GXBR4C_TX_CH3N	AY2	QSFPA_TX_N3
	AU3	GXBR4C_RX_CH4P,GXBR4C_REFCLK4P	GXBR4C_TX_CH4P	AV1	
	AU4	GXBR4C_RX_CH4N,GXBR4C_REFCLK4N	GXBR4C_TX_CH4N	AV2	
	AR3	GXBR4C_RX_CH5P,GXBR4C_REFCLK5P	GXBR4C_TX_CH5P	AT1	
	AR4	GXBR4C_RX_CH5N,GXBR4C_REFCLK5N	GXBR4C_TX_CH5N	AT2	
QSFPA_REFCLK_p	AH5	REFCLK_GXBR4C_CHTP			
QSFPA_REFCLK_n	AH6	REFCLK_GXBR4C_CHTN			
R263 10K	AK5	REFCLK_GXBR4C_CHBP			
	AK6	REFCLK_GXBR4C_CHBN			

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Title
DE5a-Net Board

Size	Document Number	Rev
B	FPGA GXB 4C, 4D, 4E, 4F	C

Date: Thursday, May 26, 2016 Sheet 15 of 42

DDR3 SO-DIMM A

DDR3A_CK[1..0] 10,22
DDR3A_CK_n[1..0] 10,22
DDR3A_BA[2..0] 10,22
DDR3A_ODT[1..0] 10,22
DDR3A_CS_n[1..0] 10,22

DDR3A_DQ[63..0] 10,22
DDR3A_DQS[7..0] 10,22
DDR3A_DQS_n[7..0] 10,22

DDR3A_A[15..0] 10,22
DDR3A_DM[7..0] 10,22
DDR3A_CKE[1..0] 10,22

DDR3A_WE_n 10,22
DDR3A_CAS_n 10,22
DDR3A_RAS_n 10,22
DDR3A_RESET_n 10,22

DDR3A_SDA 9,10
DDR3A_SCL 9,10
DDR3A_EVENT_n 9,10

DDR3A_REFCLK_p 3
DDR3A_REFCLK_n 3

QDRII+ PORT C

QDRIIC_A[21..0] 11,26
QDRIIC_Q[17..0] 11,26
QDRIIC_D[17..0] 11,26
QDRIIC_BWS_n[1..0] 11,26

QDRII+ PORT D

QDRIID_A[21..0] 11,27
QDRIID_Q[17..0] 11,27
QDRIID_D[17..0] 11,27

Clock Input

QDRIIC_REFCLK_p 3
QDRIIC_REFCLK_n 3
QDRIID_REFCLK_p 3
QDRIID_REFCLK_n 3
CLK_50_B2J 5
CLK_50_B2L 5

SMA Clock

SMA_CLKIN 5
SMA_CLKOUT 5

Si5340 Interface

Si5340B_I2C_SDA 3
Si5340B_I2C_SCL 3
Si5340B_RST_n 3
Si5340B_INTR 3

TI TPS40422 Interface

TPS40422_ALERT 38

U16-2

ARRIA 10 Clock Bank 2

Bank 2F VCCIO = 1.5V

DDR3A_DQ45	AY31	CLK_2F_0P/LVDS2F_13P/DQ26,22	PLL_2F_CLKOUT0P,PLL_2F_CLKOUT0,PLL_2F_FB0/LVDS2F_15P/DQ26,18
DDR3A_DM5	BA31	CLK_2F_0N/LVDS2F_13N/DQ26,23	PLL_2F_CLKOUT0N/LVDS2F_15N/DQ26,19
DDR3A_DQ56	AT27	CLK_2F_1P/LVDS2F_12P/DQ25,24	PLL_2F_CLKOUT1P,PLL_2F_CLKOUT1,PLL_2F_FB1/LVDS2F_10P/DQS25/CQ25,28
DDR3A_DQ57	AU27	CLK_2F_1N/LVDS2F_12N/DQ25,25	PLL_2F_CLKOUT1N/LVDS2F_10N/DQSN25/CQN25,29

AW28	DDR3A_DQ47
AW29	DDR3A_DQ46
AV30	DDR3A_DQS7
AW30	DDR3A_DQS_n7

Bank 2G VCCIO = 1.5V

DDR3A_A10	AW35	CLK_2G_0P/LVDS2G_13P/DQ22,22	PLL_2G_CLKOUT0P,PLL_2G_CLKOUT0,PLL_2G_FB0/LVDS2G_15P/DQ22,18
DDR3A_A11	AW36	CLK_2G_0N/LVDS2G_13N/DQ22,23	PLL_2G_CLKOUT0N/LVDS2G_15N/DQ22,19
R281 100 DDR3A_REFCLK_p	AV33	CLK_2G_1P/LVDS2G_12P/DQ21,24	PLL_2G_CLKOUT1P,PLL_2G_CLKOUT1,PLL_2G_FB1/LVDS2G_10P/DQS21/CQ21,28
DDR3A_REFCLK_n	AW33	CLK_2G_1N/LVDS2G_12N/DQ21,25	PLL_2G_CLKOUT1N/LVDS2G_10N/DQSN21/CQN21,29

AY36	DDR3A_A6
AY37	DDR3A_A7
AT31	DDR3A_A13
AT32	DDR3A_A14

Bank 2H VCCIO = 1.5V

DDR3A_DQ9	AP34	CLK_2H_0P/LVDS2H_13P/DQ18,22	PLL_2H_CLKOUT0P,PLL_2H_CLKOUT0,PLL_2H_FB0/LVDS2H_15P/DQ18,18
DDR3A_DM1	AP35	CLK_2H_0N/LVDS2H_13N/DQ18,23	PLL_2H_CLKOUT0N/LVDS2H_15N/DQ18,19
DDR3A_DQ30	AR37	CLK_2H_1P/LVDS2H_12P/DQ17,24	PLL_2H_CLKOUT1P,PLL_2H_CLKOUT1,PLL_2H_FB1/LVDS2H_10P/DQS17/CQ17,28
DDR3A_DQ24	AR36	CLK_2H_1N/LVDS2H_12N/DQ17,25	PLL_2H_CLKOUT1N/LVDS2H_10N/DQSN17/CQN17,29

AM35	DDR3A_DQ10
AN35	DDR3A_DQ8
AP38	DDR3A_DQS3
AR38	DDR3A_DQS_n3

Bank 2I VCCIO = 1.8V

QDRIIC_A12	C30	CLK_2I_0P/LVDS2I_13P/DQ14,22	PLL_2I_CLKOUT0P,PLL_2I_CLKOUT0,PLL_2I_FB0/LVDS2I_15P/DQ14,18
QDRIIC_A13	C31	CLK_2I_0N/LVDS2I_13N/DQ14,23	PLL_2I_CLKOUT0N/LVDS2I_15N/DQ14,19
R215 100 QDRIIC_REFCLK_p	G24	CLK_2I_1P/LVDS2I_12P/DQ13,24	PLL_2I_CLKOUT1P,PLL_2I_CLKOUT1,PLL_2I_FB1/LVDS2I_10P/DQS13/CQ13,28
QDRIIC_REFCLK_n	F24	CLK_2I_1N/LVDS2I_12N/DQ13,25	PLL_2I_CLKOUT1N/LVDS2I_10N/DQSN13/CQN13,29

C27	QDRIIC_A8
C28	QDRIIC_A9
K24	QDRIIC_A15
J24	QDRIIC_A16

Bank 2J VCCIO = 1.8V

CLK_50_B2J	W36	CLK_2J_0P/LVDS2J_13P/DQ10,22 DQ5	PLL_2J_CLKOUT0P,PLL_2J_CLKOUT0,PLL_2J_FB0/LVDS2J_15P/DQ10,18
TPS40422_ALERT	V36	CLK_2J_0N/LVDS2J_13N/DQ10,23 DQ5	PLL_2J_CLKOUT0N/LVDS2J_15N/DQ10,19
SMA_CLKIN	AC32	CLK_2J_1P/LVDS2J_12P/DQ9,24 DQ4	PLL_2J_CLKOUT1P,PLL_2J_CLKOUT1,PLL_2J_FB1/LVDS2J_10P/DQS9/CQ9,28
	AC31	CLK_2J_1N/LVDS2J_12N/DQ9,25 DQ4	PLL_2J_CLKOUT1N/LVDS2J_10N/DQSN9/CQN9,29

AA36	SMA_CLKOUT
Y36	QDRIIC_Q9
AA35	QDRIIC_D8
AB35	QDRIIC_BWS_n0

Bank 2K VCCIO = 1.8V

QDRIID_A12	T31	CLK_2K_0P/LVDS2K_13P/DQ6,22 DQ3	PLL_2K_CLKOUT0P,PLL_2K_CLKOUT0,PLL_2K_FB0/LVDS2K_15P/DQ6,18
QDRIID_A13	R31	CLK_2K_0N/LVDS2K_13N/DQ6,23 DQ3	PLL_2K_CLKOUT0N/LVDS2K_15N/DQ6,19
R225 100 QDRIID_REFCLK_p	M34	CLK_2K_1P/LVDS2K_12P/DQ5,24 DQ2	PLL_2K_CLKOUT1P,PLL_2K_CLKOUT1,PLL_2K_FB1/LVDS2K_10P/DQS5/CQ5,28
QDRIID_REFCLK_n	L34	CLK_2K_1N/LVDS2K_12N/DQ5,25 DQ2	PLL_2K_CLKOUT1N/LVDS2K_10N/DQSN5/CQN5,29

T32	QDRIID_A8
R32	QDRIID_A9
L37	QDRIID_A15
K36	QDRIID_A16

Bank 2L VCCIO = 1.8V

CLK_50_B2L	H32	CLK_2L_0P/LVDS2L_13P/DQ2,22 DQ1	PLL_2L_CLKOUT0P,PLL_2L_CLKOUT0,PLL_2L_FB0/LVDS2L_15P/DQ2,18
Si5340B_I2C_SDA	H31	CLK_2L_0N/LVDS2L_13N/DQ2,23 DQ1	PLL_2L_CLKOUT0N/LVDS2L_15N/DQ2,19
Si5340B_I2C_SCL	G37	CLK_2L_1P/LVDS2L_12P/DQ1,24 DQ0	PLL_2L_CLKOUT1P,PLL_2L_CLKOUT1,PLL_2L_FB1/LVDS2L_10P/DQS1/CQ1,28
Si5340B_RST_n	G38	CLK_2L_1N/LVDS2L_12N/DQ1,25 DQ0	PLL_2L_CLKOUT1N/LVDS2L_10N/DQSN1/CQN1,29

H33	QDRIID_Q8
G32	Si5340B_INTR
F36	QDRIID_D3
E36	QDRIID_D0

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Title: **DE5a-Net Board**

Size	Document Number	Rev
B	FPGA Clock Bank 2	C

Date: Thursday, May 26, 2016 Sheet 16 of 42

DDR3 SO-DIMM B

DDR3B_CK[1..0] 12,23
DDR3B_CK_n[1..0] 12,23
DDR3B_BA[2..0] 12,23
DDR3B_ODT[1..0] 12,23
DDR3B_CS_n[1..0] 12,23

DDR3B_DQ[63..0] 12,23
DDR3B_DQS[7..0] 12,23
DDR3B_DQS_n[7..0] 12,23

DDR3B_A[15..0] 12,23
DDR3B_DM[7..0] 12,23
DDR3B_CKE[1..0] 12,23

DDR3B_WE_n 12,23
DDR3B_CAS_n 12,23
DDR3B_RAS_n 12,23
DDR3B_RESET_n 12,23

DDR3B_SDA 9,12
DDR3B_SCL 9,12
DDR3B_EVENT_n 9,12

DDR3B_REFCLK_p 3
DDR3B_REFCLK_n 3

QDRII+ PORT A

QDRIIA_A[21..0] 13,24
QDRIIA_Q[17..0] 13,24
QDRIIA_D[17..0] 13,24

QDRII+ PORT B

QDRIIB_A[21..0] 13,25
QDRIIB_Q[17..0] 13,25
QDRIIB_D[17..0] 13,25

Clock Input

QDRIIA_REFCLK_p 3
QDRIIA_REFCLK_n 3

QDRIIB_REFCLK_p 3
QDRIIB_REFCLK_n 3

CLK_50_B3D 5

CLK_50_B3F 5

CLK_50_B3H 5

CLK_100_B3D 5

RS-422 LED

RJ45_LED_L 35
RJ45_LED_R 35

System MAX-V Interface

M5A10_R_IO[31..0] 6,13

M5A10_R_CLK 6

Si5344 Interface

Si5340A_I2C_SDA 4
Si5340A_I2C_SCL 4
Si5340A_RST_n 4
Si5340A_INTR 4

U16-3

ARRIA 10 Clock Bank 3

Bank 3A VCCIO = 1.5V

DDR3B_DQ12	AW18	CLK_3A_0P/LVDS3A_13P/DQ62,22	PLL_3A_CLKOUT0P,PLL_3A_CLKOUT0,PLL_3A_FB0/LVDS3A_15P/DQ62,18	AY17	DDR3B_DQ8
DDR3B_DM1	AY18	CLK_3A_0N/LVDS3A_13N/DQ62,23	PLL_3A_CLKOUT0N/LVDS3A_15N/DQ62,19	BA17	DDR3B_DQ9
DDR3B_DQ23	BB18	CLK_3A_1P/LVDS3A_12P/DQ61,24	PLL_3A_CLKOUT1P,PLL_3A_CLKOUT1,PLL_3A_FB1/LVDS3A_10P/DQS61/CQ61,28	BD13	DDR3B_DQS2
DDR3B_DQ16	BB17	CLK_3A_1N/LVDS3A_12N/DQ61,25	PLL_3A_CLKOUT1N/LVDS3A_10N/DQSN61/CQN61,29	BD14	DDR3B_DQS_n2

Bank 3B VCCIO = 1.5V

R272 100

DDR3B_A10	AY11	CLK_3B_0P/LVDS3B_13P/DQ58,22	PLL_3B_CLKOUT0P,PLL_3B_CLKOUT0,PLL_3B_FB0/LVDS3B_15P/DQ58,18	BA12	DDR3B_A6
DDR3B_A11	BA11	CLK_3B_0N/LVDS3B_13N/DQ58,23	PLL_3B_CLKOUT0N/LVDS3B_15N/DQ58,19	BB12	DDR3B_A7
DDR3B_REFCLK_p	AP14	CLK_3B_1P/LVDS3B_12P/DQ57,24	PLL_3B_CLKOUT1P,PLL_3B_CLKOUT1,PLL_3B_FB1/LVDS3B_10P/DQS57/CQ57,28	AM13	DDR3B_A13
DDR3B_REFCLK_n	AR14	CLK_3B_1N/LVDS3B_12N/DQ57,25	PLL_3B_CLKOUT1N/LVDS3B_10N/DQSN57/CQN57,29	AN13	DDR3B_A14

Bank 3C VCCIO = 1.5V

DDR3B_DQ40	AK12	CLK_3C_0P/LVDS3C_13P/DQ54,22	PLL_3C_CLKOUT0P,PLL_3C_CLKOUT0,PLL_3C_FB0/LVDS3C_15P/DQ54,18	AM12	DDR3B_DQ44
DDR3B_DM5	AL12	CLK_3C_0N/LVDS3C_13N/DQ54,23	PLL_3C_CLKOUT0N/LVDS3C_15N/DQ54,19	AN12	DDR3B_DQ45
DDR3B_DQ37	AT7	CLK_3C_1P/LVDS3C_12P/DQ53,24	PLL_3C_CLKOUT1P,PLL_3C_CLKOUT1,PLL_3C_FB1/LVDS3C_10P/DQS53/CQ53,28	AV7	DDR3B_DQS4
DDR3B_DQ35	AT6	CLK_3C_1N/LVDS3C_12N/DQ53,25	PLL_3C_CLKOUT1N/LVDS3C_10N/DQSN53/CQN53,29	AV6	DDR3B_DQS_n4

Bank 3D VCCIO = 1.8V

CLK_50_B3D	AN7	CLK_3D_0P/LVDS3D_13P/DQ50,22	PLL_3D_CLKOUT0P,PLL_3D_CLKOUT0,PLL_3D_FB0/LVDS3D_15P/DQ50,18	AN6	Si5340A_RST_n
Si5340A_I2C_SDA	AN8	CLK_3D_0N/LVDS3D_13N/DQ50,23	PLL_3D_CLKOUT0N/LVDS3D_15N/DQ50,19	AM6	Si5340A_INTR
Si5340A_I2C_SCL	AJ11	CLK_3D_1P/LVDS3D_12P/DQ49,24	PLL_3D_CLKOUT1P,PLL_3D_CLKOUT1,PLL_3D_FB1/LVDS3D_10P/DQS49/CQ49,28	AE11	RJ45_LED_L
CLK_100_B3D	AH11	CLK_3D_1N/LVDS3D_12N/DQ49,25	PLL_3D_CLKOUT1N/LVDS3D_10N/DQSN49/CQN49,29	AF11	RJ45_LED_R

Bank 3E VCCIO = 1.8V

R231 100

QDRIIA_A12	N6	CLK_3E_0P/LVDS3E_13P/DQ46,22	PLL_3E_CLKOUT0P,PLL_3E_CLKOUT0,PLL_3E_FB0/LVDS3E_15P/DQ46,18	N7	QDRIIA_A8
QDRIIA_A13	M7	CLK_3E_0N/LVDS3E_13N/DQ46,23	PLL_3E_CLKOUT0N/LVDS3E_15N/DQ46,19	N8	QDRIIA_A9
QDRIIA_REFCLK_p	L9	CLK_3E_1P/LVDS3E_12P/DQ45,24	PLL_3E_CLKOUT1P,PLL_3E_CLKOUT1,PLL_3E_FB1/LVDS3E_10P/DQS45/CQ45,28	L7	QDRIIA_A15
QDRIIA_REFCLK_n	K9	CLK_3E_1N/LVDS3E_12N/DQ45,25	PLL_3E_CLKOUT1N/LVDS3E_10N/DQSN45/CQN45,29	K7	QDRIIA_A16

Bank 3F VCCIO = 1.8V

CLK_50_B3F	G12	CLK_3F_0P/LVDS3F_13P/DQ42,22	DQ21	PLL_3F_CLKOUT0P,PLL_3F_CLKOUT0,PLL_3F_FB0/LVDS3F_15P/DQ42,18	G10	QDRIIA_Q8
M5A10_R_IO0	G13	CLK_3F_0N/LVDS3F_13N/DQ42,23	DQ21	PLL_3F_CLKOUT0N/LVDS3F_15N/DQ42,19	F11	M5A10_R_IO3
M5A10_R_IO1	F10	CLK_3F_1P/LVDS3F_12P/DQ41,24	DQ20	PLL_3F_CLKOUT1P,PLL_3F_CLKOUT1,PLL_3F_FB1/LVDS3F_10P/DQS41/CQ41,28	D9	QDRIIA_D4
M5A10_R_IO2	F9	CLK_3F_1N/LVDS3F_12N/DQ41,25	DQ20	PLL_3F_CLKOUT1N/LVDS3F_10N/DQSN41/CQN41,29	D10	QDRIIA_D6

Bank 3G VCCIO = 1.8V

R229 100

QDRIIB_A12	E16	CLK_3G_0P/LVDS3G_13P/DQ38,22	DQ19	PLL_3G_CLKOUT0P,PLL_3G_CLKOUT0,PLL_3G_FB0/LVDS3G_15P/DQ38,18	F15	QDRIIB_A8
QDRIIB_A13	D16	CLK_3G_0N/LVDS3G_13N/DQ38,23	DQ19	PLL_3G_CLKOUT0N/LVDS3G_15N/DQ38,19	F16	QDRIIB_A9
QDRIIB_REFCLK_p	N18	CLK_3G_1P/LVDS3G_12P/DQ37,24	DQ18	PLL_3G_CLKOUT1P,PLL_3G_CLKOUT1,PLL_3G_FB1/LVDS3G_10P/DQS37/CQ37,28	G17	QDRIIB_A15
QDRIIB_REFCLK_n	M18	CLK_3G_1N/LVDS3G_12N/DQ37,25	DQ18	PLL_3G_CLKOUT1N/LVDS3G_10N/DQSN37/CQN37,29	G18	QDRIIB_A16

Bank 3H VCCIO = 1.8V

CLK_50_B3H	D21	CLK_3H_0P/LVDS3H_13P/DQ34,22	DQ17	PLL_3H_CLKOUT0P,PLL_3H_CLKOUT0,PLL_3H_FB0/LVDS3H_15P/DQ34,18	F21	QDRIIB_Q7
M5A10_R_IO4	D20	CLK_3H_0N/LVDS3H_13N/DQ34,23	DQ17	PLL_3H_CLKOUT0N/LVDS3H_15N/DQ34,19	E21	M5A10_R_CLK
M5A10_R_IO5	A19	CLK_3H_1P/LVDS3H_12P/DQ33,24	DQ16	PLL_3H_CLKOUT1P,PLL_3H_CLKOUT1,PLL_3H_FB1/LVDS3H_10P/DQS33/CQ33,28	E19	QDRIIB_D2
M5A10_R_IO6	A20	CLK_3H_1N/LVDS3H_12N/DQ33,25	DQ16	PLL_3H_CLKOUT1N/LVDS3H_10N/DQSN33/CQN33,29	D19	QDRIIB_D3

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Title
DE5a-Net Board

Size	Document Number	Rev
B	FPGA Clock Bank 3	C

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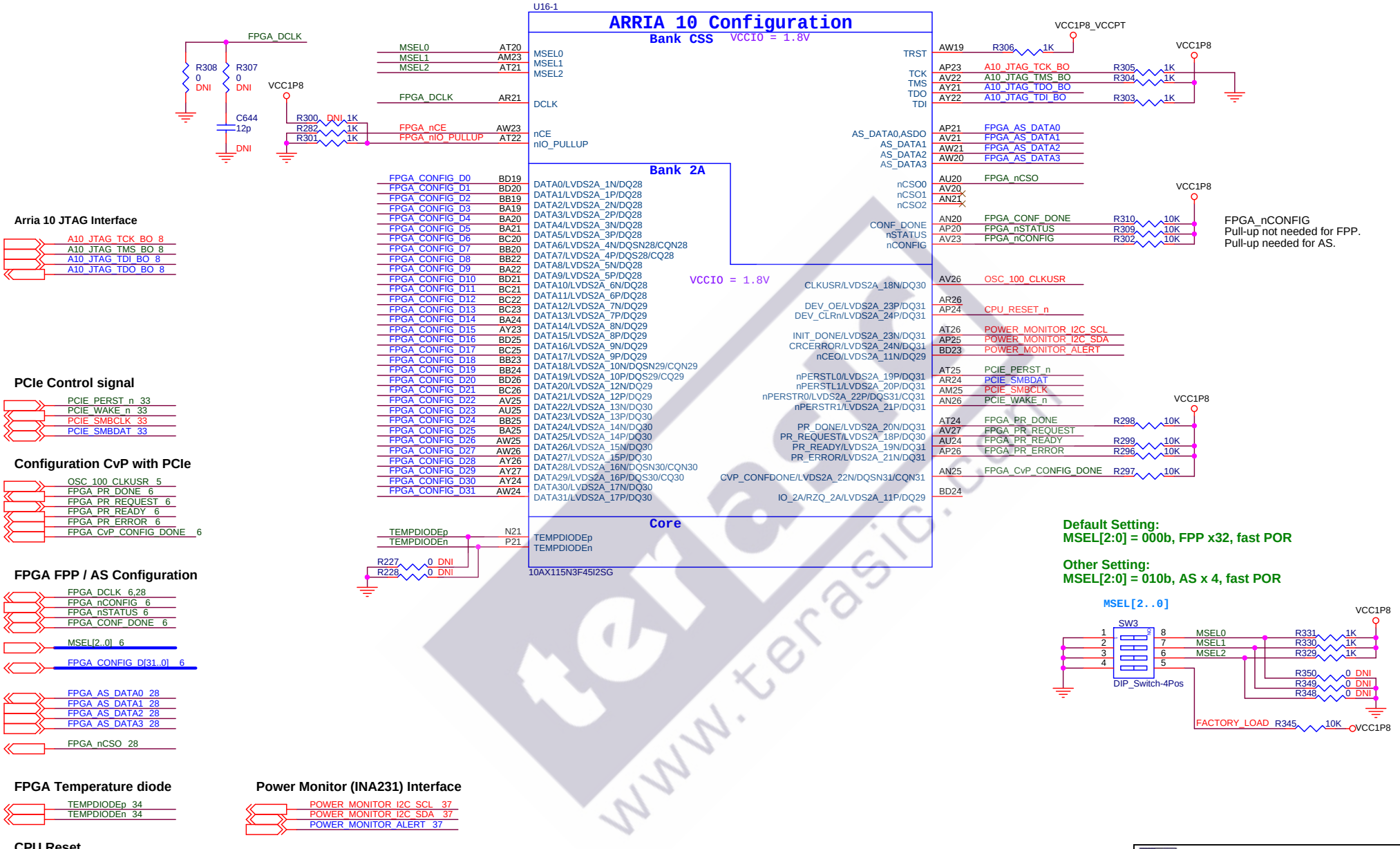

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Title
DE5a-Net Board

Size	Document Number	Rev
B	FPGA Configuration	C

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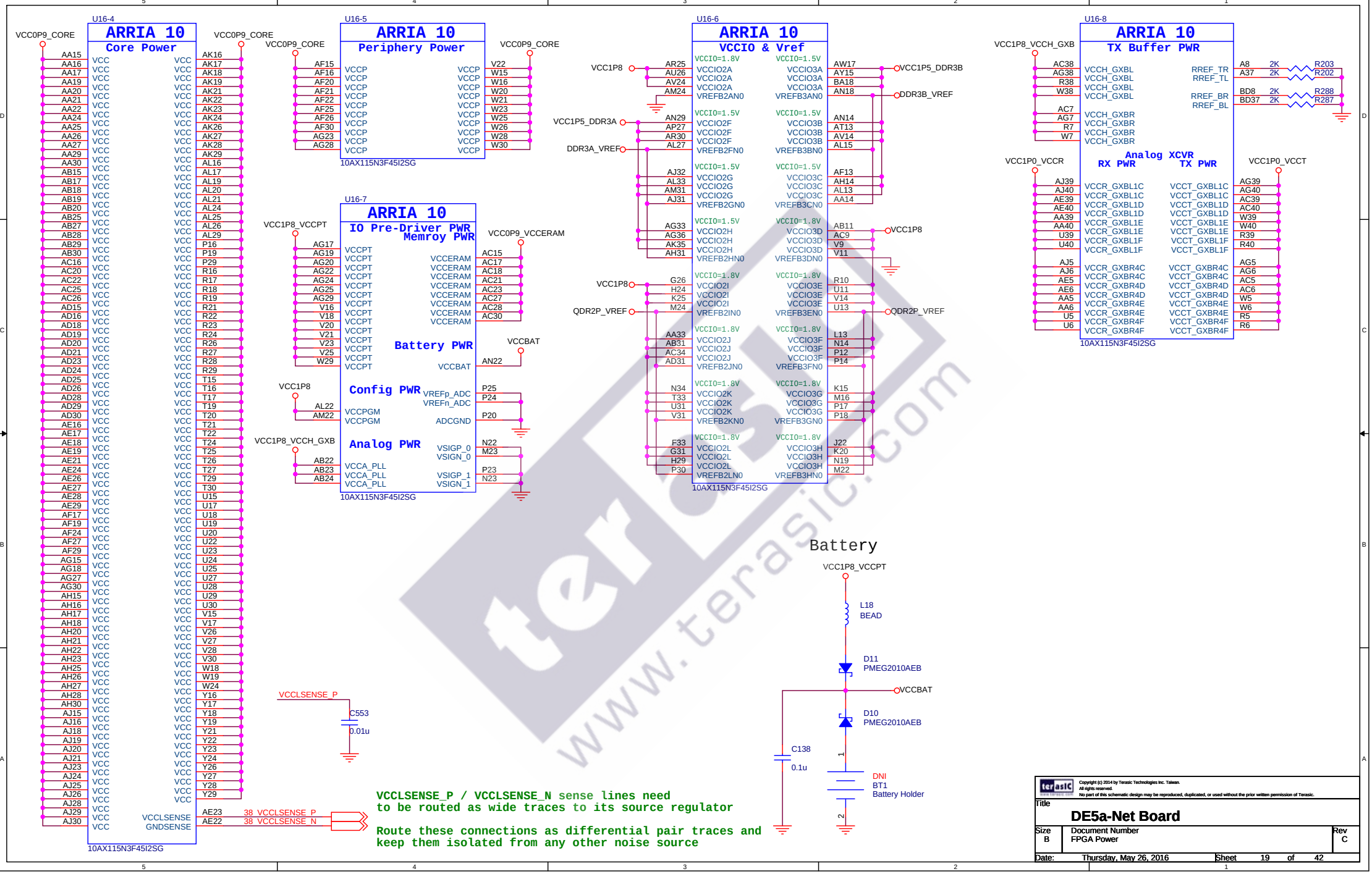
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VCCLSENSE
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VCCP
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U16-6
ARRIA 10
VCCIO & Vref
VCC1P8
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DDR3A_VREF
VCC1P5_DDR3B
DDR3B_VREF
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U16-7
ARRIA 10
IO Pre-Driver PWR
Memroy PWR
VCC1P8_VCCPT
VCC0P9_VCCERAM
VCCPT
VCCERAM
Battery PWR
VCCBAT
Config PWR
VCC1P8
VREFp_ADC
VREFn_ADC
VCCPGM
ADCGND
Analog PWR
VCC1P8_VCCH_GXB
VCCA_PLL
VSIGP_0
VSIGN_0
VSIGP_1
VSIGN_1
10AX115N3F45I2SG
U16-8
ARRIA 10
TX Buffer PWR
VCC1P8_VCCH_GXB
VCCH_GXBL
VCCH_GXBR
RREF_TR
RREF_TL
RREF_BR
RREF_BL
Analog XCVR
RX PWR
TX PWR
VCC1P0_VCCR
VCC1P0_VCCT
VCCR_GXBL1C
VCCT_GXBL1C
VCCR_GXBR4C
VCCT_GXBR4C
10AX115N3F45I2SG
VCCLSENSE_P
C553
0.01u
VCCLSENSE_P / VCCLSENSE_N sense lines need
to be routed as wide traces to its source regulator
Route these connections as differential pair traces and
keep them isolated from any other noise source
Battery
VCC1P8_VCCPT
L18
BEAD
D11
PMEG2010AEB
VCCBAT
D10
PMEG2010AEB
C138
0.1u
DNI
BT1
Battery Holder
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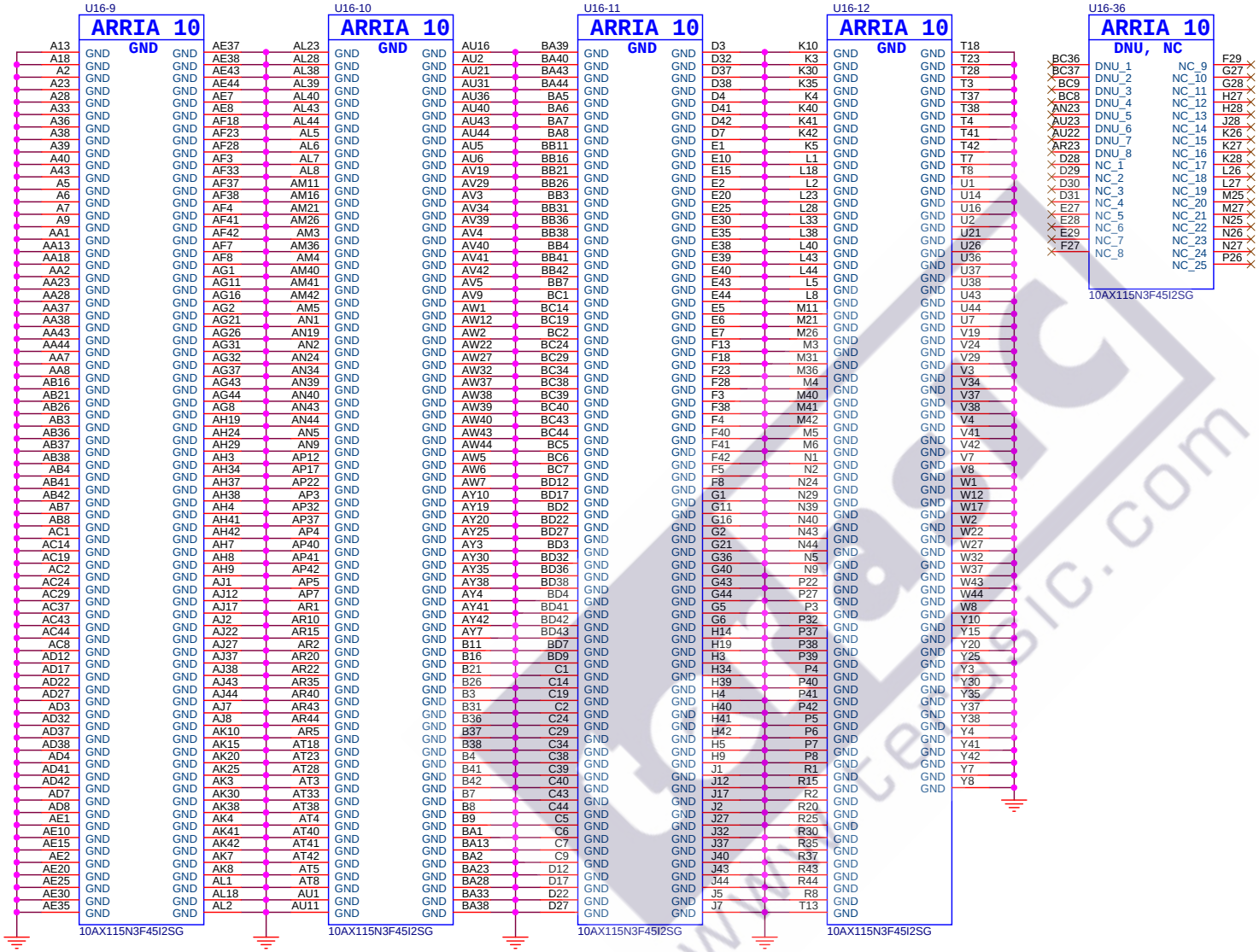
Title
DE5a-Net Board
Size
B
Document Number
FPGA Power
Rev
C
Date:
Thursday, May 26, 2016
Sheet
19
of
42



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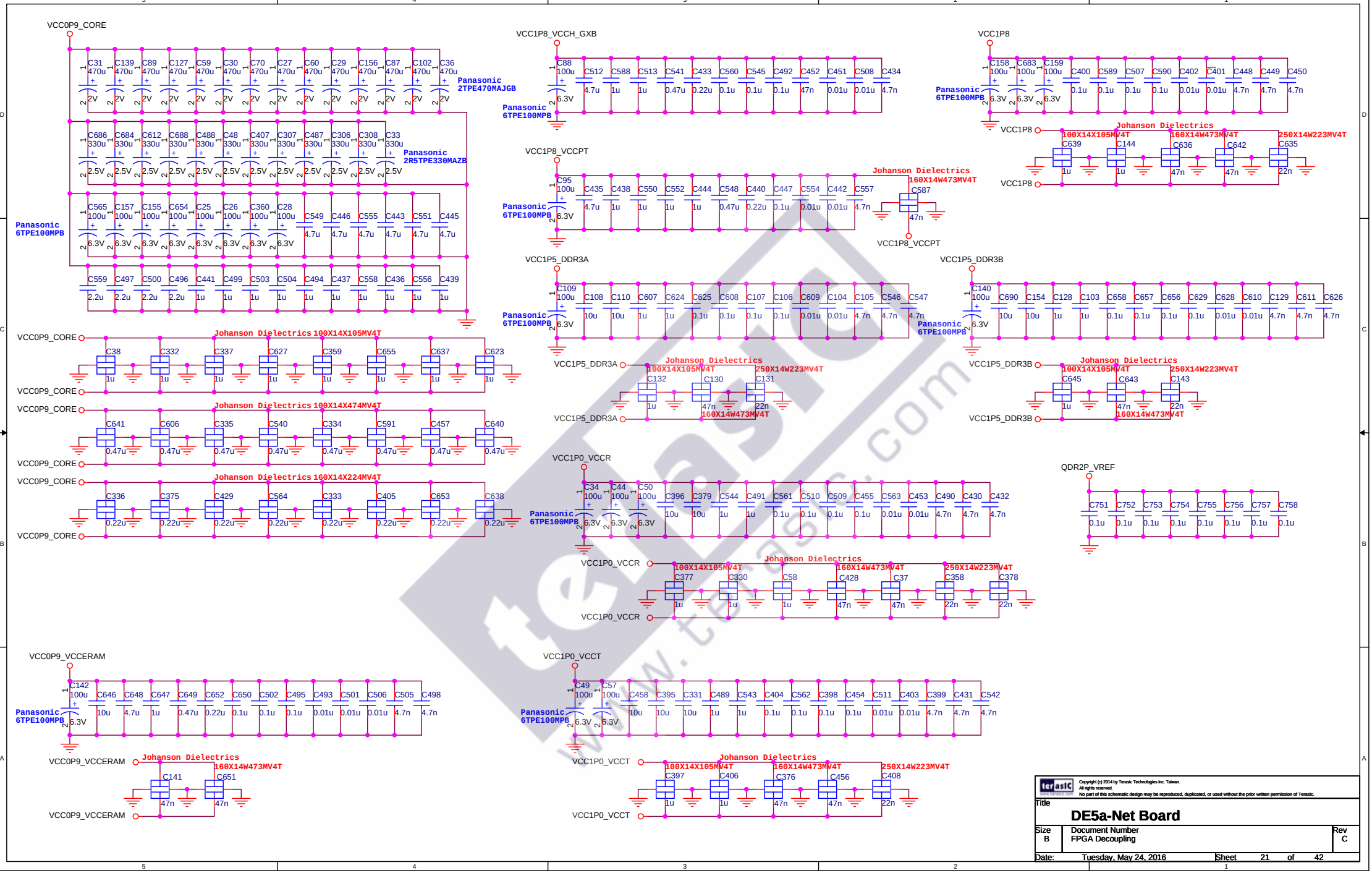
Title
DE5a-Net Board

Size	Document Number	Rev
B	FPGA GND	C

Date: Thursday, May 26, 2016 Sheet 20 of 42



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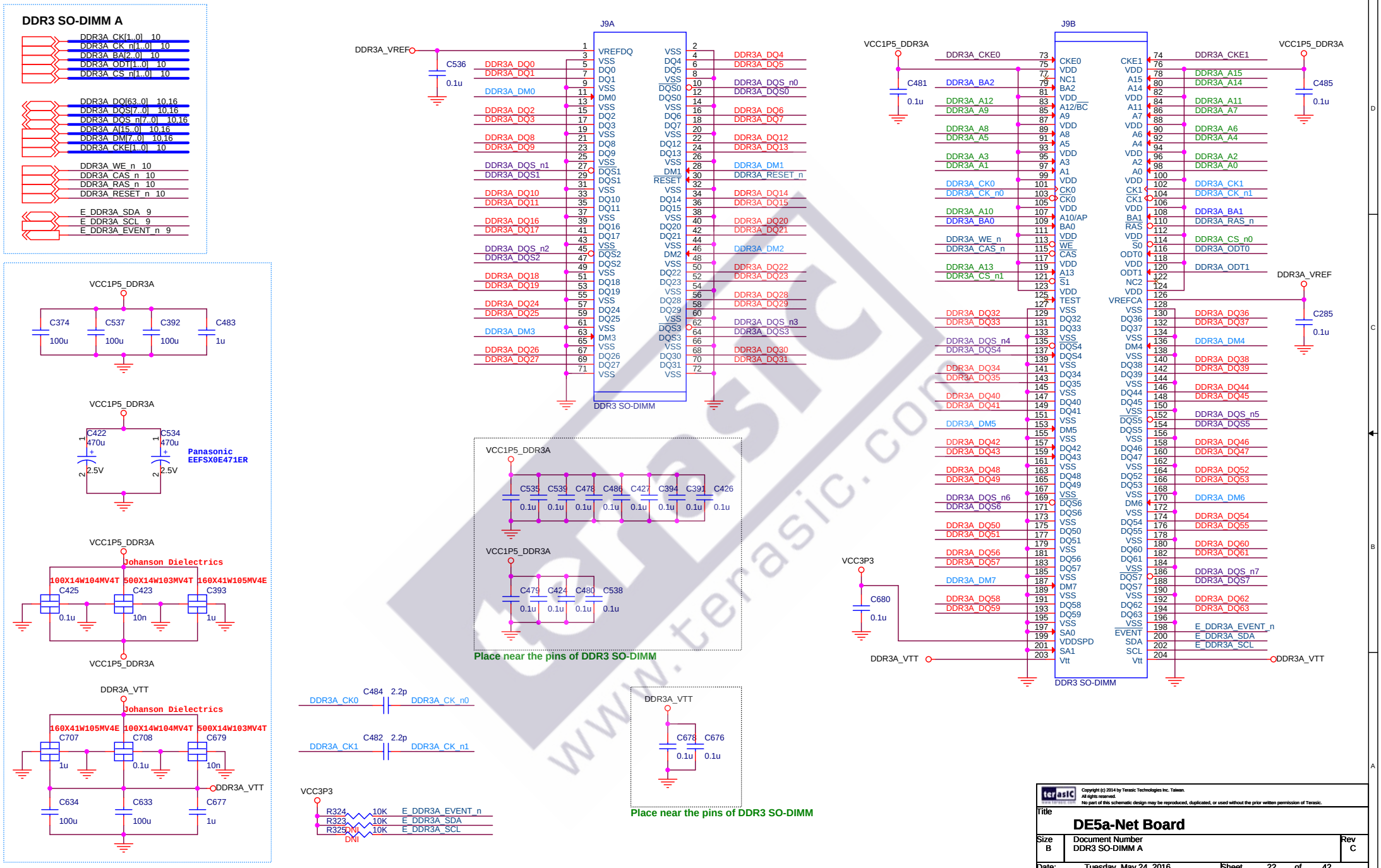
Title
DE5a-Net Board

Size	Document Number	Rev
B	FPGA Decoupling	C

Date: Tuesday, May 24, 2016 Sheet 21 of 42


DDR3 SO-DIMM A
DDR3A_CK[1..0] 10
DDR3A_CK_n[1..0] 10
DDR3A_BA[2..0] 10
DDR3A_ODT[1..0] 10
DDR3A_CS_n[1..0] 10
DDR3A_DQ[63..0] 10,16
DDR3A_DQS[7..0] 10,16
DDR3A_DQS_n[7..0] 10,16
DDR3A_A[15..0] 10,16
DDR3A_DM[7..0] 10,16
DDR3A_CKE[1..0] 10
DDR3A_WE_n 10
DDR3A_CAS_n 10
DDR3A_RAS_n 10
DDR3A_RESET_n 10
E_DDR3A_SDA 9
E_DDR3A_SCL 9
E_DDR3A_EVENT_n 9
VCC1P5_DDR3A
C374 100u
C537 100u
C392 100u
C483 1u
C422 470u 2.5V
C534 470u 2.5V
Panasonic
EEFSX0E471ER
Johanson Dielectrics
100X14W104MV4T C425 0.1u
500X14W103MV4T C423 10n
160X41W105MV4E C393 1u
DDR3A_VTT
160X41W105MV4E C707 1u
100X14W104MV4T C708 0.1u
500X14W103MV4T C679 10n
C634 100u
C633 100u
C677 1u
DDR3A_VREF
C536 0.1u
J9A
DDR3 SO-DIMM
VREFDQ
VSS
DQ0
DQ1
DM0
DQ2
DQ3
DQ8
DQ9
DQS1
DQ10
DQ11
DQ16
DQ17
DQS2
DQ18
DQ19
DQ24
DQ25
DM3
DQ26
DQ27
DQ4
DQ5
DQS0
DQ6
DQ7
DQ12
DQ13
DM1
RESET
DQ14
DQ15
DQ20
DQ21
DM2
DQ22
DQ23
DQ28
DQ29
DQS3
DQ30
DQ31
DDR3A_DQ0
DDR3A_DQ1
DDR3A_DM0
DDR3A_DQ2
DDR3A_DQ3
DDR3A_DQ8
DDR3A_DQ9
DDR3A_DQS_n1
DDR3A_DQS1
DDR3A_DQ10
DDR3A_DQ11
DDR3A_DQ16
DDR3A_DQ17
DDR3A_DQS_n2
DDR3A_DQS2
DDR3A_DQ18
DDR3A_DQ19
DDR3A_DQ24
DDR3A_DQ25
DDR3A_DM3
DDR3A_DQ26
DDR3A_DQ27
DDR3A_DQ4
DDR3A_DQ5
DDR3A_DQS_n0
DDR3A_DQS0
DDR3A_DQ6
DDR3A_DQ7
DDR3A_DQ12
DDR3A_DQ13
DDR3A_DM1
DDR3A_RESET_n
DDR3A_DQ14
DDR3A_DQ15
DDR3A_DQ20
DDR3A_DQ21
DDR3A_DM2
DDR3A_DQ22
DDR3A_DQ23
DDR3A_DQ28
DDR3A_DQ29
DDR3A_DQS_n3
DDR3A_DQS3
DDR3A_DQ30
DDR3A_DQ31
VCC1P5_DDR3A
C535 0.1u
C539 0.1u
C478 0.1u
C486 0.1u
C427 0.1u
C394 0.1u
C391 0.1u
C426 0.1u
C479 0.1u
C424 0.1u
C480 0.1u
C538 0.1u
Place near the pins of DDR3 SO-DIMM
C484 2.2p
DDR3A_CK0
DDR3A_CK_n0
C482 2.2p
DDR3A_CK1
DDR3A_CK_n1
VCC3P3
R324 10K E_DDR3A_EVENT_n
R323 10K E_DDR3A_SDA
R325 DNI 10K E_DDR3A_SCL
DNI
DDR3A_VTT
C678 0.1u
C676 0.1u
Place near the pins of DDR3 SO-DIMM
J9B
DDR3 SO-DIMM
VCC1P5_DDR3A
C481 0.1u
C485 0.1u
DDR3A_VREF
C285 0.1u
VCC3P3
C680 0.1u
DDR3A_VTT
DDR3A_CKE0
DDR3A_BA2
DDR3A_A12
DDR3A_A9
DDR3A_A8
DDR3A_A5
DDR3A_A3
DDR3A_A1
DDR3A_CK0
DDR3A_CK_n0
DDR3A_A10
DDR3A_BA0
DDR3A_WE_n
DDR3A_CAS_n
DDR3A_A13
DDR3A_CS_n1
DDR3A_DQ32
DDR3A_DQ33
DDR3A_DQS_n4
DDR3A_DQS4
DDR3A_DQ34
DDR3A_DQ35
DDR3A_DQ40
DDR3A_DQ41
DDR3A_DM5
DDR3A_DQ42
DDR3A_DQ43
DDR3A_DQ48
DDR3A_DQ49
DDR3A_DQS_n6
DDR3A_DQS6
DDR3A_DQ50
DDR3A_DQ51
DDR3A_DQ56
DDR3A_DQ57
DDR3A_DM7
DDR3A_DQ58
DDR3A_DQ59
DDR3A_CKE1
DDR3A_A15
DDR3A_A14
DDR3A_A11
DDR3A_A7
DDR3A_A6
DDR3A_A4
DDR3A_A2
DDR3A_A0
DDR3A_CK1
DDR3A_CK_n1
DDR3A_BA1
DDR3A_RAS_n
DDR3A_CS_n0
DDR3A_ODT0
DDR3A_ODT1
DDR3A_DQ36
DDR3A_DQ37
DDR3A_DM4
DDR3A_DQ38
DDR3A_DQ39
DDR3A_DQ44
DDR3A_DQ45
DDR3A_DQS_n5
DDR3A_DQS5
DDR3A_DQ46
DDR3A_DQ47
DDR3A_DQ52
DDR3A_DQ53
DDR3A_DM6
DDR3A_DQ54
DDR3A_DQ55
DDR3A_DQ60
DDR3A_DQ61
DDR3A_DQS_n7
DDR3A_DQS7
DDR3A_DQ62
DDR3A_DQ63
E_DDR3A_EVENT_n
E_DDR3A_SDA
E_DDR3A_SCL
DDR3A_VTT
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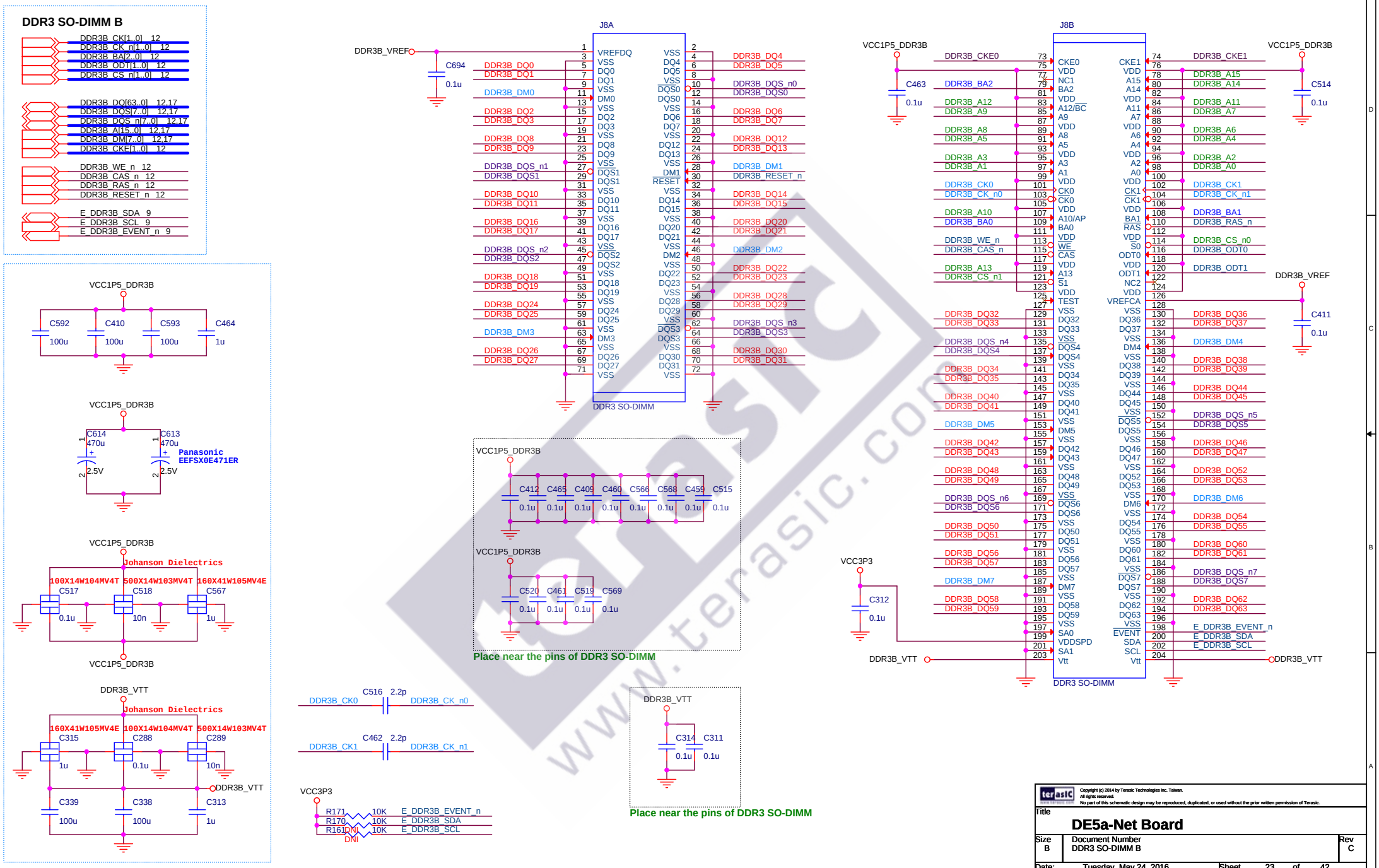
Title
DE5a-Net Board
Size B
Document Number
DDR3 SO-DIMM A
Rev C
Date: Tuesday, May 24, 2016
Sheet 22 of 42


DDR3 SO-DIMM B
DDR3B_CK[1..0] 12
DDR3B_CK_n[1..0] 12
DDR3B_BA[2..0] 12
DDR3B_ODT[1..0] 12
DDR3B_CS_n[1..0] 12
DDR3B_DQ[63..0] 12,17
DDR3B_DQS[7..0] 12,17
DDR3B_DQS_n[7..0] 12,17
DDR3B_A[15..0] 12,17
DDR3B_DM[7..0] 12,17
DDR3B_CKE[1..0] 12
DDR3B_WE_n 12
DDR3B_CAS_n 12
DDR3B_RAS_n 12
DDR3B_RESET_n 12
E_DDR3B_SDA 9
E_DDR3B_SCL 9
E_DDR3B_EVENT_n 9
VCC1P5_DDR3B
C592 100u
C410 100u
C593 100u
C464 1u
C614 470u
C613 470u
Panasonic
EEFSX0E471ER
2.5V
Johanson Dielectrics
100X14W104MV4T
500X14W103MV4T
160X41W105MV4E
C517 0.1u
C518 10n
C567 1u
DDR3B_VTT
160X41W105MV4E
100X14W104MV4T
500X14W103MV4T
C315 1u
C288 0.1u
C289 10n
C339 100u
C338 100u
C313 1u
DDR3B_VREF
C694 0.1u
J8A
DDR3 SO-DIMM
VREFDQ
VSS
DQ0
DQ1
DM0
DQ2
DQ3
DQ8
DQ9
DQS1
DQ10
DQ11
DQ16
DQ17
DQS2
DQ18
DQ19
DQ24
DQ25
DM3
DQ26
DQ27
DQ4
DQ5
DQS0
DQ6
DQ7
DQ12
DQ13
DM1
RESET
DQ14
DQ15
DQ20
DQ21
DM2
DQ22
DQ23
DQ28
DQ29
DQS3
DQ30
DQ31
DDR3B_DQ0
DDR3B_DQ1
DDR3B_DM0
DDR3B_DQ2
DDR3B_DQ3
DDR3B_DQ8
DDR3B_DQ9
DDR3B_DQS_n1
DDR3B_DQS1
DDR3B_DQ10
DDR3B_DQ11
DDR3B_DQ16
DDR3B_DQ17
DDR3B_DQS_n2
DDR3B_DQS2
DDR3B_DQ18
DDR3B_DQ19
DDR3B_DQ24
DDR3B_DQ25
DDR3B_DM3
DDR3B_DQ26
DDR3B_DQ27
DDR3B_DQ4
DDR3B_DQ5
DDR3B_DQS_n0
DDR3B_DQS0
DDR3B_DQ6
DDR3B_DQ7
DDR3B_DQ12
DDR3B_DQ13
DDR3B_DM1
DDR3B_RESET_n
DDR3B_DQ14
DDR3B_DQ15
DDR3B_DQ20
DDR3B_DQ21
DDR3B_DM2
DDR3B_DQ22
DDR3B_DQ23
DDR3B_DQ28
DDR3B_DQ29
DDR3B_DQS_n3
DDR3B_DQS3
DDR3B_DQ30
DDR3B_DQ31
VCC1P5_DDR3B
C412 0.1u
C465 0.1u
C409 0.1u
C460 0.1u
C566 0.1u
C568 0.1u
C459 0.1u
C515 0.1u
C520 0.1u
C461 0.1u
C519 0.1u
C569 0.1u
Place near the pins of DDR3 SO-DIMM
C516 2.2p
DDR3B_CK0
DDR3B_CK_n0
C462 2.2p
DDR3B_CK1
DDR3B_CK_n1
VCC3P3
R171 10K E_DDR3B_EVENT_n
R170 10K E_DDR3B_SDA
R161 DNI 10K E_DDR3B_SCL
DNI
DDR3B_VTT
C314 0.1u
C311 0.1u
Place near the pins of DDR3 SO-DIMM
J8B
DDR3 SO-DIMM
VCC1P5_DDR3B
C463 0.1u
C514 0.1u
C411 0.1u
DDR3B_VREF
VCC3P3
C312 0.1u
DDR3B_VTT
CKE0
VDD
NC1
BA2
A12/BC
A9
A8
A5
A3
A1
CK0
A10/AP
BA0
WE
CAS
A13
S1
TEST
DQ32
DQS4
DQ34
DQ35
DQ40
DQ41
DM5
DQ42
DQ43
DQ48
DQ49
DQS6
DQ50
DQ51
DQ56
DQ57
DM7
DQ58
DQ59
SA0
VDDSPD
SA1
Vtt
CKE1
A15
A14
A11
A7
A6
A4
A2
A0
CK1
BA1
RAS
S0
ODT0
ODT1
NC2
VREFCA
DQ36
DQ37
DM4
DQ38
DQ39
DQ44
DQ45
DQS5
DQ46
DQ47
DQ52
DQ53
DM6
DQ54
DQ55
DQ60
DQ61
DQS7
DQ62
DQ63
EVENT
SDA
SCL
DDR3B_CKE0
DDR3B_BA2
DDR3B_A12
DDR3B_A9
DDR3B_A8
DDR3B_A5
DDR3B_A3
DDR3B_A1
DDR3B_CK0
DDR3B_CK_n0
DDR3B_A10
DDR3B_BA0
DDR3B_WE_n
DDR3B_CAS_n
DDR3B_A13
DDR3B_CS_n1
DDR3B_DQ32
DDR3B_DQ33
DDR3B_DQS_n4
DDR3B_DQS4
DDR3B_DQ34
DDR3B_DQ35
DDR3B_DQ40
DDR3B_DQ41
DDR3B_DM5
DDR3B_DQ42
DDR3B_DQ43
DDR3B_DQ48
DDR3B_DQ49
DDR3B_DQS_n6
DDR3B_DQS6
DDR3B_DQ50
DDR3B_DQ51
DDR3B_DQ56
DDR3B_DQ57
DDR3B_DM7
DDR3B_DQ58
DDR3B_DQ59
DDR3B_CKE1
DDR3B_A15
DDR3B_A14
DDR3B_A11
DDR3B_A7
DDR3B_A6
DDR3B_A4
DDR3B_A2
DDR3B_A0
DDR3B_CK1
DDR3B_CK_n1
DDR3B_BA1
DDR3B_RAS_n
DDR3B_CS_n0
DDR3B_ODT0
DDR3B_ODT1
DDR3B_DQ36
DDR3B_DQ37
DDR3B_DM4
DDR3B_DQ38
DDR3B_DQ39
DDR3B_DQ44
DDR3B_DQ45
DDR3B_DQS_n5
DDR3B_DQS5
DDR3B_DQ46
DDR3B_DQ47
DDR3B_DQ52
DDR3B_DQ53
DDR3B_DM6
DDR3B_DQ54
DDR3B_DQ55
DDR3B_DQ60
DDR3B_DQ61
DDR3B_DQS_n7
DDR3B_DQS7
DDR3B_DQ62
DDR3B_DQ63
E_DDR3B_EVENT_n
E_DDR3B_SDA
E_DDR3B_SCL
DDR3B_VTT
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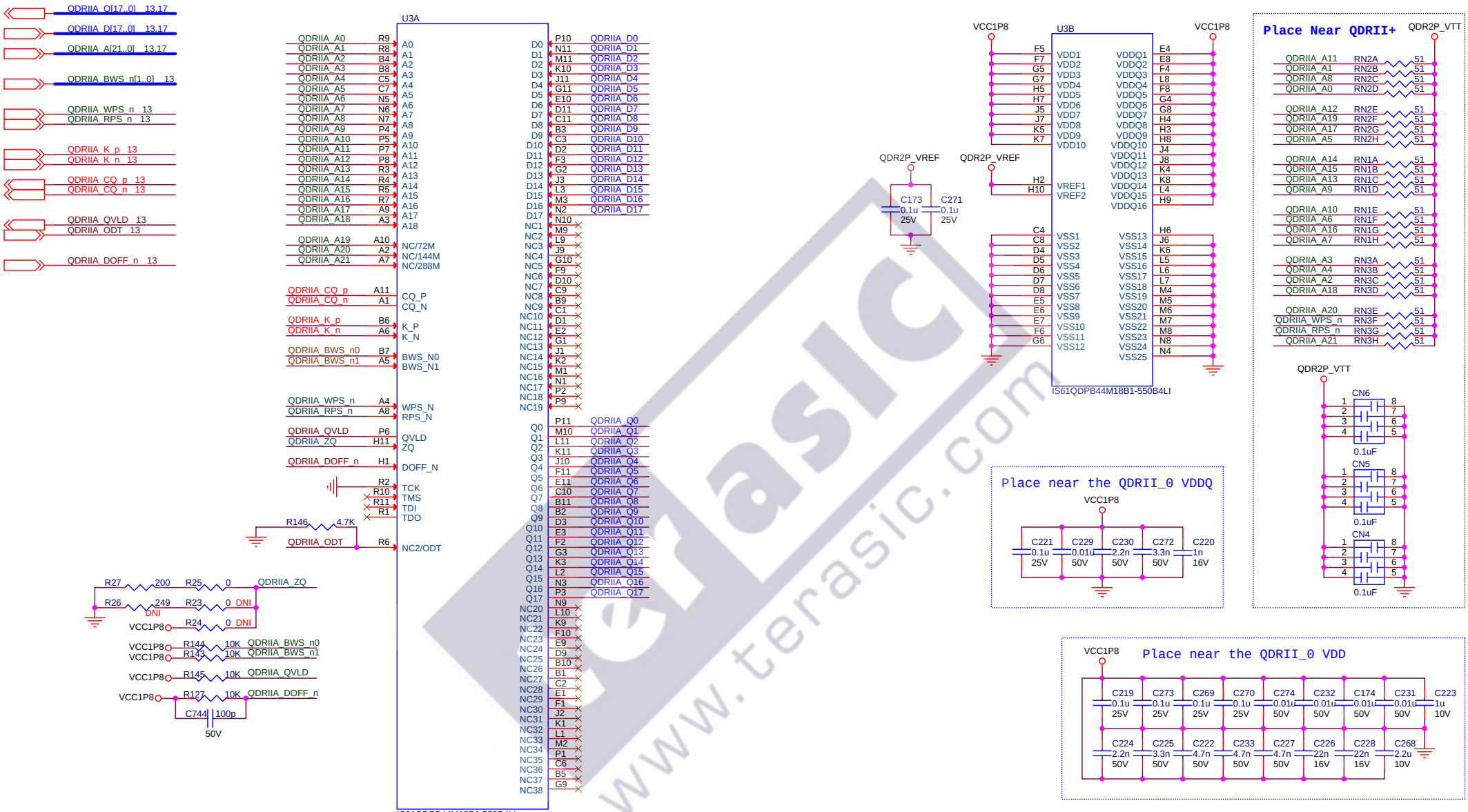
Title
DE5a-Net Board
Size B
Document Number
DDR3 SO-DIMM B
Rev C
Date: Tuesday, May 24, 2016
Sheet 23 of 42

QDRII+ PORT A



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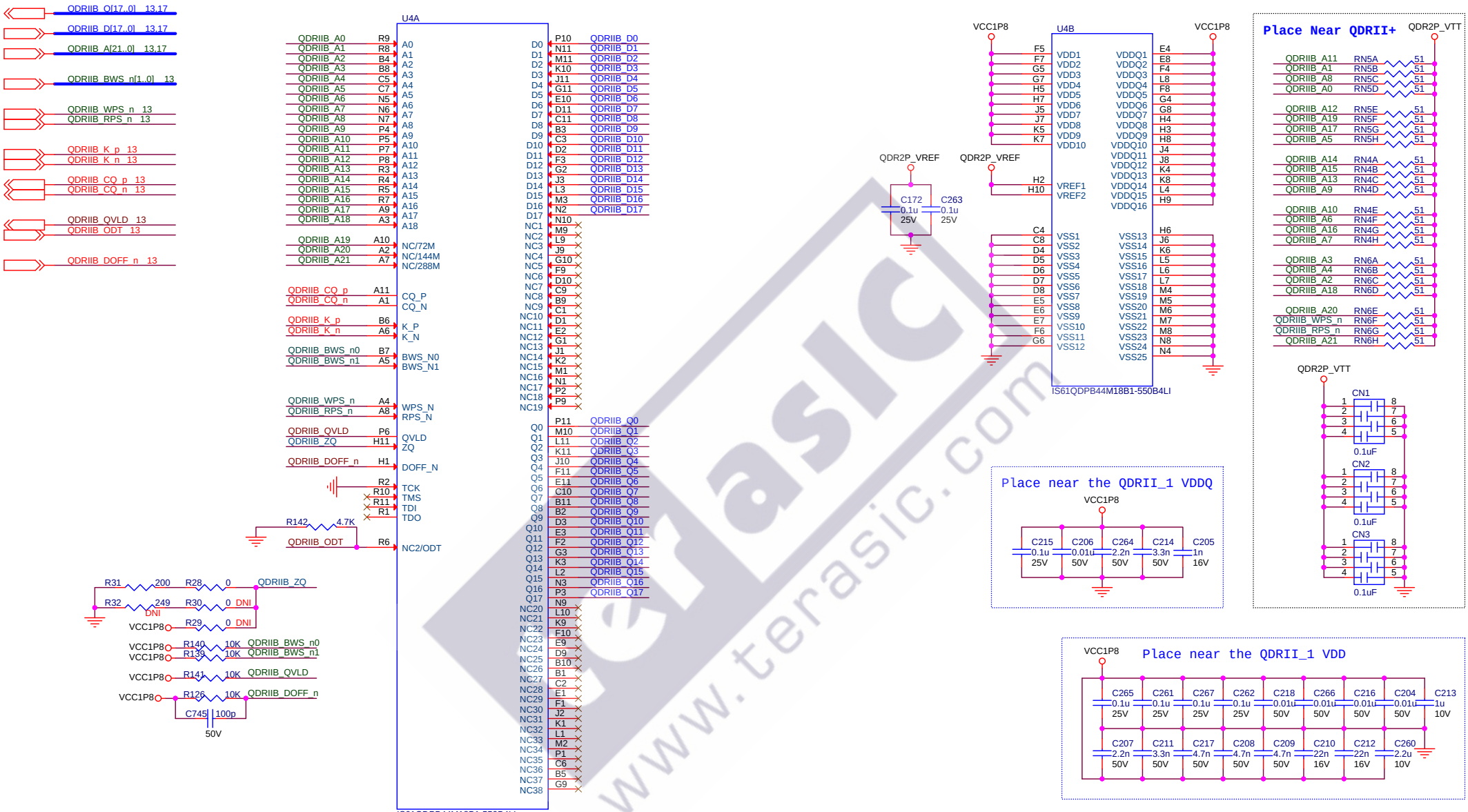
Title: **DE5a-Net Board**

Size	Document Number	Rev
B	QDRII+ SRAM Port A	C

Date: Tuesday, May 24, 2016 Sheet 24 of 42

QDRII+ PORT B



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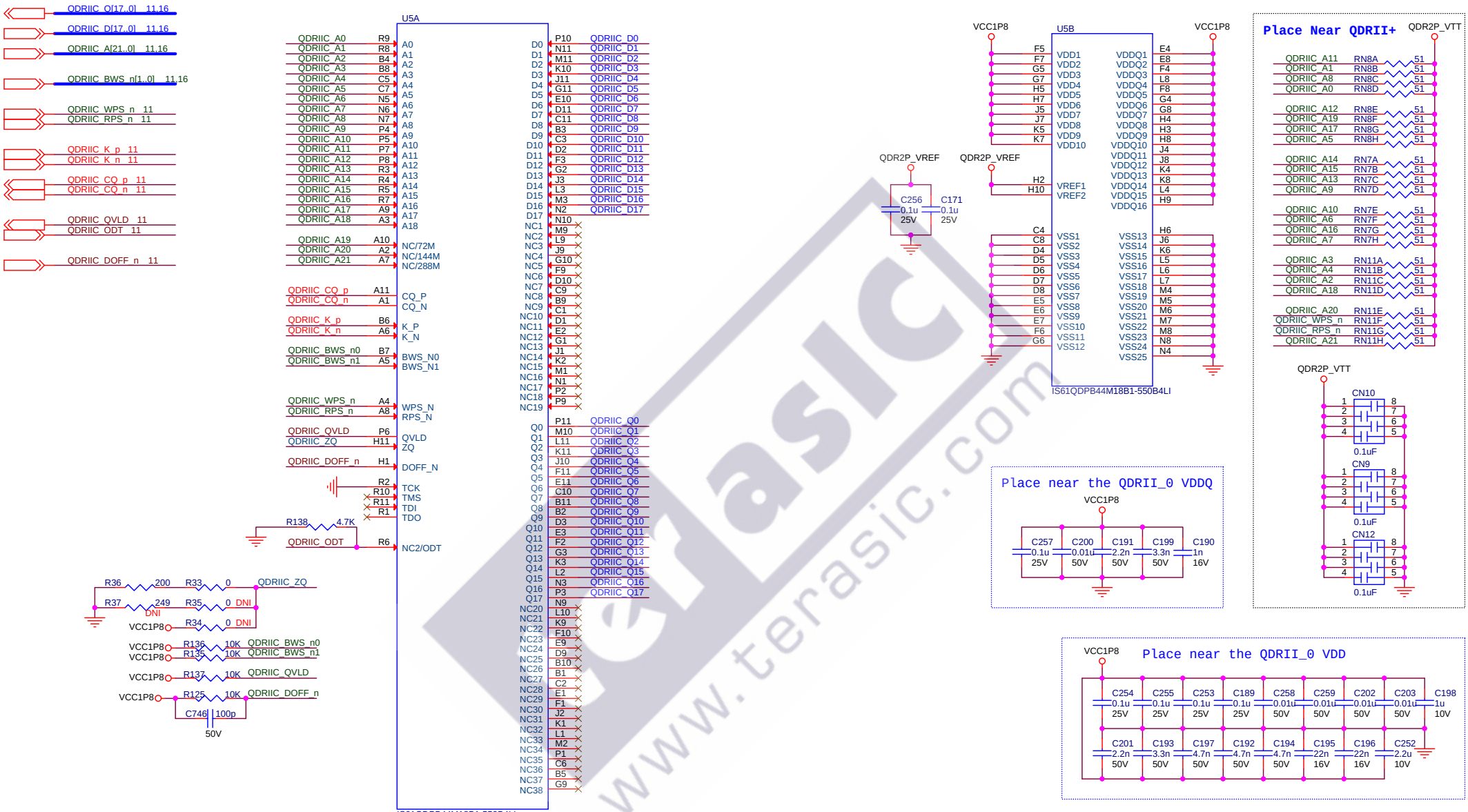
Title: **DE5a-Net Board**

Size	Document Number	Rev
B	QDRII+ SRAM Port B	C

Date: Tuesday, May 24, 2016 Sheet 25 of 42

QDRII+ PORT C



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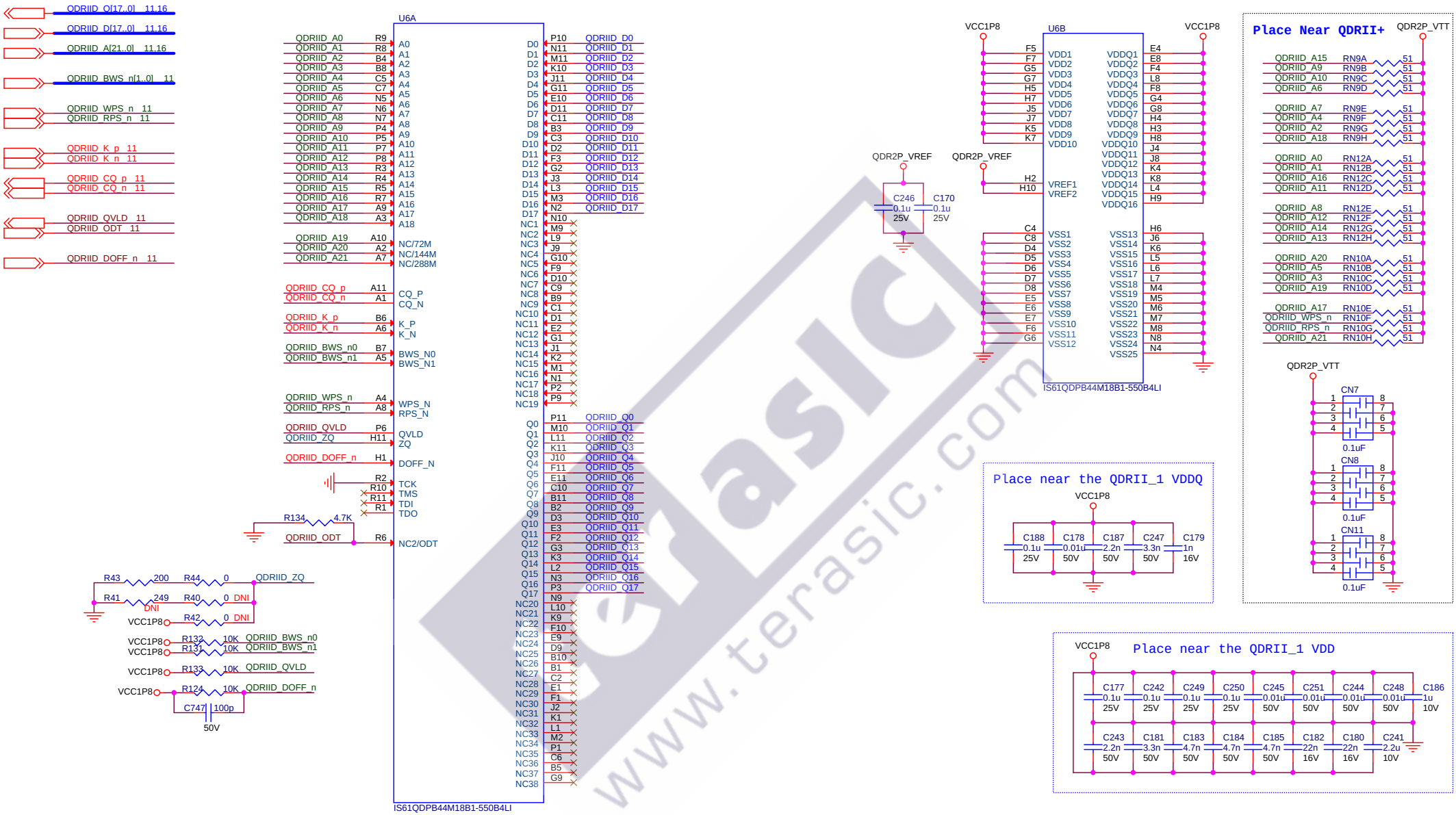
Title: **DE5a-Net Board**

Size	Document Number	Rev
B	QDRII+ SRAM Port C	C

Date: Tuesday, May 24, 2016 Sheet 26 of 42

QDRII+ PORT D



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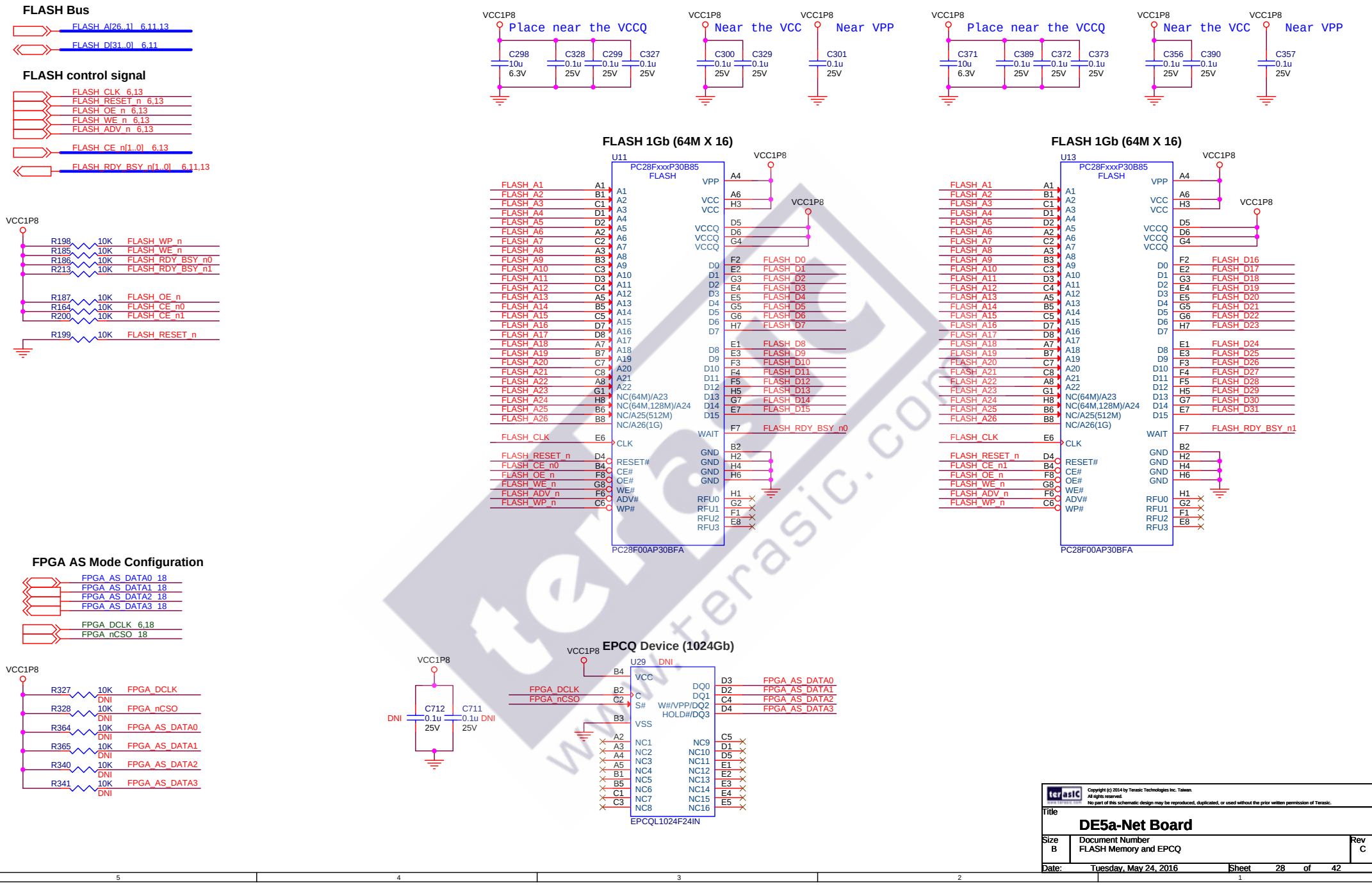
Title: **DE5a-Net Board**

Size	Document Number	Rev
B	QDRII+ SRAM Port D	C

Date: Tuesday, May 24, 2016 Sheet 27 of 42



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Title
DE5a-Net Board

Size	Document Number	Rev
B	FLASH Memory and EPCQ	C

Date: Tuesday, May 24, 2016 Sheet 28 of 42

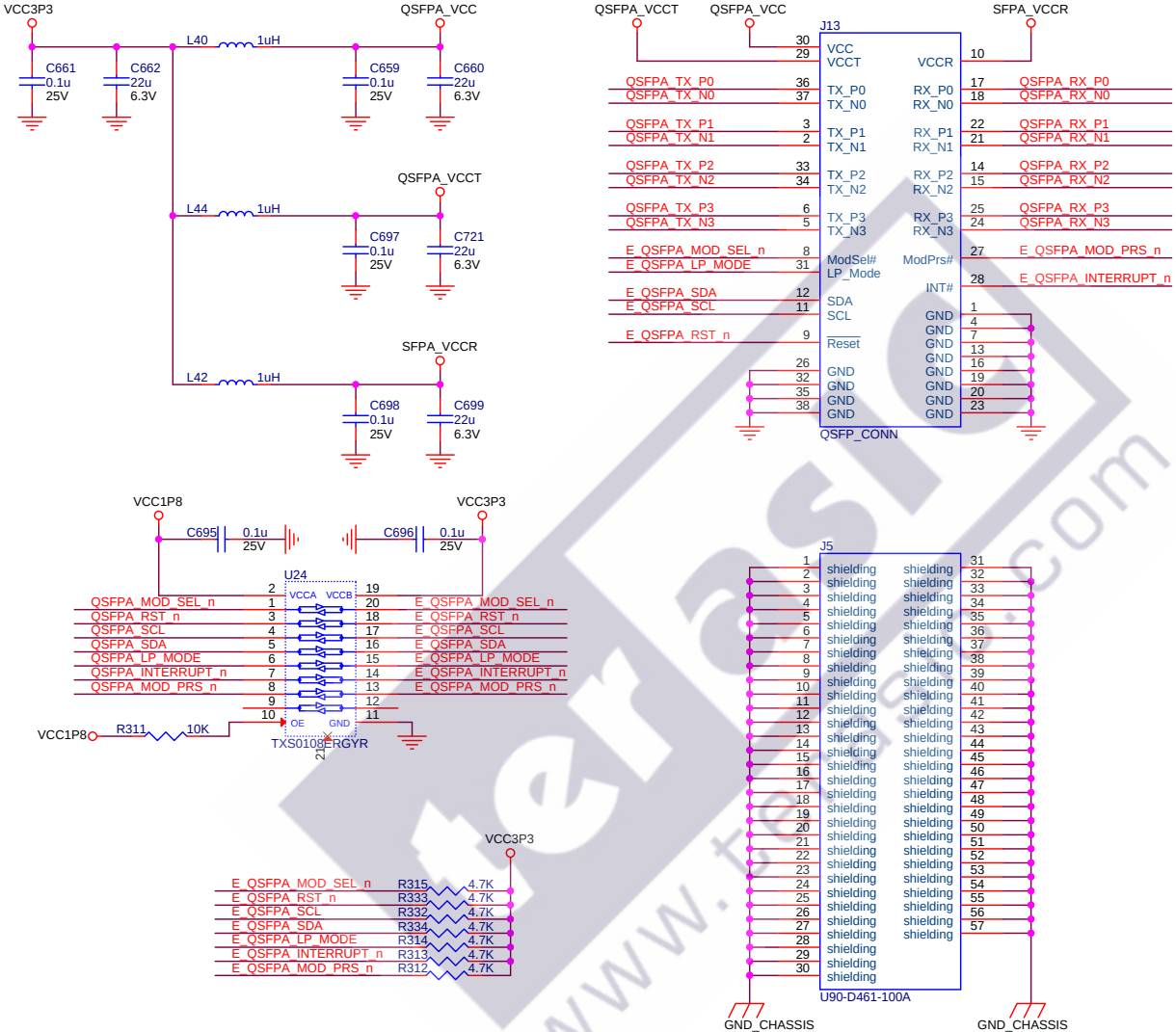
QSFP Port A Transceivers

QSFPA_TX_P[3:0] 15
QSFPA_TX_N[3:0] 15
QSFPA_RX_P[3:0] 15
QSFPA_RX_N[3:0] 15

QSFP Port A Control Interface

QSFPA_MOD_SEL_n 12
QSFPA_RST_n 12
QSFPA_SCL 12
QSFPA_SDA 12
QSFPA_LP_MODE 12
QSFPA_INTERRUPT_n 12
QSFPA_MOD_PRS_n 12

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.
NOTE 3: DC blocking capacitors are in the module for RX and TX.
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



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Title
DE5a-Net Board

Size	Document Number	Rev
B	QSFP+ Connector Port A	C

Date: Tuesday, May 24, 2016 Sheet 29 of 42

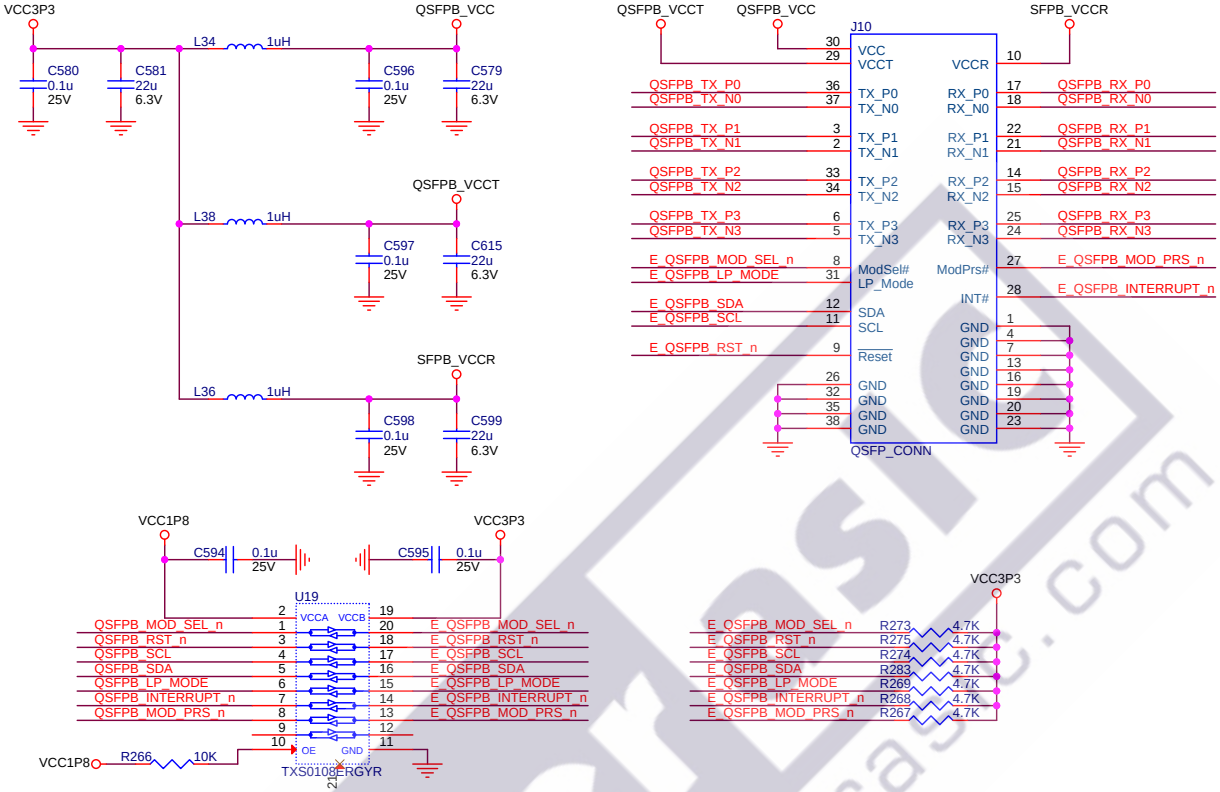
QSFP Port B Transceivers

QSFPB_TX_P[3:0] 15
QSFPB_TX_N[3:0] 15
QSFPB_RX_P[3:0] 15
QSFPB_RX_N[3:0] 15

QSFP Port B Control Interface

QSFPB_MOD_SEL_n 12
QSFPB_RST_n 12
QSFPB_SCL 12
QSFPB_SDA 12
QSFPB_LP_MODE 12
QSFPB_INTERRUPT_n 12
QSFPB_MOD_PRS_n 12

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.
NOTE 3: DC blocking capacitors are in the module for RX and TX.
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



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Title
DE5a-Net Board

Size	Document Number	Rev
B	QSFP+ Connector Port B	C

Date: Tuesday, May 24, 2016 Sheet 30 of 42

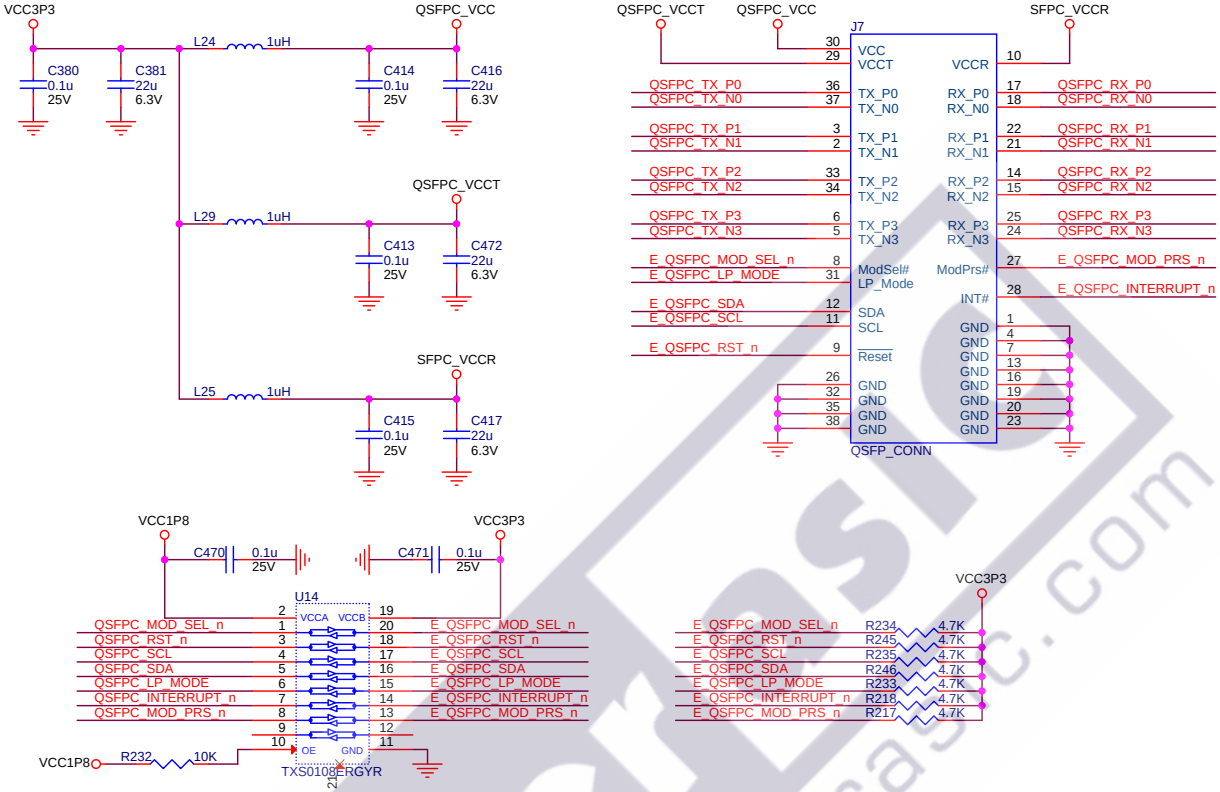
QSFP Port C Transceivers

QSFPC_TX_P[3:0] 15
QSFPC_TX_N[3:0] 15
QSFPC_RX_P[3:0] 15
QSFPC_RX_N[3:0] 15

QSFP Port C Control Interface

QSFPC_MOD_SEL_n 12
QSFPC_RST_n 12
QSFPC_SCL 12
QSFPC_SDA 12
QSFPC_LP_MODE 12
QSFPC_INTERRUPT_n 12
QSFPC_MOD_PRS_n 12

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.
NOTE 3: DC blocking capacitors are in the module for RX and TX.
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



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Title
DE5a-Net Board

Size	Document Number	Rev
B	QSFP+ Connector Port C	C

Date: Tuesday, May 24, 2016 Sheet 31 of 42

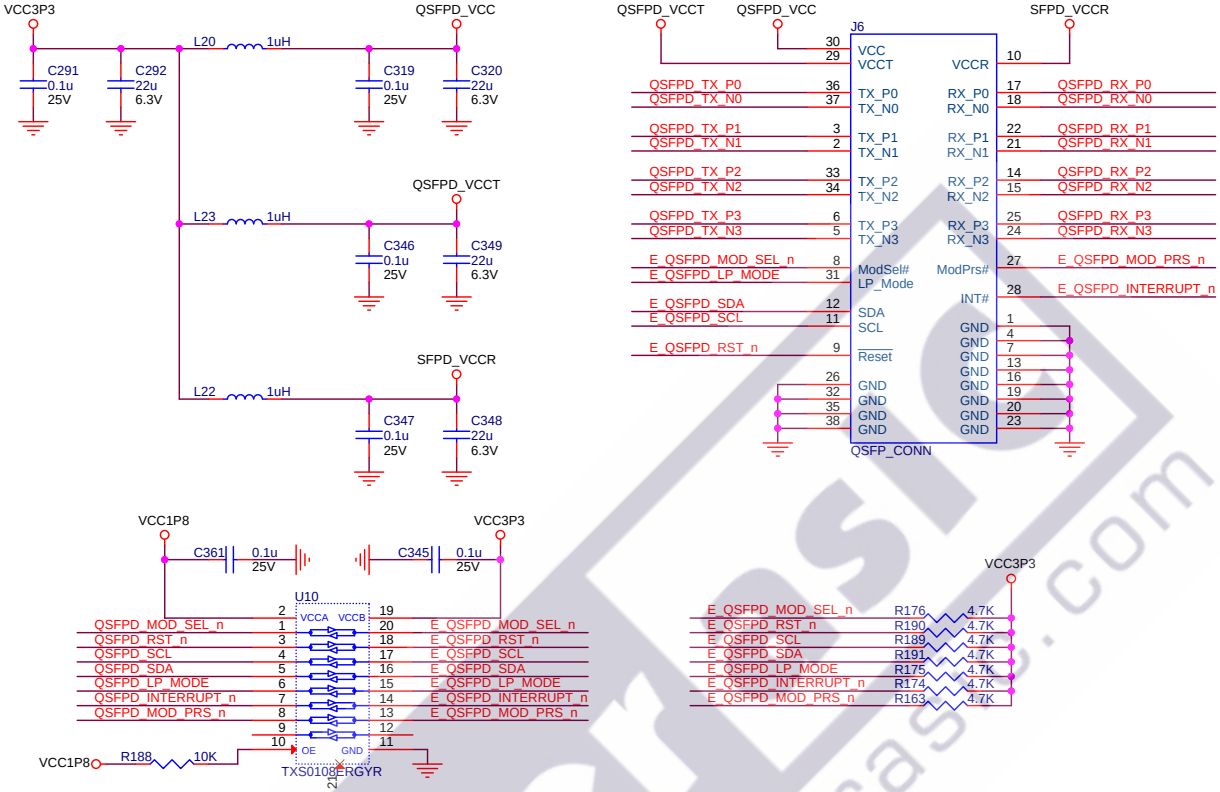
QSFP Port D Transceivers

QSFPD_TX_P[3:0] 15
QSFPD_TX_N[3:0] 15
QSFPD_RX_P[3:0] 15
QSFPD_RX_N[3:0] 15

QSFP Port D Control Interface

QSFPD_MOD_SEL_n 12
QSFPD_RST_n 12
QSFPD_SCL 12
QSFPD_SDA 12
QSFPD_LP_MODE 12
QSFPD_INTERRUPT_n 12
QSFPD_MOD_PRS_n 12

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.
NOTE 3: DC blocking capacitors are in the module for RX and TX.
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



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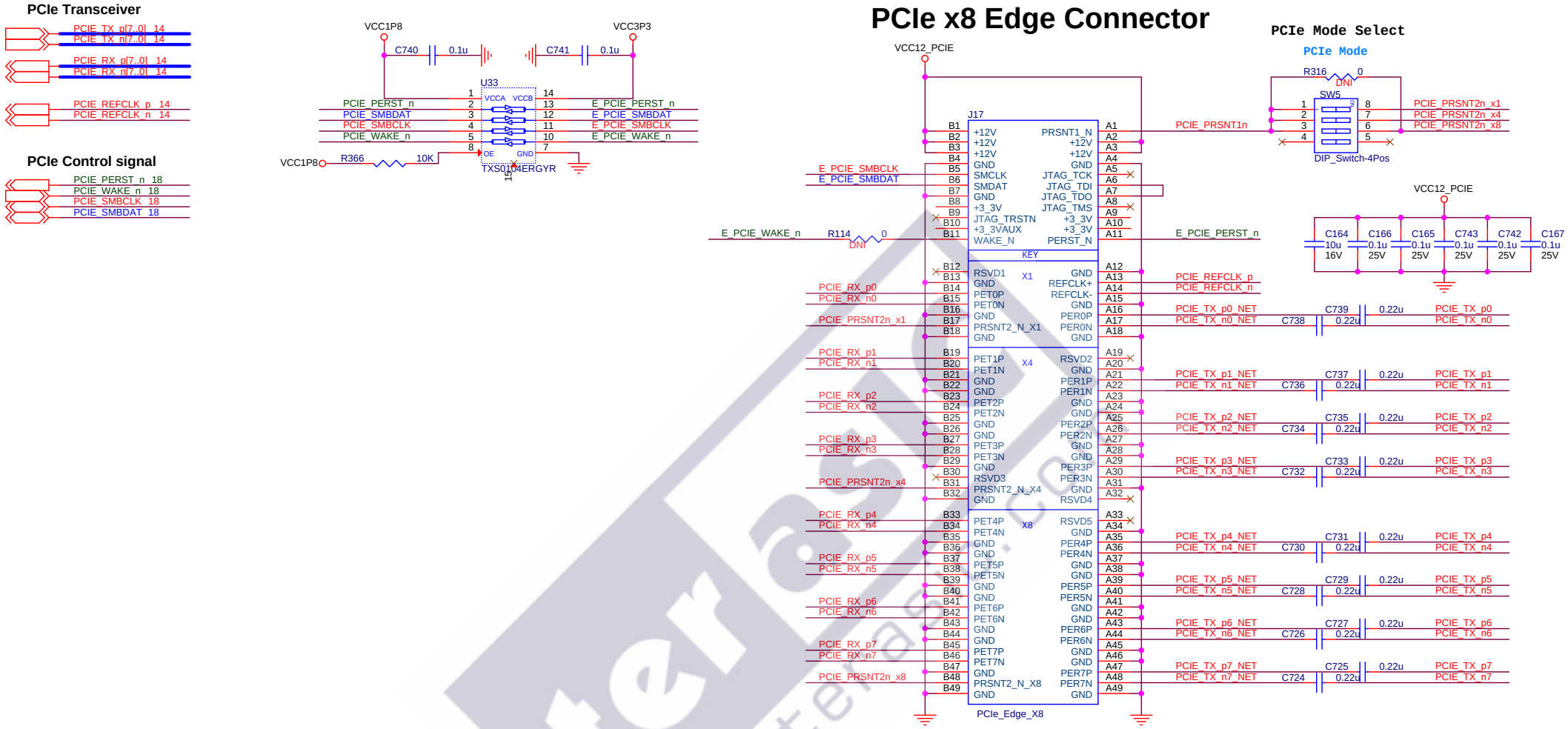
Title
DE5a-Net Board

Size	Document Number	Rev
B	QSFP+ Connector Port D	C

Date: Tuesday, May 24, 2016 Sheet 32 of 42

PCIe x8 Edge Connector



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Title: **DE5a-Net Board**

Size	Document Number	Rev
B	PCIe x 8	C

Date: Tuesday, May 24, 2016 Sheet 33 of 42

FPGA Temperature diode

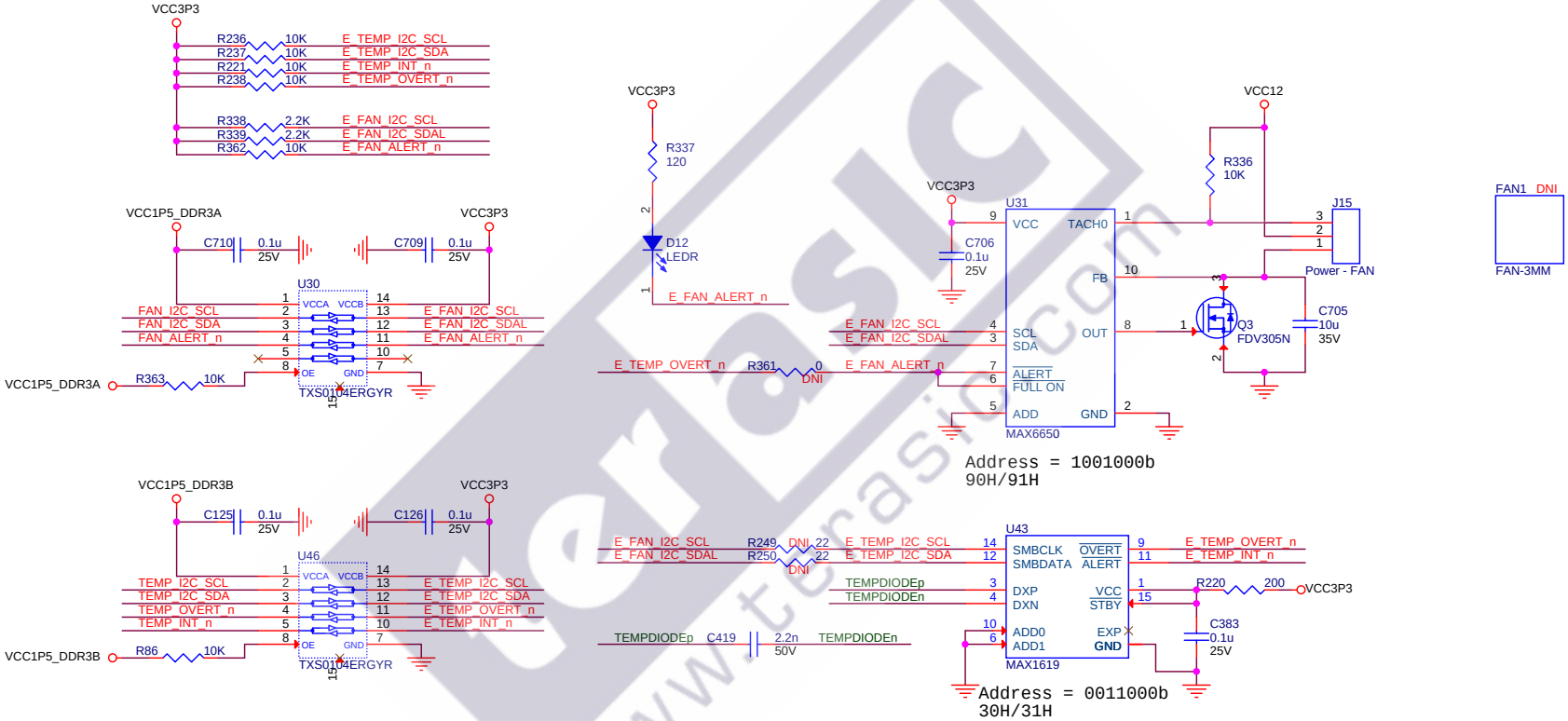
TEMPDIODEp 18
TEMPDIODEn 18

FPGA Temperature Control and Monitor

TEMP_I2C_SCL 12
TEMP_I2C_SDA 12
TEMP_OVERT_n 12
TEMP_INT_n 12

FAN Control Interface

FAN_I2C_SCL 10
FAN_I2C_SDA 10
FAN_ALERT_n 10



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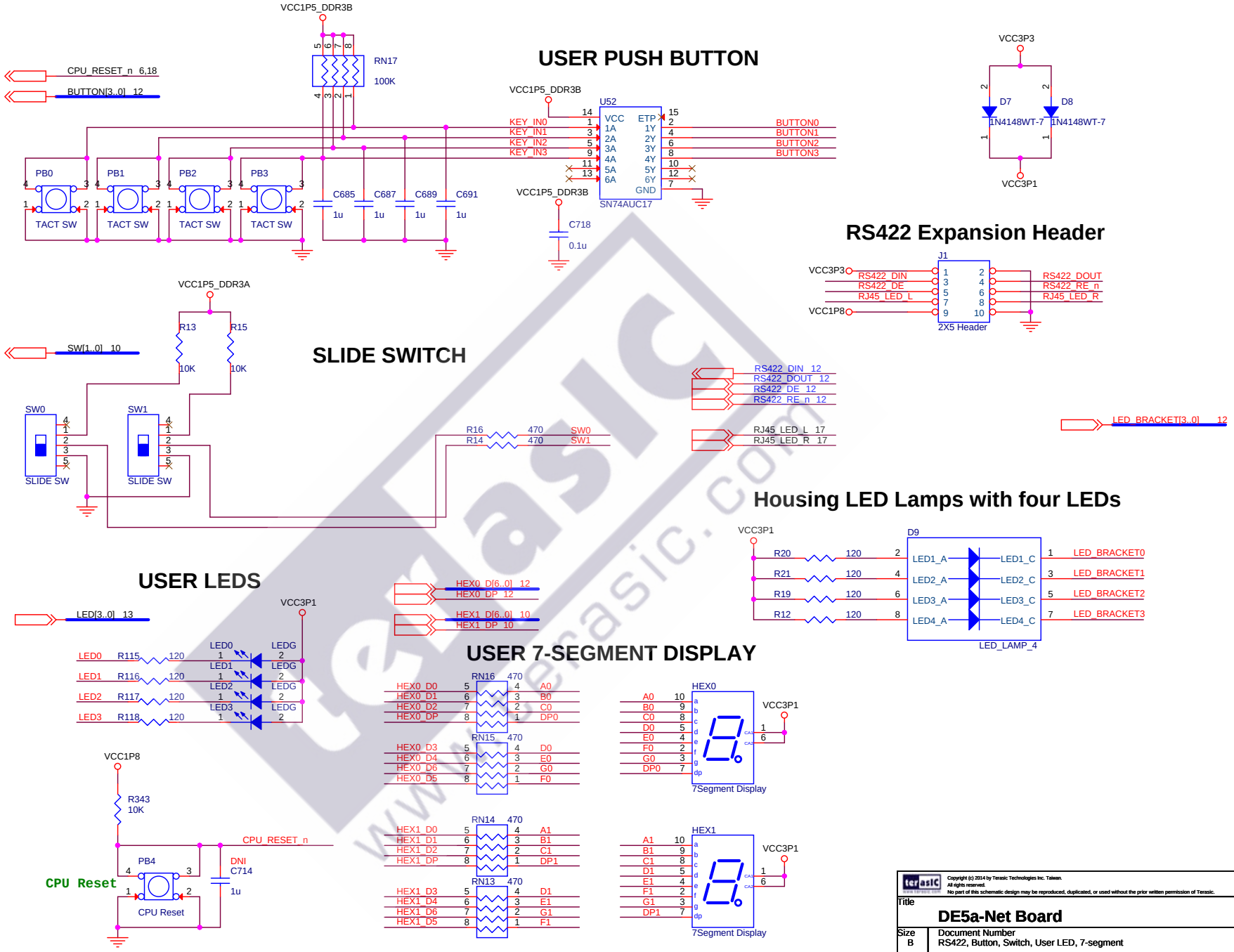
Title
DE5a-Net Board

Size	Document Number	Rev
B	FAN Control and Temperature Monitor	C

Date: Tuesday, May 24, 2016 Sheet 34 of 42


USER PUSH BUTTON
VCC1P5_DDR3B
RN17
100K
CPU_RESET_n 6,18
BUTTON[3..0] 12
PB0
PB1
PB2
PB3
TACT SW
C685
C687
C689
C691
1u
U52
SN74AUC17
KEY_IN0
KEY_IN1
KEY_IN2
KEY_IN3
BUTTON0
BUTTON1
BUTTON2
BUTTON3
C718
0.1u
VCC3P3
D7
D8
1N4148WT-7
VCC3P1
RS422 Expansion Header
J1
2X5 Header
RS422_DIN
RS422_DE
RJ45_LED_L
RS422_DOUT
RS422_RE_n
RJ45_LED_R
VCC1P8
VCC1P5_DDR3A
SW[1..0] 10
R13
R15
10K
SLIDE SWITCH
SW0
SW1
SLIDE SW
R16
R14
470
RS422_DIN 12
RS422_DOUT 12
RS422_DE 12
RS422_RE_n 12
RJ45_LED_L 17
RJ45_LED_R 17
LED_BRACKET[3..0] 12
Housing LED Lamps with four LEDs
D9
LED_LAMP_4
R20
R21
R19
R12
120
LED1_A
LED2_A
LED3_A
LED4_A
LED1_C
LED2_C
LED3_C
LED4_C
LED_BRACKET0
LED_BRACKET1
LED_BRACKET2
LED_BRACKET3
USER LEDS
LED[3..0] 13
LED0
LED1
LED2
LED3
R115
R116
R117
R118
LEDG
USER 7-SEGMENT DISPLAY
HEX0_D[6..0] 12
HEX0_DP 12
HEX1_D[6..0] 10
HEX1_DP 10
RN16
RN15
RN14
RN13
HEX0
HEX1
7Segment Display
VCC1P8
R343
10K
CPU_RESET_n
PB4
CPU Reset
DNI
C714
1u
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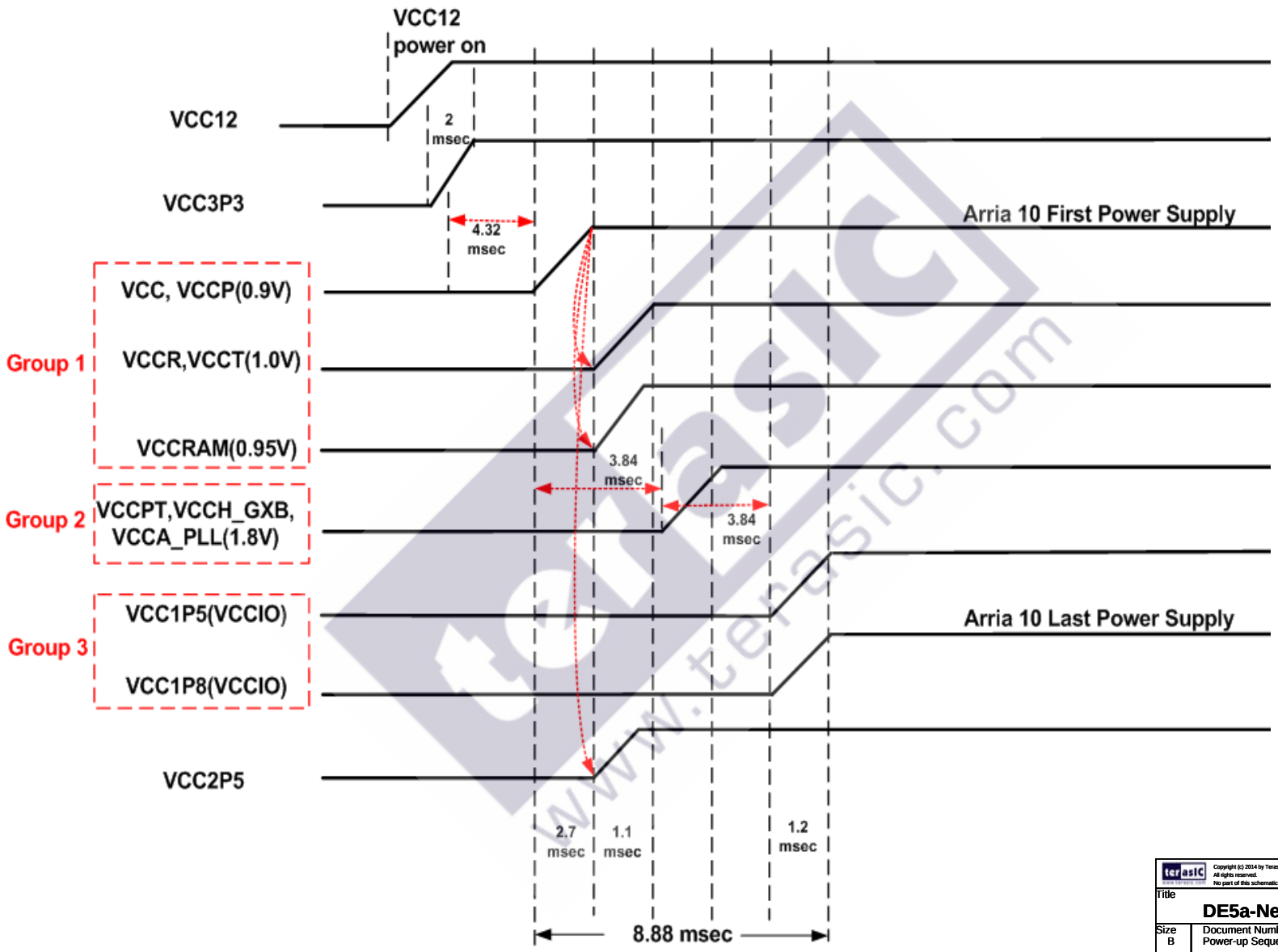
Title
DE5a-Net Board
Size
B
Document Number
RS422, Button, Switch, User LED, 7-segment
Rev
C
Date:
Friday, June 03, 2016
Sheet
35
of
42

Arria 10 Power-up Sequence Design Diagram

The power-down sequence is the reverse of the power-up sequence



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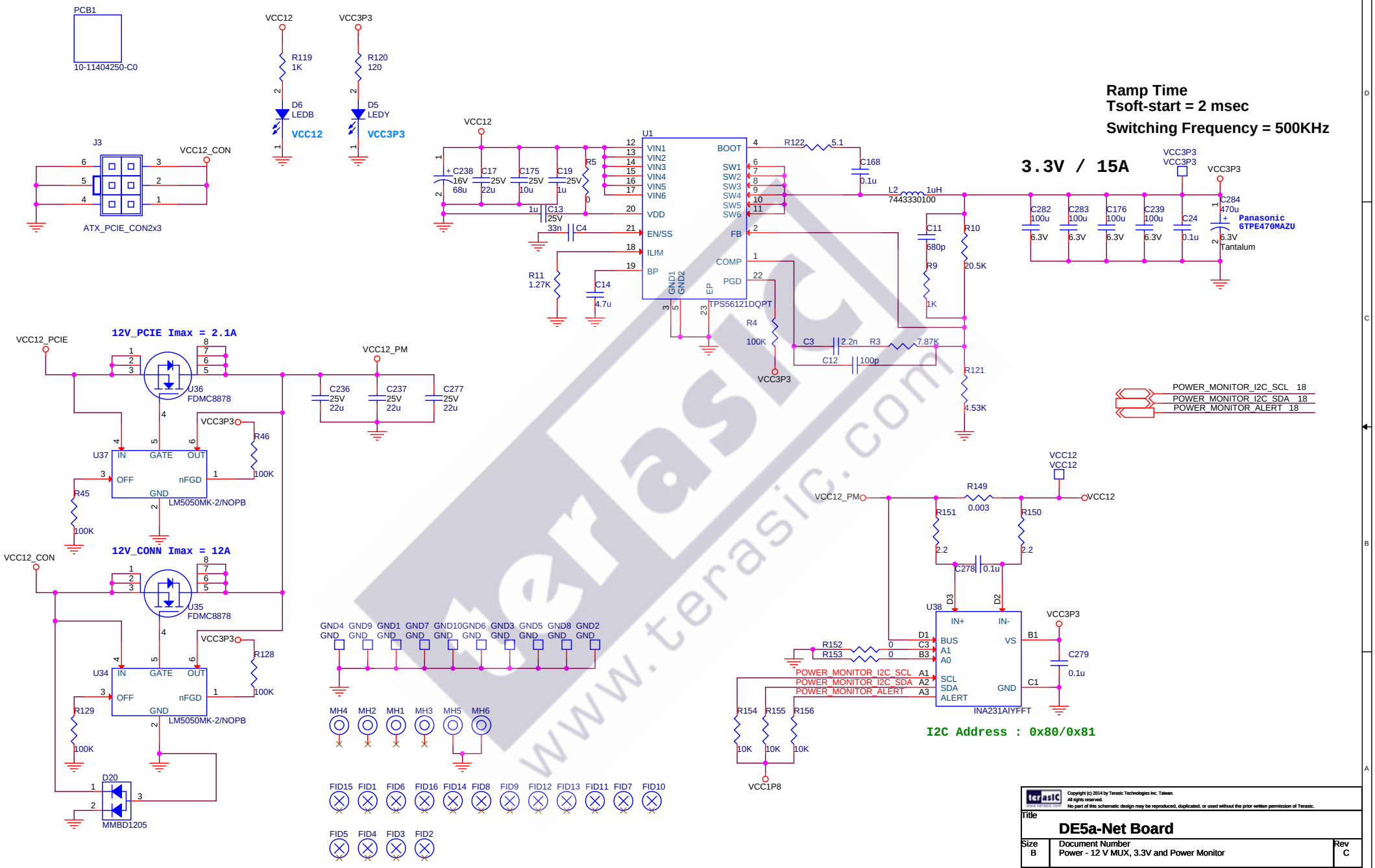
Title
DE5a-Net Board

Size	Document Number	Rev
B	Power-up Sequence	C

Date: Tuesday, May 24, 2016 Sheet 36 of 42



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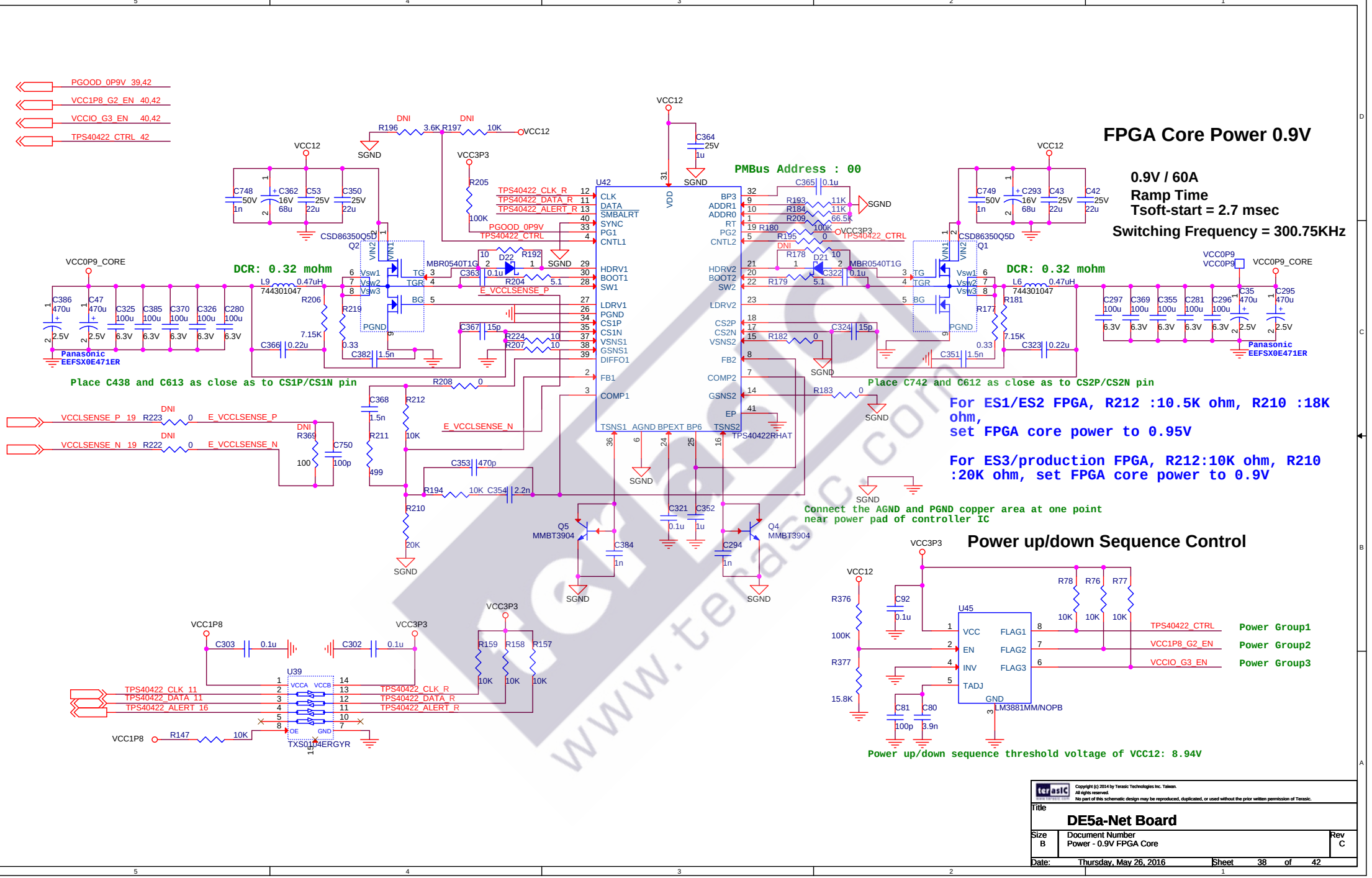
Title
DE5a-Net Board

Size	Document Number	Rev
B	Power - 12 V MUX, 3.3V and Power Monitor	C

Date: Thursday, May 26, 2016 Sheet 37 of 42



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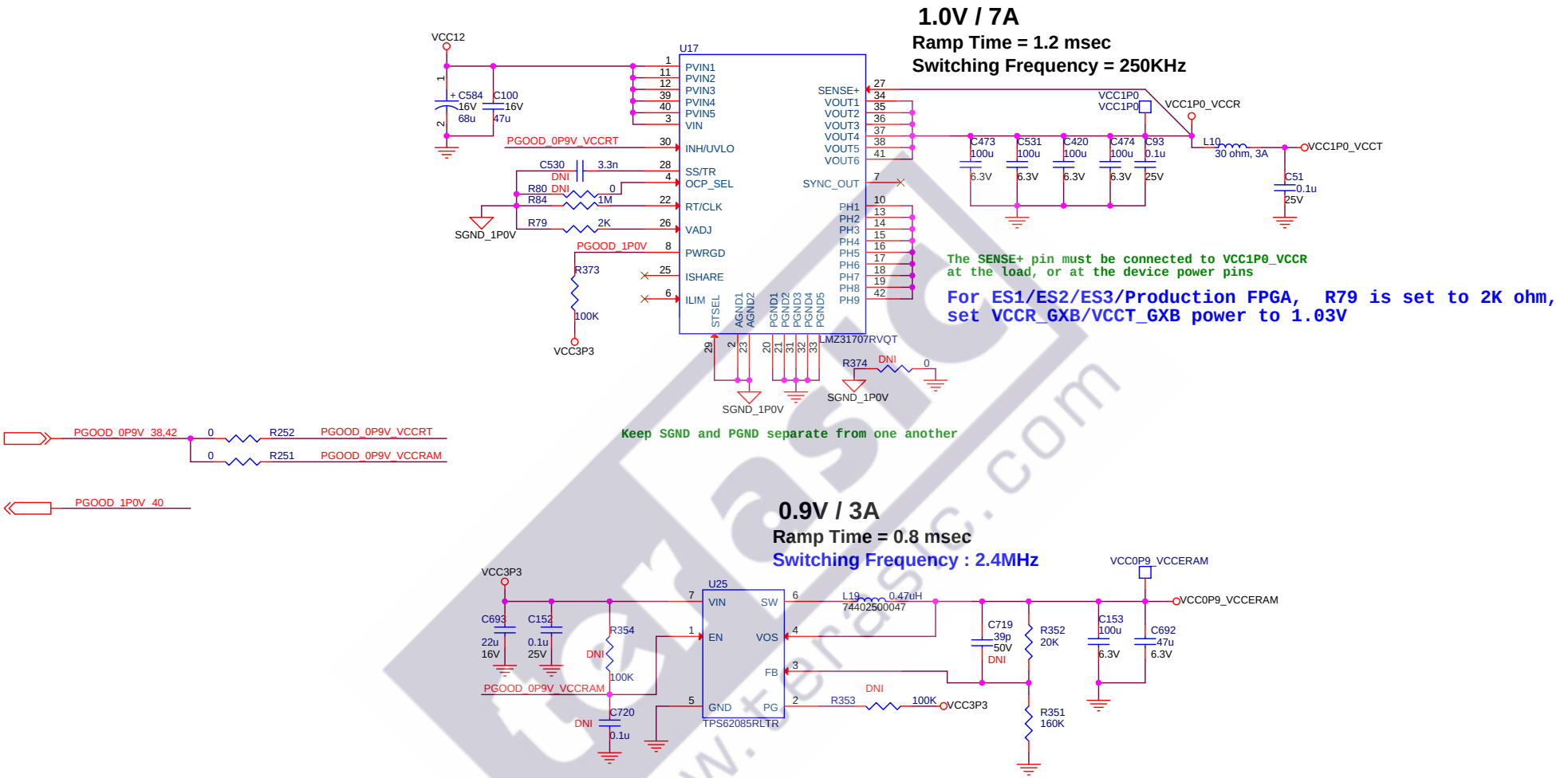
Title
DE5a-Net Board

Size	Document Number	Rev
B	Power - 0.9V FPGA Core	C

Date: Thursday, May 26, 2016 Sheet 38 of 42



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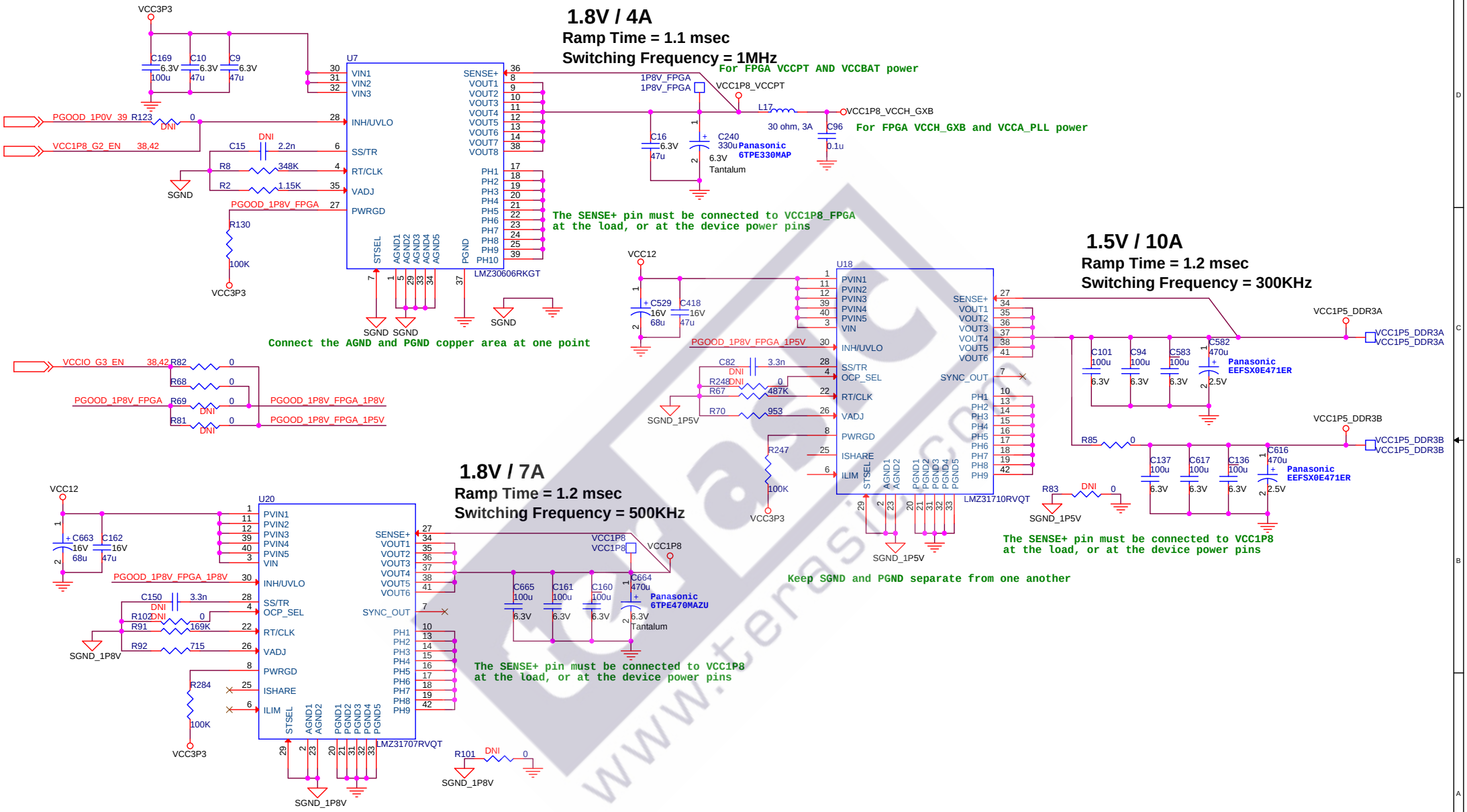
Title
DE5a-Net Board

Size	Document Number	Rev
B	Power - 0.9V (VCCERAM) and 1.03V	C

Date: Thursday, May 26, 2016 Sheet 39 of 42


1.8V / 4A
Ramp Time = 1.1 msec
Switching Frequency = 1MHz
For FPGA VCCPT AND VCCBAT power
For FPGA VCCH_GXB and VCCA_PLL power
The SENSE+ pin must be connected to VCC1P8_FPGA at the load, or at the device power pins
Connect the AGND and PGND copper area at one point
U7
LMZ30606RKGT
1.5V / 10A
Ramp Time = 1.2 msec
Switching Frequency = 300KHz
U18
LMZ31710RVQT
The SENSE+ pin must be connected to VCC1P8 at the load, or at the device power pins
Keep SGND and PGND separate from one another
1.8V / 7A
Ramp Time = 1.2 msec
Switching Frequency = 500KHz
U20
LMZ31707RVQT
The SENSE+ pin must be connected to VCC1P8 at the load, or at the device power pins
Keep SGND and PGND separate from one another
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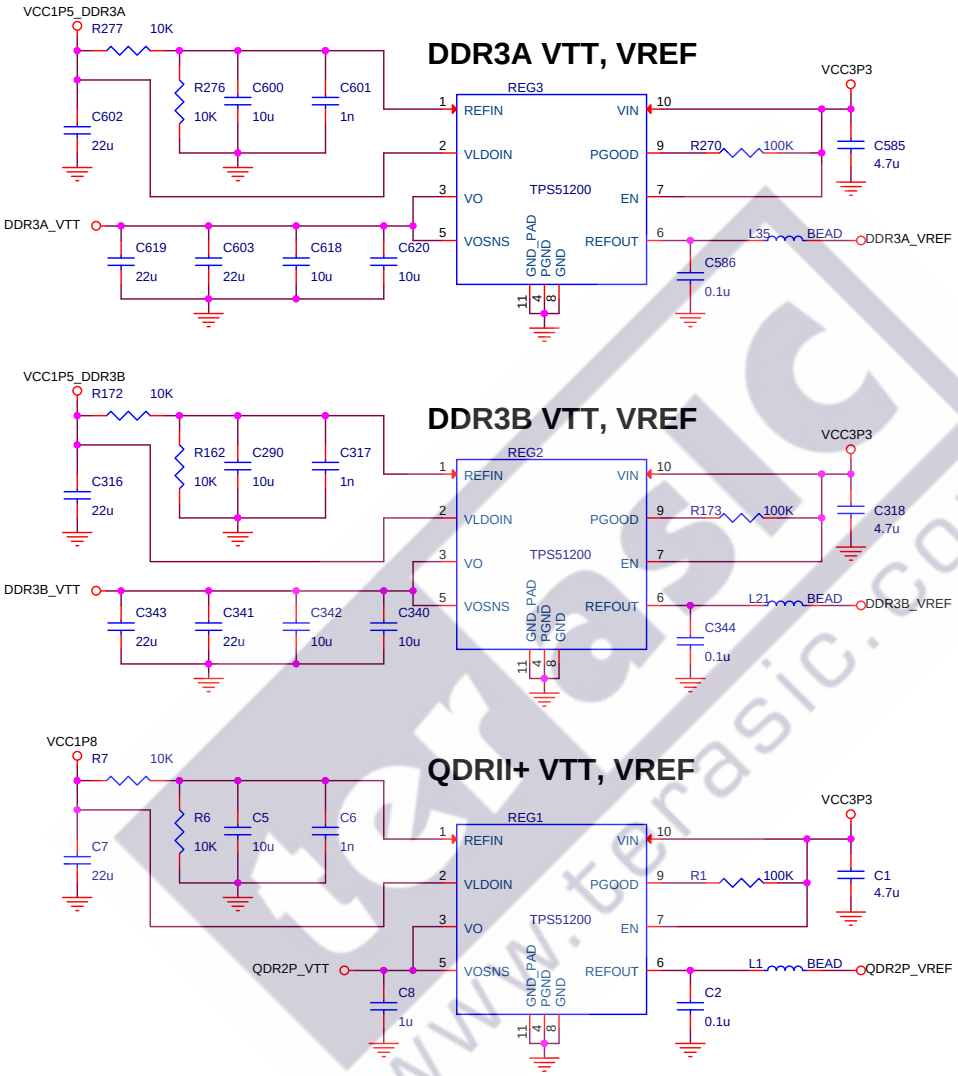
Title
DE5a-Net Board
Size B
Document Number
Power - 1.5V and 1.8V
Rev C
Date: Thursday, May 26, 2016
Sheet 40 of 42



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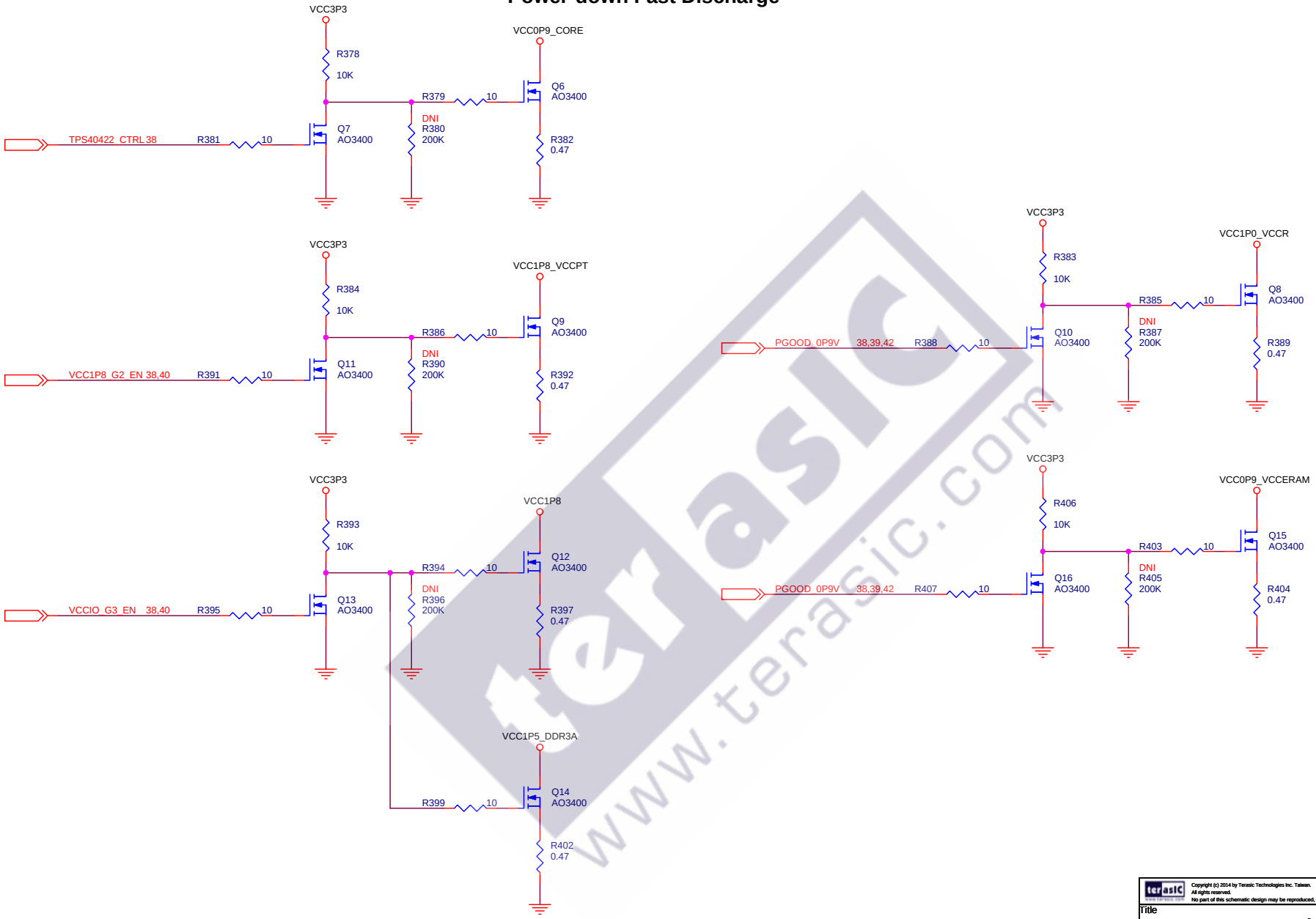
Title
DE5a-Net Board

Size	Document Number	Rev
B	Power - DDR3/QDRII VTT/VREF	C

Date: Tuesday, May 24, 2016 Sheet 41 of 42

Power-down Fast Discharge



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Title
DE5a-Net Board

Size	Document Number	Rev
B	Power-Down Discharge	C

Date: Thursday, May 26, 2016 Sheet 42 of 42