

REBL Nanowriter: Reflective Electron Beam Lithography

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ABSTRACT

REBL (Reflective Electron Beam Lithography) is being developed for high throughput electron beam direct write maskless lithography. The system is specifically targeting 5 to 7 wafer levels per hour throughput on average at the 45 nm node, with extendibility to the 32 nm node and beyond. REBL incorporates a number of novel technologies to generate and expose lithographic patterns at estimated throughputs considerably higher than electron beam lithography has been able to achieve as yet. A patented reflective electron optic concept enables the unique approach utilized for the Digital Pattern Generator (DPG). The DPG is a CMOS ASIC chip with an array of small, independently controllable cells or pixels, which act as an array of electron mirrors. In this way, the system is capable of generating the pattern to be written using massively parallel exposure by ~1 million beams at extremely high data rates (~ 1Tbps). A rotary stage concept using a rotating platen carrying multiple wafers optimizes the writing strategy of the DPG to achieve the capability of high throughput for sparse pattern wafer levels. The exposure method utilized by the DPG was emulated on a Vistec VB-6 in order to validate the gray level exposure method used in REBL. Results of these exposure tests are discussed.

Keywords: Ebeam, direct write, rotary stage, DPG, maskless, lithography, TDI, gray level, reflective electron optics

1. INTRODUCTION

Electron Beam Lithography (EBL) is well known to produce excellent resolution, good line edge roughness (LER) and good line width roughness (LWR) at the cost of throughput. The cost paid by throughput is because the electron dose must be high enough to mitigate the statistical effects of the electron beam (shot noise) and of the resist and developing process, to achieve an acceptable LER/LWR. Unfortunately, with increased beam current comes increased beam blur as a result of the electron-electron coulomb interaction^{1, 2} within the beam. Presently, it can take many hours to expose a wafer level using EBL systems. The REBL (Reflective Electron Beam Lithography) Nanowriter has the potential to break through the traditional performance/throughput tradeoff and achieve economically attractive throughputs while maintaining the advantage of maskless lithography.

EBL has for many years tried to become a major competitor in the lithographic market but has not succeeded in any meaningful way outside certain specialized markets. Mask making³ is the most notable case. Another is high resolution lithography and personalization for specialized products^{4, 5}. Quick-Turn-Around of small lot manufacturing has also proven to be quite successful^{6, 7, 8, 9}. Two competing Electron Projection Lithography (EPL) programs for high throughput manufacturing, SCALPEL^{10, 11} and PREVAIL^{12, 13, 14, 15} developed starting in the early 90's, did not utilize maskless technology and for various market reasons were never adopted by the semiconductor industry.

The high cost of masks for today's chip manufacturing has contributed greatly to a change in the market paradigm, together with technology improvements which have rendered the storage and transfer of large amounts of digital data routine. This has elevated electron beam maskless lithography to a viable technology status not only for the above mentioned specialized markets, but also for low volume manufacturing¹⁶ and perhaps some aspects of medium or higher volume manufacturing. One obvious application is the lithography of vias and contact levels in non-memory chips. These are well suited for EBL because these levels are generally very sparse, which means they can be written at very high throughputs using beam currents which satisfy the blur requirements of this lithography.

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The REBL Nanowriter, though its use of novel technology, promises higher throughputs than other electron beam approaches existing today. The REBL system has been architected to be almost entirely digital eliminating all settling times normally associated with analog control of beam deflection and/or shaping. The use of a rotating stage platen instead of the more typical oscillating linear stage, greatly reduces the stage overhead resulting in nearly a factor of two improvement in the total time to expose a wafer. The system is specifically targeting 5 to 7 wafers levels per hour on average at the 45 nm node with extendibility to the commercial mainstream lithography market for the 32-nm node and below. Throughput for dense patterned levels is limited by the beam current at the required blur. For very sparse levels the throughput is limited by other system capabilities such as the stage which is capable of achieving throughputs of up to 40 wph. In the remainder of this paper wph will be used for the unit of throughput. By definition, this is for 300 mm wafers and it is implied that it is for a wafer *level* per hour.

2. REBL NANOWRITER CONCEPT

Figure 1 depicts the system concept of the REBL Nanowriter. Six core technologies will be discussed in this paper: reflective electron optics, the Digital Pattern Generator, Time Domain Integration, gray tone exposure, the rotary stage, and optical wafer registration.

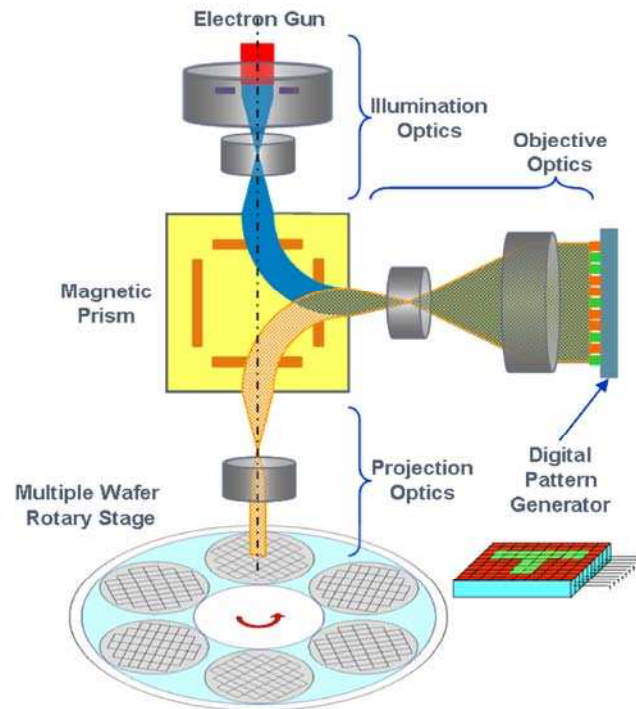


Figure 1. Block diagram of the REBL Nanowriter concept, showing how the reflective electron optics enables the use of a non-transmission DPG chip to modulate the reflected beam with the pattern to be written. This concept also employs the use of a rotary stage with multiple wafers which increases throughput and greatly decreases system disturbances during the exposure process.

Reflective electron optics enable the use of a low voltage Digital Pattern Generator (DPG) chip to independently control ~ 1 million beams for massively parallel exposure. This is unlike other ebeam maskless approaches which generally utilize a “transmission” aperture and blanker array to modulate the beam with the pattern to be exposed at the wafer. Using the CMOS DPG chip solves the daunting problem of how to switch a large number of beams

independently at high speed. One million beams are being implemented in the first system design but this number could be extended as the design evolves and if the system requirements dictate a need.

The DPG further provides for a rather sophisticated network of logic control that enables Time Domain Integration (TDI) & gray tone exposure without overburdening the data path and data transmission rate. TDI integrates the electron contribution of 248 beams in the TDI scan direction. This reduces the brightness requirements by over two orders of magnitude and distributes the exposure time over several microseconds, greatly reducing instantaneous resist heating effects. Gray tone exposure will be used to produce patterns with the required resolution, placement accuracy and pattern fidelity with a much finer incremental edge placement resolution than a larger size binary pixel would allow.

The rotary stage removes the throughput barriers normally associated with linear stages conventionally used in wafer lithography. This is especially important when a relatively small swath (few 100's of microns in height) is used during the exposure process. In addition, it behaves quasi-statically, imparting virtually no disturbances to the system during the writing process. In fact, it is self-stabilizing. One could greatly reduce the demands on a linear stage by adopting a very large swath height, that is, expose a very large area with each pass of the stage. This was expressly ruled out during the concept and architectural phase of the REBL program because it was considered much more difficult to maintain beam calibration over such a large area during the exposure process. The exposure of a large swath height at greatly slower stage speeds, also produces heating effects in the wafer which can significantly alter the beam to beam calibration.

REBL uses optical wafer registration to acquire registration marks on the wafer at the very high speeds required of a high throughput EBL system. This approach does not expose the resist over the mark area, avoiding the destruction of the marks during processing and the subsequent added terms in the error budget. Global wafer distortions, such as those resulting from wafer heating by the electron beam, are virtually eliminated through this technique. It is desirable to use marks already established in IC manufacturing to better integrate with the manufacturing process and also to better adapt to mix and match lithography.

3. REFLECTIVE ELECTRON OPTICS

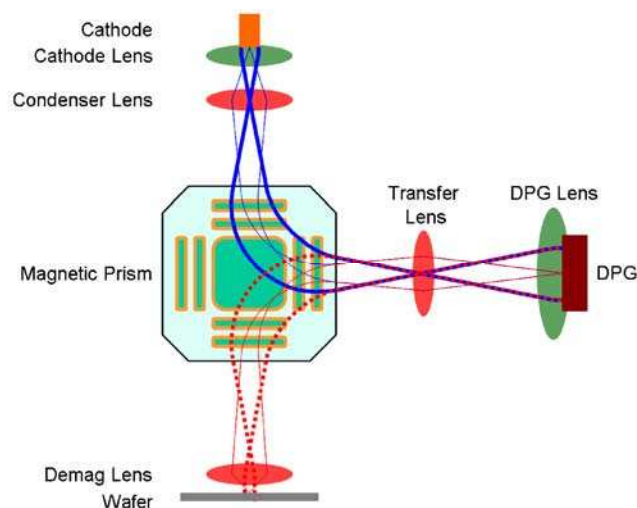


Figure 2. Ray diagram of the REBL Reflective Electron Optics. The blue rays indicate the illuminating beam from the gun to the DPG. The red rays indicate the modulated reflected beam from the DPG to the wafer.

The electron optics ray diagram of the REBL Nanowriter is shown in figure 2. A large area cathode of relatively low reduced brightness ($B_r < 10^4 \text{ Am}^{-2}\text{sr}^{-1}\text{V}^{-1}$) generates an illuminating electron beam (the blue solid ray trace). The cathode lens forms a crossover at the center of the condenser lens. The condenser lens forms an image of the source at the virtual center of the magnetic prism. The virtual center of the prism refers to the point on a 45° diagonal through the physical center of the prism which is intersected by the curved optical axis. The prism is setup to bend the optical axis exactly 90° and establish the focal lengths in the x and y planes to be equal, and with equal magnifications in the x and y axes. When these three conditions are satisfied, the prism behaves as a 1:1 imaging lens, imaging the crossover from the center of the condenser lens to the center of the transfer lens. The transfer lens in turn images the source image at the virtual prism center onto the DPG through the DPG lens.

The electrostatic DPG lens serves a dual purpose: it forms a virtual image of the crossover at infinity, and it decelerates the electrons to within a few volts of the cathode potential. When a mirror is turned “on” at the DPG it will reflect electrons from the illuminating beam. These reflected electrons are re-accelerated back toward the prism as they travel through the accelerating field of the electrostatic DPG lens.

A crossover is formed at the center of the transfer lens by the DPG lens. The transfer lens images the DPG at the virtual center of the prism but along the diagonal 90° clockwise from the first image formed on the illuminating arm. The purpose of the prism is to act as a 1:1 lens and to separate the illuminating beam from the projection beam by using the Lorentz Force which applies a force according to $e(\mathbf{v} \times \mathbf{B})$. Because \mathbf{v} is a vector quantity the electron beam is bent in one direction coming from the gun and going to the DPG. The reflected electron beam, going in the opposite direction is therefore, bent in the opposing direction. The prism thus, bends the reflected beam (the red dashed ray trace) away from the gun to project it onto the wafer. The prism also forms a crossover at the back focal plane of the demagnification lens, while the demagnification lens focuses the DPG image from the virtual center of the prism onto the wafer plane.

The demagnification of the present column design is fixed at 50x but will be increased as the column design evolves to allow smaller pixel sizes. The DPG pixel pitch may also decrease from its current value of $1.5 \mu\text{m}$ as the DPG design evolves. The first REBL system and column, shown in figure 3, produces a pixel pitch at the wafer plane of 30 nm. This pixel size is obviously too large for 45 nm node lithography and beyond, however, it was set by constraints imposed by the current prism design.

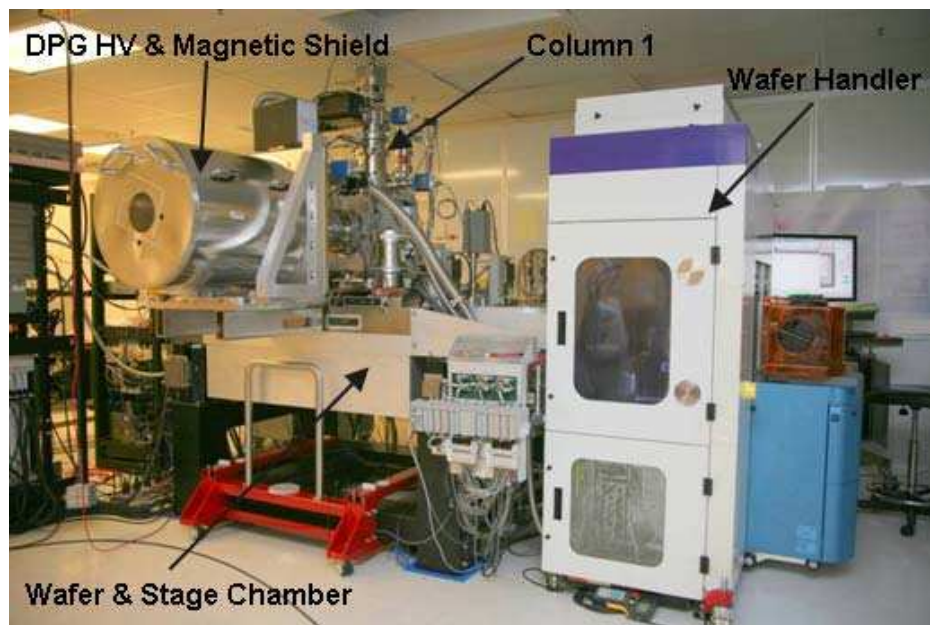


Figure 3. The first REBL system and Column. This system uses a linear stage and automatic 200 & 300 mm wafer loading.

An exposure model was developed incorporating the relationships between exposure dose, CD control, process latitude, gray tone dose, proximity effect and LER/LWR parameters. This exposure model was used to estimate the requirements for the pixel size to CD ratio and the beam blur to pixel size ratio. This model is discussed further in the following sections. From this model it was estimated that a pixel pitch at the wafer of approximately 15-20 nm will be necessary for the 45 nm node and 10-14 nm will be needed for the 32 nm node with a beam blur between 1 and 1.5 times the pixel size.

4. ROTARY STAGE

Consider the linear stage case in which a swath with height H is written at constant speed over the area of the wafer. At the end of each written swath a cosine acceleration ramp is applied to slow the stage to zero speed and then re-accelerates it back to the writing speed in the reverse direction. This is repeated for each swath until the entire wafer area is written at a constant speed. For the case where acceleration is the limiting factor in throughput, one can solve for the minimum time to write a wafer by using the optimum speed for a given turn around acceleration, a , given by equation 1.

$$t_w = \frac{4}{H} \sqrt{\frac{\pi D_w^3}{8a}} \quad (1)$$

Where: D_w is the diameter of the wafer. Rearranging this equation, using the throughput in wafers per hour T_{wph} and solving for the peak cosine acceleration in G 's is given by equation 2.

$$G_{\cos} = \frac{\pi^2}{9.8} \left[\frac{D_w^3}{H^2 (3600/T_{wph})^2} \right] \quad (2)$$

For simplicity, this equation only considers the stage and does not include any overhead terms for load/unload time and calibration/registration times and assumes no limitations to writing time based on beam current and resist sensitivity.. In other words, this is a best case scenario for a linear stage.

A plot of constant throughput (in wph) curves is shown in figure 4. A swath height of 100 microns, which is in the region of interest for REBL, would require a linear stage turn around acceleration of over 20 G 's for a throughput of 10 wph. These accelerations are way beyond any known linear stage technology that is suitable for lithography. This is neither practical nor maybe even possible, while maintaining lithography performance. Therefore, in order to reach the throughputs required by the REBL Nanowriter we required a different approach. That approach is the rotary stage concept.

A rotary stage renders the dynamic problem insignificant even at peak writing speeds greater than 10 wph throughput, provided that the rotary stage can accommodate 5 or more wafers. The rotary stage can be balanced to the point where the main dynamic force is imbalance due to weight mismatch of wafers. This small imbalance is easily countered by feed-forward compensation, leaving only a small residual to the beam feedback control.

The REBL Nanowriter will expose batches of wafers by moving them under the electron beam on a rotating stage. This technique eliminates the frequent reversals of direction and percussive accelerations associated with a high-speed linear stage. A throughput of 10 wafers per hour would require a constant linear speed of the wafer relative to the electron beam of ~ 2.5 m/s. Simultaneously, the rotating stage assembly traverses laterally on a linear stage at a relatively slow speed of ~ 0.15 mm/s. The apparent path of the image of the DPG across the circle of wafers is therefore a spiral.

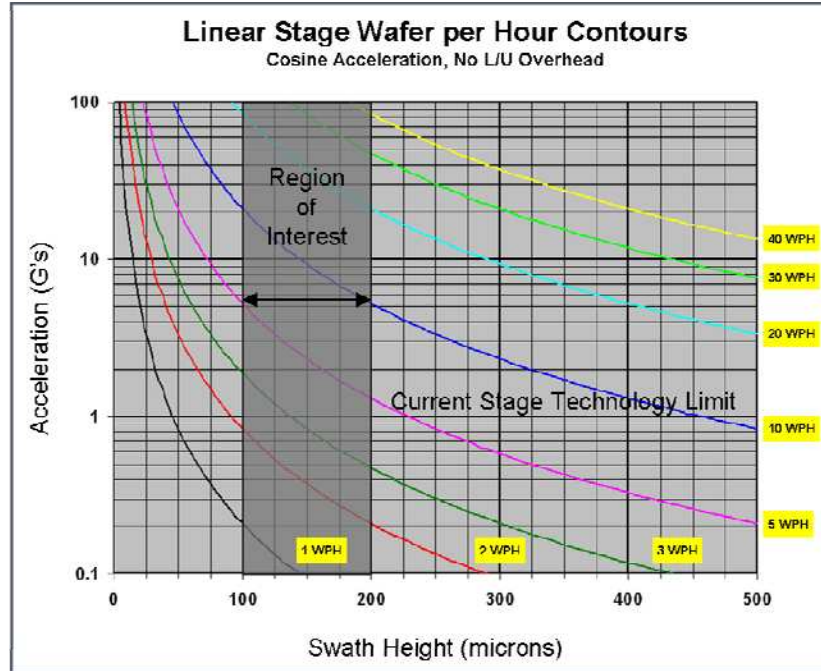


Figure 4. Graph showing iso-throughput curves for a linear stage, plotting the stage turn-around acceleration vs. the swath height. The REBL Nanowriter region of interest for the swath height is also shown.

Figure 5a shows the concept design for a rotary stage loaded with six wafers. The number of wafers, N_w , the stage will hold per batch is a parameter which affects the system performance. A batch size of six wafers was chosen as a reasonable compromise for the first rotary stage prototype which is shown in figure 5b and is now under test. This batch size may change in the future when integration to actual Fab conditions is taken into consideration.

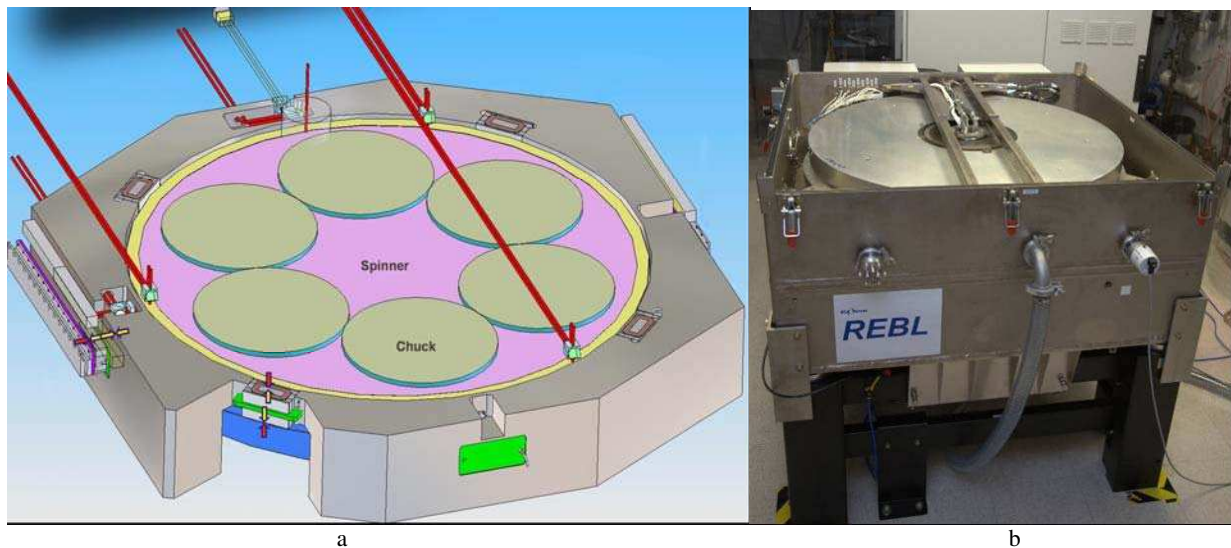


Figure 5. a) Concept design of a rotary stage using a six wafer batch. b) The prototype rotary stage installed in a test stand used to characterize the rotary stage performance.

The wafers lie in a horizontal plane and the stage rotates about an axis which is parallel to the axis of the column. Exposure on the rotary stage proceeds in a spiral path with a pitch nearly equal to H , starting from the outer diameter of the wafers and moving to the inner diameter of the wafers. The swath pitch is slightly smaller than H because there is a few percent overlap of adjacent swaths.

The size of the DPG patterned image at the wafer is dependent on the DPG pixel size and the final demagnification used. For the purpose of discussion consider an image height of 100 μm and a width of 6.2 μm at the wafer. This will write on a circular path (actually a spiral) as described above and results in three errors, two position errors and a dose error, because the swath describes a curved path instead of a straight path. The radial position error for the minimum radius of the spiral (worst case) is negligible at ~ 0.03 nm and the tangential position error is less than 1 nm (some of which can be corrected) for the rotary stage example with 6 wafers. The dose error is less than 0.06%.

As a simple illustration of throughput for the average wafer consider the case that half of the wafers are metal at 50% coverage and half are contact/via at 20% coverage. A throughput analysis using the results from the exposure model has shown that a throughput of ~ 2 wph for metal and 10 wph for vias with lithographic fidelity for the 45 nm node is achievable with about 10 μA of beam current delivered to the wafer and 18 $\mu\text{C}/\text{cm}^2$ resist sensitivity.

An equation for the speed (or velocity) of the rotary stage surface relative to the electron beam for a given throughput is shown in equation (3).

$$v_{wph} = \frac{\pi}{3600} \frac{D_w \cdot D_{ave}}{H} \frac{T_{wph}}{N_w} \quad (3)$$

Where: D_{ave} is the average swath diameter and N_w is the number of wafers contained on the rotary stage per batch.

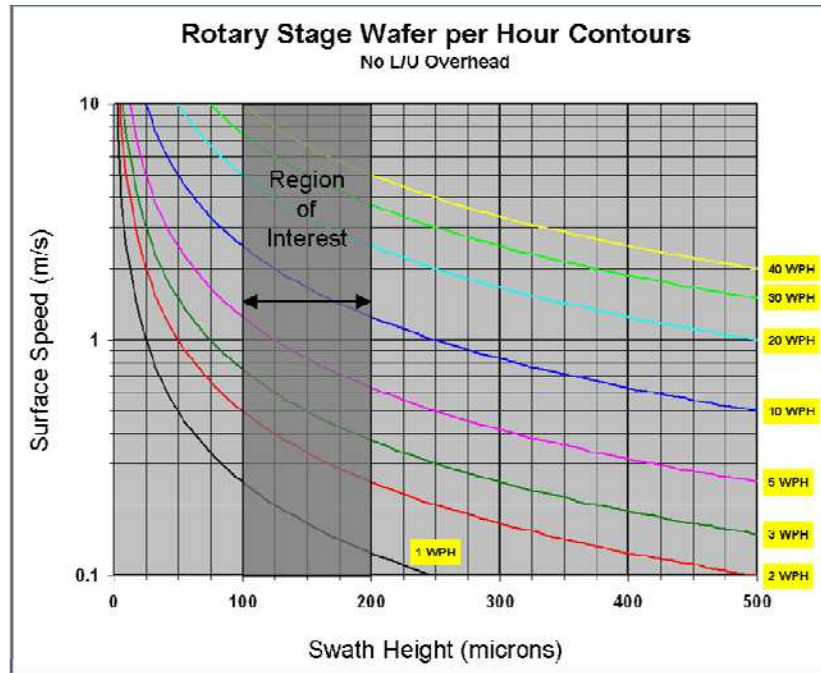


Figure 6. Graph showing iso-throughput curves for a rotary stage, plotting the stage surface speed vs. the swath height. The REBL Nanowriter region of interest for the swath height is also shown.

From this expression it can be shown that for a throughput of 10 wph, the rotary stage will require a speed of 3.4 m/s. Equation 3 is plotted in figure 6 for various contours of constant throughput (in wph). The design spec for the REBL rotary stage is for a surface speed up to 10 m/s. This would produce a throughput of ~40 wph provided the beam current, resist sensitivity and blur are commensurate with the lithography requirements.

The beam current required to sustain throughput is given by equation (4)

$$I_{beam} = H \cdot v_{wph} \cdot S_{resist} \cdot \%Coverage \quad (4)$$

Where: S_{resist} is the resist sensitivity and $\%Coverage$ is the per cent of the area to be written with a pattern. For the via and metal levels described above a throughput of 10 wph and 2 wph respectively using a resist sensitivity of $18 \mu C/cm^2$ requires a beam current of $10 \mu A$ (no load/unload or calibration overhead is considered in this value). The value of $18 \mu C/cm^2$ is a target set by contract requirements and has been established as the resist sensitivity of record for the REBL program. The roadmap for the REBL system is to deliver up to $11 \mu A$.

5. DIGITAL PATTERN GENERATOR

The heart of the maskless patterning system for the REBL Nanowriter is the Digital Pattern Generator (DPG). The DPG is a CMOS ASIC chip with an array of small, independently controllable metallic cells or pixels, which act as an array of electron mirrors exactly analogous to the DLP® technology from Texas Instruments used in projection television.

REBL's reflective technology involves illuminating an array of small electrodes on the DPG with low-energy electrons which have been decelerated by the DPG lens to ~ 1 eV. A small negative bias of 1-2 volts is applied to the entire mirror array, creating sufficient repulsive force in the region immediately above the electrodes of this array to reflect the electrons which illuminate it back into a region where the DPG lens re-accelerates them away from the DPG. A small positive potential when applied to some electrodes absorb the portion of the illumination beam that strikes them. The electron image is thus, "dark" (i.e., there are no electrons reflected) at the points in the image corresponding to absorbing electrodes, and "bright" at the points corresponding to reflecting electrodes. The pixels are digital, they are either on or off.

REBL is intended to be a very high throughput system and the data rate for sending fully expanded pixel data to the DPG required to support the desired throughput can be upwards of 20 Terabits/sec (Tbps). It is clear that with this data rate, a data compression method compatible with REBL's rotating-stage writing strategy is required. A data compression scheme has been devised for REBL that makes direct use of small proximity corrected pattern elements, or "characters", which are encoded through a lookup table that can be dynamically down loaded to the DPG. Effective use of this scheme is a central theme of REBL's data processing. With data compression, printing sparse levels (e.g., contacts and vias) can be accomplished at the needed throughput with only ~ 1 Tbps of compressed data sent to the DPG. Denser levels will be printed at lower speed, due to beam current limitations; so this same 1 Tbps can support the printing of arbitrary device levels of almost any pattern coverage.

6. TIME DOMAIN INTEGRATION & GRAY TONE EXPOSURE

Reflection of electrons from a static arrangement of potentials on electrodes provides a 'binary' image: each electrode either reflects the electrons illuminating it, or it doesn't. However, composing a device pattern using a binary exposure would require the demagnified pixel size to be comparable to the finest pattern placement resolution needed. This approach would impose unrealistic requirements on the DPG structure, data path, and on the resolution of the electron optical system.

To avoid these complications, REBL employs a method of gray-toning¹⁷ to produce patterns with the required resolution, placement accuracy and pattern fidelity. Gray-tone patterning takes advantage of the high contrast of modern, chemically amplified resists. Numerical simulations using the exposure model have shown that a 5-bit

linear gray scale (0-31) will be sufficient for REBL's purposes. For extendibility, this could be increased to a 6-bit gray scale with a small increase in the data rate to the DPG.

To synthesize the required gray tones of exposure from a binary electron image, REBL uses a technique called Time Domain Integration (TDI). The DPG is constructed with a 2-dimensional array of mirror electrodes (pixels). The array is 4096 pixels high which defines the width of the writing swath by 248 pixels which define the number of pixels integrated in the TDI direction resulting in the gray tone dose. This produces an array of 1,015,808 individually controlled beams. At exposure time, the wafer being patterned is moved smoothly across the field of the imaging optics. As any given pixel location on the wafer passes under the image of the DPG, it is sequentially exposed to reflected electrons from a specific row of 248 DPG pixels which are individually controlled and are turned "on" or "off" according to the gray level dose required. As the wafer moves, the pattern of pixels on the DPG shifts so that the electrons reflected from successive pixels in each row of the DPG fall onto the same spot on the wafer.

The DPG mirror array is segregated into bit blocks in such a way as to produce 5-bit gray tones for exposure. These gray tones are constructed from binary pixel exposures using the TDI method by integrating the assigned dose at each pixel at the wafer from the appropriate combination of pixels at the DPG determined by the 5-bit gray tone.

The width of the DPG is 248 total pixels (with 8-fold pixel redundancy) partitioned into bit blocks as follows:

- For bit 4 (the MSB), there are 2 bit blocks, each 64 pixels wide.
- For bit 3, there are 2 bit blocks, each 32 pixels wide.
- For bit 2, there are 2 bit blocks, each 16 pixels wide.
- For bit 1, there are 2 bit blocks, each 8 pixels wide.
- For bit 0 (the LSB), there is one bit block 8 pixels wide.

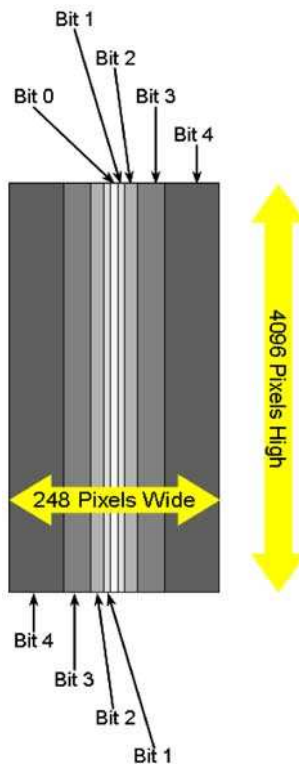


Figure 7. Layout of DPG pixel bit blocks used for gray tone dose control. The TDI and wafer scan direction is parallel to the "248 Pixels Wide" arrow in the figure.

The bit blocks (figure 7) are arranged symmetrically about the vertical midline of the DPG in order to minimize errors introduced by the curved path of the swath. The curved swath path is a result when using the rotary stage. Each bit of each gray level is displayed by being shifted across the corresponding bit blocks, in synchronous with the wafer motion.

Figure 8 illustrates how the total dose is accumulated as the pattern moves across the DPG integrating the pixel dose from the 5 bit blocks. The REBL system synchronizes the electronic movement of the pattern across the DPG with the physical movement of the silicon wafer by the stage.

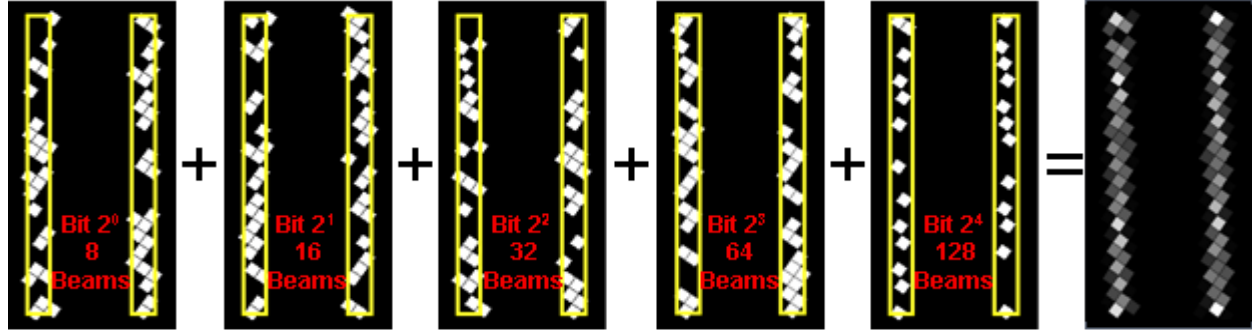


Figure 8. The TDI exposure method showing the pixel dose contribution from each of the 5 bits resulting in the integrated gray level exposure which defines the edge placement of the desired pattern.

Image blur, the point-spread function of the electron optical system, plays an important role in gray-tone patterning. As mentioned above, the contours along which the energy deposition profile in the resist crosses the development threshold become resist pattern edges as a result of resist development. REBL relies on fine gradations in the energy deposition profile to control the position of the developed contour. The slope of this profile depends principally on the blur of the electron-optical projection system. Too little blur, and fine control of pattern edges is thwarted: pixel edges, rather than gray tones, control the development contour. Too much blur and the ability of the system to produce fine patterns with stable CD's is impaired. The optimum beam blur is estimated by the exposure model to be between 1 and 1.5 times the pixel size. The exposure model considers the electron optical beam blur, gray toning and the resist blur.

7. PIXEL DOSE ASSIGNMENT

Early in the REBL project it was desirable to test the REBL exposure method before the very large investment necessary for designing and fabricating the DPG chip was made. Simulation tools were developed to investigate gray scale dose assignment and the expected lithographic quality using the REBL gray scaling strategy. With these tools it is possible to vary total printing blur (including resist effects), pixel size, pattern angles with respect to the pixel grid, maximum dose, and other parameters while observing edge roughness, CD control and dose edge slope. The edge slope is the slope of the dose with respect to position on a line perpendicular to the pattern edge.

The model uses the standard double Gaussian approximation for electron scattering to approximate the exposure at each point due to the assigned doses of all the pixels as shown in equation 5.

$$I(r) = \frac{1}{\alpha^2(1+\eta)\pi} \left[\exp\left(-\frac{r^2}{\alpha^2}\right) + \frac{\eta \cdot \alpha^2}{\beta^2} \cdot \exp\left(-\frac{r^2}{\beta^2}\right) \right] \quad (5)$$

Where: $I(r)$ is the exposure at radius r from the incident beam, α is the forward scattering radius (sigma), β is the backscattering radius (sigma), and η is the backscatter coefficient.

For the purpose of electron optics considerations, we have chosen to define blur as the 20% to 80% rise distance as the beam is scanned across an edge. This gives a sigma value of about blur/1.68 because REBL uses 50 kV and thin resist, also it is assumed that beam blur and resist effects (or “resist blur”) are the major contributors to the alpha term. The backscatter radius is quite large at 50 kV, so it was assumed that the pattern was imbedded in a large area of average exposure density equivalent to the pattern itself. This causes the backscattered electron dose to behave like a constant background dose. Finally, a simple threshold model for the resist development was assumed.

In order to optimize dose assignment, a linear programming problem was formulated which uses the Simplex method. The short comings of this approach are well known: The task is computationally expensive, it does not scale well and convergence is not guaranteed. It was determined, however, that this would be adequate for a research tool. Production-worthy algorithms are under development which will have much greater computational efficiency and speed.

The implementation requires that we define constraints and a linear cost function to be minimized by the dose assignments. The constraints are set by defining control points on the edges of the desired pattern and on the interior of the pattern. The edge control points must receive a dose within a small tolerance of the resist development threshold, so that the resulting pattern edges will be placed at those points. The interior points were intended to make sure that the interior of the patterns are also exposed. In practice, these were set as high as possible to maximize the slope of the dose profile at the edges. This maximizes CD control and minimizes edge roughness. Figure 9 shows the pixels and control points, assigned pixel dose and the resulting integrated dose with beam blur for lines and spaces having a half pitch (HP) of 60 nm.

The cost function is the sum of the weighted doses for all pixels in the pattern. The weight of each pixel is chosen depending on whether the pixel is entirely in the interior of the pattern, on the border of the pattern or outside any pattern, with the weight increasing correspondingly. In other words, it is “cheap” to put dose inside a pattern, more expensive to place it on the edge of a pattern, and very expensive to place dose outside the patterns.

In operation, the software assigns doses to pixels, and uses closed form integrals to evaluate the dose at each of the control points. The software iterates using the Simplex method to obtain first a feasible solution, where all the constraints are satisfied, and then an optimal solution, where the cost is minimized.

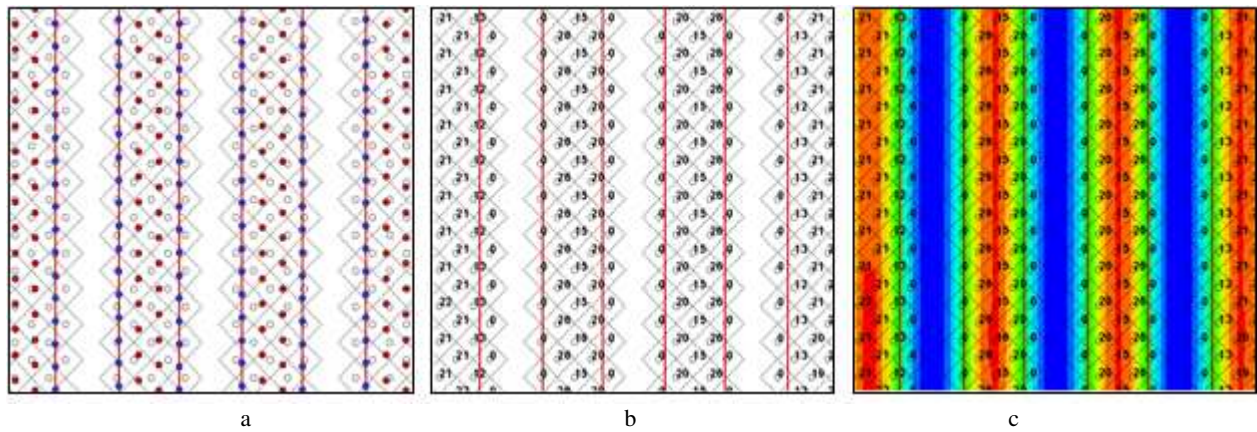


Figure 9. a) Lines to be exposed showing pixels and control points. b) Dose assignments for each pixel. Note that the pixels are rotated 45 degrees with respect to the lines to be exposed. c) Resulting dose with a beam blur of 34 nm, pixel size of 24 nm producing line/space with 60 nm HP.

Once a solution is found, a full convolution is calculated to obtain a two dimensional picture of the resulting exposure doses, and to obtain “cross-sections” of the exposure dose. The slope of these cross sections is examined at the line edges to determine the exposure latitude as a measure of the critical dimension control. Exposure latitude is the dose change allowed before the line width moves outside the CD control requirement.

8. EMULATING THE REBL EXPOSURE METHOD

More recently, the exposure modeling tools have been used to generate dose assignments and emulated the REBL exposure method using a Vistec VB-6 Gaussian vector scan e-beam lithography tool. This turned out to be a somewhat challenging exercise.

A rectangle which is exposed with a single beam spot with a dose equivalent to the lowest gray scale dose was defined as dose “1”. For pixels with higher doses, this pattern was repeated multiple times. For the higher dose values, the dose “1” exposure was repeated in a pre-determined pattern within the pixel boundary in order to approximate the convolution of the beam blur with the finite pixel size. For example a dose of “30”, exposes the area of one pixel at the wafer with a dose of “1”, 30 times. This approach of emulating the REBL exposure method is shown in figure 10.

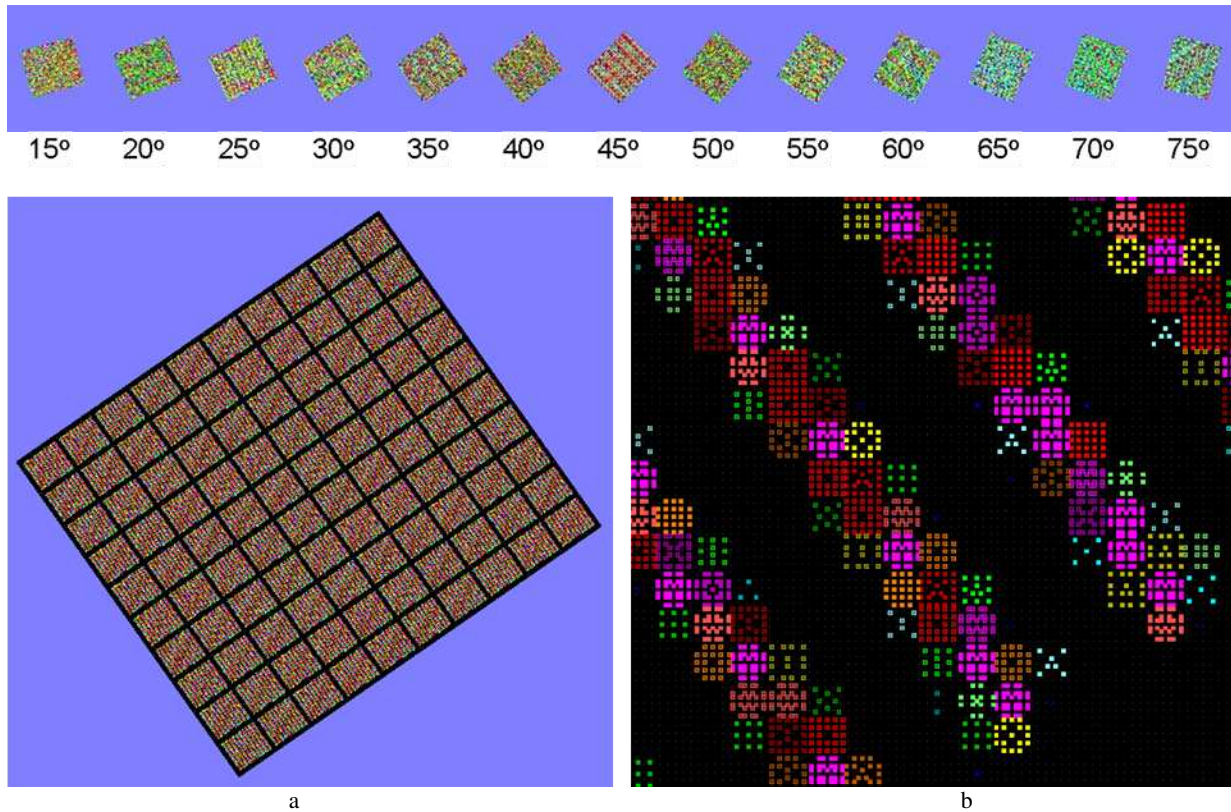


Figure 10. The top figure shows the 13 angles for which the array of 60 nm lines were exposed. a) Array of 60 nm HP lines. c) The pre-determined patterns within the pixel boundary for a few lines.

This strategy produced surprising good results on the initial attempt. The test exposures for lines and spaces with 60 nm half pitch were arrayed multiple times and exposed for line angles from 15-75 degrees. The purpose for exposing lines from 15-75 degrees was to reproduce the effect of the changing angle for the rotating stage. Figure 11a shows the total integrated pixel dose, 11b shows the convolution of the integrated dose and the beam blur and

11c is the resulting exposed resist image which was produced on the VB-6 Lithography tool. The exposures are surrounded with a “background” area which has the same average dose as the line/space arrays and extends for more than twice the backscatter radius. The pitch of the lines is chosen so that they do not fall at the same point on the pixel grid, but walk across the grid causing the gray level assignments to vary for each line. The lines appear quite uniform in width for a first exposure.

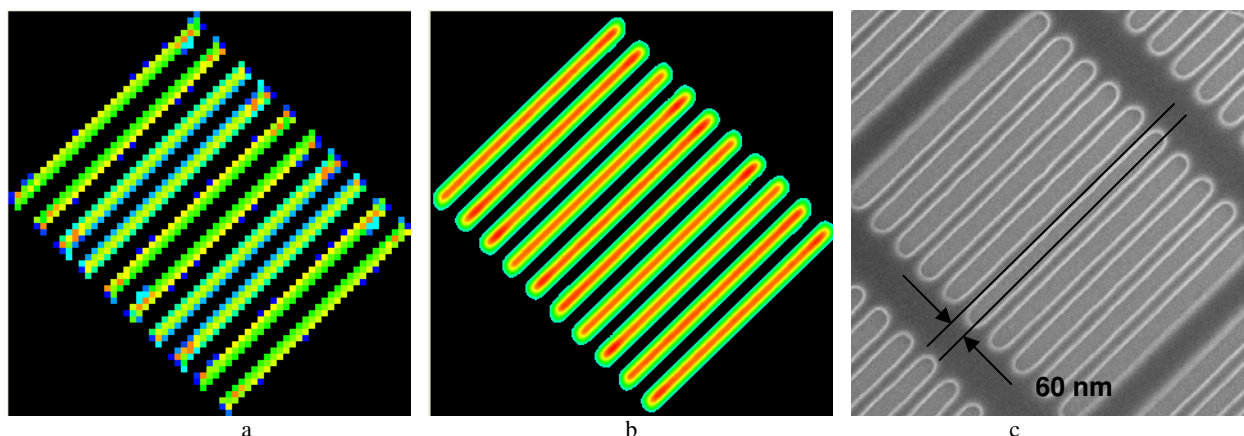


Figure 11. a) TDI Integrated gray level pixel dose. b) Beam Blur convolved with integrated pixel dose. c) Emulated exposure method using Vistec VB6 Ebeam Writer.

9. WAFER REGISTRATION

The Wafer Metrology System (WMS) is a system of sensors and associated control electronics and software that is responsible for measuring the wafer position and distortion and for maintaining the registration of the electron beam relative to the previously written wafer pattern.

The main disturbances that affect the writing accuracy include wafer rigid body motion errors resulting from stage control errors and residual vibrations, wafer distortion due to thermal input, and electron beam drift. The WMS control system relies on multiple sensors that measure multiple alignment marks on the wafer to high accuracy and precision at very high speeds.

The WMS extends the technology currently employed within the KLA-Tencor overlay products for wafer alignment and overlay metrology¹⁸ to the specific requirements of REBL.

The wafer alignment targets currently used in IC fab for overlay analysis are under investigation as a candidate for the REBL alignment marks. The marks need to be acceptable to the user and meet the size and process constraints. Using well understood targets, such as the lithography alignment marks or overlay marks employed today as part of the standard lithography process, is an advantage.

A critical aspect of the metrology system is the need to reference the measurement to the electron beam position. The WMS will acquire a set of special system alignment marks used to align the WMS with the electron beam and establish each wafer position and orientation during the first few revolutions as the stage ramps up to writing speed. The WMS tracks a large number (perhaps up to a few thousand per wafer) of alignment marks distributed across the wafer during the writing process.

Calibration targets specifically designed for accurate acquisition by the electron beam at writing speeds are located on the stage in between the wafers. These targets will be used to calibrate the electron beam to the optical sensors as often as once per wafer per revolution of the stage. This will provide a calibration update as frequently as every 10-20 ms.

10. SUMMARY

This paper has briefly reviewed the core concepts being developed for use in the REBL Nanowriter. Reflective electron optics enables the use of a very high speed CMOS ASIC chip called the Digital Pattern Generator. The DPG and writing strategy employ two technologies known as Time Domain Integration and gray tone exposure to achieve lithographic pattern placement with the proper dose for CD control. The TDI method of exposure also reduces the gun brightness requirements by more than two orders of magnitude relative to the brightness required by conventional probe electron beam systems. A rotary stage architecture is used to remove the barriers normally associated with linear stage acceleration and greatly reduce overhead time. Optical wafer registration combined with frequent calibrations to the electron beam will provide the registration accuracy and speed of mark acquisition needed for high throughput lithography.

Using these concepts makes the system appear as nearly “static”. The entire electron optics is a static imaging system. The rotary stage is quasi-static in behavior and self stabilizing compared to a linear stage. All high speed, large area analog deflection drivers have been eliminated. The one high speed element in the system is the DPG which is entirely digital. This is expected to greatly improve the REBL system’s noise immunity, which is generally a very troublesome issue for electron beam technology.

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REFERENCES

- [1] G. H. Jansen, "Coulomb interactions in Particle Beams," J. Vac. Sci. Technol. B **6**, 1977 (1988).
- [2] S. Berger, D. J. Eaglesham, R. C. Farrow, R. R. Freeman, J. S. Kraus, J. A. Liddle, "Particle-particle interaction effects in image projection lithography systems," J. Vac. Sci. Technol. B **11**, 2294 (1993).
- [3] L. R. Herriott, R. J. Collier, D. S. Alles, J. W. Stafford, "EBES: A practical electron lithographic system," IEEE Trans. Electron Devices **22**, 385-392 (1975).
- [4] G. L. Varnell, D. F. Spicer, A. C. Rodger, R. D. Holland, "High Speed Electron Beam Pattern Generation," Proc. 6th Int. Conf. on Electron and Ion Beam Science and Technology, R. Bakish, ed., San Francisco, CA, 97-110 (1974).
- [5] H. Kretz et al., "Integration of EBDW of one entire metal layer as substitution for optical lithography in 220 nm node microcontrollers," Microelectron. Eng. **85**, 792-795 (2007).
- [6] E. V. Weber, R. D. Moore, "Electron Beam Exposure for Semiconductor Device Lithography," Solid State Technol. **22**, 61 (1979).
- [7] R. Moore, G. Caccoma, H. Pfeiffer, E. Weber, O. Woodard, "Electron Beam Writes Next-Generation IC Pattern," Electronics **54**, 138 (1981).
- [8] H. C. Pfeiffer, "Direct Write Electron Beam Lithography - A Production Line Reality," Solid State Technol. **27**, 223 (1984).
- [9] R. D. Moore, G. A. Caccoma, H. C. Pfeiffer, E. V. Weber, O. C. Woodard, "EL-3: A High Throughput, High Resolution E-Beam Lithography Tool," J. Vac. Sci. Technol. **19**, 950 (1981).
- [10] L. R. Harriott, "Scattering with angular limitation projection electron beam lithography for suboptical lithography," J. Vac. Sci. Technol. B **15**, 2130-2135 (1997).
- [11] S. D. Berger, J. M. Gibson, R. M. Camarda, R. C. Farrow, H. A. Huggins, J. S. Kraus, "Projection electron-beam lithography: A new approach," J. Vac. Sci. Technol. B **9**, 2996 (1991).
- [12] H. C. Pfeiffer, W. Stickel, "PREVAIL: an e-beam stepper with variable axis immersion lenses," Microelectron. Eng. **27**, 143-146 (1995).
- [13] R. S. Dhaliwal et al., "PREVAIL - Electron projection technology approach for next generation lithography," IBM J. RES. & DEV. **45**, 615-638 (2001).
- [14] H.C. Pfeiffer et al., "PREVAIL – Latest electron optical results," Proc. SPIE **4688**, 535 (2002).
- [15] H.C. Pfeiffer, W. Stickel, "PREVAIL – IBM's e-beam technology for next generation lithography," Future Fab International, **12**, 187 (2002).
- [16] T. Maruyama et al., "EBDW technology for EB shuttle at 65nm node and beyond," Proc. SPIE **6921** (2008).
- [17] A. Murray, F. Abboud, F. Raymond, C. N. Berglund, "Feasibility study of new graybeam writing strategies for raster scan mask generation," J. Vac. Sci. Technol. B **11**, 2390 (1993).
- [18] Mike Adel et al., "Optimized overlay metrology marks: theory and experiment," IEEE Trans. Semicond. Manuf. **17**, 166-179 (2004).