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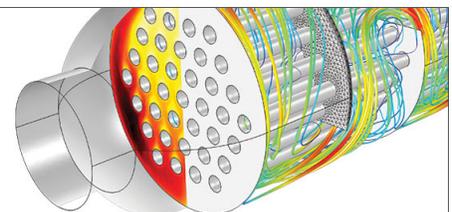
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Effective lifetimes exceeding 300 μs in gettered p -type epitaxial kerfless silicon for photovoltaics

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We evaluate defect concentrations and investigate the lifetime potential of p -type single-crystal kerfless silicon produced via epitaxy for photovoltaics. In gettered material, low interstitial iron concentrations (as low as $(3.2 \pm 2.2) \times 10^9 \text{ cm}^{-3}$) suggest that minority-carrier lifetime is not limited by dissolved iron. An increase in gettered lifetime from <20 to $>300 \mu\text{s}$ is observed after increasing growth cleanliness. This improvement coincides with reductions in the concentration of Mo, V, Nb, and Cr impurities, but negligible change in the low area-fraction ($<5\%$) of dislocated regions. Device simulations indicate that the high bulk lifetime of this material could support solar cell efficiencies $>23\%$. © 2013 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4844915>]

Kerfless crystalline silicon (c-Si) represents a promising approach to reduce the cost of solar-cell manufacturing by producing wafers directly from gaseous or molten silicon, avoiding ingot crystallization and wire-sawing.^{1–6} Kerfless materials could reduce silicon consumption by $\sim 10\times$ relative to ingot c-Si technology with high-efficiency thin devices.⁶ Kerfless materials could also streamline the manufacturing process, obviate the use of some consumables, reduce factory cost, and allow for potentially non-planar modules with thin-wafer production.^{4,6}

While a variety of approaches are available for kerfless wafer production,^{1–4,6} we posit that attempts to commercialize kerfless wafers have historically been inhibited by low bulk minority-carrier lifetime (τ_{bulk}). Wafers from vertical ribbon growth processes² contain average dislocation densities of 10^4 – $>10^6 \text{ cm}^{-2}$,^{7–9} which in combination with metal impurities including iron,⁷ limit minority-carrier lifetime and device performance (record efficiencies: 18.2% edge-defined film-fed growth, 17.8% string ribbon).^{9,10} Given the strong dependence of manufacturing^{6,11} and installation¹² costs on module efficiency, we stress the risk of bulk-defect-induced efficiency reductions to offset the cost savings of a kerfless process.

In this contribution, we evaluate the gettering response of kerfless epitaxial (epi) silicon and characterize defects in the material. Wafers grown from gas on porous silicon were introduced as the Canon ELTRAN process for integrated-circuit applications.^{3,13} Epitaxial silicon is grown atop a porous release bilayer at an average rate of $>4 \mu\text{m}/\text{min}$,^{3,14} with a low structural defect density of approximately $\leq 10^4 \text{ cm}^{-2}$.^{15–17} The epi silicon is exfoliated, leaving a single-crystal kerfless c-Si wafer and reusable substrate (over 50 cycles demonstrated).^{3,14} Epi kerfless silicon may offer additional performance advantages, such as repeatable n - and p -type doping that is tunable through the wafer thickness.¹⁷

Solar cell efficiency results up to 20.6% have been reported with epi silicon,¹⁸ however, the maximum reported effective lifetimes (τ_{eff}) of approximately 150 μs , on n -type

wafers,¹⁹ may limit device efficiency. Even for thin wafers, τ_{bulk} requirements increase for high-efficiency devices.^{20,21} For a planar high-efficiency device architecture with a 50 μm thick substrate, our PC1D simulation²² predicts $\tau_{\text{bulk}} > 340 \mu\text{s}$ (diffusion length $\sim 20 \times$ wafer thickness)²⁰ is required for maximum efficiency. Interdigitated back-contact architectures, as employed in commercial devices exceeding 24% efficiency, have more stringent requirements, $\tau_{\text{bulk}} > 5 \text{ ms}$, for maximum efficiency.²³

Herein, we demonstrate that kerfless epi silicon can achieve the τ_{bulk} required to support planar cell architectures with efficiencies $>23\%$. Wafers are produced in two generations (“Gen I” and “Gen II” henceforth) with growth system contamination control increasing by generation. After gettering with both standard and extended processes at an injection level (Δn) of 10^{15} cm^{-3} , τ_{eff} is $<20 \mu\text{s}$ in Gen I material while τ_{eff} is improved to $>300 \mu\text{s}$ in Gen II. We perform injection-dependent lifetime measurements to determine the concentration and performance-impact of interstitial iron and conclude that this defect is not the principal performance-limit in either generation of gettered material. The wafer surface area fraction of high ($>10^5 \text{ cm}^{-2}$) dislocation density is comparable between generations (both cases $<5\%$), suggesting that structural defects are not responsible for the observed lifetime improvement. Via bulk mass spectrometry, we evaluate the concentrations of metal impurities and hypothesize that reduced concentrations of slowly-diffusing impurities incorporated during growth may enable the lifetime improvement observed in the second generation of material.

As samples for this study, boron-doped p -type kerfless wafers are epitaxially grown to a thickness of 55–110 μm . Gen II material is produced in an upgraded growth system that has been developed for industrial production with improved impurity management in system components and greater automation. As-grown wafers are exfoliated and laser-cut into approximately $4 \times 4 \text{ cm}^2$ samples. Bulk resistivity is measured with a four-point probe (Keithley 4200, Cascade Microtech probe), yielding 0.50 $\Omega \text{ cm}$ (Gen I) and 1.79 $\Omega \text{ cm}$ (Gen II), with doping concentrations²⁴ and carrier diffusivities subsequently calculated.

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First, we describe the processing and characterization performed on the material. Injection-dependent τ_{eff} is measured by quasi-steady-state photoconductance (QSSPC) and transient photoconductance decay (PCD) (Sinton WCT-120) with Al_2O_3 surface passivation.^{25,26} After chemical polishing and RCA cleaning, 20 nm of Al_2O_3 is deposited on both sides with thermal atomic-layer-deposition at 200 °C (Cambridge NanoTech Savannah 200).^{27–29} Samples are then annealed in N_2 for 10 min at approximately 350 °C.²⁸

To account for the amount of illumination that is absorbed by each sample during lifetime measurements, a thickness-dependent “optical constant” is calculated (0.59–0.65) using a PC1D²² model for the short-circuit current of a sample under illumination from a Sinton WCT-120 flash lamp.^{26,30} The model assumes a 20 nm passivation layer with an index of refraction of 1.63.³¹ To minimize noise in the data, 50 measurements are averaged for high lifetime (>100 μs) samples. Error bounds for lifetime are $\pm 10\%$.³² Lifetime values are reported at an injection condition of $\Delta n = 10^{15} \text{ cm}^{-3}$ unless otherwise specified.

To estimate τ_{bulk} , the surface recombination velocity (SRV) of our Al_2O_3 passivation is evaluated²⁸ by comparing a τ_{eff} of 1.43 ms measured with a double-side polished 253 μm 3 Ωcm float zone wafer after chemical polishing (to match the preparation of the kerfless samples), to the intrinsic τ_{bulk} per the model of Richter *et al.*³³ The resulting SRV of 8.1 cm/s is applied at all injection-levels for the kerfless samples, although doping and surface differences may modify the result.²⁹ We note, however, that interstitial iron concentration ($[\text{Fe}_i]$) measurements are insensitive to SRV if it is unaffected by illumination and sufficiently passivating.

Phosphorus-diffusion gettering in a POCl_3 tube furnace (Tystar Tytan 3800) is performed after as-grown passivation and RCA cleaning followed by a HF dip. Two-sided gettering is performed on free-standing wafers. Two processes are tested: A standard process with a 25 min 845 °C plateau followed by pull-out and free cooling to room temperature, and low-temperature anneal (LTA)³⁴ process with the same plateau, but with cooling at $\sim 2.6^\circ\text{C}/\text{min}$ to a 2 h 575 °C anneal. The latter profile is inspired by the time-temperature-transformation diagram for dissolved iron in silicon³⁵ and tests for available gains from optimization of the standard process to reduce $[\text{Fe}_i]$. A sheet resistance of $75_{-20}^{+11} \Omega/\text{sq}$ is measured on the front and back of a single sample after the standard process and $77_{-11}^{+10} \Omega/\text{sq}$ after the LTA. The emitter is removed following gettering by chemical polishing (8 μm removed). Samples are re-passivated following the procedure above for post-gettering measurements.

To measure $[\text{Fe}_i]$, τ_{eff} is measured after illumination to dissociate iron-boron pairs ($\text{Fe}_i\text{-B}_s$) (20 flashes, Semilab WT-2000) and subsequent $\text{Fe}_i\text{-B}_s$ re-association (approximately 1 h Gen I, 3.5 h Gen II).^{26,36,37} Figure 1 shows the injection-level dependent lifetime of Gen II samples after dissociation and re-association, with the estimated bulk lifetime from our estimated SRV. For $[\text{Fe}_i]$ measurement, we compare lifetimes at $\Delta n = 10^{15} \text{ cm}^{-3}$, above the “crossover point” discussed in Macdonald *et al.*^{37,38} Capture cross sections for electrons and holes are taken as $\sigma_n = 5.0 \times 10^{-15} \text{ cm}^2$ and $\sigma_p = 3.0 \times 10^{-15} \text{ cm}^2$ or for $\text{Fe}_i\text{-B}_s$ pairs and $\sigma_n = 1.3 \times 10^{-14} \text{ cm}^2$ and $\sigma_p = 7.0 \times 10^{-17} \text{ cm}^2$ for Fe_i .^{37,39,40}

Lifetimes for the kerfless samples are quoted with $\text{Fe}_i\text{-B}_s$ pairs dissociated (illuminated). Five measurements are averaged to avoid re-dissociation of $\text{Fe}_i\text{-B}_s$ pairs during “dark” Gen II lifetime measurements for $[\text{Fe}_i]$, although 50 measurements are averaged in Figure 1. Error bounds for $[\text{Fe}_i]$ are calculated assuming $\pm 1.5\%$ uncertainty for repeated lifetime measurements³² and random propagation through the $[\text{Fe}_i]$ calculation.⁴¹

Next, we examine the impact of three potential lifetime-limiting defects in each generation of kerfless epi material. First, we evaluate the role of dissolved iron, a common performance-limiting defect in kerfless ribbon materials.^{7,42} In Gen I material after standard gettering, we measure a τ_{eff} of $12 \pm 1.2 \mu\text{s}$, an implied open circuit voltage (V_{OC}) at 1 sun of 647 mV, and an $[\text{Fe}_i]$ of $(5.0 \pm 7.4) \times 10^{10} \text{ cm}^{-3}$ in a 52 μm thick sample. The LTA process results in an $[\text{Fe}_i]$ of $(3.0 \pm 9.8) \times 10^{10} \text{ cm}^{-3}$, but yields a reduced τ_{eff} of $9 \pm 0.9 \mu\text{s}$ and implied- V_{OC} of 628 mV in a 57 μm sample. The change in $[\text{Fe}_i]$ between processes is inconclusive, as the observed change is within the calculated error. After standard gettering of Gen II material, τ_{eff} is $342 \pm 34 \mu\text{s}$, implied- V_{OC} is 710 mV, and $[\text{Fe}_i]$ is $(2.5 \pm 0.23) \times 10^{10} \text{ cm}^{-3}$ with a 95 μm sample (Figure 1). With the LTA process, τ_{eff} is $313 \pm 31 \mu\text{s}$, implied- V_{OC} is 713 mV, and $[\text{Fe}_i]$ is $(3.2 \pm 2.2) \times 10^9 \text{ cm}^{-3}$ with an 80 μm sample. Although the standard process provides a higher τ_{eff} than the LTA, τ_{bulk} is nearly equivalent, arising from different surface lifetimes due to different sample thicknesses. We note that the Gen II LTA sample is not centered during QSSPC measurements to maximize τ_{eff} . When centered, the Gen II LTA τ_{eff} is $294 \pm 29 \mu\text{s}$.

To identify the performance impact of Fe_i , we compare τ_{bulk} against the maximum lifetime obtainable with a given $[\text{Fe}_i]$.^{40,43} Estimated τ_{bulk} , calculated with our estimate of SRV, for champion samples after gettering and illumination are shown in Figure 2. Dashed lines show the estimated lifetime limits from Auger and radiative recombination³² and a simplified⁴⁴ Shockley-Read-Hall recombination model at Fe_i per the *QSS-Model* from Cuevas.⁴⁵ The data suggests that

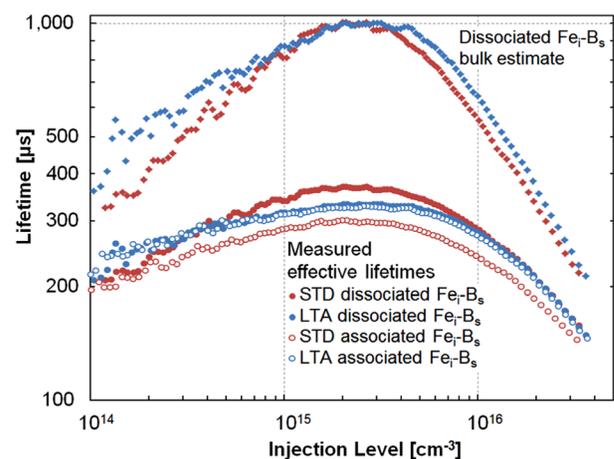


FIG. 1. Effective minority-carrier lifetimes of champion Gen II samples after P-diffusion gettering (standard process red; LTA blue) as a function of injection-level with dissociated (full symbols) and associated (open symbols) $\text{Fe}_i\text{-B}_s$ pairs. Lifetime decay and the “crossover point” can be observed with the standard process after $\text{Fe}_i\text{-B}_s$ re-association, while the LTA process does not indicate significant $[\text{Fe}_i]$. The estimated bulk lifetime is shown with $\text{SRV} = 8.1 \text{ cm/s}$.

defects other than Fe_i limit bulk minority-carrier lifetimes in both Gen I and Gen II materials after gettering because τ_{bulk} values are well below the Fe_i -limited lifetime^{40,43} and τ_{bulk} is not improved with the LTA process.

The estimated τ_{bulk} is improved by approximately two orders of magnitude in Gen II relative to Gen I material. With similar $[\text{Fe}_i]$, a reduction of another lifetime-limiting defect is suggested (Figure 2). Structural defects are one possibility and are believed to originate in single-crystal epi wafers from incomplete pore closure during porous silicon annealing.^{15,46} Stacking faults and dislocations are revealed in portions of Gen I (1 cm^2) and Gen II (4 cm^2) samples after gettering⁴⁷ and analyzed with an optical microscope and counting software.⁴⁸ The wafer surface area covered by regions of high ($>10^5 \text{ cm}^{-2}$) dislocation density, a predictor of performance loss,^{8,49} of both Gen I and Gen II materials are comparable ($<5\%$), and thus deemed not to be the defect responsible for the dramatic increase in lifetime between generations.

Next, we consider the role of impurity species besides iron. Inductively coupled plasma mass spectrometry (ICP-MS, Fraunhofer Center for Silicon Photovoltaics) is performed to measure the concentrations of 20 impurity elements before gettering in approximately 1 g of Gen I and >2 g of Gen II material (1 and 2 ICP-MS samples respectively). Gen II material exhibits reduced concentrations of deleterious impurities⁵⁰ that are slowly-diffusing and may prove difficult to getter:⁵¹ Molybdenum (82% reduction to detection limit), Vanadium (59% reduction), and Niobium (40% reduction).⁵² Chromium also decreased in Gen II material (91% reduction); however, the difference in post-gettering performance between generations leads us to suspect the aforementioned species. No change above the error of the measurement was detected for the other impurities tested (Mg, Al, P, Ti, Mn, Fe, Ni, Co, Cu, Zn, Zr, Ag, Sn, W, and Au). The evidence suggests that a reduction of slowly-diffusing impurities in the as-grown material may be critical for the observed lifetime improvement in Gen II material.

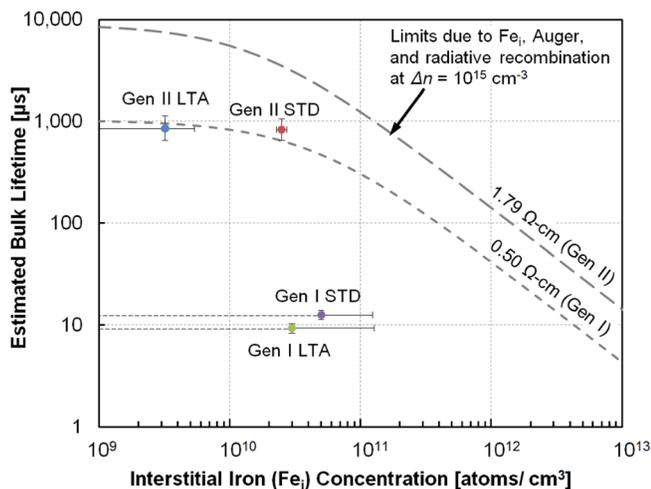


FIG. 2. Estimated bulk minority-carrier lifetimes of two generations of kerfless wafers after P-diffusion gettering compared to theoretical lifetime limits at $\Delta n = 10^{15} \text{ cm}^{-3}$. An approximate two orders of magnitude improvement in τ_{bulk} after gettering is observed for Gen II relative to Gen I material. The minimal impact of the LTA processes and difference between the realized and theoretical lifetime limits suggest that defects other than Fe_i limit post-gettering lifetimes.

In light of this analysis, we comment on the ultimate lifetime potential of epi material in comparison to industry-standard ingot multicrystalline silicon (mc-Si). The area fraction of high ($>10^5 \text{ cm}^{-2}$) dislocation density is low ($<5\%$), suggesting that dislocations may be less of a lifetime limitation for epi than even small-grained mc-Si.⁵³ We note that mc-Si wafers obtain similarly low $[\text{Fe}_i] \leq 10^{10} \text{ cm}^{-3}$ directly after low-temperature annealing,^{53,54} yet average effective lifetimes are shown to be limited to $200 \mu\text{s}$.⁵⁴ In addition, the absence of grain boundaries in epi material eliminates a potential source of open-circuit voltage loss.⁵⁵ Future work will elucidate the performance impact of structural defects in kerfless epi. However, we hypothesize that the control of impurities, especially through substrate re-uses, may be the crucial determinant of lifetime for this material.

Finally, we estimate the performance potential of epi-based solar cells using a PC1D²² simulation for a high-efficiency device architecture (Table I), and explore the optimal epi wafer thickness. The device includes a lightly-doped $120 \Omega/\text{sq}$ emitter with low series and contact resistance, and a locally contacted and passivated rear.⁵⁶ PC1D was used to simulate this 2-D architecture with cell-area-normalized values for rear contact resistance and reflectance, as is done by default in PC1D for external reflectivity.

With a $50 \mu\text{m}$ wafer, the simulation indicates that the excess electron density at the maximum-power point is approximately $1.4 \times 10^{15} \text{ cm}^{-3}$ in the bulk of the device with high lifetime material.^{20,21,57} The τ_{eff} of the champion standard gettering Gen II sample is $357 \pm 36 \mu\text{s}$ after illumination at $\Delta n = 1.4 \times 10^{15} \text{ cm}^{-3}$, resulting in an estimated τ_{bulk} of $924 \mu\text{s}$ assuming a SRV of 8.1 cm/s (Figure 1). This lifetime in the bulk of the device achieves an estimated efficiency of 22.4% with a $50 \mu\text{m}$ wafer and $>23\%$ with increased wafer thicknesses (Figure 3(a)). Lower-performance material, $\tau_{\text{bulk}} = 50 \mu\text{s}$, provides reduced cell performance and optimum thickness relative to the Gen II material due to diffusion length limitations.²¹

A cost-performance^{11,68} model explores trade-offs between efficiency, wafer thickness, and manufacturing yield for kerfless silicon (Figure 3(b)). Without input from our industrial collaborators, we have estimated an optimum wafer thickness for cost of $50\text{--}60 \mu\text{m}$ for Gen II material. Yields for the separate wafer, cell, and module manufacturing steps are $\phi = 54.47 \times t^{0.111}$ based on free standing wafers during cell processing,^{11,69} and a wafer production throughput multiplier is $\lambda = 36.38 \times t^{-0.917}$,¹⁵ with t as the

TABLE I. Solar cell simulation input parameters

Parameter	Value	Reference
Front external reflectivity [%]	5.0	58
Front/rear internal reflectance [%]	92.5/95.0	59 and 60
Series/shunt resistance [$\Omega \text{ cm}^2$]	0.3/10 000	61–63
Front/rear contact resistance [$\Omega \text{ cm}^2$]	0.027/0.027	64 and 65
Effective front/rear SRV [cm/s]	2000/30	20, 28, 29, and 60
Wafer doping [cm^{-3}]	$p, 3 \times 10^{16}$	
Peak emitter doping [cm^{-3}]	$n, 5 \times 10^{19}$	65–67
Emitter sheet resistance [Ω/sq]	120.2	63, 65, and 66

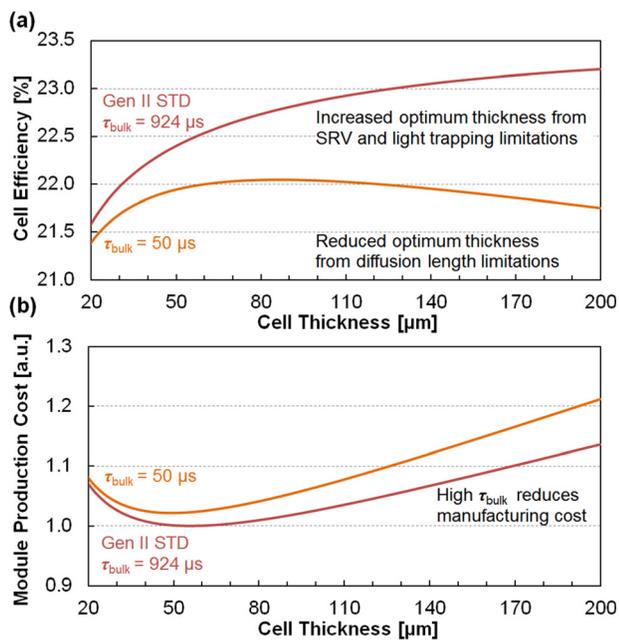


FIG. 3. (a) The lifetime of the Gen II material (red line) after a standard gettering process is sufficient to achieve simulated cell efficiencies of $>23\%$ (22.4% with a $50\ \mu\text{m}$ wafer) with a high-efficiency device architecture. (b) Estimated manufacturing cost (in $\$/\text{W}$) normalized to the minimum obtained. The predicted optimum thickness for cost is $50\text{--}60\ \mu\text{m}$. Lower performance material with $\tau_{\text{bulk}} = 50\ \mu\text{s}$ (orange line) provides a lower efficiency and optimum thickness while increasing manufacturing cost.

wafer thickness in microns. We observe a cost minimum from the trade-off of efficiency and yield, which both favor thicker wafers, and silicon usage and throughput, which both favor thinner wafers. While precise values will vary depending on process details, this calculation highlights the need for high-yield manufacturing processes, good light trapping, and good surface passivation to minimize thickness and sufficient τ_{bulk} to maximize efficiency.

In conclusion, effective minority-carrier lifetimes $>300\ \mu\text{s}$ at $\Delta n = 10^{15}\ \text{cm}^{-3}$ are demonstrated in epitaxially grown kerfless silicon after gettering. Fe_i concentrations of $(2.5 \pm 0.23) \times 10^{10}\ \text{cm}^{-3}$ are measured with a standard gettering process and $(3.2 \pm 2.2) \times 10^9\ \text{cm}^{-3}$ after a low-temperature anneal in the second generation of material. Our analysis suggests that lifetime in both generations of material is not limited by interstitial iron after gettering. We observed a low area fraction ($<5\%$) of high ($>10^5\ \text{cm}^{-2}$) structural-defect density in both generations of material. We hypothesize that reductions in the concentration of slowly-diffusing metal impurities may enable the approximately two orders of magnitude lifetime improvement observed in Gen II material. Our cost-performance model estimates that the achieved lifetimes could support cell efficiencies $>23\%$ and suggests an optimum thickness regime of $50\text{--}60\ \mu\text{m}$ for cost. We note that as successive generations of PV silicon materials become “cleaner,” there is a need to develop and employ defect characterization tools that can determine the identities and impacts of low concentrations of performance-limiting impurities.⁷⁰

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- ¹A. Goetzberger, C. Hebling, and H.-W. Schock, *Mater. Sci. Eng. R* **40**(1), 1 (2003).
- ²T. F. Ciszek, *J. Cryst. Growth* **66**(3), 655 (1984).
- ³R. Brendel, *Jpn J. Appl. Phys., Part 1* **40**, 4431 (2001).
- ⁴A. M. Gabor, *Innovations in Crystalline Silicon PV 2013: Markets, Strategies and Leaders in Nine Technology Areas* (Webinar, Greentech Media Research, 2013).
- ⁵A. Goodrich, P. Hacke, Q. Wang, B. Sopori, R. Margolis, T. L. James, and M. Woodhouse, *Sol. Energy Mater. Sol. Cells* **114**, 110 (2013).
- ⁶D. M. Powell, M. T. Winkler, H. J. Choi, C. B. Simmons, D. Berney Needleman, and T. Buonassisi, *Energy Environ. Sci.* **5**, 5874 (2012).
- ⁷J. P. Kalejs, *Solid State Phenom.* **95–96**, 159 (2003).
- ⁸K. Nakayashiki, V. Meemongkolkiat, and A. Rohatgi, *IEEE Trans. Electron Devices* **52**(10), 2243 (2005).
- ⁹A. Augusto, D. Pera, H. J. Choi, P. Bellanger, M. C. Brito, J. Maia Alves, A. M. Vallêra, T. Buonassisi, and J. M. Serra, *J. Appl. Phys.* **113**(8), 083510 (2013).
- ¹⁰A. Rohatgi, D. S. Kim, K. Nakayashiki, V. Yelundur, and B. Rounsaville, *Appl. Phys. Lett.* **84**(1), 145 (2004).
- ¹¹D. M. Powell, M. T. Winkler, A. Goodrich, and T. Buonassisi, *IEEE J. Photovoltaics* **3**(2), 662 (2013).
- ¹²A. Goodrich, T. James, and M. Woodhouse, “Residential, commercial, and utility-scale photovoltaic (PV) system prices in the United States: Current drivers and cost-reduction opportunities,” NREL Technical Report No. NREL/TP-6A20-53347, 2012.
- ¹³T. Yonehara, K. Sakaguchi, and N. Sato, *Appl. Phys. Lett.* **64**(16), 2108 (1994).
- ¹⁴T. S. Ravi, “Technology development for high-efficiency solar cells and modules using thin ($<80\ \mu\text{m}$) single-crystal silicon wafers produced by epitaxy,” NREL Subcontract Report No. NREL/SR-5200-58593, 2013.
- ¹⁵N. Sato, K. Sakaguchi, K. Yamagata, Y. Fujiyama, and T. Yonehara, *J. Electrochem. Soc.* **142**(9), 3116 (1995).
- ¹⁶J. Kraiem, E. Tranvouez, S. Quozola, A. Fave, A. Kaminski, J. P. Boyeaux, G. Bremond, and M. Lemiti, in *Proceedings of the 31st IEEE Photovoltaic Specialists Conference (PVSC)*, Lake Buena Vista, FL (IEEE, 2005), pp. 1107–1110.
- ¹⁷K. Van Nieuwenhuysen, I. Gordon, T. Bearda, C. Boulord, M. Debucquoy, V. Depauw, F. Dross, J. Govaerts, S. Granata, R. Labie, X. Loozen, R. Martini, B. O’Sullivan, H. S. Radhakrishnan, K. Baert, and J. Poortmans, in *Proceedings of the 38th IEEE Photovoltaic Specialists Conference (PVSC)*, Austin, TX (IEEE, 2012), pp. 001833–001836.
- ¹⁸J. H. Petermann, D. Zielke, J. Schmidt, F. Haase, E. Garralaja Rojas, and R. Brendel, *Prog. Photovoltaics* **20**(1), 1 (2012); Applied Nanotech Holdings, Inc., *Solexel Achieves Record 20.62% Thin-Silicon Cell*

- Efficiency Utilizing Applied Nanotech's Proprietary Aluminum Metallization Material*, 2013.
- ¹⁹H. S. Radhakrishnan, M. Debucquoy, F. Korsós, K. Van Nieuwenhuysen, V. Depauw, I. Gordon, R. Mertens, and J. Poortmans, *Energy Procedia* **38**, 950 (2013).
- ²⁰G. Coletti, *Prog. Photovoltaics* **21**(5), 1163 (2013).
- ²¹B. Michl, M. Kasemann, W. Warta, and M. C. Schubert, *Phys. Status Solidi (RRL)* **7**(11), 955–958 (2013).
- ²²D. A. Clugston and P. A. Basore, in *Proceedings of the 26th IEEE Photovoltaic Specialists Conference (PVSC)*, Anaheim, CA (IEEE, 1997), pp. 207–210.
- ²³D. Diouf, J.-P. Kleider, and C. Longeaud, in *Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells*, edited by W. G. J. H. M. van Sark, L. Korte, and F. Roca (Springer, Berlin, 2012), pp. 483–519; P. J. Cousins, D. D. Smith, L. Hsin-Chiao, J. Manning, T. D. Dennis, A. Waldhauer, K. E. Wilson, G. Harley, and W. P. Mulligan, in *Proceedings of the 35th IEEE Photovoltaic Specialists Conference (PVSC)* (IEEE, 2010), pp. 000275–000278.
- ²⁴A. Giannattasio, A. Giaquinta, and M. Porrini, *Phys. Status Solidi A* **208**(3), 564 (2011).
- ²⁵R. A. Sinton, A. Cuevas, and M. Stuckings, in *Proceedings of the 25th IEEE Photovoltaic Specialists Conference (PVSC)*, Washington, DC (IEEE, 1996), pp. 457–460.
- ²⁶Sinton Instruments, *WCT-120* Documentation, 2006.
- ²⁷B. Veith, F. Werner, D. Zielke, R. Brendel, and J. Schmidt, *Energy Procedia* **8**, 307 (2011); J. A. van Delft, D. Garcia-Alonso, and W. M. M. Kessels, *Semicond. Sci. Technol.* **27**(7), 074002 (2012); Polishing: (CP4, HF, 30% KOH 1 min, HF); RCA cleaning: (RCA1 70 °C 10 min, HF, RCA2 70 °C 10 min).
- ²⁸J. Schmidt, B. Veith, and R. Brendel, *Phys. Status Solidi (RRL)* **3**(9), 287 (2009).
- ²⁹G. Dingemans, M. C. M. van de Sanden, and W. M. M. Kessels, *Electrochem. Solid-State Lett.* **13**(3), H76 (2010).
- ³⁰Sinton Instruments, Customer Note: Optical Constant Calculation.
- ³¹J. M. Rafi, M. Zabala, O. Beldarrain, and F. Campabadal, *J. Electrochem. Soc.* **158**(5), G108 (2011).
- ³²Semiconductor equipment and materials international, SEMI AUX026-1012, 2012.
- ³³A. Richter, F. Werner, A. Cuevas, J. Schmidt, and S. W. Glunz, *Energy Procedia* **27**, 88 (2012).
- ³⁴M. Rinio, A. Yodyunyong, S. Keipert-Colberg, Y. P. Botchak Mouafi, D. Borchert, and A. Montesdeoca-Santana, *Prog. Photovoltaics* **19**(2), 165 (2011).
- ³⁵M. D. Pickett and T. Buonassisi, *Appl. Phys. Lett.* **92**(12), 122103 (2008).
- ³⁶D. H. Macdonald, L. J. Geerligs, and A. Azzizi, *J. Appl. Phys.* **95**(3), 1021 (2004); D. Macdonald, T. Roth, P. N. K. Deenapanray, K. Bothe, P. Pohl, and J. Schmidt, *J. Appl. Phys.* **98**(8), 083509 (2005).
- ³⁷D. Macdonald, T. Roth, P. N. K. Deenapanray, T. Trupke, and R. A. Bardos, *Appl. Phys. Lett.* **89**(14), 142107 (2006).
- ³⁸D. Macdonald provided calculation spreadsheet.
- ³⁹A. A. Istratov, H. Hieslmair, and E. R. Weber, *Appl. Phys. A* **69**(1), 13 (1999).
- ⁴⁰D. Macdonald, J. Tan, and T. Trupke, *J. Appl. Phys.* **103**(7), 073710 (2008).
- ⁴¹E. O. Doebelin, *Measurement Systems: Application and Design* (McGraw-Hill, New York, 2004), pp. 67–71.
- ⁴²T. Buonassisi, A. A. Istratov, M. D. Pickett, M. Heuer, J. P. Kalejs, G. Hahn, M. A. Marcus, B. Lai, Z. Cai, S. M. Heald, T. F. Ciszek, R. F. Clark, D. W. Cunningham, A. M. Gabor, R. Jonczyk, S. Narayanan, E. Sauar, and E. R. Weber, *Prog. Photovoltaics* **14**(6), 513 (2006).
- ⁴³B. Sopori, *J. Electron Mater.* **31**(10), 972 (2002); A. A. Istratov, H. Hieslmair, and E. R. Weber, *Appl. Phys. A* **70**(5), 489 (2000).
- ⁴⁴D. Macdonald and A. Cuevas, *Phys. Rev. B* **67**(7), 075203 (2003).
- ⁴⁵A. Cuevas, QSS-Model v5.2, 2012.
- ⁴⁶H. S. Radhakrishnan, F. Dross, M. Debucquoy, P. Rosenits, K. Van Nieuwenhuysen, I. Gordon, J. Poortmans, and R. Mertens, “Evaluation of the influence of an embedded porous silicon layer on the bulk lifetime of epitaxial layers and the interface recombination at the epitaxial layer/porous silicon interface,” *Prog. Photovoltaics* (published online).
- ⁴⁷B. L. Sopori, *J. Electrochem Soc.* **131**(3), 667 (1984).
- ⁴⁸D. Berney Needleman, H. J. Choi, D. M. Powell, and T. Buonassisi, *Phys. Status Solidi (RRL)* **7**, 1041–1044 (2013); M. L. Vogl, S.M., “Dislocation density reduction in multicrystalline silicon through cyclic annealing” Massachusetts Institute of Technology, 2011. Available at: <http://hdl.handle.net/1721.1/68956>; H. Galda, *Image Processing with Scilab and Image Processing Design Toolbox*, 2011.
- ⁴⁹B. Sopori, P. Rupnowski, S. Shet, V. Mehta, M. Seacrist, G. Shi, J. Chen, and A. Deshpande, in *Proceedings of the 37th IEEE Photovoltaic Specialists Conference (PVSC)* Seattle, WA (IEEE, 2011), pp. 003440–003445; T. Trupke, J. Nyhus, and J. Haunschild, *Physica Status Solidi (RRL)* **5**(4), 131 (2011).
- ⁵⁰J. R. Davis, Jr., A. Rohatgi, R. H. Hopkins, P. D. Blais, P. Rai-Choudhury, J. R. McCormick, and H. C. Mollenkopf, *IEEE Trans. Electron Devices* **27**(4), 677 (1980).
- ⁵¹D. Macdonald, A. Cuevas, A. Kinomura, and Y. Nakano, in *Proceedings of the 29th IEEE Photovoltaic Specialists Conference (PVSC)*, New Orleans, LA (IEEE, 2002), pp. 285–288; A. Rohatgi, R. H. Hopkins, J. R. Davis, R. B. Campbell, and H. C. Mollenkopf, *Solid-State Electron.* **23**(11), 1185 (1980).
- ⁵²K. Graff, *Metal Impurities in Silicon-Device Fabrication* (Springer, Berlin, 1999), p. 150.
- ⁵³Y. M. Yang, A. Yu, B. Hsu, W. C. Hsu, A. Yang, and C. W. Lan, “Development of high-performance multicrystalline silicon for photovoltaic industry,” *Prog. Photovoltaics* (published online).
- ⁵⁴J. Hofstetter, D. P. Fenning, D. M. Powell, A. E. Morishige, and T. Buonassisi, “Total iron concentration: a simple sorting metric for customized phosphorus diffusion gettering” (unpublished).
- ⁵⁵R. B. Bergmann, *Appl. Phys. A* **69**(2), 187(1999); T. F. Ciszek and T. H. Wang, *J. Cryst. Growth* **237–239**(Part 3), 1685 (2002); S. Steingrube, O. Breitenstein, K. Ramspeck, S. Glunz, A. Schenk, and P. P. Altermatt, *J. Appl. Phys.* **110**(1), 014515 (2011).
- ⁵⁶J. Zhao, A. Wang, and M. A. Green, *Prog. Photovoltaics* **7**(6), 471 (1999).
- ⁵⁷PCID Application Help: Defined Graphs (Graph menu).
- ⁵⁸M. A. Green, *Solar Cells: Operating Principles, Technology and System Applications* (University of New South Wales, Kensington, NSW, 1998), pp. 92–93; S. W. Glunz, R. Preu, and D. Biro, in *Comprehensive Renewable Energy*, edited by A. Sayigh (Elsevier, Oxford, 2012), pp. 353–387; A. Blakers, N. Zin, K. R. McIntosh, and K. Fong, *Energy Procedia* **33**, 1 (2013).
- ⁵⁹A. Lorenz, J. John, B. Vermang, and J. Poortmans, in *Proceedings of the 25th European Photovoltaic Solar Energy Conference and Exhibition/5th World Conference on Photovoltaic Energy Conversion* Valencia, Spain (2010), pp. 2059–2061.
- ⁶⁰A. Rohatgi, D. L. Meier, B. McPherson, Y.-W. Ok, A. D. Upadhyaya, J.-H. Lai, and F. Zimbardi, *Energy Procedia* **15**, 10 (2012).
- ⁶¹J. Zhao, A. Wang, P. P. Altermatt, S. R. Wenham, and M. A. Green, *Sol. Energy Mater. Sol. Cells* **41–42**, 87 (1996).
- ⁶²A. G. Aberle, S. R. Wenham, and M. A. Green, in *Proceedings of the 23rd IEEE Photovoltaic Specialists Conference (PVSC)*, Louisville, KY (IEEE, 1993), pp. 133–139; R. Low, A. Gupta, N. Bateman, D. Ramappa, P. Sullivan, W. Skinner, J. Mullin, S. Peters, and H. Weiss-Wallrath, in *Proceedings of the 35th IEEE Photovoltaic Specialists Conference (PVSC)*, Honolulu, HI (IEEE, 2010), pp. 001440–001445.
- ⁶³J. S. Renshaw, I. B. Cooper, and A. Rohatgi, *Appl. Phys. Lett.* **102**(1), 013502 (2013).
- ⁶⁴C.-H. Lin, B.-C. Chen, C.-H. Lung, W.-H. Lu, Y.-F. Chen, Y.-W. Tai, M.-H. Wu, C.-C. Wang, and W.-C. Hsu, in *Proceedings of the 25th European Photovoltaic Solar Energy Conference and Exhibition/5th World Conference on Photovoltaic Energy Conversion*, Valencia, Spain (2010), pp. 2010–2013; P. Pavlovic, A. Dastgheib-Shirazi, F. Book, B. Raabe, and G. Hahn, in *Proceedings of the 24th European Photovoltaic Solar Energy Conference*, Hamburg, Germany (2009), pp. 2185–2189; S. Gatz, T. Dullweber, and R. Brendel, *IEEE J. Photovoltaics* **1**(1), 37 (2011).
- ⁶⁵D.-H. Neuhaus and A. Münzer, *Adv. Optoelectron.* **2007**, 24521.
- ⁶⁶G. Hahn, in *25th European Photovoltaic Solar Energy Conference and Exhibition/5th World Conference on Photovoltaic Energy Conversion*, Valencia, Spain (2010), pp. 1091–1096.
- ⁶⁷D. Rudolph, K. Peter, A. Meijer, O. Doll, and I. Köhler, in *26th European Photovoltaic Solar Energy Conference and Exhibition*, Hamburg, Germany 2011, pp. 1349–1352.
- ⁶⁸SEMI PV Group, *International Technology Roadmap for Photovoltaic: Results 2012* (SEMI PV Group, 2013); With a 98% cell to module power ratio and 90% area utilization.
- ⁶⁹K. A. Munzer, K. T. Holdermann, R. E. Schlosser, and S. Sterk, *IEEE Trans. Electron Devices* **46**, 2055 (1999).
- ⁷⁰J. Schmidt, P. Pohl, K. Bothe, and R. Brendel, *Adv. Optoelectron.* **2007**, 92842 (2007).