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Planarization Efficiency of Electrochemical Mechanical Deposition and Its Dependence on Process Parameters

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Electrochemical mechanical deposition (ECMD) is a technique that has the ability to deposit planar metal films on nonplanar substrate surfaces with cavities. The method involves electrochemical deposition and simultaneous sweeping of the substrate surface with a planarization pad. Mechanical action of the pad increases suppression at the swept surface and therefore, mechanically induced superfilling of the cavities takes place. In this study we show that the planarization efficiency of the ECMD process for copper deposition is a strong function of the plating chemistry. Electrolytes containing no organic additives or only accelerators do not yield any planarization. Plating baths with only suppressors show low planarization capability, whereas those containing both suppressors and accelerators yield the highest planarization efficiency. Soaking the wafer surface in an accelerator-containing solution before the ECMD process step increases the planarization efficiency significantly. The presence of levelers in the plating electrolyte is detrimental to planarization efficiency of ECMD. High-acid copper plating solutions display higher planarization capability than low-acid electrolytes.
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Electrochemically deposited (ECD) copper is the preferred material for the fabrication of advanced interconnect structures for integrated circuits because of copper's low resistivity and high electromigration resistance.[1] In an interconnect fabrication process, copper is filled into and coated over the various size features, such as trenches and vias, formed in the dielectric layers on wafer surfaces. The plated copper is then annealed and the excess material over the top surface or the field region of the wafer is removed by chemical mechanical polishing (CMP), leaving the metal only within the cavities of the various features.

Figure 1a schematically shows the surface topography of a copper layer deposited on a patterned wafer surface by the standard ECD process. As can be seen from this figure, the nonuniform topography of the electrochemically deposited copper surface is due to the bumps or protrusions over the high-pattern-density regions with submicrometer-size high aspect-ratio (AR) cavities, as well as the dips or steps over the large, low-AR features which may have a width of 5 μm or more. In a typical ECD process, specially formulated electrolytes containing chloride ions and organic additives such as suppressors and accelerators are employed to achieve void-free superfilling or bottom-up filling of submicrometer-size high-AR features.[2,3] Suppressors are typically polyethylene glycol (PEG)-related polymers, which form a film over the copper surface, increasing polarization. Accelerators are usually sulfur-containing compounds such as bis(sodiumsulfopropyl)disulfide (SPS), which depolarize surfaces that already contain suppressors. Accelerators that enable superfilling in the narrow features also cause overfilling of these features, giving rise to the bumps shown in Fig. 1a. Use of levelers in the bath formulation reduces the height of the protrusions because levelers attach themselves at these high-current-density regions and help suppress the current. The superfilling mechanism is not operative in the large features and therefore, conformal copper plating into such features yields the dips or steps shown in Fig. 1a, where the depth of the step d_s, is approximately equal to the depth of the features, d. The total within-die copper surface profile range in Fig. 1a, therefore, is $d_p + d$, where d_p is the thickness of the protrusion. For an interconnect structure with 0.5-μm-deep features and 1-μm-thick plated copper, i.e., $t = 1.0$ μm, the within-die copper range may be as large as 0.9 μm, assuming a protrusion amount of 0.4 μm. This large topography needs to be planarized during the CMP step and the 1-μm-thick copper overburden needs to be completely removed without causing excessive dishing and erosion defects. This is a challenging task for the CMP process.

The electrochemical mechanical deposition (ECMD) process was developed to planarize copper during the deposition step so that an already planarized copper layer would be delivered to the CMP process.[4,5] Figure 1b schematically shows the surface topography of a copper layer deposited by the ECMD process. As can be seen from this figure the copper layer has a thickness t and it is totally planar with zero within-die profile range. Benefits of such planar copper layers for interconnect fabrication have already been discussed and demonstrated.[6-8]

ECMD, as applied to copper deposition on patterned wafers, involves sweeping the surface of the wafer with strips of a pad material as electroplating commences. When this mechanical action is applied to the wafer surface during plating, the process provides enhanced deposition of copper in large features, even with aspect ratios much smaller than 0.01.[6,9] This phenomenon is called mechanically induced superfilling. The mechanism of mechanically induced superfilling in an ECMD process was recently studied and a model was proposed.[9] According to this model, the sweeping action of the planarization pad induces a differential in the copper growth rates between the top surface of the wafer and the cavities by inducing a disparity in the surface coverage of active organic additives at the top surface and the internal surfaces of the cavities. Accordingly, every time the planarization pad strip sweeps a region on the surface of the wafer, it removes a substantial amount of accelerators from the top surface, and when the swept region enters into the solution and deposition initiates, the effective surface coverage of accelerators at that location is low, i.e., current is suppressed. Because sweeping does not directly affect the cavities, the surface coverage of accelerator and suppressor within the cavities are undisturbed, at their steady-state values. Therefore, under galvanostatic plating conditions less current density goes to the top surface due to higher suppression compared to the cavities which have more accelerator surface coverage.

In our previous work we had studied the transient behavior of mechanically induced superfilling of copper into large cavities using an ECMD process employing a single pad strip and a high acid plating chemistry with specific concentrations of accelerator and suppressor species.[9] In the present work, using both single and multistrip pads, we investigated the dependence of ECMD planarization efficiency on various experimental parameters such as additive compositions and concentrations, plating bath acidity, and the additive content of the wafer surface before the ECMD process is initiated.

Experimental

A schematic top view of the plating cell used in the experiments is shown in Fig. 2. The field-shaping plate is a porous rigid plate through which the plating solution rises up and reaches the wafer surface to be plated. The porosity on the shaping plate was designed to assure uniform film deposition. A rectangular copper anode was

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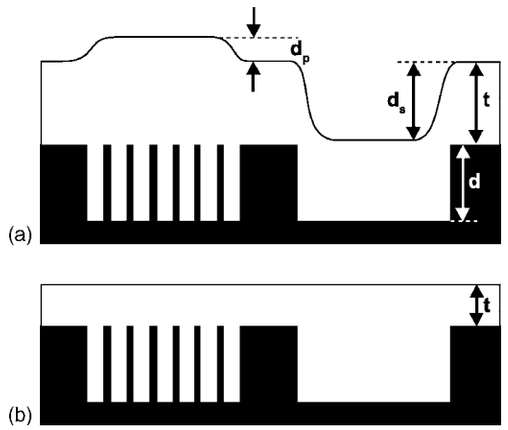

Figure 1. Cross-sectional schematic of copper layers deposited on a patterned wafer surface by (a) the ECD process and (b) the ECMD process.

placed in a cavity under the shaping plate and either one or multiple strips of a planarization pad were attached over the shaping plate. For some of the experiments an 18-mm-wide horizontal single strip pad (shown with dotted lines in Fig. 2) was used. For other experiments the single strip pad was removed and multiple strips of pad (shown with slanted solid lines) were installed over the shaping plate where the width of the strips was about 2 mm and the distance or gap between them was about 4 mm. The planarization pad was a fixed-abrasive-type material supplied by 3M Company and it had a soft subpad made of a spongy material. In the ECMD process, the planarization efficiency at a location on the wafer is a strong function of the plating time between pad sweeps, t_p, at that location.[9] For a given rotation speed of the wafer, if multiple strips of pads are used for surface sweeping, t_p values are minimized and they vary from point to point on the wafer, also varying with time. Therefore, although variations in process results such as planarization efficiency can be investigated as a function of process parameters using such a setup, it is easier to carry out fundamental studies using the horizontal single pad strip of Fig. 2 because t_p values for such a setup is exactly known for every point on the wafer at all times during the process. The reader is referred to Ref. 9 for details on the use of a single-pad strip in an experimental ECMD setup. The wafer was lowered face-down toward the shaping plate with a holder that could rotate as well as translate in x direction by controlled amounts and at controlled speeds. Multiple electrical contacts were made to the wafer surface at the two locations indicated in the figure. When the wafer was lowered down toward the shaping plate, the wafer

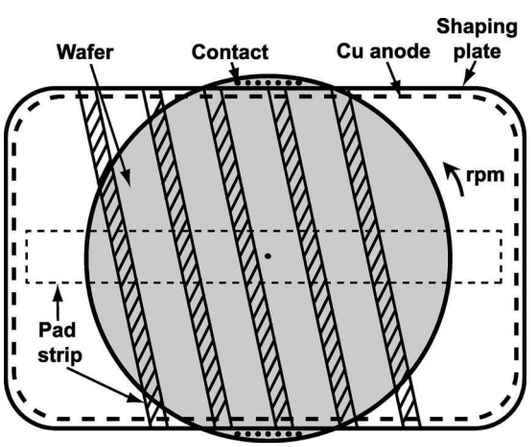

Figure 2. Top-view schematic of the ECMD cell used in this work.

surface touched the plating solution. For the ECMD process, the wafer surface was pushed against the surface of the planarization pad strip(s) at a preselected force level of about 0.8 psi and plating was initiated.

Patterned wafers of 200-mm-diam with pattern density of about 30% were used in this study. Substrates were sputter-coated with a 40-nm-thick Ta barrier layer and a 100-nm-thick copper seed before plating. An area with parallel lines was selected in each die for step height measurements and evaluation of mechanically induced bottom-up growth. This area had four 12-μm-wide trenches with 50-μm spacing between them. At the two ends there were regions with 33% pattern density and 2-μm-wide trenches, as can be seen in Fig. 6a. Feature depth for the patterned wafers was 500 nm. About 300-μm-long scans were taken from dies near the edge (80 mm away from the wafer center) and middle (60 mm away from the center) of the wafers using a Veeco Dektak 300-Si scanner system. The center of the wafer was not used for measurements because deposition was blocked in this area by the central part of the pad strip.

A high-acid copper sulfate electrolyte with 17 gm/L copper, 175 gm/L H_2SO_4, and 50 ppm Cl^- as well as a low-acid solution with 40 gm/L copper, 10 gm/L H_2SO_4, and 50 ppm Cl^- were used for the plating work. Cubath Viaform Suppressor, Cubath Viaform Accelerator, and Cubath Viaform Leveler available from Enthone were used in various concentrations as the organic additives. In some experiments wafers with copper seed layers were directly processed by ECMD. In other experiments a thin ECD layer was first deposited on the copper seed layers before the ECMD process was initiated. Yet some other wafers were first exposed to solutions containing organic additives and then processed by ECMD. In all cases, planarization efficiencies were measured and compared. In experiments where the nature and the concentrations of additives were changed, the plating cell was carefully cleaned and the copper anode was etched after each plating experiment and before introducing the electrolyte for the new experiment. This was found to be very important to avoid cross contamination of experimental baths by organic additives. Depositions were carried out on wafers galvanostatically. Wafers were translated by ±2 mm in the x-direction at a speed of 5 mm/s during processing with a single pad strip. In experiments employing a multistrip pad, translation was increased to ±25 mm at a speed of 50 mm/s to improve the uniformity of sweeping by the pad strips, especially near the center of the wafer. An FEI Expida 1265 focused ion beam-scanning electron microscopy (FIB/SEM) system was used to obtain cross sections of the plated layers for thickness measurement.

Results and Discussion

A set of copper surface profiles taken across 12-μm-wide trenches on four different wafers is given in Fig. 3. These wafers were plated under ECMD conditions using the single planarization pad strip and the high-acid plating chemistry, and the measurements were taken from the edge dies located about 80 mm away from the wafer center. In this study, 250-nm-equiv of copper was electroplated on each wafer rotating at 50 rpm using a current density of 20 mA/cm^2. The organic additive content of the bath, i.e., concentrations of accelerator (A) and suppressor (S), were varied to evaluate the relationship between the planarization capability of the ECMD process and the plating solution composition. The profile (a) in Fig. 3 is from a wafer plated in an additive-free electrolyte (A = 0 mL/L, S = 0 mL/L) and shows a rough top surface and excess copper deposition or pileup along the top edges of the measured trench. Ignoring the copper bumps at the top edges, the actual step height measured with respect to the wafer top surface is 5000 Å, indicating that the ECMD process did not achieve any planarization when copper was plated out of an additive-free electrolyte. The copper bumps that formed along the edges of the trenches point to the fact that the ECMD process of this work did not physically polish and remove copper from the surface. Otherwise, one would expect a mechanically polished flat copper layer surface free of the surface

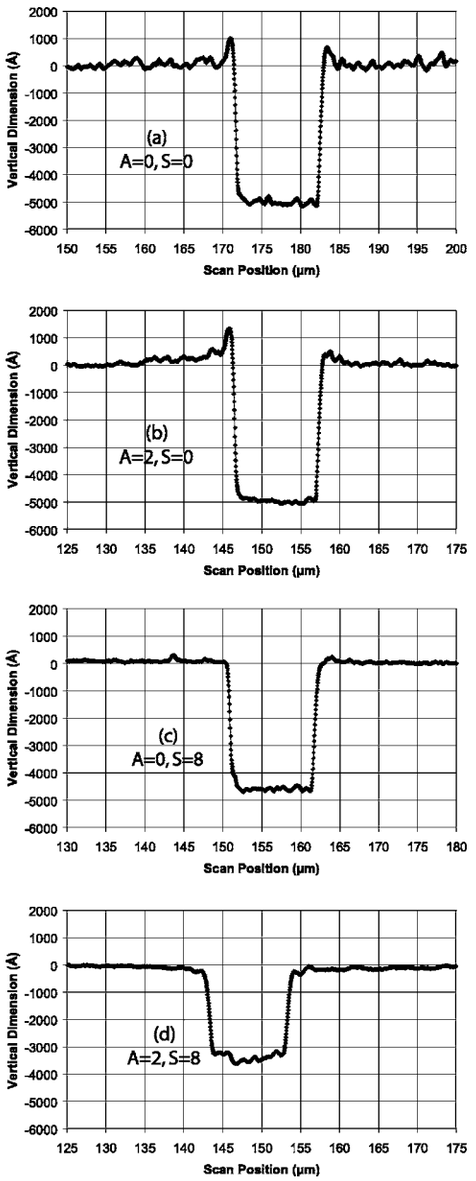

Figure 3. Surface scans taken across 12-μm-wide trenches on wafers processed by ECMD in high-acid electrolytes with accelerator (A) and suppressor (S) concentrations of (a) $A = 0$ mL/L, $S = 0$ mL/L, (b) $A = 2$ mL/L, $S = 0$ mL/L, (c) $A = 0$ mL/L, $S = 8$ mL/L, and (d) $A = 2$ mL/L, $S = 8$ mL/L. Starting step height was 5000 Å, and 2500 Å of copper was deposited during the ECMD process using a single planarization pad strip.

roughness and the protrusions at the trench top edge seen in the data of Fig. 3a. For wafers plated in suppressor-free electrolytes, we have typically seen pileup of copper deposit along the top edges of trenches which is due to current crowding at these sharp corners. Suppressor-containing electrolytes showed less pileup. Baths containing both suppressors and accelerators did not show any excess copper deposition along the top edges of the trenches.

The step-height measurement shown in profile (b) of Fig. 3 was for a wafer plated in a suppressor-free electrolyte that contained 2 mL/L of accelerator, i.e., an electrolyte composition of $A = 2$ mL/L, $S = 0$ mL/L. The copper pileup at the upper edges of the trench is still present in this data and the step height is 5000 Å, suggesting that there was no step height reduction and therefore no planarization by the ECMD process. As shown by profile (c) of Fig. 3, the ECMD process carried out in an electrolyte containing only 8 mL/L of suppressor, i.e., an electrolyte composition of $A = 0$ mL/L, $S = 8$ mL/L, resulted in a small reduction in the step height from 5000 to about 4600 Å. There is no copper pileup at the trench edges in this case, indicating improved suppression of current density at these sharp corners. The profile (d) of Fig. 3 was taken from a wafer plated in a bath containing both accelerator and suppressor species ($A = 2$ mL/L, $S = 8$ mL/L) and shows the largest reduction in the step height, which went from 5000 to 3400 Å. This corresponds to about 1600 Å of planarization within the trench upon plating of 2500 Å of copper by ECMD. The top surface of the Cu layer is also much smoother in this case compared to the film deposited out of the additive-free electrolyte. Wafers plated with the standard ECD process out of this electrolyte showed no planarization and a step height of 5000 Å.

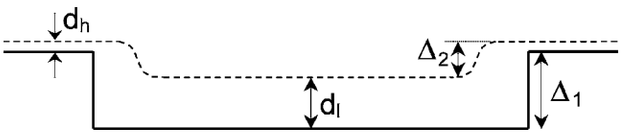

Figure 4. Copper profile evolution at a low-aspect-ratio feature during the ECMD process. Step height reduces from Δ_1 to Δ_2 as a result of ECMD. Copper thickness deposited into the feature, d_l, is larger than the copper thickness deposited on the top surface, d_h, in an ECMD process with planarization capability.

Figure 4 schematically shows how the ECMD process planarizes a low-aspect-ratio feature on a wafer. The initial step height over the large feature in Fig. 4 is Δ_1. After plating under ECMD conditions for a time period of Δt, the step height is reduced to Δ_2. During the ECMD process the copper thickness deposited on the top surface swept by the pad strip is d_h and the copper thickness deposited into the feature is d_l. From Fig. 4 it can be seen that reduction in step height, Δ, is given by

$$\Delta = \Delta_1 - \Delta_2 = d_l - d_h \quad [1]$$

and

$$d_l DA + d_h(1 - D)A = tA \quad [2]$$

or

$$d_l D + d_h(1 - D) = t \quad [3]$$

where D is the pattern density (ratio of the total feature area to total wafer area), A is the wafer area, and t is the total thickness of copper plated on the wafer surface based on the total charge applied to the surface. Equation 2 states that the total charge applied to the wafer during plating is distributed between the top surface area and the patterned area depending upon the planarization capability of the process. ECMD planarization efficiency, PE, is defined as

$$PE = [(d_l - d_h)/(d_l)] \times 100 \quad [4]$$

Solving Eq. 1 and 3 for d_l and d_h and substituting into Eq. 4, the planarization efficiency may be represented in terms of the measured step height reduction, pattern density, and the total charge-based copper thickness deposited on the wafer

$$PE = \{\Delta/[\Delta(1 - D) + t]\} \times 100 \quad [5]$$

Figure 5 shows the step height data and the calculated planarization efficiencies obtained from four wafers processed using the single-strip pad. Measurements were taken from dies near the edge and the middle of the wafers, and they represent average values from multiple dies at each location. As can be seen from Fig. 5, the electrolyte with no organic additives ($A = 0$, $S = 0$) yielded totally conformal copper deposition with no reduction in the original step height of 500 nm after the ECMD step. This is in-line with the ECMD mechanism model, which requires presence of additives to explain the accelerated bottom-up fill in large features. Likewise, the

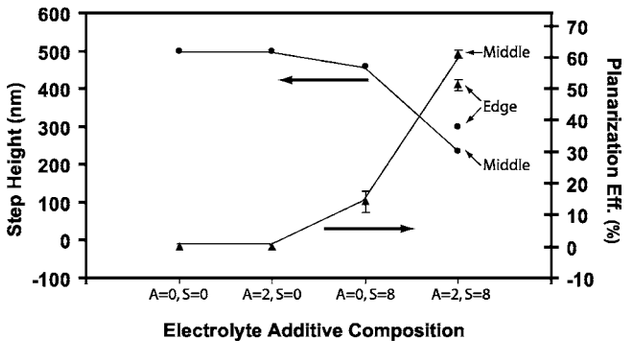

Figure 5. Step height and planarization efficiency as a function of electrolyte additive composition for an ECMD process employing a single planarization pad strip and high-acid electrolyte.

electrolyte containing only the accelerator ($A = 2$, $S = 0$) did not show any planarization capability. This is also understandable because the accelerator by itself, in the absence of suppressor, does not change the surface polarization appreciably, and therefore, any differential in the accelerator surface coverage that may be set by the pad sweeping cannot result in any appreciable differential in the plating current densities between the top surface and the cavities. What is interesting to note in Fig. 5 is the third data point, suggesting a small decrease in the step height to about 460–470 nm after ECMD of the copper in a solution containing only the suppressor ($A = 0$, $S = 8$). This suggests that the sweeping action by the pad strip actually improves suppression at the top surface compared to the cavity internal surface, however small the effect may be. The step height for the wafer plated in an electrolyte containing both the accelerator and suppressor ($A = 2$, $S = 8$) is reduced appreciably (to 235 nm at the middle and to 300 nm at the edge of the wafer), demonstrating good planarization due to superfilling of the features by the ECMD process.

The planarization efficiency numbers in Fig. 5 were calculated using a pattern density, D, of 0.3; charge-based plating thickness, t, of 250 nm; and measured step-height reduction amounts, Δ, of 0, 40, and 265 nm for the middle section of the wafers plated out of baths containing only accelerator, only suppressor, and both accelerator and suppressor, respectively. The planarization efficiencies corresponding to the three plating baths above were found to be 0, about 14, and about 61%. The step height reduction for the wafer plated in the electrolyte with the composition of (S = 8, A = 2) was 200 nm at the edge region of the wafer. This corresponds to a planarization efficiency of about 51%, which is lower than the planarization efficiency at the middle section of the wafer. For an ECMD process employing a single planarization pad strip as shown in Fig. 2, the observed decrease of the planarization efficiency toward the edge of the wafer is expected and was mathematically formulated in our previous work.[9] Accordingly, higher planarization capability is expected toward the center of the wafer because with a single rectangular planarization pad strip, the plating time-to-sweeping time ratio decreases toward the center of the wafer, i.e., plating time after the pad sweeps an area on the wafer is shorter toward the wafer center and the accelerator readsorption to the top surface is less due to more frequent pad sweeps. The reader is referred to Ref. 9 for a full mathematical treatment of this phenomenon.

Because the planarization factor, n, is defined as[9]

$$n = d_l/d_h \quad [6]$$

we can represent the planarization efficiency in terms of n by substituting Eq. 6 in Eq. 4

$$PE = (1 - 1/n) \times 100 \quad [7]$$

Using Eq. 7, n values for the data of Fig. 5 were calculated from the planarization efficiency values and they were found to be in the range of 2–2.6 for the wafer plated in accelerator and suppressor containing bath. These n values are somewhat lower than our previously published planarization factor data,[9] which showed n values in the range of 3–3.4 for similar locations on the wafer surface. There were, however, two major differences between the present experiments and the previously reported work: (*i*) the previous data set was obtained using wafers with a pattern density of about 20% compared to the present pattern density of about 30%, and (*ii*) in the previous experiments we had electroplated a 50-nm-thick copper film on the wafer surface by standard ECD technique before the ECMD process step was carried out. In the present experiments the ECMD process was initiated directly onto the copper seed layer without any prior ECD step.

A change in pattern density can affect the planarization factor, n, because under constant current plating conditions charge gets distributed to a larger cavity area for the wafer with the larger pattern density. This can be mathematically seen from the equation of planarization factor, n[9]

$$n = [it_p - (1 - D)(i_{h0} - i)(1 - e^{-ktp})/kD]/ [it_p + (i_{h0} - i)(1 - e^{-ktp})/k] \quad [8]$$

where i is the steady-state plating current density, k is a characteristic constant containing information about the chemistry and the accelerator adsorption rate on the copper surface, i_{h0} is the suppressed current density at the top surface of the wafer right after the surface is swept by the planarization pad strip and enters the electrolyte, and t_p is the plating time period between the sweeps by the pad. The derivative, or rate of change, of n with respect to D is proportional to $(-1/D^2)$, suggesting a reduction of n with increased D.

Possible influence of copper preplating on the planarization efficiency was checked by processing four additional wafers that first received 35 nm of copper plating under ECD conditions in a bath containing both accelerator and suppressor. This was then followed by 150 nm of copper deposition under ECMD conditions in the same electrolyte. The measured step-height after the ECMD step was in the range of 320–330 nm in the middle section of these wafers. Using Eq. 5, a pattern density, D, of 0.3, charge-based plating thickness, t, of 150 nm, and measured step height reduction amount, Δ, of 180 nm, the planarization efficiency for these wafers was calculated to be about 65%, which is higher than the 61% found for the wafers that received ECMD copper directly on their seed layers. The planarization factor corresponding to 65% planarization efficiency is about 2.9, which is closer to the finding of Ref. 9. Another experiment was carried out to clarify if the higher ECMD planarization efficiency observed for wafers preplated by an ECD process was due to the presence of the preplated copper layer on the surface of the wafer or simply because the wafer surface was exposed to the plating bath additives during the preplating period. This time four wafers with copper seed layers were immersed into the plating solution with ($A = 2$, $S = 8$) composition. No plating was carried out on the wafers during this immersion step, and then the wafers were planarized by ECMD in the same electrolyte. The planarization efficiency was again found to be about 65%. These results point to the fact that additives preadsorbed on the wafer surface may influence the planarization efficiency of the ECMD process. With the above discussion in mind, it is reasonable to assume that the planarization factors obtained in this study are comparable to those reported earlier, if one takes into account the effect of the increased pattern density and the effect of preplated copper on the planarization factor values.

The above experiments demonstrated that if the seed-layer-coated wafers were presoaked in an additive-containing solution before the ECMD process, planarization efficiency was improved. This suggests that if accelerators could be preferentially adsorbed onto cavity surfaces of a wafer and then this wafer is subsequently processed by ECMD, the planarization efficiency could be improved even further. One way to promote accelerator adsorption onto the

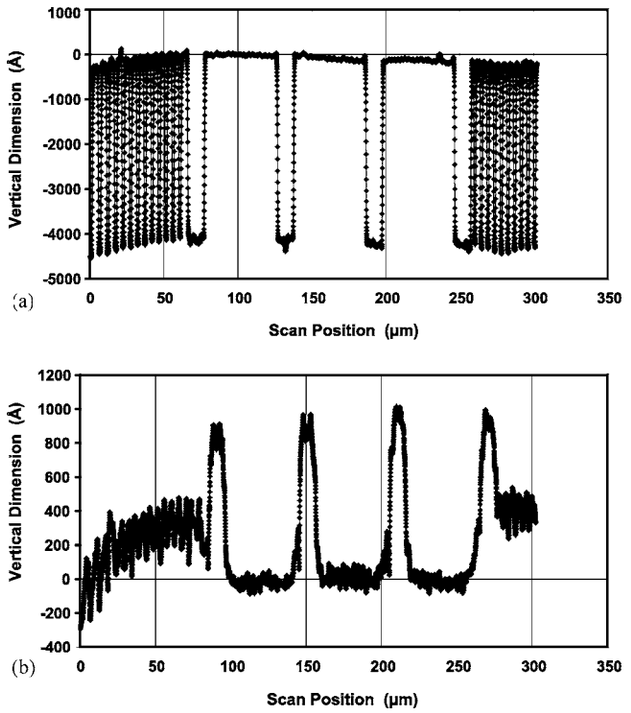

Figure 6. (a) Surface profile taken from a wafer after a first ECMD step that deposited 140 nm of copper out of a high-acid electrolyte with $A = 10$ mL/L and $S = 8$ mL/L. The step height at the 12-μm-wide trenches is about 400 nm. (b) Surface profile taken from the wafer of Fig. 6a after a second ECMD step that deposited 175 nm of copper out of a high-acid electrolyte with $A = 10$ mL/L and $S = 8$ mL/L. The step height at the 12-μm-wide trenches is about −100 nm, meaning the trenches are actually overfilled during the second ECMD step and "bumps" have been formed over the original trenches.

cavity surfaces is to perform a partial ECMD process on the wafer. Because in an ECMD process the surface coverage of the accelerator is higher within the cavities than on the top surface which is swept by the pad, accelerator adsorption onto cavity surfaces is expected to be more than the accelerator adsorption on the top surface. This hypothesis was tested by plating a 140-nm-thick copper layer by ECMD on a wafer surface in an electrolyte with a high accelerator concentration of $A = 10$ mL/L. The suppressor concentration was $S = 8$ mL/L. At the end of the plating period the wafer surface was swept by the pad for an additional 2–3 s to assure reduced accelerator content on the top surface before rinsing the wafer. After this partial ECMD step the wafer was rinsed by DI water and spin-dried. Figure 6a shows the surface profile taken from this wafer at an edge die location. The measured step height is about 4000 Å, suggesting a planarization efficiency of about 48% (see Eq. 5).

After the measurements, this wafer was again processed in the ECMD cell using the same electrolyte. This time 175-nm-thick copper was plated over the partially planarized wafer and the surface profile was again measured at the exact location of Fig. 6a. Figure 6b is the surface profile after the second ECMD step and it shows about 1000-Å-high protrusions over the originally 4000-Å-deep cavities. This is indicative of overplating at the cavity locations due to the preadsorbed accelerator surface concentration within the cavities which caused excessive copper deposition. If the planarization efficiency of the second ECMD step was equivalent to the planarization efficiency of the first step, i.e., if the planarization efficiency was 48%, the reduction in step height would be about 126 nm, which can be calculated from Eq. 5, $\Delta = (0.48)(0.7\Delta + 175)$, and $\Delta = 126$ nm. In other words, the step height would reduce from 400 to 274 nm after the second ECMD step. However, as the data in Fig. 6b shows, the step height actually is negative, i.e., there are protrusions instead of steps at the location of the trenches. If we assume that the total reduction of step height during the second ECMD step is the sum of the original step height and the height of the protrusion, i.e., 400 + 100 = 500 nm, then the effective planarization efficiency of the second ECMD process step can be calculated from Eq. 5 to be $PE = \{500/[(0.7 \times 500) + 175]\} \times 100 = 95\%$. This high efficiency is because the cavity surfaces of the partially plated wafer contained more adsorbed accelerator than its top surface before the second ECMD step was initiated. Higher surface concentration of accelerator within the cavities, therefore, increased the mechanically induced bottom-up growth rate during the second ECMD process.

The above findings and the data of Fig. 3, 5, and 6 are in agreement with our previously proposed model which explained the planarization capability of the ECMD process by the presence of both accelerator and suppressor species in the plating bath.[9] According to this model, pad sweeping removes at least part of the accelerators from the high surfaces. Therefore, right after sweeping when the swept area is exposed to the electrolyte and the plating current starts to pass, the fractional surface coverage of the accelerator at the swept top surface is lower than its coverage within the unswept cavity surfaces and the surface coverage of suppressor is high at the swept top surface. As a result, current preferentially flows into the cavities until the accelerator readsorbs at the top surface. Enhanced suppressor surface coverage right after the sweep by the pad may be explained by various mechanisms: (*i*) the pad sweep disturbs and minimizes the diffusion layer on the wafer surface and increases mass transfer, bringing more suppressor to the swept surface, (*ii*) the pad removes at least a portion of the suppressors along with the accelerators from the top surface; however, immediately after the pad sweep, suppressors adsorb on the freshly swept surface more strongly, partly because their concentration is higher in the solution compared to the concentration of the accelerators, and (*iii*) pad action pushes the film of the suppressor onto the copper surface, forming a more continuous film with better suppression properties.

As shown in Fig. 5, we have observed about 14% planarization efficiency for wafers ECMD-plated in electrolytes containing only suppressors. Work is in progress to determine the origin of this phenomenon and the findings will be the subject of a future publication. We now concentrate on the ECMD process carried out in electrolytes with the highest planarization capability, i.e., electrolytes containing both suppressor and accelerator species, and present data on the dependence of planarization capability on various process parameters.

As can be seen from Eq. 8, for an infinite plating time, t_p, between sweeps, the planarization factor approaches 1 and the planarization efficiency is zero. This is the case for ECD where there is no sweeping of the surface. As t_p is reduced, n and the planarization efficiency increase. To reduce t_p, the wafer rpm can be increased and/or a multistrip planarization pad can be used, as shown in Fig. 2. Once the planarization pad design and the process rpm are selected, the influence of other factors on the planarization capability of ECMD can be studied.

Figure 7 shows the dependence of the planarization efficiency on the electrolyte type and the concentration of the accelerator in the bath. A multistrip ECMD pad was used in these experiments to minimize t_p values. Planarization factors were calculated using the relationship given in Eq. 6. Planarization efficiencies were then calculated using Eq. 7. As can be seen from Fig. 7, planarization efficiencies are higher in high-acid chemistries, probably due to the higher activity of the accelerators in such electrolytes. There is a general improvement in planarization at higher accelerator concentrations within the process window tested. For the specific Cubath Viaform chemistries employed in this work, the typical accelerator concentrations used for standard ECD processes are 2 and 5–6 mL/L for the high-acid and low-acid electrolytes, respectively. Therefore, we have shown that in an ECMD process these concentrations may be approximately doubled to improve the planarization efficiency.

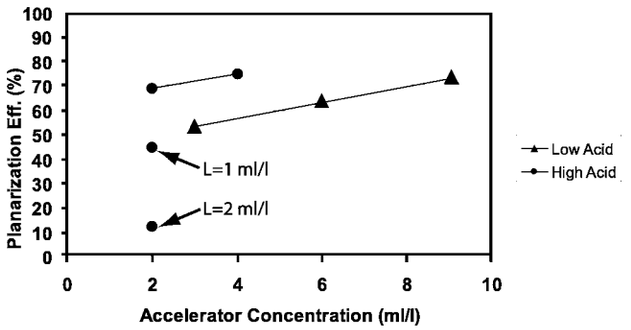

Figure 7. Planarization efficiency vs accelerator concentration in low-acid (LA) and high-acid (HA) electrolytes. The suppressor concentration was 8 mL/L and 2 mL/L for the HA and LA solutions, respectively. The two additional data points show the effect of leveler additive on planarization for the HA bath.

The effect of leveler additives on ECMD planarization was also studied by adding 1–2 mL/L of Cubath Viaform Leveler into the high-acid electrolyte with $A = 2$ mL/L and $S = 8$ mL/L. The two data points in Fig. 7 show that addition of 1 mL/L of leveler reduces the planarization efficiency of ECMD to about 45% and addition of 2 mL/L of leveler almost totally destroys the planarization capability in a high-acid bath. This result agrees with reports on the deleterious effect of levelers on ECMD planarization[8] and can be explained by the fact that leveler functions as a leveling additive by attaching itself to parts of the copper surface that receive high current density and suppressing growth there. This way, formation of protrusions is arrested and the copper surface is leveled. In the case of ECMD, as we have previously seen, cavities receive high current density due to the mechanically induced superfilling mechanism. However, this superfilling mechanism is suppressed in the presence of leveler because of leveler attaching itself to surfaces receiving high-current-density surface, i.e., internal surfaces of large cavities. Therefore, the ECMD process should be carried out in leveler-free electrolytes to achieve the highest planarization efficiencies.

Conclusions

Planarization efficiency of the ECMD technique was studied as a function of various process parameters. Planarization was found to be a strong function of the nature of the organic additives in the copper plating bath. While no planarization was observed in an additive-free bath and a bath containing only accelerators, a small degree of planarization was found in a bath containing only suppressors. The best copper layer planarization results and efficiencies over 70% were observed in plating electrolytes containing both accelerators and suppressors. This is in agreement with the mechanism of planarization for the ECMD process which works by establishing a differential in the relative surface coverage of accelerator and suppressor species. During sweeping by the planarization pad, accelerator surface coverage at the top surface is reduced and suppressor surface coverage increases, decreasing the current density at the top surface. During the plating period, more of the current flows into the cavities where the accelerator-to-suppressor surface coverage ratio is higher compared to the top surface. Addition of levelers into the plating bath was found to be detrimental for planarization efficiency. Planarization efficiency was found to increase with increased accelerator concentration within the process window used in this study. Higher planarization was observed in the high-acid electrolyte compared to the low-acid electrolyte.

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