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Planar Copper Plating and Electropolishing Techniques

B. M. BAŞOL, C. E. UZOH, H. TALIEH, T. WANG, G. GUO, S. ERDEMLI, M. CORNEJO, J. BOGART, AND E. C. BASOL

ASM NuTool Inc., Fremont, California

Electrochemical mechanical deposition (ECMD) is a novel technique that has the ability to deposit planar conductive films on non planar substrate surfaces. This technique involves electrochemical deposition (ECD) while simultaneously polishing the substrate surface. Preferential deposition of the conductor into the cavities on the substrate surface may be achieved through two different mechanisms. The first mechanism is more mechanical in nature and it involves material removal from the top surface. The second mechanism is more chemical in nature, and it involves enhancing the deposition into the cavities where mechanical sweeping does not reach and reducing deposition onto surfaces that are swept. In this study we demonstrate that in an ECMD process, low-pressure mechanical sweeping of the wafer surface during copper plating can establish a differential in the activity of the organic accelerator species between the surface and the cavity regions of the substrate and thus give rise to bottom-up filling in even the lowest aspect-ratio cavities. Planar layers obtained by the ECMD technique have been successfully employed in an electrochemical polishing technique for stress-free removal of Cu.

Keywords Copper; Electroplating; Electropolishing

Introduction

Electrochemically deposited (ECD) copper and copper alloys are important materials for integrated circuit interconnect and packaging applications (Edelstein et al., 1999). Copper's low resistivity value and high electromigration resistance make this material especially attractive for 90 nm and beyond technology nodes of integrated circuit manufacturing, where integration of electroplated Cu and low-k and ultralow-k dielectrics will be essential to further reduce the circuit time delay.

Figures 1(a) and 1(b) schematically show two of the critical steps of fabricating a damascene interconnect structure, namely electrodeposition and chemical mechanical polishing (CMP). The high aspect ratio lines, T_1 and T_2, and the low aspect ratio trench, T_3, shown in cross-sectional view in Figure 1(a) are etched into a dielectric layer. The whole patterned surface is then coated with a barrier layer such as a TaN/Ta stack. This is followed by the deposition of a Cu seed layer, which forms the conductive base upon which a thicker Cu layer can be electroplated. The barrier and seed layers are not shown in the figures for brevity. The three profiles P_1, P_2,

Address correspondence to B. M. Başol, ASM NuTool Inc., 3501 W. Warren Ave., Fremont, CA 94538. E-mail: bulent.basol@asm.com

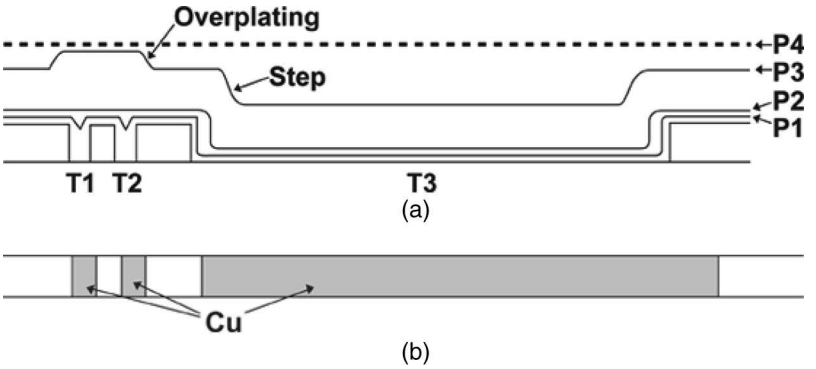

Figure 1. Copper interconnect structure after (a) electrochemical deposition (ECD) of Cu, (b) chemical mechanical planarization.

and P_3 in Figure 1(a) show the evolution of Cu film thickness as a function of time during electrodeposition. The small features, T_1 and T_2, quickly fill during the early stages of the ECD due to bottom-up growth. However, to assure complete filling of the large feature T_3, a copper thickness of at least 1.2 times the feature depth typically needs to be deposited on the wafer. The final Cu profile P_3 is non planar and it has a step over the large feature, step height being approximately equal to the depth of the feature. As shown in Figure 1(a), there may also be overplating above the dense small features (T_1, T_2). Such overplating can be reduced by employing special plating waveforms and electrolytes containing levelers.

The Cu overburden shown in Figure 1(a) and the barrier layer are typically planarized and removed using CMP with the goal of obtaining the ideal structure shown in Figure 1(b). A Post-CMP interconnect structure should have a flat surface and good electrical isolation between the wires formed in the cavities.

CMP is a costly process, much of its cost being attributable to the consumables such as the pad and the slurries, among others. Minimization of dishing, erosion, and defectivity are some of the technical challenges for the CMP process to overcome. As the technology incorporates the employment of porous ultralow-k dielectric materials with poor mechanical properties, the high force applied on the wafer surface during the CMP process becomes an issue. To avoid problems such as delamination, force applied on the wafer surface during the CMP process needs to be minimized, i.e., the mechanical component of the CMP process needs to be reduced and the chemical component needs to be enhanced. Planarization capability of the present CMP processes, however, depends on a delicate balance between their mechanical and chemical aspects. As the CMP process becomes more and more chemical in nature, its planarization capability typically deteriorates. As the force is reduced, on the other hand, removal rates go down. Therefore, it is a challenge to planarize copper layers under low stress conditions and at the same time meet the demand for a high throughput CMP process, using low-cost consumables.

One cost-effective technique that can be employed for the removal of Cu overburden from the wafer surface under extremely low stress is electropolishing. However, electropolishing or electrochemical polishing does not normally have substantial planarization capability, especially for large features with low aspect ratios, unless it is used in an electrochemical mechanical polishing (ECMP) mode

in conjunction with a planarization pad, which applies force on the wafer surface. If the Cu film with profile P_3 in Figure 1(a) were to be subjected to an electrochemical polishing process, the overburden above the small features would be effectively cleared. However, during this removal period the Cu layer portion over the large trench T_3 would also be removed at the same rate, causing excessive Cu loss from within this trench. Lack of significant planarization in large topographic features is one of the intrinsic challenges of the electropolishing approach.

The above discussions demonstrate that if the incoming Cu film was planar as shown by the dotted profile P_4 in Figure 1(a), then a highly chemical, low-stress CMP process or a stress-free electropolishing process could be employed to remove the already planarized Cu film. The recently developed ECMD technique has the unique capability of planarizing Cu layers on wafers with widely varying feature sizes (Talieh, 2001; Basol et al., 2002; Basol, 2003).

Electrochemical Mechanical Deposition of Copper

ECMD, as applied to copper deposition on patterned wafers, involves sweeping the surface of the wafer with a pad material as electroplating commences. Planar deposition or planarization may be achieved through different mechanisms. The first mechanism, which is operative at high pad pressures of $\gg 1$ psi, is mainly mechanical in nature, and it involves removal of Cu, through polishing, from the top surface of the substrate by an abrasive pad during deposition of material into the cavities as well as the top surface. The net Cu growth rate in the features is thus higher than on the top surface where material deposition as well as removal takes place. The second mechanism, which is operative at low process pressures, is chemical in nature, and it involves enhancing the deposition rate of Cu into the cavities where mechanical sweeping does not reach, compared to the top surface region that is swept by the pad. In this case no Cu is physically removed from the top surface. At intermediate pressures using highly abrasive pads it is possible to combine various aspects of the mechanical and chemical planarization processes described above. In this study we will concentrate on the low-force ECMD process, which has application to low-k and ultralow-k wafer processing at pressures of ≤ 1 psi.

A schematic of the plating cell used for ECMD is shown in Figure 2. The cell consists of a wafer holder to place the wafer face down into the plating electrolyte, an anode assembly to deliver the electrolyte onto the wafer surface, a Cu anode placed in the anode assembly, and a planarization pad/sweeper to sweep the surface of the wafer during ECMD. The pad consists of multiple strips that sweep the whole surface of the wafer when the wafer is moved. The plating cell of Figure 2 has the capability of pressing the wafer surface onto the pad surface at selected pressure values. The pad surface sweeps the wafer surface effectively as a cathodic voltage is applied to the wafer, which is rotated and also laterally translated on the multi-strip pad. The wafer has the copper seed layer extended all the way to the edge. Contact is made to the wafer edge at two locations on two sides of the anode assembly as shown in Figure 2.

A high-acid Cu-sulfate electrolyte was used in the experiments. The organic additive concentrations were varied in the electrolytes to study their influence on the ECMD planarization process. Electrolyte-I contained just the basic elements of Cu-sulfate (17 gm/L of Cu), water, sulfuric acid (170 gm of acid/L), and about 50 ppm of chloride. Electrolyte-II was obtained by blending 8 mL/L of CUBATH

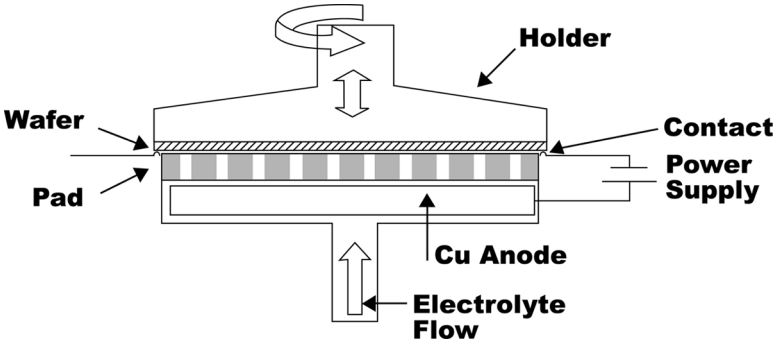

Figure 2. Schematic of an electrochemical mechanical deposition (ECMD) cell.

ViaForm Suppressor and 2 mL/L of CUBATH ViaForm Accelerator into Electrolyte-I. Trench wafers 200 mm in diameter with feature depth of 570 nm were used in the experiment. The dielectric was fluorinated silicate glass (FSG). A 30 nm Ta barrier layer and 60 nm Cu seed layer were deposited over the patterned surface. Plating was carried out using the plating cell of Figure 2, by pressing the wafer surface against the multi-strip pad at a pressure of about 1 psi. Total pad surface area touching the wafer surface was about 30 cm^2. The wafer was rotated at 50 rpm. Plating current was 3A, and the total charge passed was 5.3 A-min.

Figures 3(a) and 3(b) show the focused ion bean (FIB) cross sections obtained from two wafers plated with Electrolyte-I and Electrolyte-II, respectively. The trench shown in the FIB cross sections is 5000 nm wide. It should be noted that a thin W layer was deposited over the Cu surface before the FIB cross sections to improve the resolution of the Cu surface and thus measure the Cu layer thickness more accurately. This W layer appears as the dark section above the cross-sectioned Cu in the figures.

As can be seen from Figure 3(a), Electrolyte-I, which contained no organic additives, yielded a Cu layer with rough and nodular surface morphology. Many areas of the top copper surface appeared to be cold worked by the action of the pad. The Cu layer in Figure 3(a) is totally conformal within the 5000 nm wide trench despite the fact that the planarization pad was applied to the wafer surface at a pressure of about 1 psi. The thickness of Cu obtained from the cross section in Figure 3(a) is about 170 nm, which is lower than the estimated 200–300 nm based on the deposited charge and the approximate pattern factor of the wafer. This can be explained by the irregular nature of the film as is evidenced by the large nodules observed on the surface. Since the film was nonuniform, the local thickness measurement is not expected to be accurate. However, two important conclusions can be drawn from the data in Figure 3(a). First is the fact that under the specific experimental conditions used, there was no measurable physical material removal of Cu from the surface regions where the pad made contact with Cu. This is easily seen since Cu thickness on the surface region is about the same as the thickness at the bottom of the trench where the pad does not touch. It should be noted that it would be possible to remove Cu from the field regions by operating the ECMD process at higher pressures using highly abrasive pad surfaces. However, this was avoided in this work to demonstrate the capability of the process for planarization through chemical means at low pressures. The second conclusion that can be drawn from the FIB cross section of Figure 3(a) is the fact that under the specific experimental conditions employed here

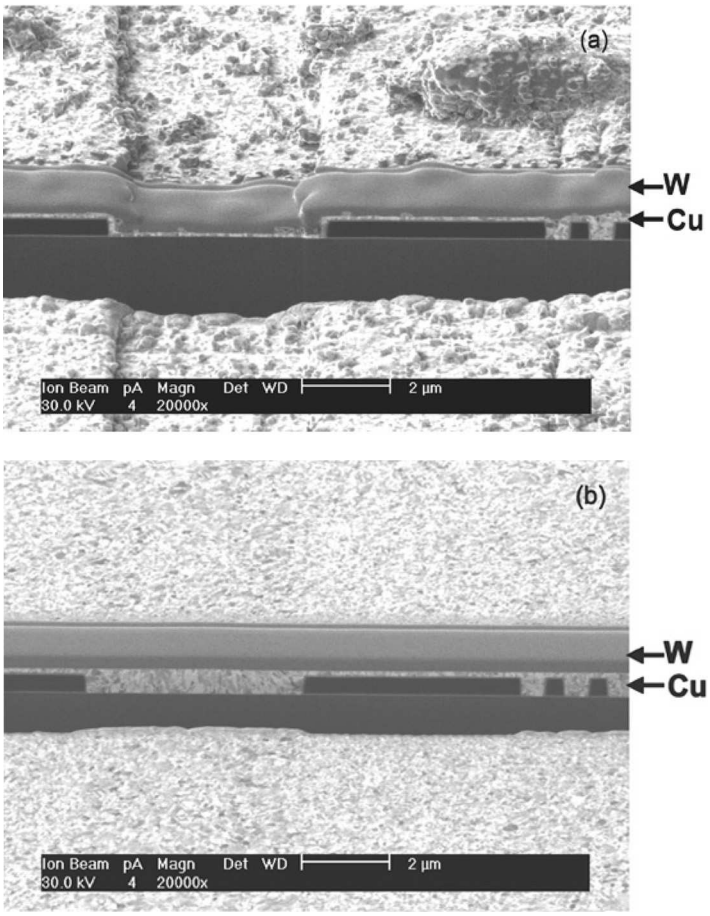

Figure 3. Cu layers obtained by ECMD approach at 1 psi using (a) an additive-free electrolyte, (b) an electrolyte containing organic suppressor and accelerator additives. A tungsten (W) layer is deposited on part of the surface before the FIB cut to obtain better resolution of Cu thickness.

ECMD did not yield bottom-up Cu growth in the large features when an electrolyte, which was free from organic additives, was employed. Deposition rates of the material onto the top surface regions and onto the bottom surface of the trench were very similar, yielding a conformal deposit. Therefore, physical masking of the top surface by the pad is not an appreciable factor in the experiment.

Figure 3(b) shows the FIB cross section taken from the wafer plated in Electrolyte-II under exactly the same processing conditions used for the wafer of Figure 3(a). The resulting Cu film has smoother surface morphology despite the mechanical action of the pad on its surface. The second observation from Figure 3(b) is the perfect planarity of the deposited film. Since physical removal of Cu from the top surface and possible masking effect by the pad have already been eliminated as possible mechanisms of planarization, the result of Figure 3(b) can attributed only be to the presence of organic additives in the electrolyte, which promote super-filling of the low aspect ratio features under the action of the

planarization pad. It should be noted that although the data shown in Figure 3(b) is for a 5000 nm wide trench, the same planarization was observed and measured for trenches as wide as 100,000 nm on the same wafer.

Planarization Mechanism

It is very important in interconnect fabrication to fill high aspect-ratio vias and trenches with good quality, defect-free copper. Conformal copper deposits, where growth initiates uniformly from the side and bottom walls of such features, yield voids and seams. Copper ECD electrolytes employ chloride ions, suppressors, and accelerators to promote smooth morphology of the deposited films and bottom-up filling or super-filling of the high aspect-ratio features. A third organic additive, leveler, may be added to the electrolyte composition to improve within-die uniformity by suppressing overplating at sites with a high density of small features. There have been various models offered to explain the bottom-up growth mechanism in high aspect ratio features. According to one model, super-filling in small features is driven by the establishment of a diffusion gradient of suppressing polymers (Andricacos et al., 1998). Initially, deposition into the features may start in a conformal manner since the accelerator and suppressor species are distributed relatively uniformly on the surface regions as well as on the inner walls of the features. As Cu grows and the gap between the feature walls gets smaller, accelerator-to-suppressor concentration ratio increases within the narrow gap. This additive gradient gives rise to an accelerated growth rate from the bottom of the feature and the gap is filled without closing off the entry to the feature and thus causing defects such as voids. More recent publications proposed a ''curvature enhanced accelerator coverage'' mechanism to explain and model the super-filling process within narrow gaps (Moffat et al., 2001). One other model suggested that consumption of chloride in the narrow gap reduced the effectiveness of the suppressor at that location, causing higher deposition rate and thus bottom-up growth (Hayase et al., 2002). In any case, the super-filling mechanism of Cu in high aspect ratio features is due to interaction of chloride ions, suppressor, and accelerator molecules, such that the effectiveness or concentration of the suppressor is decreased and the effectiveness or concentration of the accelerator is increased within the narrow gap. As can be appreciated, Cu deposition into large features with aspect ratios $\ll 1.0$ progresses in a very different fashion. For such structures accelerator, suppressor, and chloride species can diffuse freely in and out of the features and therefore are uniformly adsorbed on all surfaces. Furthermore, curvature-enhanced accelerator coverage mechanism is not applicable within such large features. This gives rise to conformal deposition and the Cu layer profile P_3 over the feature T_3 as shown in Figure 1(a).

Planar deposition of Cu observed in Figure 3(b) indicates that in the (ECMD) process, planar film surface formation is achieved through accelerated growth of Cu in the large feature. In other words, low-pressure mechanical sweeping of the wafer surface during copper plating establishes a differential in the concentration or activity of the organic additive species between the surface and cavity regions of the substrate and thus gives rise to bottom-up filling in even the lowest aspect ratio cavities. In a previous study we had investigated the evolution of planarization in an ECMD process and found that the average deposition rate of Cu into the large features may be as high as approximately six times its deposition rate onto the surface region, i.e., the planarization constant could be as high as six

(Basol et al., 2002). Mechanical action on the wafer surface may give rise to bottom-up fill in low aspect ratio features by various different mechanisms. For example, the sweeping pad may affect the adsorption of the accelerator on the top surface. If the accelerator is preferentially swept from the top surface, metal growth rate in the field region may be suppressed compared to the trench region. Alternatively, the close proximity of the pad and vigorous mass transfer may improve accelerator adsorption or increase accelerator concentration within the trench. The end result from both cases would be more suppression in the field region compared to the trench and therefore bottom-up growth within the trench. In our experiments we made the observations that (a) the best planarization in the process was obtained when both accelerator and suppressor was present in the electrolyte and (b) the planarization constant increased with increased accelerator concentration. A detailed discussion of the ECMD planarization phenomenon and a proposed mathematical model based on accelerator surface coverage differential can be found in Basol (2004).

The chemical nature of the planarization process in ECMD was further supported by the relative insensitivity of the planarization efficiency to variation in the area of the planarization pad and the wafer rpm. If the planarization process were mostly mechanical in nature, i.e., if removal of Cu from the field region was mainly responsible for the observed planarization, then increased pad area and increased rpm, which translate into increased mechanical action on the wafer surface, would improve planarization efficiency. This was not the case, as will be discussed next.

Figure 4 shows data collected from a series of wafers processed at various rpms, keeping the rest of the ECMD process parameters constant. For efficient planarization, the wafers were also moved in a lateral direction at a speed of about 5 cm/sec during this experiment. Copper field thickness (t_{Cu}) was measured after complete planarization at the center, middle, and edge dies of the wafers near isolated large

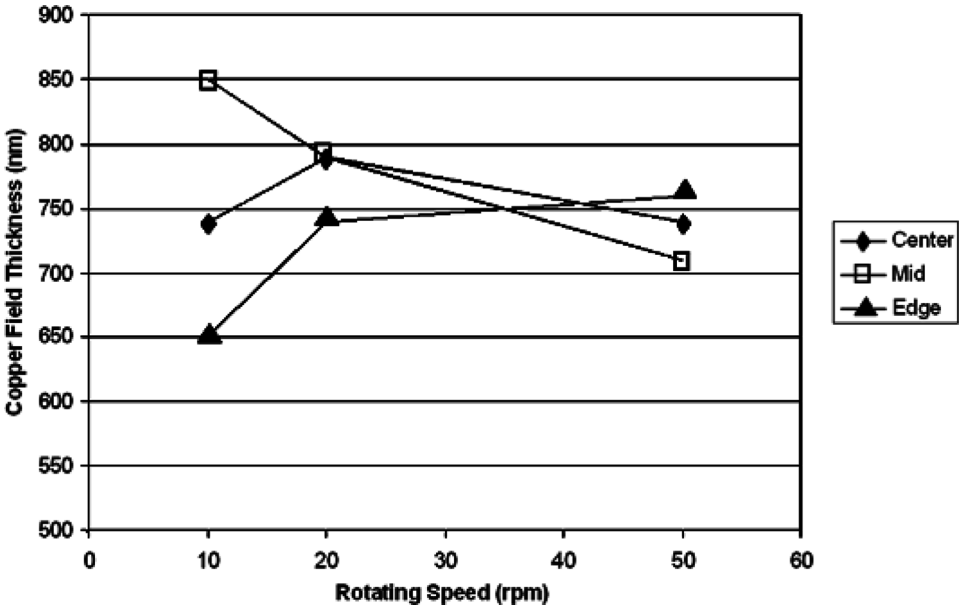

Figure 4. Effect of wafer rotation (rpm) during ECMD process on the field Cu thickness.

trenches. Keeping the total plating charge constant, the thickness difference measured at the field regions of the wafers was within the uniformity range of the samples for rpms larger than 20, indicating that there was no appreciable change in the planarization efficiency. Similar measurements made by changing the pad surface area in the 30–150 cm^2 range showed that planarization efficiency was not a strong function of the pad area either, but that there was a minimum mechanical action required on the wafer surface for the process to work. This can also be seen from Figure 4, where rpm values of smaller than 20 caused considerable scattering in the data. It should be noted that we achieved planarization using only 10 cm^2 area pad, i.e., only 3% of the wafer surface area, provided that rpm was higher than 20. This is contrary to experience in processes that are more mechanical in nature, such as CMP. In CMP processes pressure, rpm, and pad area would play a strong role in determining material removal rates. In ECMD we observed uniform planarization over the whole wafer surface for pressures in the range of 0.2–1.0 psi. Below 0.2 psi nonuniformities were observed due to incomplete contact between the pad surface and the wafer surface for the setup used in these experiments. Lack of a strong relationship between planarization efficiency and pressure indicates once again that the process is not highly mechanical in nature, as is the case for CMP.

Figure 5 schematically shows the time evolution of the Cu film profile during ECMD process at a trench with a depth "d" and width "W." The growth rate of Cu at the top surface is "g" and the growth rate from the bottom and side walls of the trench is assumed to be "G." Planarization constant "n" is defined as the ratio "G/g." It is straightforward to calculate that when planarization is complete:

$$Gt_p = d + gt_p, \quad t_p = d/(G - g) = d/[(n - 1)g] \tag{1}$$

where t_p is the planarization time. Accordingly the thickness of Cu deposited by ECMD on the top surface, t_{Cu} can be calculated

$$t_{Cu} = gt_p = d/(n - 1) \tag{2}$$

for large features with width of

$$W > 2Gt_p = 2ngt_p = 2nd/(n - 1) \tag{3}$$

For smaller features, planarization is complete when

$$2Gt_p = W = 2ngt_p, \quad t_p = W/2ng \tag{4}$$

Surface Cu thickness in this case would be W/2n. The FIB cross section of Figure 3(b) has three sub micron-size trenches in the field of view. It is interesting to note that no seams are seen in these small features.

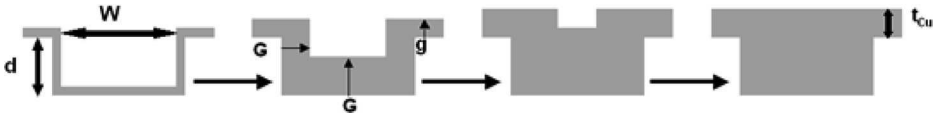

Figure 5. Schematic demonstration of the Cu film profile evolution as a function of time for a low aspect ratio trench during ECMD process.

For the sample of Figure 3(b), d = 570 nm and W = 5000 nm. Assuming a planarization constant of 6, the factor (2nd/(n − 1)) of Equation (3) is smaller than the trench width. Therefore the Cu thickness due to ECMD at the top surface upon planarization can be calculated from Equation (2) to be 114 nm. With 60 nm of seed layer under the electroplated Cu, the total thickness expected is around 170 nm. The copper thickness measured from the cross section of Figure 3(b) is about 190 nm, which is within the accuracy of our measurement. Present work concentrated on fully planarized Cu layers. Careful partial plating studies made on thicker Cu films deposited by the ECMD process demonstrated that the pad action on the wafer surface suppresses current in the field regions while enhancing current within cavities. In other words, ECMD reduces Cu deposition on the field regions while enhancing Cu deposition into the wide cavities compared to standard ECD. Details of this study can be found in Basol (2004).

Electrochemical Polishing

Planar Cu deposits obtained by the ECMD process were electrochemically polished using a cathode assembly similar to the one shown in Figure 2. No planarization pad was mounted over this cathode. A phosphoric acid based solution was employed for electropolishing the planar wafers at current densities in the range of 50–100 mA/cm^2. The resulting surface was mirror finished with a roughness of around 5 nm. The average Cu removal rate was in the range of 300–800 nm/min depending on the current density, electrolyte temperature, and the rpm used. Figure 6 shows the Cu removal profiles obtained from electropolishing in solutions with temperatures varying from 27° to 49°C. All other process parameters were fixed in these experiments and polishing was carried out for a period of one minute. As can be seen from the data of Figure 6, material removal non uniformity was <2%

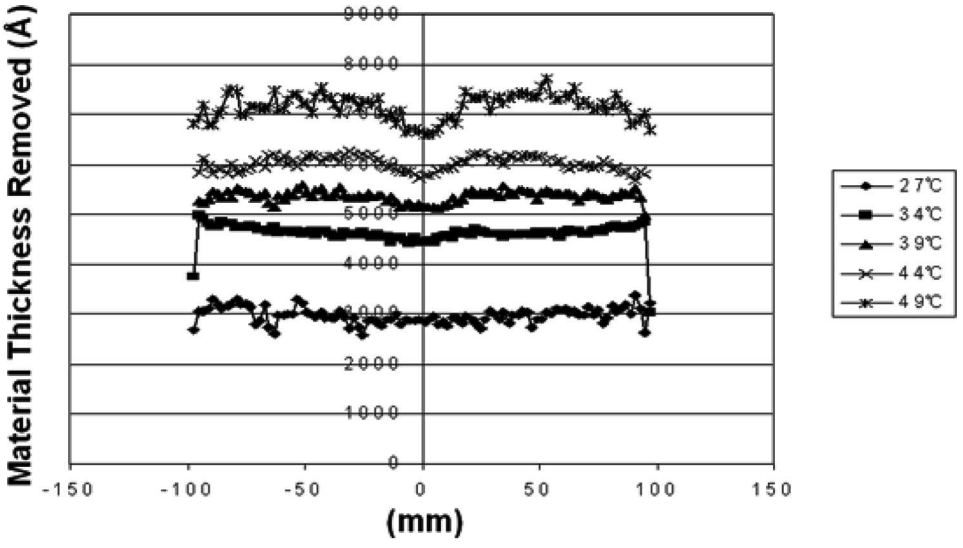

Figure 6. Copper removal profile for electrochemical polishing process carried out on flat Cu layers obtained by the ECMD technique.

(one sigma) for optimized process conditions and the removal rate increased sharply from 300 nm/min to over 700 nm/min with increased temperature.

The FIB cross sections of a wafer that was first planarized by the ECMD process and then polished by the electrochemical technique are given in Figures 7(a) and (b). The data in Figure 7(a) shows 1 μm thick planar Cu layer obtained by the ECMD technique. Although not shown in this micrograph, pads as large as 50 μm size were also planarized on this wafer. The cross section in Figure 7(b) was taken from the same wafer, near the same location after removing all but about 0.1 μm of the Cu film. What is interesting to note is that the electropolishing step removed the Cu

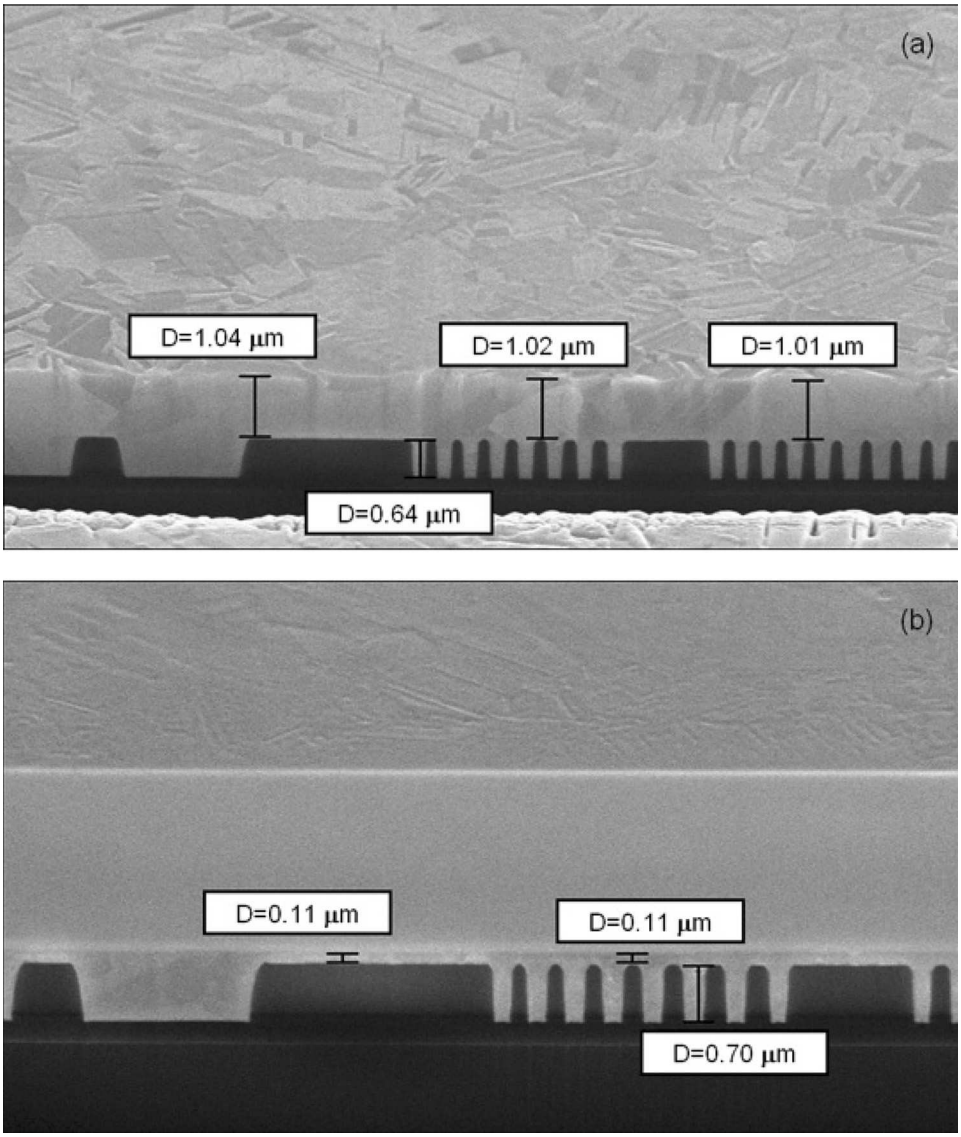

Figure 7. FIB cross sections of a wafer after (a) Cu layer planarization by ECMD technique and (b) Cu electropolishing down to about 100 nm thickness.

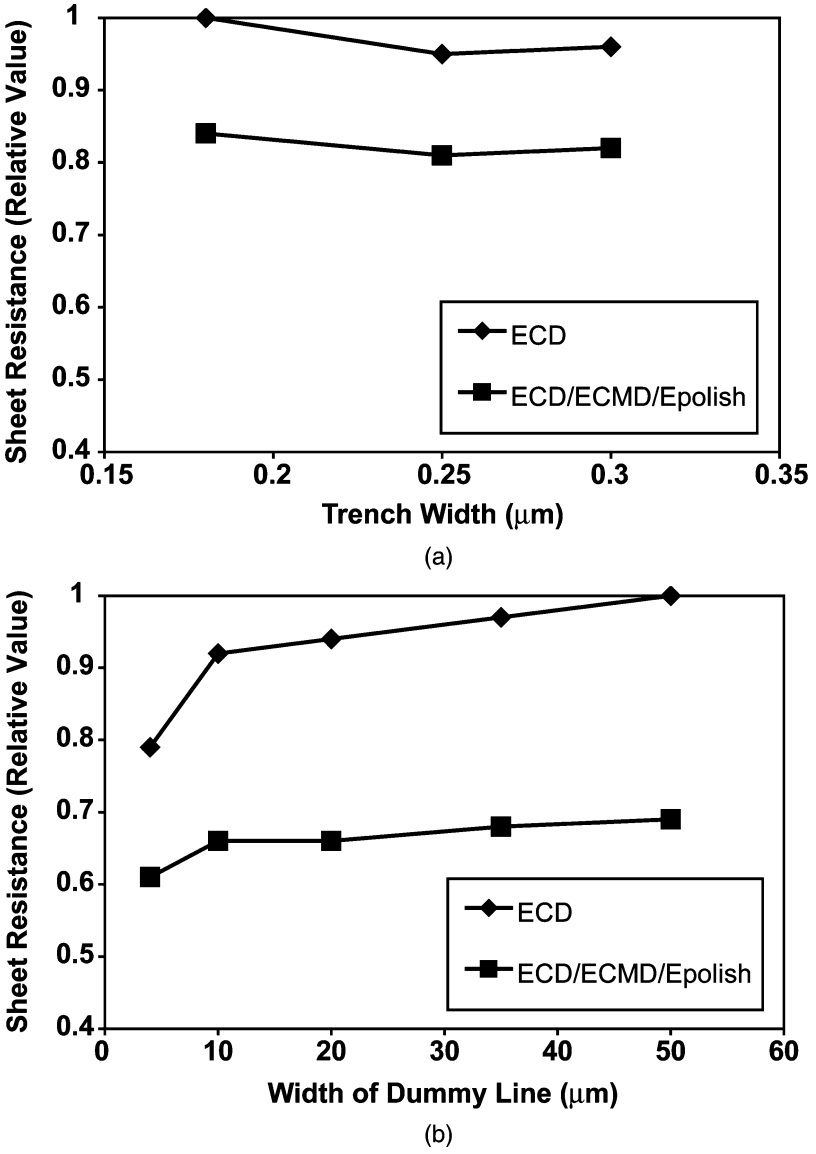

Figure 8. Post-CMP electrical data showing (a) relative sheet resistance as a function of trench width for isolated Kelvin resistor structures, for two wafers, one with a 1.0 μm thick ECD Cu layer and the other with a 0.2 μm thick planar Cu layer, (b) relative sheet resistance as a function of dummy feature width for dense Kelvin resistor structures for two wafers, one with a 1.0 μm thick ECD Cu layer and the other with a 0.2 μm thick planar Cu layer. Trench width for the structure measured was 0.18 μm.

layer in a planar fashion and uniformly irrespective of the density of the features underneath. This is a unique strength of a process employing ECMD planarization followed by low-cost electrochemical polishing steps. It should be noted that electrochemical polishing may be continued to remove all Cu from the wafer surface,

including the seed layer. However, since electrochemical removal is highly uniform, the limitation to go all the way to the barrier is mainly due to the total thickness range on the wafer surface, which may be in the 30–80 nm range.

Some of the technical benefits of a thin and planar Cu layer can be seen from the post-CMP electrical data of Figures 8(a) and (b), which were obtained from 48 dies on the tested wafers. Figure 8(a) shows the relative Cu sheet resistance values for two wafers, one with a standard 1 μm thick ECD Cu layer and the other with a nominally 0.2 μm thick flat Cu obtained by the (ECMD + electropolishing) process sequence described above. For sheet resistance we have taken the values at the 50% point of the cumulative probability curves. The data were collected at isolated Kelvin resistor structures as a function of the line width (0.18 μm, 0.25 μm, and 0.30 μm), showing more than 15% reduction in the sheet resistance value for the wafer with thin flat Cu layer. Although not shown here, one other observation made was the fact that the within-wafer sheet resistance distribution was tighter for the wafer with thin flat Cu than for the ECD wafer. Data in Figure 8(b) were collected at dense Kelvin resistor structures with a fixed line width of 0.18 μm, and they are presented as a function of the width of dummy features at the two sides of the resistor line. As expected, the sheet resistance increased as the dummy features got wider since total metal loss due to dishing and erosion increased. This increase, however is much less for the case of thin flat Cu, and the overall sheet resistance values are 20–35% lower than those of the wafer with ECD Cu. It is interesting to note that the improvement in sheet resistance gets larger as the dummy features of the test structure get wider. All these electrical results are indicative of less Cu loss for the wafer with thin flat Cu, which in turn is due to the reduction of Cu CMP overpolish time, which was about 40% of the Cu polish time. To assure that lower overpolish times for the wafer with thin flat Cu did not result in Cu residues at dense areas, bridging structures were tested for line-to-line leakage for both of the wafers. Leakage current values were in the 1×10^{-11}A range for both wafers, indicating that the thin flat Cu was indeed properly cleared off the top of the dense features with reduced overpolish time compared to the ECD wafer.

Conclusions

The electrochemical mechanical deposition (ECMD) technique has been described for planar deposition of copper on nonplanar surfaces. It was shown that the planarization mechanism of ECMD requires the presence of organic accelerator and suppressor species in the electrolyte and that this mechanism involved bottom-up growth of Cu in even the largest features with low aspect ratios. Bottom-up growth in the ECMD process is achieved by the use of a planarization pad, which sweeps the wafer surface during Cu deposition and thus establishes a gradient in the additive activity between the cavities and the surface regions. Planar layers obtained by the ECMD process offer advantages over CMP process, especially for low-force approaches with lower planarization capability. Planar films also make it possible to employ the electrochemical polishing technique for Cu overburden removal, which is a truly low-cost and stress-free approach with possible application to porous low-k integration. Post-CMP electrical data obtained from wafers with thin planar Cu layers showed lower metal loss than wafers with standard Cu films obtained by the ECD technique.

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