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Hydrogen silsesquioxane-based hybrid electron beam and optical lithography for high density circuit prototyping

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The authors report on a hybrid lithography process that integrates electron beam lithography (EBL) and optical photolithography. To maximize resolution and density, the EBL exposure is performed using a hydrogen silsesquioxane-based resist, while the photolithographic exposure is performed using standard positive or negative tone 248 nm photoresists. Both exposures take place on a common underlayer consisting of an antireflective coating (ARC). During pattern transfer into the ARC layer, a composite image of the two lithographic exposures is formed creating a robust and versatile etch mask for further pattern transfer into the substrate. They demonstrate the utility of this technique by using it to pattern the active, gate, and wiring levels of complementary metal oxide semiconductor devices and circuits consisting of trigated Fin-based field effect transistors. These devices have a minimum active area pitch of 50 nm, minimum gate pitch of 90 nm, and achieve densities suitable for 15 nm node static random access memory cells. Details of the exposure process and device fabrication are discussed along with electrical results from the resulting devices and circuits built using this technique. © *2009 American Vacuum Society.*
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I. INTRODUCTION

Hybrid lithography is a term broadly applied to the use of two or more lithography techniques to create a composite pattern. A variety of methods to combine photolithography and electron beam lithography (EBL) in a common layer of chemically amplified resist have been reported.[1–5] These techniques leverage the flexibility and high resolution patterning capabilities of EBL while capitalizing on the high throughput nature of photolithography. The presence of both images in the same layer of resist enables the use of a single process for pattern transfer into the underlying substrate. This avoids any increase in process integration complexity after lithography relative to process flows involving a single lithographic exposure technique. For these reasons, hybrid lithography has proven particularly useful in the prototyping of advanced complementary metal oxide semiconductor (CMOS) devices and circuits[1–3] as well as devices for data storage.[5]

Using a chemically amplified resist for hybrid lithography is not without limitation. Identifying a process window where both exposures are optimized can be challenging. Furthermore, the use of chemically amplified resists limits the ultimate resolution and density of the EBL patterning when compared to less sensitive, higher contrast materials. In particular, recent reports of ultrahigh resolution EBL exposures in resists based on hydrogen silsesquioxane (HSQ) have shown results that far surpass what is possible using chemically amplified resist materials.[6]

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Optical exposures of HSQ-based resists have been reported using 157 nm (Ref. 7) and extreme ultraviolet (EUV) sources.[8] Unfortunately, lithography tools operating at these wavelengths are not in widespread use at this time, limiting the pursuit of this approach. To circumvent this dilemma, we report a strategy for integrating EBL exposures performed with HSQ-based resists and photolithographic exposures performed in commercial positive or negative tone photoresists. Both resist processes are performed on a common underlayer consisting of an antireflective coating (ARC), resulting in the formation of a composite image during pattern transfer. The composite image provides a robust and versatile etch mask for further pattern transfer that can be removed using conventional wet and dry polymer stripping techniques. Moreover, this process integrates both lithography techniques without compromising the resolution of either one or increasing the complexity of the postlithography pattern transfer process. We demonstrate the utility of this technique by using it to pattern the active, gate, and wiring levels of CMOS devices and circuits consisting of trigated Fin-based field effect transistors (FinFETs). Details of the exposure process and device fabrication are presented along with the electrical data obtained from the resulting devices and circuits.

II. HYBRID LITHOGRAPHY PROCESS

An overview of the HSQ-based hybrid lithography process is shown in Fig. 1. Substrates used in this work consisted of 200 mm diameter Si or Si on insulator (SOI) wafers that were patterned with an alignment mark level composed of 1 μm deep etched features. This layer was necessary to register the EBL and optical exposures to each other for

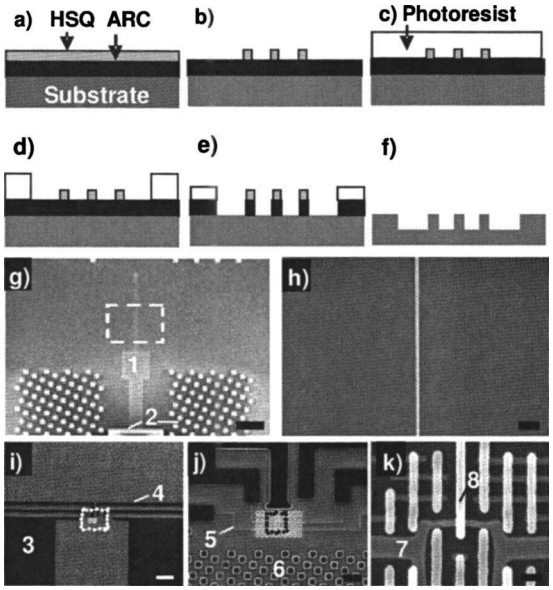

FIG. 1. [(a)–(f)] Overview of the HSQ-based hybrid lithography process. (g) SEM images of a composite pattern printed using HSQ (1) and UV110G (2) on AR3G. The scale bar corresponds to 4 μm. The region of interest (ROI) highlighted in (g) is shown in (h). The CD of the HSQ line is 25 nm. The scale bar in (h) corresponds to 200 nm. (i) SEM image showing an example of a two-level pattern after pattern transfer printed using HSQ and TDUR N700 showing (3) probing pads and (4) coarse interconnects printed by photolithography. The ROI highlighted in (i) is shown in (j), displaying (5) interconnects printed by EBL and (6) fill features printed by photolithography. The ROI in (j) is shown in (k), displaying (7) active area and (8) gate level features patterned with EBL. The scale bars in (i)–(j) are 10, 2, and 0.1 μm, respectively.

single or multiple patterning events. The substrates were coated with an ARC. This layer served as a common medium for mixing the subsequent EBL and optical lithography exposures during postlithography pattern transfer.

Three ARC materials were evaluated for this study, a 248 nm polymer ARC (AR3G, Rohm and Haas), a 248 nm Si containing polymer ARC (SiARC, SHBA 470, Shinetsu), and a proprietary plasma deposited ARC composed of amorphous carbon nitride (ACN). A summary of their properties is provided in Table I. The selection of this layer is governed by many factors including pattern resolution requirements, substrate topography, and the postlithography pattern transfer process. For the purposes of this discussion AR3G will be used as an example.

AR3G was spin cast onto the substrate and subjected to a two-step postapply bake (PAB) of 140 °C for 60 s, followed by 225 °C for 60 s. A HSQ-based EBL resist [XR1541, Dow Corning, Fig. 1(a)] was deposited onto the substrates by spin casting. HSQ films ranging from 20 to 40 nm were selected for this work. Substrates were exposed using a Vistec VB6 operated at 100 keV with a 5 nm pixel size and a 600 μm main field size. All exposures were performed using proximity effect corrected patterns prepared using the method described by Rooks *et al.*[9] Typical feature doses ranged from 12 to 16 mC/cm^2. Consequently, a beam current of 10 nA was selected to enhance exposure throughput. This choice of beam current had no noticeable impact on the resolution of exposures with features ranging in pitch from 40 to 200 nm. Following exposure, the substrates were developed using a standard 0.26*N* developer [OPD 7262, Fujifilm, Fig. 1(b)] for 4 min in a double puddle process on a conventional track coat and bake system (Mark 8, Tokyo Electron Limited). To maximize contrast, a PAB and postexposure bake (PEB) for the HSQ were omitted.[10]

The integration of broadband photoresist with previously exposed HSQ patterns formed directly on a substrate without an underlayer was demonstrated by Baek *et al.*[11] In that work, it was found that the photoresist processing had negligible interaction with the underlying HSQ pattern. In the present work, we found this also to be true for commercially available positive and negative tone 248 nm resists. While a number of resists were explored for this work, we will limit the discussion to a single resist of each tone. UV110G (Rohm and Haas) was used for positive tone exposures. A 450 nm thick film was deposited and processed with a PAB of 135 °C for 60 s and a PEB of 130 °C for 90 s. TDUR N700 (TOK) was used for negative tone exposures. A 700 nm thick film was deposited and processed with a PAB of 100 °C for 60 s and a PEB of 110 °C for 90 s [Fig. 1(c)]. All optical patterns were exposed using an ASML PAS 5500 248 nm stepper [Fig. 1(d)]. The presence of the ARC avoided the need for additional substrate preparation prior to photoresist coating and enabled the resists to be processed without modifying the baking, exposure, or develop conditions practiced for standard photolithographic exposures.

Postlithographic pattern transfer was performed using reactive ion etching (RIE). The ARC layer was etched using a $N_2/O_2/C_2H_4$ RIE chemistry. This chemistry is selective to the HSQ layer, allowing it to serve as an etch mask during the AR3G etch. Although this chemistry is not selective to photoresist, the thickness of the resist was sufficient to survive this process. Pattern transfer into the substrate using additional RIE processes was performed at this time [Figs. 1(e) and 1(f)]. The composite HSQ/ARC bilayer provides a robust mask for the etching of a variety of semiconductor, dielectric, and metal materials similar to the scheme demonstrated by Van Delft *et al.* using a HSQ/novolak resin bilayer.[12] Post-RIE removal of any remaining masking mate-

TABLE I. Summary of ARC properties evaluated for HSQ-based hybrid lithography.

Material	Deposition	Conformality	HSQ adhesion	Pattern transfer
AR3G	Spin casting	Planarizing	Good for CD > 15 nm	Selective to HSQ
SiARC	Spin casting	Planarizing	Excellent	Non selective to HSQ
ACN	PECVD	Nonplanariazing	Excellent	Selective to HSQ

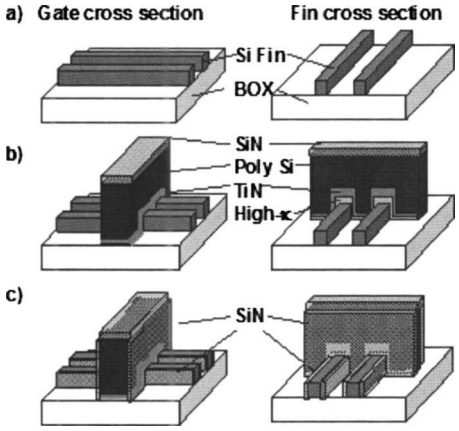

FIG. 2. (a) Process flow for the devices fabricated for this work. HSQ-based hybrid lithography and RIE were used to define active Si regions, referred to as fins. (b) A multilayer gate stack is deposited over the fins and patterned using HSQ-based hybrid lithography followed by RIE (b). (c) A SiN offset spacer was formed through chemical vapor deposition and RIE. Junction, silicide, contact, and wiring formation processes are not shown.

rials was conducted using a conventional O_2-based dry stripping process. The HSQ layer was typically consumed during RIE into the substrate or undercut by the removal of the ARC layer during the dry stripping process. Consequently, wet or dry stripping processes specifically tailored for HSQ removal were not required.

An example of a composite pattern consisting of HSQ and UV110G is shown in Figs. 1(g)–1(i) patterned with a bright field mask. An example of a two-level field effect transistor (FET) structure fabricated using the HSQ-based hybrid lithography scheme is shown in Figs. 1(g)–1(i) where the photolithography was performed using dark field masks and TDUR N700.

III. DEVICE FABRICATION

Fully depleted (undoped channel) trigated FinFET devices show great promise for continued CMOS device scaling beyond the 22 nm node.[13–15] The presence of the gate electrode on the three sides of the channel substantially improves the electrostatics of the device compared to planar devices enabling continued gate length scaling without loss of device performance. However, the three-dimensional nature of the active area (referred to as a fin) makes the fabrication of these devices more challenging than planar devices primarily due to the increased complexity of the gate RIE. The removal of the gate stack from the fin sidewalls while maintaining an acceptable gate profile and preserving the Si in the source and drain regions of the device becomes exceedingly difficult as the gate and fin pitch are decreased. Therefore, the feasibility of scaling these devices to densities where their application is relevant cannot be assumed. Consequently, we have employed HSQ-hybrid lithography to explore trigated FinFET scaling to integration densities suitable for 15 nm node static random access memory (SRAM) cells.

The process flow for fabricating these devices is outlined in Fig. 2. The devices were built on SOI wafers with a 30-nm-thick Si layer and a 140 nm buried oxide (BOX) layer. After forming the alignment mark patterns, HSQ-based hybrid lithography was performed using a 60-nm-thick AR3G layer, 1% HSQ, and TDUR N700 photoresist. The active area patterns consisted of lines with a minimum postlithography critical dimension (CD) of ~15 nm and a feature pitch ranging from 50 to 200 nm. Following the AR3G etch as described above, RIE using an HBr-based chemistry was used to define active Si regions, referred to as fins [Fig. 2(a)]. The postpattern transfer CD of these features was ~12 nm.

A 2 nm sacrificial oxide was grown on the Si fins and stripped using wet chemical etching in order to remove any surface damage created by the RIE process. This procedure reduced the final minimum CD of the Si fins to 8–9 nm. A multilayer gate stack was deposited onto the fins. This stack consisted of a 2 nm Hf-based high-κ gate dielectric deposited by chemical vapor deposition (CVD), a 10 nm TiN gate electrode deposited by physical vapor deposition (PVD), a 50-nm-thick poly-Si film and a 40-nm-thick SiN capping layer both deposited by CVD. In this case, the incoming substrate topography created by the presence of the underlying fins necessitated an increase in the AR3G thickness to 90 nm. This adequately planarized the surface, allowing the continued use of 1% HSQ. TDUR N700 was used as the photoresist. The gate level pattern consisted of features ranging in CD from 15 to 90 nm with a feature pitch ranging from 90 to 110 nm.

A multistep RIE process was used to transfer the pattern into the gate stack [Fig. 2(b)]. After etching the AR3G layer, the SiN was etched with a CF_4/CHF_3-based RIE chemistry using the ARC/HSQ/TDUR N700 as a mask. Following this etch, the remaining masking materials were removed using dry stripping. From this point, the SiN served as a hard mask for the duration of the gate etch. This choice was made due to the complexity associated with etching the multilayer gate stack over the topography of the fins, while maintaining a suitable gate profile and preserving the Si in the source and drain regions of the fins.

A self-aligned ~6–7 nm SiN implant offset spacer was formed through CVD and RIE [Fig. 2(c)]. EBL was used to define implant blocking patterns for *n*-MOS and *p*-MOS devices using UV110G with hexamethyl disilizane as an adhesion promoter. For this lithography process, ARC and HSQ were not used. Shallow source/drain extension implants using As^+ and B^+ species were performed for the *n*-MOS and *p*-MOS devices, respectively. An additional 2–3-nm-thin SiN offset spacer was formed as described above for use as a silicide offset spacer. Dopant activation was performed by rapid thermal annealing and a thin Ni silicide was formed. The devices were annealed in forming gas at 400 °C for 30 min to remove any trapped charge in the gate stack created during device processing.

Contacts and interconnects to the devices were formed after encapsulating the devices in a layer of 6% HSQ, cured with broadband VUV/DUV irradiation at 400 °C for 5 min and capped with a plasma enhanced CVD (PECVD) layer of

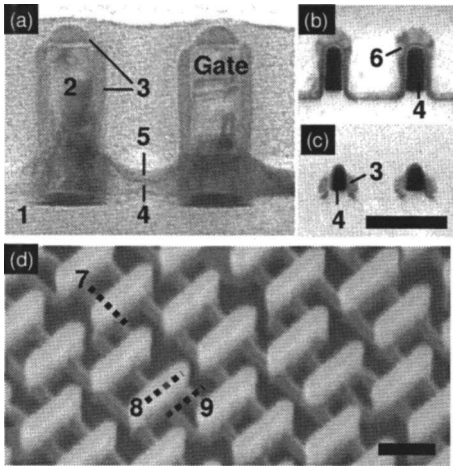

FIG. 3. TEM and SEM images of completed devices. (a) Gate cross section obtained from devices with a 90 nm gate pitch showing (1) BOX, (2) poly-Si, (3) SiN, (4) SOI fin, and (5) NiSi. The gate wraps around the fin, causing a projection of both the gate and fin in the channel regions. The gate length is ~22 nm. (b) Cross section through the fins in the gate stack region showing (6) TiN and high-κ gate dielectric stack. (c) Cross section through the fins in the source/drain region. (d) SEM image taken at 30° tilt from normal incidence with 45° substrate degree rotation revealing the intersection of the gate and the fin. The cross section locations of (a)–(c) are shown by (7)–(9), respectively. The scale bars shown in (c) and (d) are 50 and 100 nm, respectively. Images (a)–(c) are shown at the same scale.

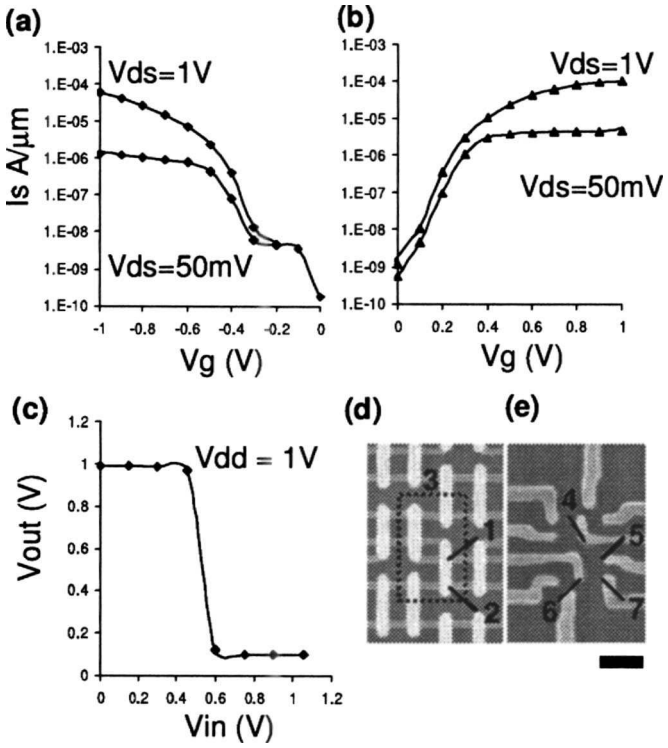

FIG. 4. Source current, I_s, vs gate voltage, V_g, at a 1 V and 50 mV drain-to-source bias, V_{ds}, from (a) *p*-MOS and (b) *n*-MOS devices working at a 90 nm gate pitch. The width-to-length ratio of both transistors is 70/22 nm. (c) Transfer curve from a CMOS inverter circuit contained within a 6 T SRAM bit cell with a cell area of 0.045 μm^2. The cell was operated at V_{dd}=1 V. This cell features a 90 nm gate pitch and a minimum fin pitch of 50 nm. (d) SEM image showing the layout of (1) *p*-MOS and (2) *n*-MOS devices from an inverter within a 0.045 μm^2 SRAM cell. (e) SEM image showing the wiring and contacts for the 0.045 μm^2 SRAM bit cell. The input (4), V_{dd} (5), output (6), and ground (7) terminals for a single inverter are shown. The scale bar corresponds to 100 nm.

SiO_2. The total stack thickness was ~150 nm at the conclusion of this process. Contact vias were patterned using a trilayer masking scheme consisting of a 175 nm organic planarizing layer (NFC-1400, JSR), a 20 nm PECVD SiO_2 film deposited at 200 °C, and a proprietary positive tone resist. Contact via etching was conducted using an $Ar/C_2F_6/C_4F$ RIE chemistry that removes oxide selective to SiN, Si, and Ni silicide. The vias were filled using a CVD TiN/CVD W fill process. W was removed from the field area by chemical mechanical polishing. A 100-nm-thick refractory metal multilayer stack was deposited onto the substrates using PVD. HSQ-based hybrid lithography was performed on this layer to define wiring patterns. For this application, a 60 nm thick AR3G layer was used in combination with a 2% HSQ film and TDUR N700. Once the AR3G etch was completed, the target stack was etched with a $Cl2/BCl_3/O_2$-based RIE chemistry.

IV. DEVICE RESULTS

Transmission electron microscope (TEM) and scanning electron microscope (SEM) images of completed devices are shown in Figs. 3(a)–3(d). Electrical results from single *p*-FET and *n*-FET devices are shown working independently and in concert as a CMOS inverter circuit [Figs. 4(a)–4(c)]. These results were obtained from devices arranged in a 6T SRAM cell configuration with a cell area of 0.045 μm^2. A SEM image of this layout is shown in Fig. 4(d). An image of the completed test cell showing interconnects and contacts is shown in Fig. 4(e). The fabricated devices show good short channel effect control but limited drive current due to high parasitic resistance. This is caused in part by the doping limitations imposed by the presence of the parasitic spacer on the fin sidewall [Fig. 3(d)] and the limited silicide-to-Si contact area. Fully functioning SRAM cells were not achieved in this work. However, this result clearly demonstrates the feasibility of trigated FinFET CMOS scaling to densities suitable for 15 nm node SRAM integration.

V. CONCLUSION

We have demonstrated a hybrid lithography scheme combining EBL and photolithography that leverages the high resolution printing capability of HSQ-based EBL resists and conventional 248 nm optical photoresists. This scheme was used to fabricate fully functioning CMOS devices and circuits with CD and feature pitch requirements that exceed what can currently be accessed using previously demonstrated hybrid lithography schemes. The device fabrication process flow presented in this work demonstrates that this patterning scheme creates a composite masking layer that is suitable for pattern transfer into Si, SiN, and refractory metals. While this work focused on the use of 248 nm optical

resists and ARC layers, there is no fundamental reason why this technique cannot be applied to i-line, 193 nm or EUV imaging materials.

The primary drawback of this technique is that the low sensitivity of HSQ results in long exposure times compared to processes using more sensitive chemically amplified resists. Consequently, a balance between throughput and patterned area must be reached. The presence of the photolithographicaly printed patterns on each die is sufficient for feature loading requirements for both RIE and CMP. This enables flexibility in the choice of the number of die populated with EBL features. For research purposes, throughput is not a limitation, making this technique ideally suited for device and circuit prototyping where density is a primary motivating factor.

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