Towards the Industrial Deployment of the Silicon Photonics Technology

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Abstract — **Silicon Photonics will become a mature technology at industrial level in one or two years. An overview including the status of the art of this technology is reported, and the main technological issues still to be focused on are discussed. Finally, ST view of the manufacturability status and of volume applications is provided as well as our vision of a Silicon Photonic roadmap.**

Keywords—Optical integration; silicon photonics; modulators; waveguide devices; waveguide photodiode; grating coupler; integrated laser; optical packaging; manufacturability; CMOS

I. INTRODUCTION

A huge R&D effort in many laboratories of big companies, like HP,IBM, Intel…, research centers and start-ups, has been done worldwide on photonic integration on Silicon (Si) since the early ’90s. The basic reasons of their technological developments are related to the necessity to overcome the physical limits of the interconnection [1] between a transmitting, Tx, and a receiving, Rx, device: while exponential reduction in feature sizes on electronic chips is progressively scaling with the More law, enabling faster and cheaper devices, the interconnections between them do not. Moreover, the dimensional scaling of on-chip interconnections degrades their performance and increases their energy dissipation relative to that of transistors. Interconnections also add noise and jitter to signals and are today a major issue for gigascale integration [2].

The main consequences are a strong limitation on the maximum distance of the electrical interconnection between Tx and Rx, the increase of power consumption of the link, and the increasing delay of distributed clock in intra-chip communications. The targets of Si Photonics for datacom and telecom applications are: the increase of the bitrate per channel, the increase of total capacity of a link, the reduction of the dimensions of the optical circuits and, finally, a very high level of integration to dramatically reduce the overall fabrication cost. For intra-chip communications the main targets are different: to reduce the energy per bit and to reduce as much as possible the latency.

Surprisingly, in the recent years, the most relevant role to move the key steps of Si Photonics technology in the telecom field was played by small start-ups, like Luxtera and SiOptical - then Lightwire, now Cisco. Though a lot of demonstrators have been realized pushing far ahead the leading edge of the device performances in several applications, some critical issues are still missing today: in particular, low power consumption and reliable integrated light sources for transmission or computing applications. Other important missing steps to reach the market will be discussed.

This article is organized in six Sections. Section II will introduce the main topics of Si Photonics technology and will briefly describe the state of the art of the technology today. Section III describes the necessary steps toward industrial manufacturability of Si Photonics and highlights the main bottlenecks for the evolution of this technology toward low cost and mass production devices. Section IV introduces forecasted volume applications in Telecom and other markets. Finally, Section V provides our vision of a roadmap of Si Photonics, then the main conclusions are drawn.

II. SILICON PHOTONICS: TECHNOLOGY OVERVIEW

A. Silicon Optical Modulator

Present solutions for the integrated optical modulators for Si Photonics are based on plasma dispersion effect and can be categorized as either carrier injection, depletion, or accumulation modulators. Two main structures are used: Mach-Zehnder Interferometer (MZI) and Ring Resonator (RR). Alternatively Franz-Keldish or Quantum Confined Stark Effect in Ge or SiGe have been successfully demonstrated to modulate light using an hybrid approach.

The carrier injection mechanism is the most efficient in terms of $V_{\pi}L$ product but is limited in bandwidth because of the characteristic carrier diffusion time through the junction.

Carrier depletion technique (nearly 10 times weaker than injection) has been adopted in commercial active cables for interconnections up to few kilometers [3]. This version of plasma dispersion based modulator however can be fast (up to 40 Gbps or more) but suffers of both the proximity effects of the electrodes close to the active area and of the carriers’ absorption in the active junction. Typical insertion loss of 4- 6 dB for a moderate modulation extinction ratio of less than 10dB is the common result for a MZI type Si modulator up to 50Gbps [4].

The carrier accumulation type is the best performing in the plasma dispersion category. Reference [5] demonstrated excellent results even in long haul applications of SISCAP modulator based on a thin dielectric placed in the middle of a Si waveguide for charge accumulation. The advantage of this geometry is that the electrical field overlaps the center of the optical mode with a good result in terms of power consumption, as low as < 3mW/Gbps, and a low driving voltage of 1V. Conversely this modulator requires a waveguide made of a polySi layer on top of a crystalline layer to include a thin oxide in the middle of these two layers. The insertion loss of such modulator waveguide is of the order of 10dB/cm but the total length required by this MZI is only 400 μm.

Integrated RR modulated up to 60 Gbps was demonstrated with good Extinction Ratio (ER) of 4.2 dB [4] enabling a 4x50 Gbps Wavelength Division Multiplexing (WDM) transmitter. Modulator total footprint is only 0.5 mm^2 and the dynamic ER is equal to 5.3~6.1 dB. Other RR structures were designed mainly for High Performance Computing (HPC) systems where the key quality factors are relatively high bandwidth, very low power, and scalable optical interconnects to maintain balanced communications in future exascale machines. The first vertical junction microdisk modulator demonstrated [6] it was able to achieve an open eye diagram at 25Gbps, using a circularly contacted microdisk with a 3μm radius, and a 1.2Vpp drive, reaching an energy consumption of ~13fJ/bit.

Hybrid solutions based on the direct bonding of compound semiconductors on Si have been also successfully demonstrated. In this case 10dB of dynamic extinction ratio, 5dB insertion loss at 50Gbps have been obtained with a driving voltage as low as 2V [7].

Diode	V_pL_p	Active region length	40 Gbit/s ER	On-chip IL (maximum transmission)	Optical loss at 40 Gbit/s operat. point
lateral pn [Chinese Acad. Scie.]	1.65 V.cm	0.75 mm	4.4 dB (*)	1 dB	< 2 dB (*)
lateral pn [Uni Surrey]	2.7 V.cm	3.5 mm	10 dB	15 dB	15 dB
lateral pn [Uni Surrey]	2.7 V.cm	1mm	3.5 dB	5 dB	5 dB
lateral pn [Uni Surrey]	2.7 V.cm	1mm	7 dB	5 dB	8 dB
wrapped around pn [Uni.Surrey]	14 V. cm	1.3 mm	6.5 dB	15 dB	25 dB
pipin [Uni.Paris Sud]	3.5 V.cm	4.7 mm	6.6 dB	6 dB	6 dB
pipin [Uni. Paris Sud]	3.5 V.cm	0.95 mm	3.2 dB	4.5 dB	4.5 dB

Tab. 1. State of the Art of Silicon MZI Modulators. (*) Values measured at 60 Gbps.

B. *Ge-on-Si Photodetectors*

Ge is a CMOS compatible material used in Si Photonics circuits for signal detection [8]. Ge operates either in the 1310 nm band and in the 1550 nm band. The bulk Ge band edge is naturally red-shifted when the material is grown directly on Si. The small lattice mismatch can induce up to a 0.24% strain that favorably extends the absorption edge of Ge to 1550 nm. Slight compensation with device length can countervail the weak absorption in the long wavelength range approaching 1600nm. Ge grown on Si waveguide has shown responsivity near the quantum limit of 1.24 A/W @ 1.54μm and a good handling of misfit dislocations during the growth process has shown to limit the dark current down to the range of few nA.

Reference [9], for instance, shows optical interconnection cables using photonic integrated transceivers with Ge detectors operating up to 25Gbps while [10] reports opto-electronic integrated receivers including vertically illuminated Ge photodiodes up to 10Gbps. Both products are on the market.

Research showed many Ge on Si photodetector with good performance and presently it is widely accepted that this type of detector is mature for applications with a very low dark current (at -1V: 25nA at RT; 100nA at 50˚C) operating at 40Gbps operation under zero bias at a wavelength of 1.55μm [11] and even at bitrate above 100 Gbps per single channel as showed in Fig. 1.

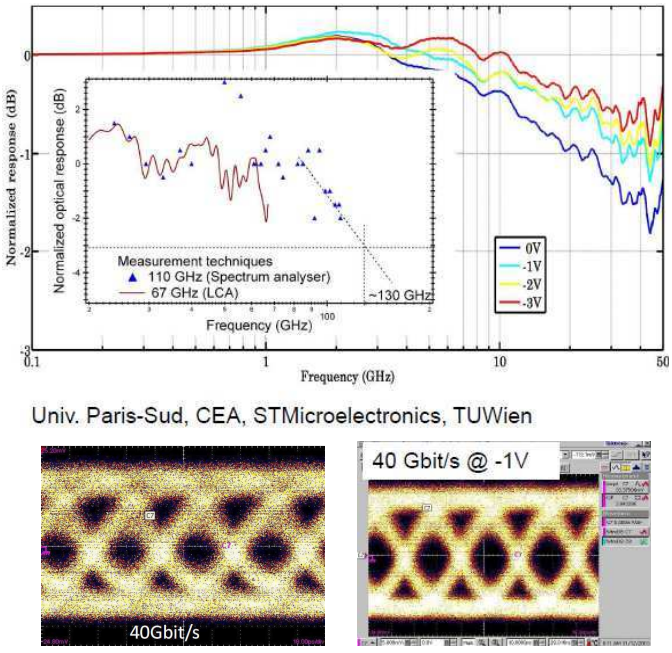

Fig.1. Lateral germanium PIN diode integrated in a SOI strip waveguide: Cut-off frequency up to 50GHz and 40Gbps eye diagram (left) obtained with zero-bias at a wavelength of 1.55μm and low dark current (25nA @-1V at RT). Responsivity is 0.8A/W at 1.55μm. Measured bandwidth is over 100GHz with zero bias.

C. *Silicon photonic passives*

Si photonic passive devices are based on SOI platform, and the most common waveguide is a buried strip with 400x200 nm^2 section [12]. Main challenge in manufacturing these waveguides is the edge roughness control that must be < 2nm

to target ≤ 2dB/cm propagation loss. Our ST multimode waveguides have 0.17dB/cm @1.3μm, while single-mode ones have 1.6dB/cm @1.3μm (1.2dB/cm @1.55μm). The advantage of a Si waveguide is the high index contrast that allows a control of bending losses down to curvature radii of ~ 2μm. Very tight curvatures are fundamental to design filters with large Free Spectral Ranges (FSR). In fact Si microrings can easily be designed with FSR's larger than 2 THz, up to 4 THz. Si is also a good thermo-optical material with index sensitivity of $2.4 \cdot 10^{-4}$/°C, about 20 times the silica coefficient. The combination of large thermo-optical effect and large FSR makes microrings ideal for miniaturized filters. Filter tuning can be implemented by trimming or heating the microrings with metal electrodes placed in the cladding on top of the microring. Tuning efficiency of ~ 3-10mW/nm was reported [13].

Si microring fabrication tolerances are an important issue. Average waveguide width variation in the ring determines a variation of the resonant frequency in the order of 133GHz for 1 nm of geometrical tolerance at 1.55 μm wavelength. In other words, fabrication tolerances should be at sub-nanometer level to have an accurate matching of specifications. Practical conditions indicate that best fabrication errors on the average waveguide width is of the order of 1 nm and Si layer thickness variation across the wafer is of the order of few nm's. This means that an accurate control of the resonant frequency of the ring has to be active. The heater and a feedback monitoring circuit are required to set and stabilize the resonance of the microrings against fabrication errors and temperature changes. This mechanism is valid for few rings but, assuming applications with several rings as a complex WDM switching network, the energy cost and control may become difficult to handle.

Other types of filters can be implemented in Si Photonics [13], in all cases fabrication errors on the waveguide have to be compensated as for microrings. The energy consumption is an issue that can be mitigated by introducing a capacitive tuning mechanism rather than heaters based on a continuous current flow. A waveguide similar to those in SISCAP modulator can be a useful approach for trimming or tuning with low energy.

D. Fiber to Chip coupling

The large dimensional mismatch between the SM fiber core and the cross section of a Si waveguide, implies a coupling loss of the order of 15 to 20 dB in the case of simple butt-coupling. Improving the coupling efficiency is therefore a major task in device engineering to facilitate the commercialization of PICs. End-fire coupling techniques using inverse tapers [14,15], grating directional couplers [16] and 3D tapers [17] as mode converter have been studied. Coupling efficiency better than –1 dB can normally be achieved using the inverse taper approach. The best results are 0.25dB loss @1.55μm for polarization-insensitive coupling, and 1dB bandwidth around 100 nm as reported in [18].

However, these couplers need to be located at the edge of the chip, and cannot be used without a careful polishing of the edge facets or precise control of the cleaving process in combination with an antireflecting coating. A small-core optical fiber would also be required for highly efficient coupling in butt-coupling approaches. Strongly diffractive waveguide grating couplers [19] were initially demonstrated in 2002 as an alternative. These waveguide grating couplers have become of practical interest in recent years because of their many advantages, which include simpler back-end processing without facet polishing, flexibility of placement of the optical input/output ports (anywhere on the chip or on the wafer), and compatibility with wafer-scale testing before dicing.

In a grating coupler, the fundamental mode from the nanophotonic waveguide is first expanded laterally by an adiabatic taper into a waveguide of about 10μm width, which matches the mode size of an optical fiber on the y axis. The light is then coupled out by the diffraction of shallow-etched gratings with proper geometry on the propagation axis into the optical fiber. The simplest grating coupler works for a single polarization, which is the practical situation when interfacing a laser to a grating, and the best available products have a 1.2dB coupling loss at the center wavelength of an optical bandwidth of nearly 30nm measured at -1dB from the peak [20].

The randomly changing polarization of the optical signal received from a conventional optical fiber communication link can be coupled into the transverse electric mode of two orthogonally orientated SOI waveguides connected to two sets of identical photonic integrated circuits, or to the same photonic circuit but with the light propagating in opposite directions. Dual polarization grating couplers (see Fig. 2) separate the two polarizations and couple them in two waveguides in such a way that they propagates in the 'same' TE way; so they can be used in two symmetrical single polarization circuits and then recombined at the exit of the circuit. The best coupling loss demonstrated by our technology at ST is around 3.8 dB at 1.3 (3.2 dB at 1.49) μm wavelength.

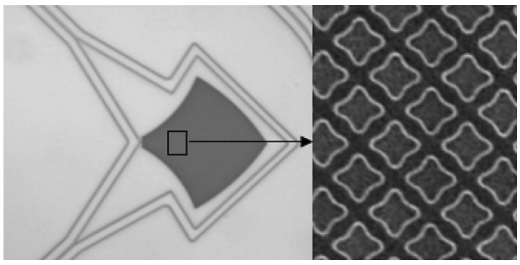

Fig. 2. Dual polarization Grating Coupler (Luxtera)

For all the kinds of grating couplers mentioned above, the lithography and etching processes needed to fabricate the relative structures must be distinct from the corresponding fully etched waveguides, because of the different etch depths or special fabrication. Fully etched subwavelength grating couplers that can be fabricated in the same etch step as the waveguides were first experimentally demonstrated in 2009 [21]. Apodized subwavelength grating couplers have also been demonstrated [22].

E. Laser Sources

Si is an indirect bandgap material, and is not naturally capable of accomplishing efficient radiative recombination. Free electrons tend to reside in the X valley of the conduction band, which is not aligned with free holes in the valence band.

To overcome this basic limit two approaches can be considered: to grow some other elements with opto-electronic capabilities to fabricate an integrated source on Si, or the hybrid integration of such direct gap materials on Si.

The realization efforts on the first category are based on the recent and widespread availability of nanotechnology processes which has allowed the traditional phonon-selection rule in indirect bandgap materials to be relaxed by breaking the crystal-symmetry or by phonon localization through the creation of nanostructures in crystalline Si. Here we find three main classes of integrated lasers: strained Ge Laser [23], Rear Earths doped Si nanocrystals [24], and new epitaxial growths of III-V material on Si [25]. However, achieving room-temperature continuous-wave lasing based on these techniques, temperature dominated processes remains a big challenge mainly because of low gain and/or high defect density.

The most promising approach for the industrial deployment is the heterogeneous integration of III-V semiconductors on Si. In order to densely integrate the III-V semiconductors with the Si waveguide circuits, mainly DVS-BCB adhesive, metal and molecular wafer bonding techniques are used [26-29]. In these approaches, unstructured InP dies are bonded, epitaxial layers down, on a SOI waveguide circuit wafer; at a further step, the InP growth substrate is removed and the III-V epitaxial film is processed. Recent results have demonstrated [30] widely tunable III-V/Si lasers, exhibiting 45 nm tuning range and hybrid tunable transmitters integrating a Si MZI modulator exhibiting 9 nm wavelength tuneability, high ER, between 6 and 10 dB, and excellent BER performance at 10 Gbps.

An alternative approach [31] enabled tunable lasers for telecom applications and uncooled, wavelength stable, 2x8 WDM laser arrays for datacom applications, processed simultaneously on the same wafer with performance approaching native InP devices.

Following the hybrid approach, the III-V epitaxial material was embedded in the silicon on insulator (SOI) chip, metal-bonded directly onto the silicon substrate [32], planar with the silicon device layer. Advantages of this approach include good thermal conductivity through the silicon substrate, avoidance of strains associated with lattice mismatch, and high efficiency direct optical coupling to the adjacent silicon waveguides. Furthermore, having the III-V epitaxial material hermetically sealed under silicon dioxide, such a solution presents new opportunities in commercialization of Si Photonics, as the necessity of high cost hermetic packages is removed. With this technique an integrated tunable laser, operating over the C band, and fabricated in a commercial CMOS foundry was demonstrated [32], even if the threshold current at 20°C is about 41 mA and L-I curve shows still some mode hopping .

III. SILICON PHOTONICS MANUFACTURABILITY

All the technological issues described above have been the focus of worldwide research effort and the best results seem very promising for several applications. Anyway, the industrial manufacturability in volume of Si Photonics requires not only the CMOS compatibility, low loss structures, device speed with low power and small size, good optical coupling between the chip and the external world, but also integrated Optical Electronic Design Automation (OEDA) with related libraries, in-line photonic test systems and low cost automated wafer testing, very precise statistical-process control, low-cost packaging enabling mass production and easy interfacing to optical PCB and backplanes.

In-line photonic test systems do not yet exist, meaning that photonic parameters must often be inferred from metrology and electronic test data. Today, transistor models often use hundreds of parameters to create faithful and predictive results. Photonic components are every bit as complex in many cases, but the available models are comparatively primitive.

Today's photonic design tools have difficulty in scaling up to large-scale circuits, and electronic design automation tools cannot cope with photonic parameters. Photonic circuit and link simulators (VPI, ASPIC, PICWAVE, OPTSIM) typically handle photonics-only or linear systems, or links with limited complexity. Many EDA tools do support complex circuit simulation, but are limited to electrical signals. Some custom adaptations allow the representation of optical signals. However, this approach scales poorly with many wavelength channels or full-spectrum information.

Manufacturing of Si Photonics requires interfacing models of photonic building blocks to EDA tools and to the commonly used EDA design flow to allow the integration of photonic and electronic building blocks into one unique design, effectively enabling full photonic plus electronic codesign and even cosimulation. Incorporating production tolerances and variability into relevant building blocks is one of the major step forward needed to optimally design analog photonic circuits.

If we look at the industrial maturity of Si Photonics in terms of the nine Technology Readiness Levels (TRL) we see that most of the laboratories have validated their components in house (TRL3-4) and some have tested them in relevant environment (TRL4-5). Only very few, typically some startups, have full system models based on integrated optical EDA tools, low cost wafer testing and packaging solution to be successfully compliant with the requirements of an actual complete system qualified through small volume production operating in field conditions (TRL 7-8). System-level integration has not yet received enough attention within the silicon photonic community. No one reaches the last level, up to now, with successful volume production. Pushing Si Photonics to reach full maturity requires today to afford two main key issues: packaging and cheaper costs.

A. Packaging issues

The most relevant technical bottleneck preventing Si Photonics from the mass production is the packaging area, which is still in his infancy. So a big effort is required here to pave the way towards fulfillment of market requirements of low cost products in volumes. In fact, most of the cost (50-80%) today is due to not optimized 'traditional' packaging solutions. Presently the optics community must figure out how to attach fibers without the need for active alignment. So far, the only silicon photonic products to integrate a light source have used package-level integration, which involves bonding the light source to the back-end dielectric of a CMOS process [20]. Many new approaches are being explored, including full

front-end integration [33], front-end bonding [34] and multichip system-in-package approaches [35], although none of these are yet in commercial production. So packaging and die-attach costs will continue to represent a substantial fraction of the cost of any finished photonic device, at least until the chip value or the global volumes, i.e. the total revenues, are increased in such a way to justify the investments to reduce the packaging costs.

In line with the history of system-on-a-chip and system-in-package development in the electronics world, it is clear that a diversity of processes will continue to be valuable for silicon photonics and that heterogeneous process integration is going to remain the dominant paradigm for the immediate future.

The development of high-density interconnect technologies by the electronics industry has substantially mitigated the penalty due to the parasitic effects for multichip integration. Furthermore, given the costs of modifying high-end CMOS processes, implied by node evolution in the monolithic approach, multichip solutions are likely to become dramatically more economical in the near future for a wide variety of applications.

B. Low cost issues

An interesting study [36] explores the economic viability and technical advances necessary for silicon photonics to compete with traditional optoelectronic design and material platform alternatives in the long term. MIT paper leverages a case study of four functionally equivalent 1310nm, 100 Gigabit Ethernet (GE) Local Area Network (LAN) transceiver designs to reach a broader insights into the production economics of the competing architectures and material platforms across a specific market application.

The analysis shows that many parameters can affect the projected costs of a new technology but the main impact on the cost is due to three factors: to annual production volume (APV), manufacturing location, and yield. Then the case study shows that the most competitive technical solution is highly dependent on the APV. At APV below 900.000 units, a directly modulated laser array on an InP platform will likely be the most competitive solution. At APVs above 900.000 the 'Hybrid' and, above 1.7 million, the 'Si two chips' designs appear to be more competitive. The exact volumes at which each design is most cost competitive depends significantly on the yields achieved.

Most of the published literature presents Si Photonics as the best technology to make products with the lowest cost. On the basis of a sound analytical approach like [36] we can say that this statement is correct, provided that APV of a certain device are above a certain threshold, estimated around 1-2 million units per year for a 100GE LAN transceiver, depending on specific yields of that product.

This type of conclusion, which is more general than the specific case considered, establishes a direct link between costs and volumes, given a particular application. The volumes offered today by real applications are well below these thresholds, so that today Silicon Photonics has several competitors, but many companies believe this situation is temporary and can dramatically change as soon as an application with the proper volumes will emerge.

IV. SILICON PHOTONIC APPLICATIONS

Considering volume applications for Si Photonics three main fields could be considered: a) Telecom b) Data Center and c) High Performance Computing. Other potential applications are discussed in [10].

A. Telecom

Mobile data subscriptions are expected to grow strongly in the next years and will drive the rise in data traffic along with a continuous increase in the average data volumes per subscription while voice communication is already become a very small portion of the mobile traffic. Such a huge demand for an extreme bandwidth expansion is needed at each mobile site/node. Moreover, the trend to add a large number of small cells as a complement to the macro layer, to increase the network capacity and performances, will lead to augment the amount of equipments to be deployed in the network. This translates in two direct consequences for the hardware platforms of Radio Base Station (RBS) products: increased capacity in the interconnections of Baseband units, also called Digital Units (DUs), to the Radio Units (RUs) and increased computational complexity in the (DU) to handle transmission combined with a shrinking latency budget.

The properties of Si Photonics make it a very promising technology for the implementation of devices in next generation optical communication systems that require ultra high speed > 28 Gbps, very low power consumption and very small device area with respect to the technologies currently under development. Si Photonics adds and improves the functionalities, flexibility and performances. Two areas of Telecommunication applications, with potential volumes above the threshold previously discussed, can be envisaged for Si Photonics in optical communications: 1) optical links between DUs and RUs (back-hauling) shown in Fig. 3; and 2) optical intra-board and intra-rack interconnects.

1) In this case Si Photonics can fulfill the requirements of optical interconnects of future RBS and Router platforms developing the following key devices covering link length up to 2 Km:

- 4x10Gbps and 12x10Gbps optical transceivers for DU to RU and high density intra-system interconnects in RBS

- 1x25Gbps and 4x25Gbps transceivers, parallel optics or WDM, for intra-system interconnect as evolution of the present 10 Gbps to scale up the capacity.

2) In this case Si Photonics can fulfill the requirements of intra board/rack interconnects by providing miniaturized optical embedded modules for short distances (< 100m), for example: a 200Gbps/link transceiver assembled on Electro Optical PCB, enabling close proximity with the host IC, with aggregate full duplex bandwidth of 50 Gbps x 4λ = 200 Gbps/link, an estimated power consumption around 600mW/link and estimated module size for a total capacity of 800 Gbit/s in about 500 mm^3.

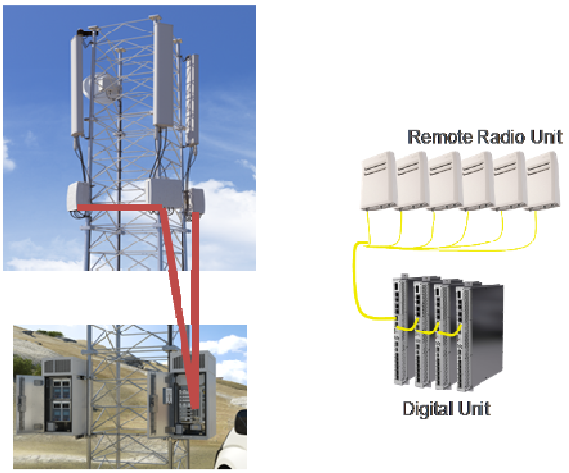

Fig. 3: DU-RU optical interconnections

To cope with the huge bandwidth demands foreseen in the next years it is necessary not only to rely on Moore's law, with the consequent increase in the clock rate toward 50 Gbps, but also to stack the ASIC chips in an implementation named 3D as depicted in Fig. 4. With 3D assembly, ASIC implementation and high signal rate optical interconnection are the most practical inter-chip communication alternatives for power efficient hardware unit fabrication. A Si optical interposer is added at the ASICs base providing all the optical circuits and functions for the inter-chip communication.

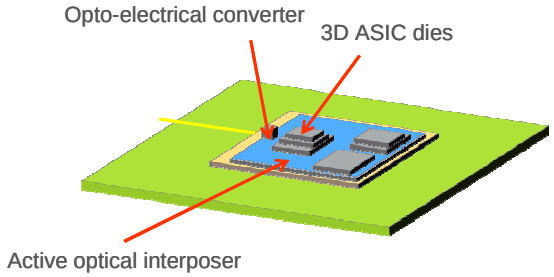

Fig. 4: 3D ASIC implementation in RBS Baseband Processing card

B. *Data Center applications*

Data Centers are today the platforms providing the huge communication bandwidth and computational strength required by the new ICT intensive services, like Cloud Computing. This requires an extensive data exchange between the nodes of the Data Centers: high bandwidth, low latency, low complexity and low power consumption are essential characteristics of the architectures and technologies to be used in Data Centers. Today the use of low cost, low power consumption Si integrated, parallel optical interfaces capable of transmitting up to 4x25 Gbps are demonstrated and they are close to commercial availability. WDM can also be used to reduce the interconnection complexity and better exploit fiber capacity.

A further step to reduce the power consumption, cost and complexity is the adoption of new interconnection architectures which include optical switching fabrics as reported in [37-38]. Suitable optical switches have to be scalable, transparent to high rate (28 Gbps and beyond), with a cost of a fraction of $/Gbps of capacity, and a power consumption of few mW/Gbps. Si Photonics is an optimum candidate for implementing such type of optical switches. One of the proposed device architectures is depicted in Fig. 5 showing an 8x8 optical switch capable of supporting up to 48 wavelengths. If 100Gbps is the rate used for each interconnection link, this modular switch will be capable of switching a total capacity above 38 Tbps.

The large amount of 100G optical interfaces that will be used in large structured Data Centers to create suitable mesh networks interconnecting servers, switches and routers, associated with new concepts about 'virtualization', will change the traffic pattern from primarily client-server (or north-to-south) flows to a combination of client-server and server-server (or east-to-west) streams.

This shift has an impact on application response time and end-user experience, since today's Data Centers are not designed for these dual-flows but only for the north-to-south ones. In order to make Data Centers more dynamic and energy efficient, IT managers are looking at architectures to improve application level flexibility.

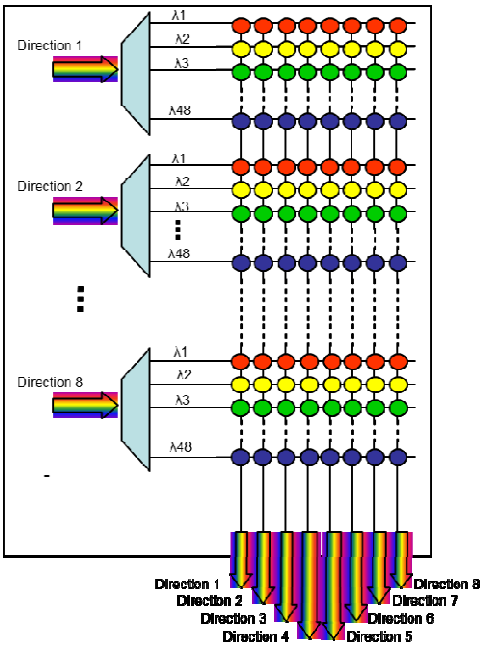

Fig. 5: Optical switch architecture based on Ring Resonator elements at each cross

New solutions have been investigated, for instance, a recent standard called Fiber Channel over Ethernet (FCoE), or the 'unified fabric' approach, or TRILL (Transparent Interconnection of Lots of Links) technology enable the convergence of multiple protocols onto a single physical network [39-41]. The most probable chosen network fabric is Ethernet: 40Gbps and 100Gbps Ethernet standards.

Considering the quickly evolving new scenarios it comes quite straightforward to imagine the future adoption of an Optical Switching Layer in Data Centers, as already happened

in core and metro networks to provide more scalable, flatter, dynamic, highly available network infrastructures. The new Data Center architectures could provide similar advantages following the same strategy. Here, however, the different scale of dimensions will bring even more stringent requirements in term of miniaturization, power consumption and, most important aspect, cost. In this environment Si Photonics is the enabling technology to produce the suitable hardware platform using ring resonator based architectures like the one showed in Fig 5 which can gain further volumes coming from similar applications also in Access Network.

C. High Performance Computing (HPC)

HPC is another area of interest for Si Photonics. In particular, with the appearance of Cloud Computing, HPC will also strongly overlap with all kinds of ICT applications. Inside HPC optical technologies are already massively used. IBM's Roadrunner system contains active optical cables with a total fiber length of 90 km, the cost of optics being less than 2% of the total cost. But it is expected that by 2016, cost of optics will be 20% of the total supercomputer cost and by 2020 this number could be as high as 40% (source IBM). Low-latency, scalable, and high-throughput interconnection are essential for future HPC. As massively parallel computing architectures and large data storage systems on the scale of petaflops are being deployed today, the critical performance bottleneck has shifted from the computing systems to the communication infrastructure based on traditional technologies.

As far as exascale HPC [42] is concerned it is already clear that it can only be achieved with CMOS logic enabled with Si photonic interconnects based on parallelism and high capacity of WDM techniques. So, a ring based approach [43] similar to the switching architecture showed in Fig 5 has the potential to provide suitable answers to some key requirements put by HPC: no loss of data, minimum end-to-end delay, huge bandwidth and fast switching speed, network scalability with simple topology.

V. SILICON PHOTONICS ROAD MAP

Based on the status of the today Si Photonics technology, described in sections II and III, on the new class of photonic devices already demonstrated in the R&D labs, and on the main volume applications introduced in Section IV, we could envision [44] a Si Photonics technology road map as synthesized in Fig. 6.

The reference generation is based on the assessment of the today technology built on a 200mm SOI wafers with CMOS 130nm. The reference key characteristics are summarized in a total aggregate bandwidth of 40 Gbps on 4 links, with energy per bit below 20 pJ/bit. The Si photonic chip is integrated in a QSFP module form factor with a total cost close to 5$/Gbps.

Porting this technology on 300mm SOI wafers, with CMOS 65nm, we can expect to increase the bit rate per link by a factor of about 3x. Thus, extending the aggregate bandwidth and reducing the energy consumption, the cost per bit is scaled down. The driving applications of this generation can be envisaged in HPC and modern Data Centers where the intensive computing and huge routing are strongly requiring wide bandwidth at low power and low latency. We can expect the second generation to be mature for industrial application in 2015. Cost will be around 1$/Gbps.

The next technology breakthrough will be offered by the micro ring modulators able to dramatically scale down both the modulator size and consumed energy, so enabling compact coarse WDM. This third generation may be expected to be mature for massive production in 2018 and, associated with improved electronics (CMOS 28 nm), could reach power consumption below 2pJ/bit. At this stage the low latency will offer relevant advantages for chip to chip applications. Here a key role could be played by Si photonic interposers capable to scale down the multi layers electrical board size by a factor of 5. The cost will drop around 0.2 $/Gbps.

Based on the recent R&D demos, a possible fourth generation could be ready around 2021. The next breakthrough will appear thanks to the introduction of multi-wavelength hybrid integrated lasers on Si, for example: micro-ring-lasers. They will enable the usage of compact, low power, dense WDM, very likely associated with 3-D Si technologies [42]. This generation could enable the intra-chip interconnections with the characteristics shown in Fig. 6. When this will happen, the traditional semiconductors IC volumes will finally occur, and the intra-chip communications, today based on copper, could be even achieved by the multi-λ integrated micro/nano-photonics [45].

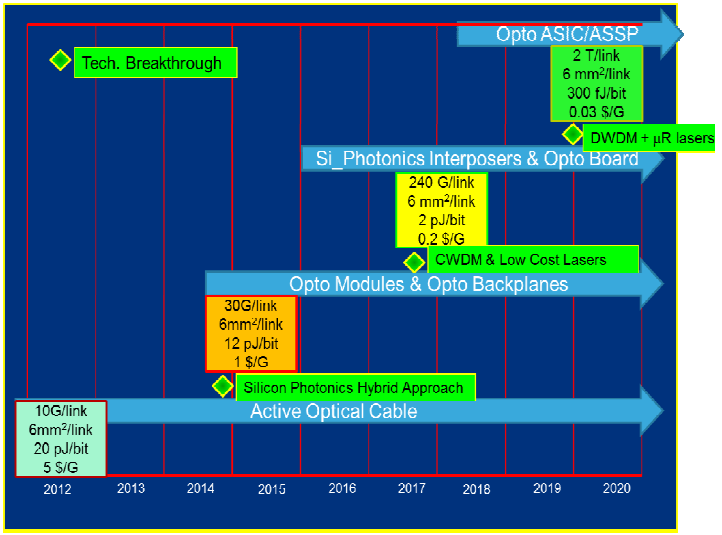

Fig. 6: Silicon Photonics road map

VI. CONCLUSIONS

From all the above examples it emerges clearly the huge potential market impact of Silicon Photonics technology to face the dramatic improvement in terms of performances and cost that Telecommunications, Data Centers and HPC will need. The convergence of these fields will help to overcome the volume thresholds required for Silicon Photonics to become the cheaper solution. Furthermore, the current efforts toward the industrialization make us confident that those achievements are not so far in time.

ACKNOWLEDGMENT

The Author acknowledges S. Rotolo and M. Zuffada (ST) and F. Testa (Ericsson) for the cooperation and technical discussions.

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