Lithography Options for the 32 nm Half Pitch Node and Beyond

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***Abstract*—Three major technological lithography options have been reviewed for high volume manufacturing at the 32 nm half pitch node: 193 nm immersion lithography with high index materials, enabling $\mathrm{NA} > 1.6$; 193 nm double patterning and EUV lithography. In this paper the evolution of these three options over 2008 is discussed. The extendibility of these options beyond 32 nm half pitch is important for the final choices to be made. During 2008, the work on high index 193 nm immersion lithography has been stopped due to lack of progress in high index optical material and high index liquid development. Double patterning has made a lot of progress but cost concerns still exist. Preferred are those resists which support pattern or image freezing techniques in order to step away from the complex litho-etch-litho-etch approach and make double patterning more cost effective. For EUV, besides the high power light source, the resist materials need to meet very aggressive sensitivity specifications and need to maintain simultaneously performance in terms of resolution and line width roughness. Furthermore, EUV reticles encounter serious challenges, primarily related to mask defectivity.**

***Index Terms*—Extreme ultra-violet lithography, 22 nm half pitch node, 32 nm half pitch node, 193 nm immersion lithography.**

I. Introduction

With the production of the ASML XT:1900i scanner, water-based immersion lithography has proven to be able to afford extension of numerical aperture (NA) up to 1.35. This affords printing half pitches down to ~ 45 nm with acceptable $k_1 (> 0.3)$. Further increase beyond this NA is not possible with a water-based 193 nm immersion approach and a decision is needed on the technological choice for patterning at the 32 nm half pitch node and beyond. According to the ITRS roadmap the 32 nm node should go into production in 2011, requiring that development should start in 2009; the 22 nm node should go in production in 2014, requiring development to start in 2012. The semiconductor industry is taking a lot of time to reach this decision. Two contenders are still being pursued, each with their own benefits and drawbacks: double patterning, enabling low $k_1 (< 0.25)$ patterning; or wavelength reduction by moving to the Extreme Ultra-Violet (EUV, $\lambda = 13.5$ nm) wavelength. In this paper the technological advantages and challenges of these two options will be discussed.

One option that has been pursued until the fall of 2008, was to increase NA beyond the limit of water-based systems ($\mathrm{NA} = 1.35$). The target was to achieve $\mathrm{NA} > 1.6$, which is required to resolve 32 nm half pitch in a single lithography step [1]. The advantage of this option is that much of the current infrastructure could be used for this technology. The major new requirements were new high-index glass material for the final lens element as well as high-index immersion liquid with refractive index $(\mathrm{RI}) > 1.8$ and both with high transparency. Moreover, to efficiently couple the light into the photoactive material, high-index polymers ($\mathrm{RI} > 1.9$, preferably 2.0) [2] for resist formulation are required. Therefore, three independent breakthroughs in material development were required for this route to succeed.

Towards the end of 2008, it became clear that none of the three required material developments could be demonstrated in the necessary timeframe for 32 nm half-pitch patterning in single exposure. A feasibility project was started to develop Lutetium Aluminum Garnet (LuAG) last lens elements (RI of 2.1), but despite significant efforts to control the production process and the purity of the various components, the smallest absorbance shown was 0.05 cm^{-1}, or still more than a factor 10 larger than the required specification [3]. For fluids, so called second-generation organic liquids had been identified with refractive index of 1.65 at 193 nm. When stored in the absence of oxygen, and if a suitable recycling technique was used to remove contaminants that accumulate during exposure at 193 nm, the liquids had sufficient transparency at 193 nm [4]. Nevertheless, the organic liquid refractive index was too low to enable NA of 1.70. Organic materials with higher refractive index had lower transmission or suffered from high viscosity. A promising route to increase the refractive index of fluids and resists was also identified with the addition of nano-particles, [5] but was stopped as it became clear that the interest in high-index had disappeared. Efforts to generate high-index resist were mostly exploratory and took place at universities rather than at resist vendors.

As the other two lithography techniques (double patterning and EUV) were gaining maturity for 32 nm half pitch patterning and showed the possibility to be extended beyond the 32 nm node, the interest in scanners with NA beyond 1.60 disappeared, and the three major scanner vendors announced a stop in the further development as they saw no markets for these scanners. Since the infrastructure required for EUV takes time to mature, double patterning is now commonly seen as the solution towards 32 nm half pitch patterning. For 22 nm half pitch, a choice remains to be made between EUV and further extension of multiple patterning schemes.

II. 193 nm Double Patterning

Double patterning is a technique that comes in many flavors [6]. The basic idea is that if a pitch of interest is not achiev-

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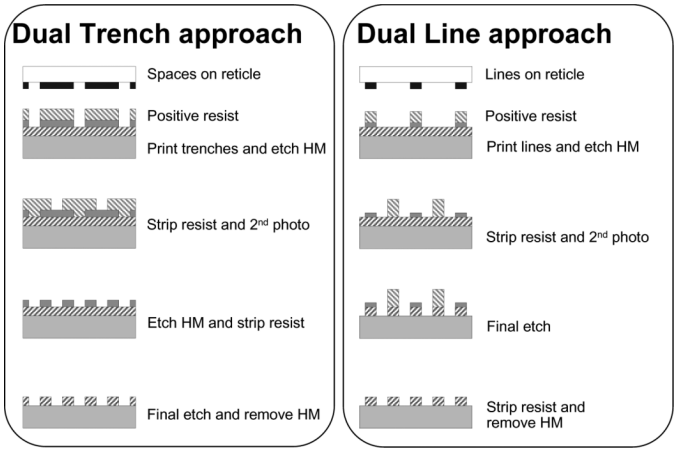

Fig. 1. Schematic representation of double trench and double line approaches for double patterning.

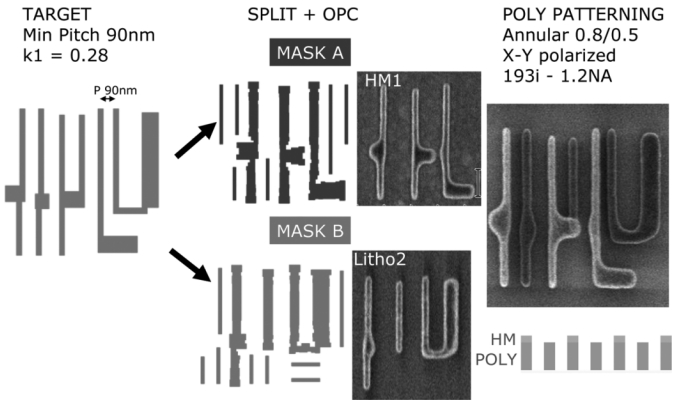

Fig. 2. Approach and results for splitting a logic gate cell, with 45 nm minimal half-pitch for double patterning at 1.2NA ($k_1 = 0.28$). A target design (left) is split and corrected for optical proximity, resulting in Mask A and B (and their corresponding individual wafer prints). The combined result before removing the hard-mask (resulting in different contrast in the SEM) is shown on the right, demonstrating the good match with the target design.

able in a single lithography step, the design is split over two lithography layers in a way that the minimum pitch is relaxed (and preferably doubled) with respect to the target pitch. In this way the effective k_1 of the total process (i.e., the combination of the two lithography steps) can drop below the theoretical limit of 0.25 for a single patterning process. From a processing standpoint, the easiest way to implement this is by transferring the first litho step into a hard-mask layer by etch and subsequent imaging and etching of a second photoresist layer. This litho-etch-litho-etch (or LELE) approach can for instance be achieved either by double trench or double line patterning as shown in Fig. 1.

A significant advantage of double patterning 193 nm lithography for the 32 nm node is that it builds on existing platforms [7], [8]. Early development of the technology is already possible with tools that are currently available on the market. Out of the two technological options that are discussed in this paper, it is the most mature and most likely to be in time for patterning at the 32 nm node. From a scanner perspective, the main technological challenge is in meeting the overlay requirements. Alignment between the first and second exposure pass is critical. Depending on the chosen double patterning process, it will impact the line or space critical dimensions (CD), the patterns' placement, and possibly the stitching quality where cut polygons recombine through the DP process.

Next to this, a full-chip automated solution is needed to split the dense layout into two sparser layouts to image separately and to recombine through the double patterning process (see proof of concept in Fig. 2) [9], [10]. The design split of a 1-D array of lines assigns every other design polygon to a different color or layer and is an easy coloring problem.

On the other hand, the design split of 2-D layouts may lead to conflicts that in the best case can be solved by cutting existing polygons to increase the degree of freedom for coloring. The cut polygons must recombine through double patterning at so-called "stitching points". However, stitching points are potentially vulnerable to process variations. Patterns from the two separate imaging steps need to overlap at the stitching points to compensate for line-end shape and position variations caused by dose, focus, mask, and overlay errors. As a result, sub-resolution pitch or gaps may be reintroduced (see Fig. 4) where the goal was to double the pitch or remove the gap. At these locations, the imaging resolution limits the benefit of double patterning. Unrestricted designs, in particular random layouts for logic applications, combine the difficulty of printing critical small gaps and pitch together. This is not compliant with double patterning, which requires relieving part of the pitch or gap constraints to improve resolution. (see Fig. 3).

Simply scaling the unrestricted designs from previous nodes may not only result in split conflicts but also in failed stitching. Only a compliant design and well-tuned cutting and stitching will guarantee an acceptable yield when using double patterning at its highest resolution.

From a processing point of view, the LELE approach requires "just" normal scaling from the approaches for the larger nodes. However, the drawback of the LELE approach is that the total lithography cost essentially doubles. The full lithography process is done twice per layer, with even an extra intermediate etch step in between (not to mention extra hard mask materials that may be required). This problem can, however, be circumvented by novel material developments [11]. The most attractive approach is the use of nonlinear optical materials, since this would allow double exposure rather than double patterning. The two exposures that are needed to print a single layer can, in this case, be performed without removing the wafer from the exposure chuck which is advantageous for overlay reasons. However, it does require materials that have "forgotten" the dose in underexposed areas from the first exposure, by the time they see the second exposure such that, $f(I_{\mathrm{Pass1}} + I_{\mathrm{Pass2}}) \neq f(I_{\mathrm{Pass1}}) + f(I_{\mathrm{Pass2}})$. [12] To achieve such a behavior, reversible contrast enhancement layers and optical threshold materials are being considered [13]. A lot of work, however, is still focusing on theoretical analysis and it is not straightforward to come up with appropriate materials that possess all the required characteristics.

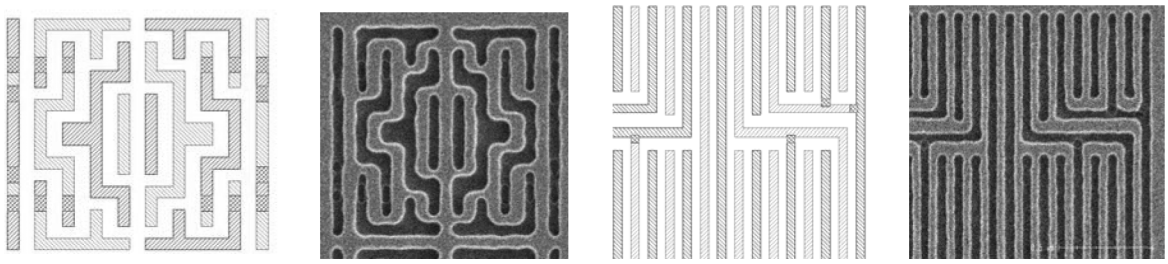

Fig. 3. Example of a random 45 nm M1 logic test clips after Double Patterning in hard mask. Robust stitching through process variations requires relaxing the pitch to pattern aggressive gaps (left). Relaxing the design in one direction allows double patterning at 90 nm pitch (right).

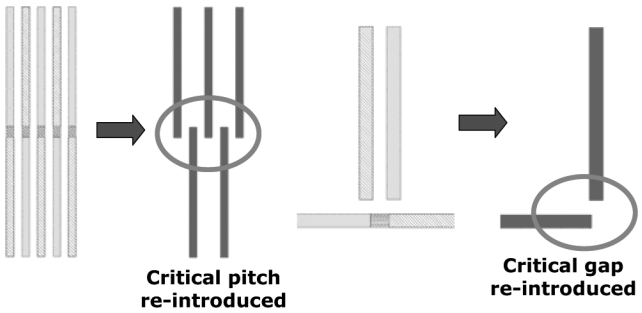

Fig. 4. Stitching overlap reintroduces the critical pitch or gaps.

An intermediate option from a processing point of view is to freeze the pattern from the first image through some additional processing (for instance in the litho track) before coating and exposing a second layer of resist over the first (litho-process-litho-etch). The principal requirement is that the process not only enables that the resist from the first image withstands the solvent that is applied when coating the second layer of resist, but also that the first layer is not further developed after the second exposure (mainly of concern for positive-tone resists in the double line approach). A method to achieve this is, for instance, by depositing an overcoat after the first layer is imaged and developed, that crosslinks in a subsequent bake step under the influence of residual acid and photo acid generator (PAG). The result is the formation of a thin crust on the resist pattern that protects the resist from the solvent of the second layer and the second development step (see Fig. 5). A drawback of this method compared to LELE is that the lines are widened by the crosslinking step and thus affects the requirement of printing even narrower lines with good CD control for double patterning.

Very promising results have been recently reported using this approach [14]. High resolution, good CD uniformity (across wafer and through batch) and excellent 2-D patterning properties could be demonstrated after litho and etch, making this approach comparable to the much more extensive and costly LELE approach (see Figs. 5 and 6).

An alternative method is to use two different resists whose chemistries are sufficiently different such that the solvent of the second resist does not react with the polymer of the first resist. Also with this technique, 32 nm dense lines and below can be patterned, as shown in Fig. 7.

A third example of an alternative process for making double patterning more cost-effective is in dual tone development [15], [16]. In this approach only a single exposure step is used for

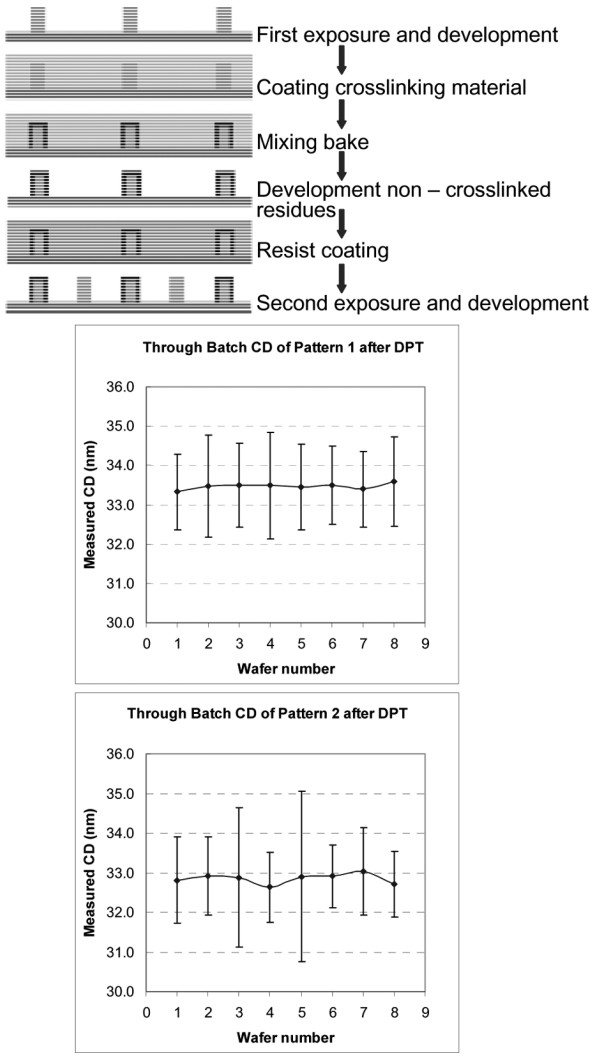

Fig. 5. Approach and results for pattern freezing through overcoat and crosslink. During the mixing bake, the residual acid from the patterns of the first litho step crosslinks the overcoat material. The crosslinked layer protects the first pattern during spin-coat of the second resist layer. The graphs show through batch across wafer critical dimension (CD) uniformity data for 32 nm half pitch lines printed using this technique (68 fields measured per wafer). The error bars show the measured 3 sigma value for each wafer.

printing the dense pattern. A sinusoid aerial image is used and two different chemistries are used in separate development steps. In the positive development process, those parts of the resist that have received a dose higher than E_P are developed. In the negative development process, parts of the resist are developed that have received a dose below E_N. This approach

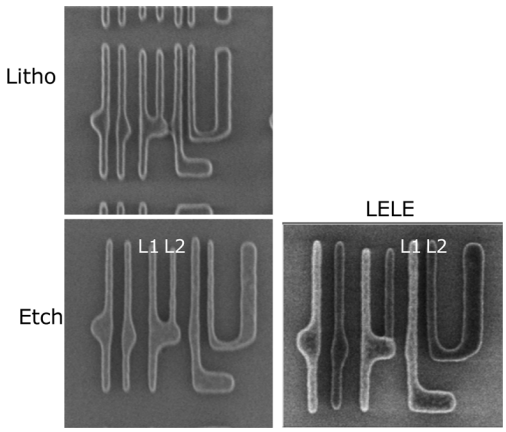

Fig. 6. 2-D 32 nm node patterning results after litho and after etch into 60 nm poly for a pattern freezing technique (showing also the comparison to LELE on the right-hand side).

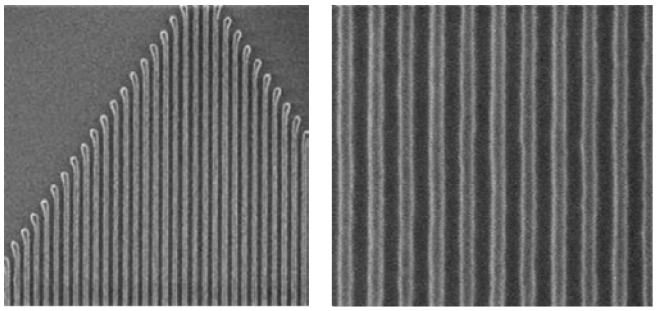

Fig. 7. Approach and results for double patterning using a positive/positive tone resist process using materials based on different polymers. The SEM image on the right shows 32 nm half pitch results at 1.35 NA.

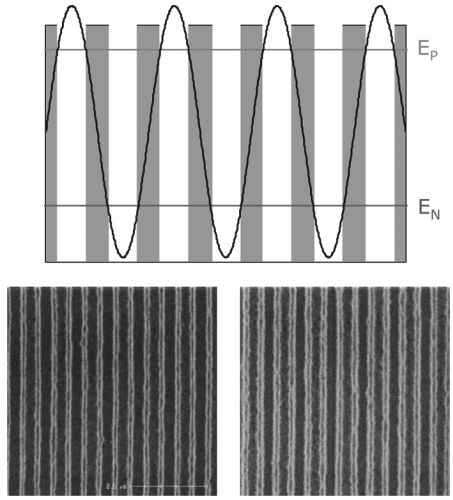

Fig. 8. Approach and results for patterning using double development. The SEM images on the show results for a 200 nm pitch (1X) mask feature printed at 0.93 NA (left; $k_1 = 0.24$) and 0.80 NA (right; $k_1 = 0.207$). After a single exposure this results in 50 nm half pitch resist lines on the wafer.

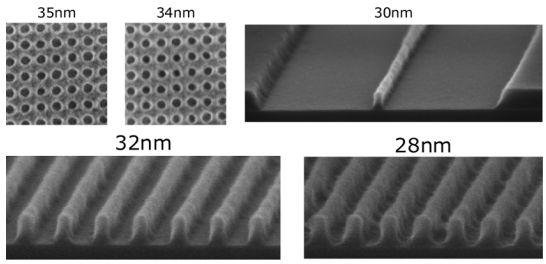

Fig. 9. Top-down CD-SEM pictures of 35 and 34 nm dense contact holes, cross-section SEM picture of 30 nm isolated, and 32 and 28 nm dense lines.

results in frequency doubling in a single exposure step and effectively the slopes of the aerial image are printed (see Fig. 8). The CDs of the printed lines will depend on the relative separation of E_N and E_P, which can be tuned by an additional bake in between the two development steps [17]. Process optimization has demonstrated the ability to print 100 nm pitch structures at $k_1 = 0.20$. Recent further material optimizations indicate that it should be achievable to push this process towards 32 nm half pitch imaging [18].

It should be emphasized that this self-aligned approach requires an extra trim exposure to remove conflict areas (such as line ends, similar to using alternating PSM). However this second exposure is less critical in terms of CD and overlay. The dual development process is an especially attractive solution for very regular designs (such as memory). Implementation in logic designs is possible, but will require a more complex design approach.

III. Extreme UV Lithography

The main benefit of Extreme UV Lithography is in its potential extendibility. The enormous jump (from 193 to 13.5 nm) that is made in imaging wavelength allows reduction in NA and increase in k_1, while maintaining the improved resolution. For instance for 32 nm half pitch imaging at 0.25 NA, (target NA for the early full-field systems) k_1 will be 0.59. The higher k_1 removes a lot of the optical proximity effects and therefore avoids the need for their corrections and for assist feature placement for mask making. Additionally, EUV lithography will be a single exposure technique and should therefore be more cost-effective than some of the techniques discussed above, especially for high volume products. However, some big technological hurdles for introducing EUV lithography in high volume manufacturing remain. [19] The highest ranked critical issue at the 2008 EUVL Symposium is the availability of EUV light sources with sufficient power for high-throughput imaging. Defect free EUVL masks and photoresists with high sensitivity and resolution were ranked as issues 2 and 3, respectively.

IMEC has recently installed one of the very first EUV full-field tools. This ASML Alpha Demo Tool (EUV ADT) is providing important learning to the industry on the implementation of EUV lithography in silicon processing. Recently quite some progress has been made on the exposure results of the EUV ADT [20], [21]. Directly after the site acceptance test of the EUV ADT in June 2008, the resolution limit of the exposure tool and its resist process was at 40 nm LS, and sub-40 nm isolated lines suffered from collapse. Improvements in the resist process meanwhile resulted in a clear shift of the resolution limit of the tool. As shown in Fig. 9, currently 34 nm contact

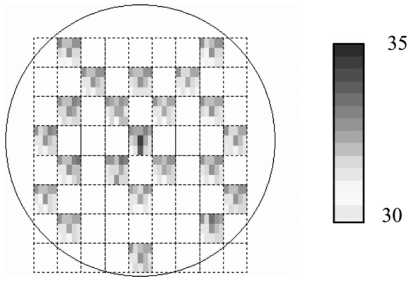

Fig. 10. Wafer CD map for 28 nm vertical lines/spaces, where 22 fields have been exposed at nominal focus and CD was measured in 15 positions per exposure field, covering most of the die.

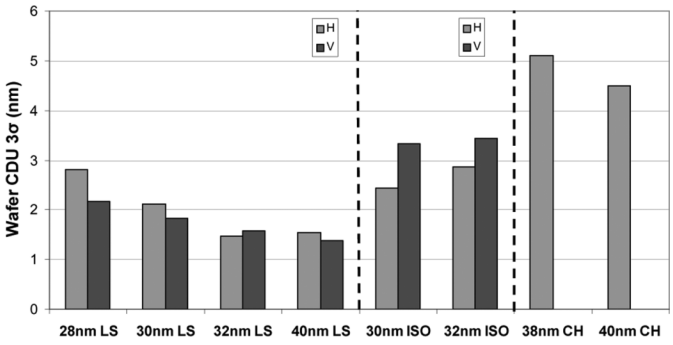

Fig. 11. CDU 3σ values for sub 40 nm dense and isolated features.

holes (CH) are resolved, 30 nm isolated lines, and 28 nm dense lines/spaces (L/S).

The 28 nm dense L/S can now also be printed over the exposure field with good uniformity. Fig. 10 has the wafer CD map for 28 nm vertical L/S, sampled over 3 rows and 5 columns, covering the 22.5×15 mm of the 26×22 mm exposure field. Good CD uniformity is obtained for 28 nm L/S, and a 3 sigma value of 2.2 nm was calculated from the experimental data.

On the same wafer, the CD uniformity was also measured for 30 and 32 nm horizontal and vertical dense lines, as well as for 30 and 32 nm isolated lines. The 3 sigma values, as summarized in Fig. 11, stay well below 10% of the CD value at 28 nm L/S, and are 2 nm or less for 30 and 32 nm L/S. The CD uniformity of 38 and 40 nm CH was measured using a similar sampling plan, but with another resist.

Besides imaging results, first implementations of EUV lithography as a technology to pattern the critical levels of the next technology nodes are being investigated. EUV lithography was used to pattern the first metal layer of electrically working 45 nm node logic devices [22] and was implemented on the contact level of a 32 nm node SRAM (see Fig. 12) and resulted in electrical functional 0.186 μm^2 6T-SRAM cells [23]. Next target is to implement EUV lithography on both the contact and the interconnect level of 22 nm node SRAM cells.

The current target for EUV photoresist sensitivity is 10 mJ/cm^2. The feasibility for reaching this sensitivity target has already been demonstrated today. However, the major challenge is to reach the sensitivity target while maintaining performance for resolution and line-width roughness (LWR) [24]. The inter-dependence of LWR, Sensitivity and Resolution has been described in literature and termed the "Triangle of Death" or "Lithographic Uncertainty Principle" (see Fig. 13).

Simultaneous optimization of resist formulations for these three performance parameters has been selected as one of the top three critical issues for successful introduction of EUV lithography for four years in a row at the annual EUVL Symposium.

The main area of concern for chemically amplified resists at the 32 nm and 22 nm node is how to meet the very tight line-edge roughness (LER) specifications $(\mathrm{LER} < 1.2\ \mathrm{nm})$. Although the problem may be somewhat more severe for EUV than for the other technologies (due to the unfavorable shot-noise statistics), it is of concern for all optical patterning technologies that target this node. Currently there are no known chemically amplified resists (for EUV or 193 nm) that meet these specifications. Besides this, metrology of such low LWR values is by far not trivial.

Various novel resist concepts are being proposed to tackle several of the issues that are thought to limit current LWR values. These include non-chemically amplified resists, molecular glass resists and many others.

Nowadays, several state-of-art EUV resists demonstrated a linear resolution down to 32 nm half pitch on the ASML EUV ADT. An ultimate resolution of 28 nm L/S, 34 nm dense contact holes, and 30 nm isolated lines is achieved in the best performing resists, as illustrated in Fig. 9. Good usable process windows with reasonable LER of 4.5 nm (3 sigma) for 32 nm L/S and 30 nm isolated line are demonstrated. Champion values for sensitivity, LER and resolution are 7.5 mJ/cm^2, 3.8 nm (3 sigma) and 28 nm, respectively. However these are not achieved with the same material. In order to further reduce LER, post processing techniques might be the only way to go.

EUV reticles impose new challenges, partially due to their reflective nature and the new materials they consist of. The main challenge is defectivity, which recently has been identified as critical issue number 2 for EUV lithography to be introduced into high volume manufacturing. First, the lack of a suitable pellicle material in EUVL, due to the high absorption of almost any material, is a big concern. As a result, it will be a challenge to keep reticles particle-free during transport from the mask shop to the wafer fab, and during their use in the wafer fab (handling, exposing and storage). Second, EUV reticles can have other types of defects than particles or regular absorber defects: 1) reflectivity loss and 2) multilayer type defects (ML). Both are EUV specific. ML defects refer to a local height distortion of the ML, which is a quarter-wave stack of alternating Mo and Si film pairs. A very shallow distortion (e.g., 2 nm) can already have a serious effect because of the short wavelength used [25], [26]. These very shallow defects are very difficult to detect for state-of-the-art reticle inspection tools using DUV wavelengths. The need to develop actinic reticle inspection tools (i.e., using the 13.5 nm wavelength) is considered a very critical issue for EUV as well. During inspection of a wafer printed on the EUV ADT several repeating defects were found and identified as mask defects. A number of printing defects found could not be visualized with a reticle SEM. Their printing impact is assumed to be due to a local distortion of the multilayer. The above results prove the methodology for the qualification of mask defectivity by wafer printing and wafer inspection, constrained to

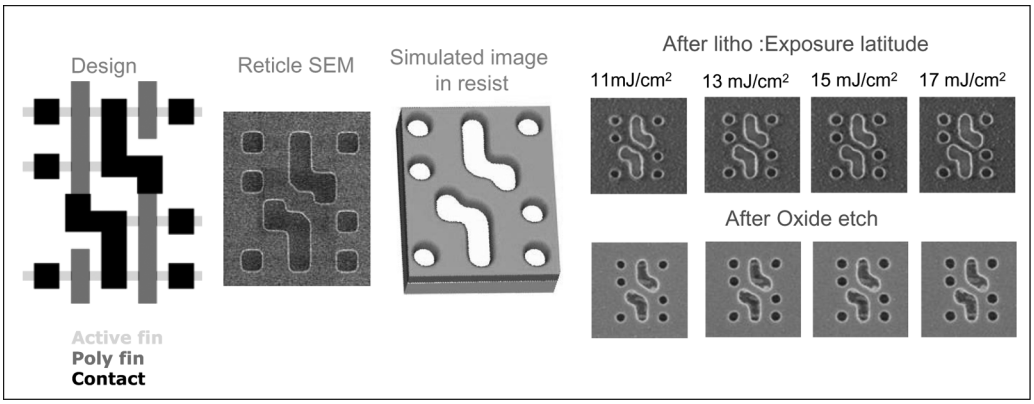

Fig. 12. Results of implementation of EUV in a 32 nm node SRAM cell.

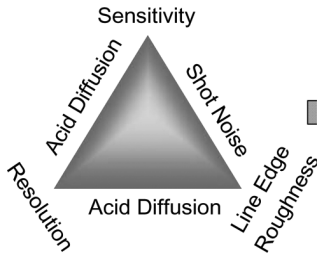

Fig. 13. Graphical representation of the "Lithographic Uncertainty Principle", which demonstrates the interdependence of LWR, sensitivity and resolution and the physical processes through which they are linked.

repeating defects. Its sensitivity is estimated better than today's available dedicated blank inspection and patterned mask inspection tools.

Reflectivity loss of the multilayer can be caused by EUV induced carbon growth or oxidation of the capping layer. This contamination phenomenon most likely is the most important reason to consider reticle lifetime as another challenge for EUV. Mask cleaning can mitigate it, and should not only remove particles, but also this kind of contamination, without affecting the tightly thickness-controlled layers of the multilayer and the capping material on top of it.

Today EUV blanks with different material stacks are commercially available. When investigating their performance differences by simulations and experimental verification, the mask stack offers opportunities to deal with some of the challenges.

The mask capping layer and its thickness can be optimized to minimize the sensitivity to carbon growth [27]. An inappropriate capping layer thickness (due to contamination or deterioration during mask making) will impact CD control on wafer. The main concern thereby is one of loosing uniformity of the printed CD over time, especially due to the enhanced impact of contamination by nonuniform thickness loss of the capping layer during the mask patterning process.

Towards future half-pitch nodes, the use of a thinner absorber [19] on the mask is highly recommended to reduce the shadowing effect, caused by non-telecentric off-axis illumination of the mask and leading to a CD variation, but also to a mask error enhancement factor (MEEF) dependence on pattern orientation. Opportunities are seen to achieve an embedded phase shift mask (PSM) [28], [29] where reduced thickness is combined with a 180 degree phase shift and a partially reflective absorber. This improves the contrast over the presently used conventional EUV masks. Other types of PSM can be explored to give further improvement. This is an example of the main strength of EUVL: it is very extendible to future nodes, by applying the same "tricks" used in 193 nm lithography to EUVL.

Thus, EUV lithography has shown important progress in its ability to resolve dense pitches and isolated lines over the last year, and currently (with the state-of-the-art resists) the resolution limit for full-field imaging is at 28 nm (at 0.25 NA). To enable EUV in production, important progress remains to be demonstrated in throughput. The highest throughput reported thus far for EUV ADT remains below 5 wafers per hour (at 5 $\mathrm{mJ/cm^2}$ and for a full 300 mm wafer exposure) [30], and production tools are targeted for 100 wafers per hour. Higher source power, from either the laser produced plasma sources that are in development or improved discharge produced plasma sources, will prove critical for the success of the technology.

IV. Conclusion

For the 32 nm half pitch node, 193 nm double patterning is the only technique capable of providing the required resolution, reliability and throughput. This node should go into pilot development in 2009, meaning that production-worthy tools and infrastructure should be in place by that time.

Both 193 nm high-index immersion and EUV lithography have suffered delays in their development and have not met this target. The further development of 193 nm high index immersion has been stopped, since the material development limited the resolution of the technique to 32 nm half pitch, and extendibility of the technique to 22 nm half pitch was not seen as possible. Both double patterning at 193 nm and EUV are still contenders for imaging at the 22 nm half-pitch node.

However, in order to make the double patterning technique more cost-effective and avoid the extensive LELE approach, significant material development is still required. This may be achieved either through the use of materials with a nonlinear optical response (double exposure) or through process-induced freezing of the first image. Whatever the final choice for patterning is going to be, it is clear that significant resist material challenges lie ahead of us.

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