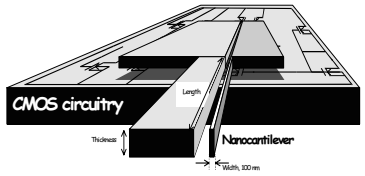


NANOMASS II

IST-2001-33068

NANORESONATORS WITH INTEGRATED CIRCUITRY FOR HIGH SENSITIVITY AND HIGH SPATIAL RESOLUTION MASS DETECTION

Final Report

Covering period: ***October 1st 2001-September 30, 2004***

Report Preparation Date: November 2004

Classification: Internal

Contract Start Date: October 1st, 2001 Duration: 3 years

Project Co-ordinator: Núria Barniol

Partners: Universitat Autònoma de Barcelona (UAB), Mikroelektronik Centret (MIC), Consejo Superior de Investigaciones Científicas (CNM-CSIC), Lunds Universitet (LU)

Information Society

FET-OPEN

Project funded by the European Community under the "Information Society Technologies" Programme (1998-2002)

Table of Contents

1. Executive summary

In this section a summary of the objectives and main achievements of the project are described. The roles of the partners involved in the project and the consortium's composition are also specified.

The objective of Nanomass II project is the development of the technologies for the combination of CMOS circuit fabrication with nanotechnology processes and techniques. The technology will be applied to the realization of mechanical mass sensors based on resonant nanometer scale silicon cantilevers integrated monolithically with the CMOS signal conditioning circuits. The excitation and detection of the cantilever displacement will be performed through the monolithically integrated CMOS circuitry.

Mass detection is based on monitoring the resonant frequency shift of the cantilever when nanometer-sized particles or molecules are deposited on the cantilever. The cantilever is electrostatically excited by means of an electrode located at submicrometer distance from the cantilever. A change in the cantilever resonance frequency is detected as a capacitance change. Electrostatic transduction in the nanometer-size regime requires the minimization of the parasitic capacitance since the magnitude of the current to be detected is proportional to the coupling capacitance between the cantilever and the driver, which is in the order of 10^{-17} F. Consequently, the readout circuitry has to be integrated "on-chip" in order to eliminate the parasitic capacitance introduced by the external bonding pads and wires. CMOS circuitry for excitation and read-out of the cantilever deflection is integrated together with the cantilever by using a monolithic technology that consists of the combination of standard CMOS processes and novel nanofabrication methods.

As a result of the developments pursued in the project a full System-on-Chip based on a nanoelectromechanical device and its read-out circuitry has been obtained. Figure 1.1 schematizes the main result achieved as a System-on-Chip. From the sensor point of view, a new type of high performance sensor devices capable of measuring one single molecule (i.e. a medium size protein as polypeptide chains) is expected: the resulting devices can be used as mass sensors, with an expected mass resolution of 10^{-19} g in vacuum, and a spatial sensitivity of less than 100 nm.

In particular, the project has developed the technology to combine standard CMOS technology with nanofabrication of resonant cantilevers. This includes nanocantilever fabrication using different techniques for nanofabrication: (i) laser/AFM nanolithography; (ii) electron beam nanolithography (EBL) and (iii) nanoimprint lithography (NIL), and its combination with CMOS integrated circuitry for the electrical readout and signal conditioning. The different nanolithography processes have been compared in order to evaluate the advantages of these techniques in terms of dimensions reduction, throughput and CMOS compatibility.

From the point of view of the material to fabricate the resonant cantilever, three approaches have been established: a) use of a polysilicon layer from the CMOS technology, b) use of crystalline silicon from SOI wafers and c) metal deposited by electroplating. The compatibilization with CMOS has provided the best results on polysilicon. On the other hand, the improvement on the mechanical properties of the cantilever resonator using crystalline silicon and the possibility to achieve smaller widths than with polysilicon (due to its granular structure), give to the SOI approach an added value to be taken into account. Concerning the metal cantilevers, preliminary

results made on non-integrated devices have shown a good resonant behavior and mass sensitivity. Integration into CMOS has not been attempted because of time constraints.

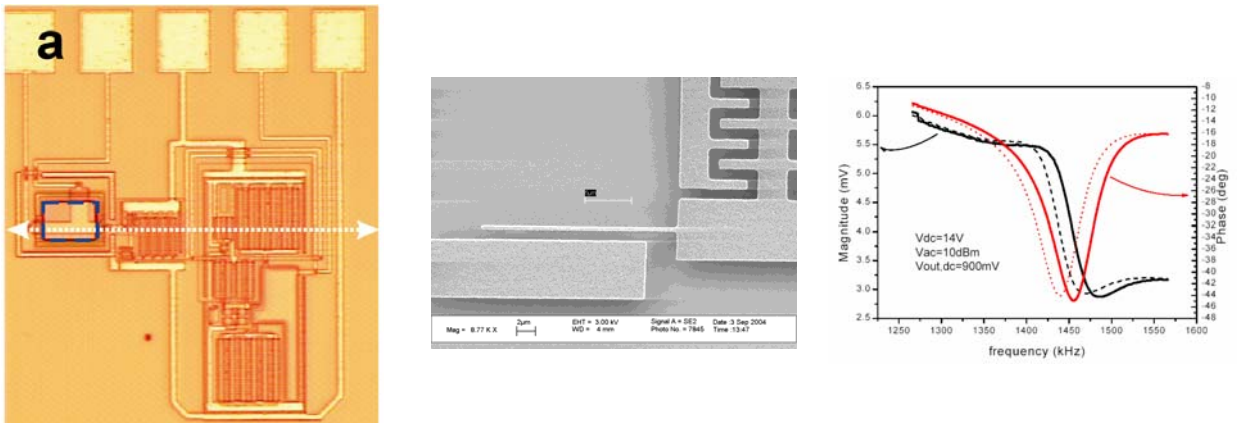


Figure 1.1. *System-on-chip fabricated sensor: a) optical image of the CMOS read-out circuit and the area in which the nanoresonator will be fabricated (blue square); b) scanning electron microscopy of a nanocantilever fabricated using electron beam lithography on the CMOS substrate; c) read-out obtained from the CMOS circuitry of the oscillation of the cantilever before mass deposition (solid line) and after mass deposition (dotted line).*

During the course of the project several demonstrators have been fabricated, which show the relative performance of each technological approach (from the point of view of the fabrication technique and also from the point of view of structural material for the cantilever):

i) Sensor formed by a single nanometer scale cantilever using Polysilicon as structural layer and laser lithography for defining the cantilever integrated monolithically with the CMOS read-out circuit. The dimensions of the cantilever are: length, l=40 μm; width, w=840 nm; thickness, t=600 nm and gap spacing s=1.3 μm. The natural resonance frequency derived from the experimental measurements is 703 kHz. The theoretical sensitivity of this cantilever is $34 \cdot 10^{-18}$ g/Hz, which is an extremely high sensitivity for punctual mass detection. In terms of distributed mass detection, the sensitivity is $12 \cdot 10^{-13}$ g/Hz/cm^2 which is comparable to quartz microbalances. In this first demonstrator the minimum measurable frequency change due to the electrical noise of the CMOS integrated circuitry and assuming that any measurement will be made in air (low Q factor) is $\delta f \approx 1.9$ Hz. In this case, the final mass sensitivity with the integrated system is below 65 attograms.

ii) Sensors formed by a single nanometer scale cantilever using Polysilicon as structural layer and fabricated by electron beam lithography integrated monolithically with the CMOS read-out circuit. The cantilever width is 420 nm, the thickness is approximately 600 nm and the length is 20 μm. The natural resonance frequency derived from the experimental measurements is 1.42 MHz. From the experimental mass measurements performed with this integrated NEMS sensor a mass sensitivity of approximately 3 ag/Hz has been determined.

iii) Sensors formed by a one-dimensional *array* of polysilicon cantilevers fabricated by standard optical lithography integrated monolithically with the CMOS read-out circuit. In this demonstrator, arrays of 2, 4 and 8 cantilevers with different excitation and detection schemes have been obtained. The dimensions of the cantilevers are 50 microns long, 1.4 microns wide and 600 nm thick. The natural resonance frequency of these cantilevers is around 750 kHz and its mass resolution is 63 ag/Hz. In this case the demonstrator will be useful for applications in which high mass sensitivity and multiple detection is needed (i.e. specific detection of different

molecules simultaneously), or when a spatial extended map is required (for example, mapping of an atom beam). It will allow performing additional signal processing like for example differential reading. It will also be possible to implement redundancy (multiple detection of the same magnitude) and interchangeability, which will increase the robustness and yield of the device.

Following there is a list of the main results achieved during the project:

1) *Electromechanical models for the cantilever-driver system (CDS).* New models for the CDS which take into account real deflection and effects on the small dimensions of the system (i.e. fringing fields) have been developed for static and dynamic operation. Evaluation of the sensor design (dimensions and layout) and polarizations of the system are derived from the models. Equivalent electrical model of the system needed for the CMOS circuit design have been also developed. Published articles related to this subject by one or more partners of the Nanomass consortium: [1, 4, 14]

2) *Fabrication of polysilicon cantilevers on CMOS substrates*. Cantilevers have been monolithically fabricated on one of the polysilicon layers of CMOS. Nanolithography techniques successfully employed on this substrate have been laser lithography and EBL. A specific post-process to release the cantilevers have been developed. Published articles related to this subject by one or more partners of the Nanomass consortium: [2, 3, 9, 10, 16]

3) *Fabrication of crystalline silicon cantilevers on CMOS substrates*. Both CMOS circuitry and cantilever transducers have been successfully fabricated on SOI substrates. Nanocantilever structures have been fabricated by EBL and AFM, combined in both cases with laser lithography. A specific procedure has been developed to ensure the connection between mechanical structures and CMOS circuits. Published articles related to this subject by one or more partners of the Nanomass consortium: [5, 6, 13]

4) *Compatibility study for the EBL technique on a CMOS pre-processed wafer.* A systematic study has been performed to determine the influence of EBL processing on the electrical performance of already processed CMOS circuits. Low electron energy combined with a laser-based lithography, has been determined as a successful combination for nanomechanical structure definition that does not affect the CMOS read-out circuitry. Published articles related to this subject by one or more partners of the Nanomass consortium: [16]

5) *Development of Direct Write Laser (DWL) lithography technique*. A CMOS compatible DWL technique has been developed for monolithic cantilever fabrication on CMOS substrates. DWL enables fast and flexible prototyping of sub-micrometric structures over large areas (cm^2). The technique is based on direct laser writing on substrates coated with a resist bi-layer. Published articles related to this subject by one or more partners of the Nanomass consortium: [11]

6) *Definition of cantilevers on the CMOS substrates by NIL using quartz stamps*. Specific stamps have been defined to imprint nanocantilever-driver structures.

7) *Design, fabrication and characterization of CMOS read-out circuits for cantilever resonance detection*. Several circuital architectures for the detection and amplification of signal coming from the cantilever based transducer, have been successfully designed,

fabricated and tested. Transimpedance and voltage amplifier configurations have given good results working on Polysilicon and SOI CMOS substrates. The mechanical resonance characteristics of polysilicon cantilevers have been successfully characterized through the output of the integrated CMOS detection circuitry. Published articles related to this subject by one or more partners of the Nanomass consortium: [2, 15, 16]

8) *Design, fabrication and test of arrays of polysilicon cantilevers on CMOS substrates*. Arrays of 4 and 8 cantilevers have been fabricated on poly-CMOS substrates. The control of the connection between cantilever and read-out CMOS circuit through a digital circuitry has been demonstrated. Simultaneous resonance and detection through the read-out circuitry of different components of the array has been also achieved.

9) *Functional evaluation in vacuum of polysilicon cantilevers on CMOS substrates*. A specific gas chamber for functionalization of the cantilevers and for the electrical characterization at different pressure and gas composition conditions has been developed. Electrical characterization of the poly-CMOS sensors in vacuum conditions has been tested. The dependence of Q-factor on pressure has been determined from ambient conditions to 0.7 mbar.

10) *Determination of mass sensitivity of polysilicon cantilevers on CMOS substrates*. A procedure for local deposition of latex beads and glycerine drops has been developed. From the detection of a glycerine drop of around 40 fg, a mass sensitivity of 3 ag/Hz in air has been determined.

For realizing the project, we have formed a consortium of **four partners** from **three different countries** who have the complementary expertise and resources and facilities for performing their part of the research program (see table 1). CNM is the National Center for Microelectronics in Spain. MIC is the Department of Micro and Nanotechnology of the Danish Technical University. CNM has expertise with the development of intelligent microsystems for sensing applications using the CNM CMOS 2,5 μm technology. MIC has expertise in micromechanics, biosensors and nanotechnology. LU is the Solid State Physics & Nanometer Structure Consortium of the University of Lund, and it has experience on nanotechnology and biosensors. UAB (Universitat Autonoma de Barcelona) has expertise in the design of integrated circuitry and it has expertise in nanotechnology (AFM-based nanofabrication). In terms of tasks, UAB has been in charge of the modelization of the cantilever, the design of the microelectronic circuits and of the electrical characterization of the mass sensor. MIC and LU are in charge of the fabrication of the nanoresonator, UAB and MIC are in charge of the functional evaluation and finally CNM is in charge of the fabrication of the CMOS circuit as well as the study of the compatibilization of the nanoprocess with the CMOS.

As it is shown in this report, the combination of CMOS technology with standard nanolithography techniques has been demonstrated through the successful fabrication of complete nano-electromechanical systems (NEMS). This has been possible due to the constant and strong collaboration of all four partners of the consortium.

This unique monolithic combination of conditioning CMOS circuitry and nano-mechanical transducer has immediate implications on high mass sensitivity and spatial resolution of the particular mass sensor devices of the project, and opens the route for industrial application of the sensors.. But also, it opens very promising perspectives in other fields where NEMS produced in a monolithic way can take a big advantage like in High Frequency Telecommunications.

Table 1: Consortium in Nanomass II project

Partic. Role*	**Partic. no.**	**Participant name**	**Country**	**Main tasks and expertise**
C	1	Universitat Autònoma de Barcelona (UAB)	Spain	Sensor modelization CMOS circuit design and electrical characterization and test
P	2	Departament of Micro and Nanotechnology of Danish Technical University (MIC)	Denmark	Nanoresonator fabrication by laser/AFM lithography. Functional evaluation Nanofabrication. Biosensors
P	3	Consejo Superior de Investigaciones Científicas (CNM)	Spain	CMOS circuit fabrication. Combination CMOS-nanofabrication CMOS technology. Microsystems
P	4	Lunds Universitet (LU)	Sweden	e-beam lithography. Nanoimprint lithography Nanolithography. Biosensors

*C = Coordinator , P - Principal contractor

2. Project objectives

The overall objective of the project is the development of nanoelectromechanical systems (NEMS) based on the combination of nanofabrication methods with standard microelectronic CMOS circuit fabrication. As demonstrator, mass sensor devices capable of sensitivity up to one single molecule will be fabricated. It is the aim of the project to explore the new frontiers in research on nanotechnologies to develop functional and applicable nanodevices and nanosystems. Figure 2.1 shows the global concept of the project.

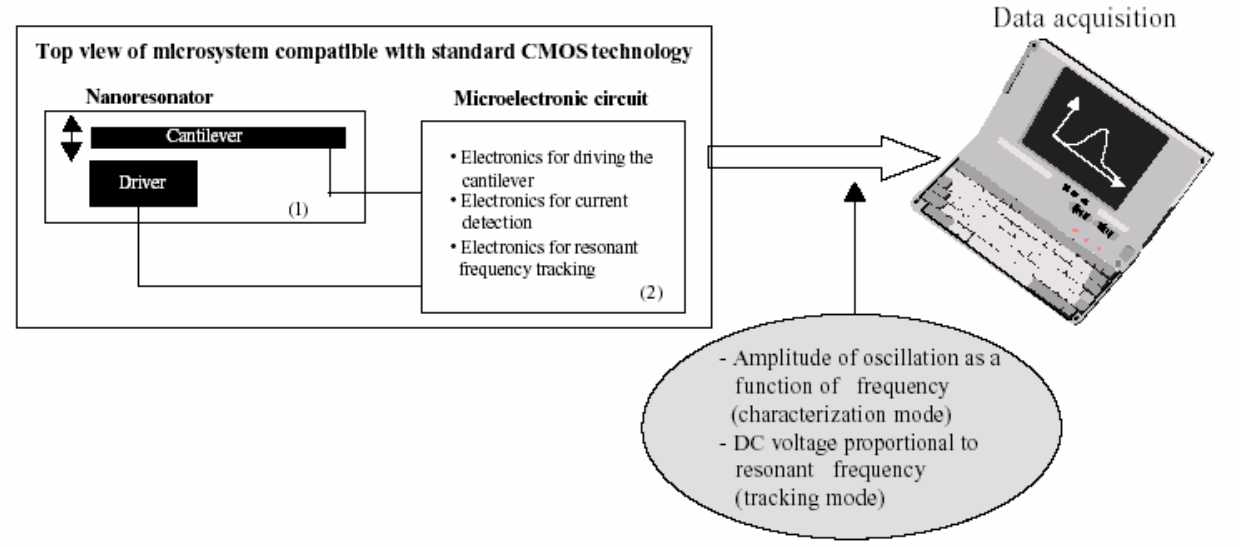


Figure 2.1 *General concept of the project. A smart micro-nanosystem will be fabricated by combination of nanotechnology for fabricating the nanoresonator and CMOS technology for circuit integration.*

The activity in the project is centered in the development of:

- technologies for combining CMOS circuitry with nanotechnology processes
- techniques for the fabrication of mechanical mass sensors based on nanometer scale resonant silicon cantilevers

The mass sensor device will be able to monitor multiple physical and/or chemical processes simultaneously. For example it can be applied as a very compact and sensitive environmental or biochemical sensor. Electrostatic excitation and capacitive detection will be used. It is necessary to have a CMOS circuitry closely integrated with the mass sensor in order to achieve the electrical read-out of the mass sensor. Thus, the final *nano-microsystem* will consist of the resonant nanocantilever and the CMOS circuit.

Two kinds of sensors will be fabricated:

b) *Sensors formed by a single nanometer scale cantilever*. The cantilever will have nearly atomic mass resolution, in the atto-gram regime (expected mass resolution of 10^{-19} gr), and a spatial resolution of less than 100 nm. The mass sensitivity is high enough to detect changes in mass corresponding to a single biomolecule, like a medium size protein as for example

polypeptide chains. It will also be useful in applications where high spatial resolution is desirable. The idea is here to scan the mass sensor, for example through an atom beam.

c) *A linear array of cantilevers*. A linear array of cantilevers will make possible the best performance of the devices. It will be useful for applications in which high mass sensitivity and multiple detection is needed (i.e. specific detection of different molecules simultaneously), or when a spatial extended map is required (for example, mapping of an atom beam). It will allow performing additional signal processing like for example differential reading. It will also be possible to implement redundancy (multiple detection of the same magnitude) and interchangeability, which will increase the robustness and yield of the device.

More specific objectives are related to the actions designed to go deeply into the combination of CMOS technology and nanofabrication processes, and to optimize the device performance:

Objective and action 1: *Optimization of CMOS circuit-transducer interface*

The optimization of the CMOS/nanodevice combination at the fabrication and circuit level for electrical excitation and read-out will be developed. Development of specific models for the cantilever-driver electro-mechanical response and equivalent electrical models will be pursued. The read-out and control of the array of cantilevers will be addressed with special attention.

Objective and action 2: *Use of alternative approach for the combination of CMOS circuitry and nanofabrication: SOI substrates and metal cantilevers*

To overcome the limitation on the reduction of dimensions of the nanocantilever by the use of the CMOS polysilicon as the structural layer of the device, silicon-on-insulator (SOI) substrates and electroplating will be used to make the cantilever on crystalline silicon and on metal respectively. Compatibilization issues with CMOS will be addressed.

Objective and action 3: *Use of several nano-fabrication techniques: laser lithography, atomic force microscope based lithography, e-beam lithography and nano-imprint lithography*

Establish a technology for integrating the different nano-fabrication techniques with the CMOS circuit fabrication. Introduction of e-beam lithography will allow comparing performance in terms of resolution between e-beam nanolithography, now a well-known technology, and laser/AFM lithography. At the appropriate stage of the project (by the mid-term period), the optimal lithography technique will be chosen for final implementation. Introduction of nanoimprint lithography will allow in the future increasing the throughput in nanocantilever fabrication. Feasibility of parallel fabrication will be evaluated in this case, and issues like alignment will be specially addressed.

Objective and action 4: *Functional evaluation*

The objective of this action is twofold: (i) Establish the methodology for the calibration of the mass sensor sensitivity. Specific experiments will be performed in air and in vacuum to test the

sensors under different conditions. (ii) Establish the methodology for functionalization of the cantilever in order to perform biochemical sensing. Passivation of the surfaces will allow to avoid undesirable contaminants or particles to deposit on the cantilevers. Functionalization will allow performing specific detection. New methods to functionalize nanometer cantilevers will be developed here.

3. Methodologies

3.1 Overview

The objective of the Project is the development of micro/nano systems based on the combination of CMOS circuits and nanofabricated mechanical devices. The methodology for achieving this goal has been based in several pre-decisions:

- Fabrication of a system on chip (SOC) device
- Use of standard CMOS technology
- Mass sensor device as a demonstrator that will exploit the improvement of reduction of the dimensions of the mechanical device

The above requirements have implied a set of decisions that have been used for defining the activities in the project. The following table shows the main implications for the different levels of activity:

Technology	Monolithically integration of the nanomechanical structure and the CMOS circuit
	Use of standard layers of the CMOS circuit as the structural layer of the nanomechanical device
	Fabrication of the mechanical device as a post-process module to the fabrication of the CMOS circuit
	Use of different advanced lithography techniques for the definition of the mechanical structure: Laser lithography, e-beam lithography, Atomic Force Microscopy lithography and Nanoimprint Lithography
Device	Mass detection is based on the change of the resonance frequency of a small cantilever Electrical excitation and capacitive read-out of the oscillation of the cantilever
	Lateral (in-plane) oscillation of the cantilever
Circuit	Use of CNM-CMOS technology for testing the concept
	Current amplification and voltage amplification schemes
	Management of array of cantilevers

3.2 Comparison with other activities in the same area

The NANOMASS concept is related with other actions in the area of nanoelectromechanical systems (NEMS). Next table show the comparison with other outstanding examples of applications of NEMS in different field:

Area	Applications	Relevant examples	Comparison with NANOMASS
MEMS/NEMS SoC	o Memory storage	MILLIPEDE (IBM-ZURICH) o Thermomechanical system based on AFM tips (Array of 1024 tips) o Density of information larger than 100 Gb/cm2, better than magnetic systems o **Heterogenous integration**	Nanomass uses **monolithically integration**: it implies constrains on the nanofabrication processes and based materials for the nanomechanical structures, but the overall fabrication is simpler and more economical
Cantilever based sensors	o Biomedicine o Defense	o Detection of DNA hybridization [2] o Detection of TNT at very low concentration values (70 picograms/litre) [3] o Use of **optical detection** o **Not integrated microsystems**, but large instruments	Nanomass implements a **capacitive electrical read-out** of the cantilever oscillation, which allows high sensitivity detection (low noise) and easiness to **integrate arrays of cantilevers with circuits for signal processing**. However, operation in liquid is not feasible.
Mechanical resonators	o RF communic. o Mass sensing	o HF Nanomechanical oscillators with high Q [4] o Mass sensors based on nanomechanical oscillators with zeptogram sensitivity [5]	NANOMASS integrates nanomechanical resonators with CMOS circuits but for mass detection. Maximum frequency operation is dictated by the CMOS technology employed. **Circuitry for the detection of the oscillation is simpler** than the one used in [5], because the circuit is integrated, reducing parasitic capacitances.

---

*[1] Vettiger, P.; Cross, G.; Despont, M.; Drechsler, U.; Durig, U.; Gotsmann, B.; Haberle, W.; Lantz, M.A.; Rothuizen, H.E.; Stutz, R.; Binnig, G.K .**The Millipede**, **Nanotechnology Entering Data Storage*** IEEE transactions on Nanotechnology. **1**, 39-55 (2002)

*[2] J.Fritz et al. **Translating biomolecular Recognition into Nanomechanics**.* Science,. ***288**, 316-318, (2000).*

*[3] L. A. Pinnaduwage, A. Gehl, D. L. Hedden, G. Muralidharan, T. Thundat, R. T. Lareau, T. Sulchek, L. Manning, B. Rogers, M. Jones, J. D. Adams. **Explosives: A microsensor for trinitrotoluene vapour** Nature **425**,474, (2003)*

*[4] J.Wang, Z.Ren, C.T.C.Nguyen. Self**-aligned 1.14 GHz vibrating radial-mode disk resonators***. The 12th International Conferences on Solid-State Sensors, Actuators and Microsystems. Transducers'03. *Boston (USA), June 8-12, pp. 947-950. (2003)*

*[5] Xue Ming Henry Huang, Christian A. Zorman, Mehran Mehregany, Michael L. Roukes, **Nanoelectromechanical systems: Nanodevice motion at microwave frequencies** Nature **421**, 496,(2003)*

3.3 Structure of the plan of work

The combination between nanofabrication and CMOS circuit fabrication has been performed following two main routes, as it is specified in the following figure.

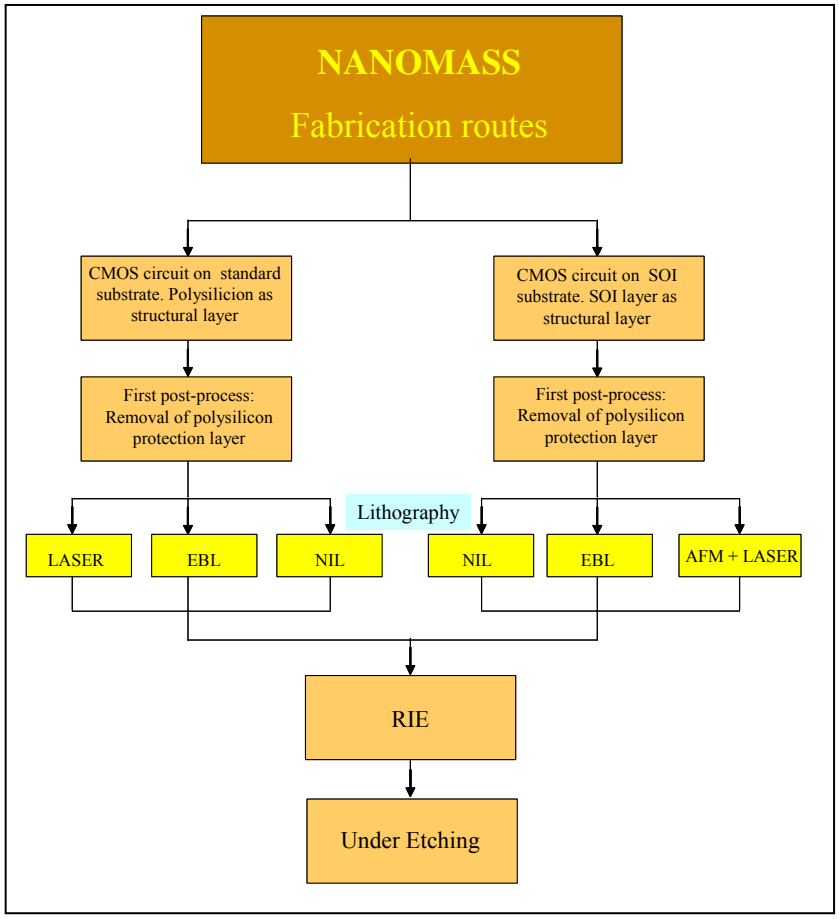


Figure 3.1. *Fabrication routes stablished for NANOMASS Project. Each fabrication route is defined by the silicon substrate where the CMOS is fabricated: standard silicon wafers (left) or SOI silicon wafers (right)*

Route 1 (left arm of the diagram) consist on using standard CMOS substrates and one of the layers of the CMOS circuit structure (polysilicon layer) as the structural layer for fabricating the device. This approach is much more standard and can be easily outsourced to other CMOS technologies, but it limits the minimum feature size of the nanomechanical structure due to the polycrystalline structure of the polysilicon. Route 2 (right arm of the diagram) consists on using SOI wafers as starting point, defining areas on the SOI wafer where the nanomechanical structure will be defined, and then the CMOS circuits are fabricated on the silicon substrate. This approach is more complex because it requires a previous step and it is not directly exported to other CMOS technologies, but it allows defining smaller structure because of the smoother SOI layer compared to the polysilicon layers.

During the fabrication of the CMOS circuit, a protection layer (polysilicon) is left in top of the area where the nanomechanical structure will be fabricated, in order to protect it during the whole CMOS fabrication process. This layer is the first process to be performed after completing

of the CMOS fabrication. Later, the lithography step is performed. AFM lithography has only been applied to the SOI substrates because it requires very smooth surfaces. After the lithography step, selective etching of the structural layer using advanced reactive ion etching (RIE) is performed. The final step is the under-etching of the oxide below the structural layer to release the cantilever. During the evolvement of the project, the development and optimization of the three processes (lithography, RIE and under-etching) have been undertaken.

The work-plan has been defined according to the above situation. Next table show how the work is divided in workpackages:

Work package	**Wokpackage title**	**Partner Leader**
WP 0	***Project Management***	UAB
WP 1	***Fabrication of sensors based on polysilicion cantilevers***	UAB
WP 2	***Fabrication of sensors using SOI substrates***	CNM
WP 3	***Fabrication of cantilevers by electroplating***	MIC
WP 4	***Fabrication of nanocantilevers using e-beam***	LU
WP 5	***Fabrication of nanocantilevers using NIL***	LU
WP 6	***Evaluation of applications***	UAB
WP 7	***Functional evaluation***	MIC
WP8	***Dissemination and Implementation***	UAB

WP1 and WP2 have form the core of the project, and define the two fabrication routes. WP3 has been defined as a completely new approach that finally has not been integrated (only non-integrated devices have been fabricated). WP3 and WP4 are devoted to optimize nanolithography (e-beam and NIL). WP6 and WP7 is where the test and characterization of the system is performed.

Another aspect that must be emphasized is that in order to achieve the full fabrication of the sensor, the participation of the four partners of the consortium is needed. In this way the sensor processing flow-graph is as follows: first the UAB design the circuitry and the layout for the nanoarea, second CNM fabricates the CMOS, third the lithography for defining the cantilevers is made at MIC or in Lund (depending on the lithographic technique employed), fourth the post-processing to obtain the cantilever is made at MIC, finally the samples come back to UAB in order to electrically test its performance. In this way we can state that the successful fabricated sensors have been made for all four partners in a serial process.

4. Project results and achievements

In this section the results of the Nanomass project are summarized. As it was explained in section 2, the main objective of the project is to achieve a system-on-chip based on nanoelectromechanical devices combining new nanoprocessing techniques with standard CMOS technology and obtaining a new kind of mass sensors with very high sensitivity. In order to achieve this final device, several actions have been undertaken as it has been explained in section 3 of this report. Following the explained plan of work, we have structured this results section in 7 main parts: 1) Nano-sensor design and modeling (results obtained from the work included in WorkPackage 1), 2) CMOS VLSI circuit design for the interface and the excitation and read-out of the nano-electromechanical devices (results obtained from the work included in Workpackage 1), 3) fabrication of polysilicon cantilevers using laser lithography and electron-beam lithography on CMOS circuits (results obtained from the work included in WorkPackages 1 and 4); 4) fabrication of silicon nanocantilevers using electron-beam lithography and atomic force microscope lithography on SOI substrates (results obtained from the work included in workpackages 2 and 4); 5) fabrication of nanocantilevers using nanoimprint lithography on CMOS substrates (results obtained from the work included in workpackage 5); 6) electrical characterization of the implemented sensors and 7) mass measurements performed with the system on chip sensors (results from the work included in Workpackage 6 and 7).

4.1 Nano-sensor design and modelling

In this section three electromechanical models (linear and non-linear) for a transducer based on a lateral resonating cantilever are described. In this transducer system, the on-plane vibrations of the cantilever are excited electrostatically by applying *DC* and *AC* voltages from a driver electrode. A capacitive read-out of the cantilever oscillation will be performed by means of a CMOS circuit, which will be integrated monolithically with the nanocantilever-driver system. The models are intended to predict the static deflection and the frequency response of the oscillation amplitude for different polarization conditions. It has to be taken into account that a knowledge as precise as possible of the electrical characteristics of the cantilever-driver system is crucial to address the CMOS circuit design. Thus the electrical specifications for the CMOS circuitry, as *DC* and *AC* driving voltages to avoid cantilever-driver collapsing, and capacitive current levels at the resonance of the cantilever-driver system have to be also predicted from these models. An electrical equivalent model of the sensor will be also derived to help on the CMOS circuit design.

Electrostatic transduction of the cantilever is accomplished by electrical force actuation and capacitive readout (see figure 4.1). An AC voltage is applied to a driver electrode, which is placed close and parallel to the cantilever, resulting in an electrostatic force that drives the cantilever oscillation. The capacitive readout consists of detecting the electrical current, i.e. the displacement current, which is induced by the change of the capacitance between the cantilever and the driver electrode as a consequence of the change of the spacing when the cantilever oscillates. In order to detect this displacement current, an additional DC voltage must be applied. The parasitic capacitance must be reduced as much as possible, and because of this a CMOS circuit must be integrated together with the cantilever/driver system.

Before starting with the description of the models developed during the project, a brief explanation of the mechanical behavior of a cantilever (beam with one fix end) is now summarized for a better understanding of the performance of the sensor. The two main cantilever parameters: i) spring constant, k, and ii) the fundamental resonance frequency, f_o, can be calculated according to the dimensions of the resonant structure and the mechanical properties of the material (Young modulus, E, and mass density, ρ):

$$k = \frac{E}{4}\ \frac{w^3}{l^3} t \quad \text{(N/m)} \tag{1}$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{E}{\rho}}\frac{w}{l^2} \quad \text{(Hz)} \tag{2}$$

where w, l and t are, respectively, the width, length and thickness of the lateral oscillating cantilever (according to figure 4.1). Approximating the cantilever tip displacement by a mass-spring model, the resonance frequency can be expressed as

$$f_o = \frac{1}{2\pi}\sqrt{\frac{k}{m_{eff}}} \quad \text{(Hz)} \tag{3}$$

where m_{eff} is the effective mass of the cantilever, $m_{eff}=0.24\rho wlt$ (kg).

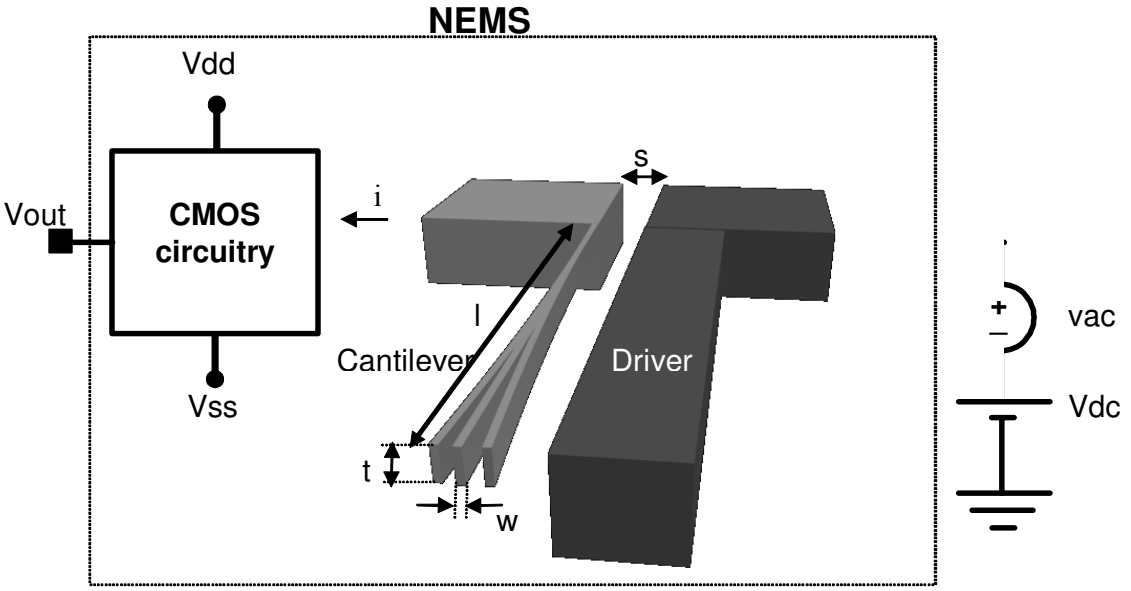


Figure 4.1. *Schematic drawing of the NEMS system based on a laterally vibrating cantilever (s direction) electrostatically excited and with a capacitive readout showing the dimensions of the cantilever-driver system.*

The resonance frequency of the cantilever will change when a mass is deposited. The dependence of the mass change (δm) on the resonance frequency shift (δf) is expressed in equation 4. This equation assumes that the extra mass is added at the tip of the cantilever, producing no change in the spring constant, but only a shift in its resonance frequency.

$$\delta m = \frac{k}{4\pi^2}\left[\frac{1}{(f_o - \delta f)^2} - \frac{1}{f_o{}^2}\right] \quad \text{(kg)} \tag{4}$$

A linear approximation of the previous equation around the resonance frequency, leads to a simpler expression for the mass sensor sensitivity:

$$\frac{\delta m}{\delta f} = \frac{1}{2\pi^2}\frac{k}{f_o^3} \text{ (kg/Hz)} \quad (5)$$

Using equations (1) and (2) and assuming a poly-Si cantilever (E=160 GPa and ρ=2330 kg/m^3), Eq. (5) can be written as

$$\frac{\delta m}{\delta f} \cong 0.9 l^3 t \text{ (kg/Hz)} \quad (6)$$

which implies that a theoretical mass sensitivity of 0.9 ag/Hz can be obtained with a cantilever of l=15 μm and t=600 nm. Note that under this approximation, the sensitivity does not depend on the width of the cantilever. Nevertheless if the resonance frequencies must be kept not very high for a simpler read-out scheme, the width must be small (i.e., for last dimensions if we want a resonance frequency below 1 MHz, the width must be 100 nm).

4.1.a) Linear electromechanical model for the cantilever-driver system

An electrical model of the sensor is required to address the CMOS circuit design. For this purpose, a simple linear electromechanical model has been used. This model makes it possible to derive the electrical requirements for the CMOS circuitry, as for example capacitive current levels at the resonance frequency, I_{res}, and DC and AC voltages for excitation and measurements.

The linear small-signal electromechanical model based on passive elements is shown in figure 4.2. The static capacitance of the cantilever-driver system, C_p, increases when a DC voltage, V_{dc}, is applied:

$$C_p = C_o(1+\kappa) \quad \text{(F)} \quad (7)$$

$$C_o = \varepsilon\frac{l \cdot t}{s} \quad \text{(F)} \quad (8)$$

where ε is the vacuum dielectric constant, s is the gap between cantilever and driver and κ is the so-called electromechanical coupling parameter, which is calculated from:

$$\kappa = \frac{\varepsilon}{2 \cdot k}\frac{l \cdot t}{s^3}V_{dc}^2 \quad (9)$$

The series R_s L_s C_s branch of the equivalent circuit describes the resonance behavior:

$$C_s = 1.789 \cdot \kappa \cdot C_o \quad \text{(F)} \quad (10)$$

$$L_s = \frac{1}{2\pi \cdot C_s \cdot f_{res}} \quad \text{(H)} \quad (11)$$

$$R_s = \frac{1}{Q}\sqrt{\frac{L_s}{C_s}} \quad (\Omega) \quad (12)$$

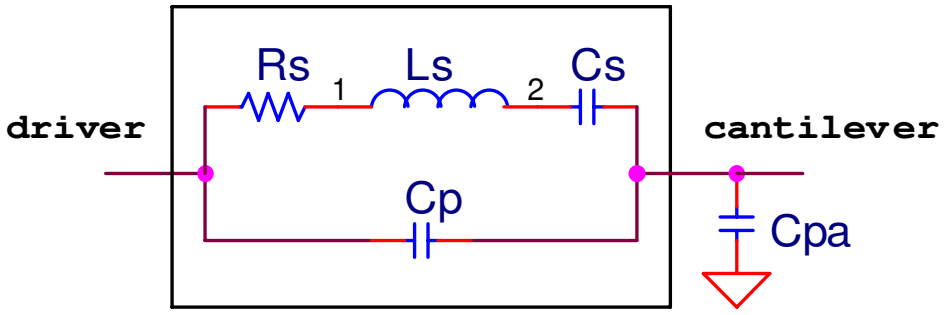


Figure 4.2. *Small-signal electromechanical model of the oscillating cantilever-driver system based on passive elements.*

In this model the quality factor, Q, and C_{pa} are both empirical parameters. C_{pa} is an additional parasitic capacitance. It accounts for the parasitic capacitance associated with the connection lines between the cantilever and the circuit (lay-out) as well as the input capacitance of the CMOS amplifier for the read-out.

Length (μm)	**20**	**30**	**40**	**50**
k (N/m)	3400	1	0.42	0.22
f_{res} (MHz)	3.55	1.58	0.89	0.58
$V_{pull\text{-}in}$ (V)	97	43	24	16
V_{DCopt} (V)	85	38	21	14
V_{ACopt} (V)	9.4	4.2	2.4	1.5
Cs (aF)	21.7	32.6	43.5	54.4
Cp (fF)	0.183	0.177	0.237	0.296
Ls (H)	92.4	312	740	1440
Rs (MΩ)	41.2	61.9	82.5	103
I_{res} (nA)	206	61.0	25.7	13.2

Table 4.1: *Theoretical electrical parameters for different nanocantilevers lengths, width =1 μm, gap = 1 μm and thickness = 600 nm and assuming polysilicon as the structural layer (E=160 Gpa and ρ=2330 kg/m^3). An expected quality factor for the cantilever-driver system in air, Q=50, has been considered for the calculation.*

In Table 4.1 electrical parameters as a function of cantilever length are listed. $V_{pull\text{-}in}$ represents the minimum voltage that causes the cantilever to collapse onto the driver electrode. V_{dcopt} and V_{acopt} are the optimal voltages applied to the driver electrode, which are used to calculate the values of the elements in the small signal model. These optimal voltages are calculated from a total optimal voltage, V_{opt}, which is obtained as a fraction of the pull-in voltage. Under these conditions, pull-in is avoided and the linearity regime of the oscillations is ensured. An expected quality factor for the cantilever-driver system in air, Q=50, has been considered for these calculations. This Q factor has been obtained from an optical characterization of the oscillation of several integrated cantilevers. Values for the parameters that correspond to a 40 μm long cantilever have been used for the design of the CMOS read-out circuits (table 4.1). With these dimensions C_p is as low as 0.236 fF and the expected current at the resonance frequency (887 kHz) is 25.7 nA when applying a DC voltage of 21.3 V and an AC voltage amplitude of 2.4 V. Note the large value of the equivalent motional resistance (R_s), which causes a low value of the

amplitude current at the resonance frequency, unlike other types of mechanical structures where an off-chip detection system is possible.

4.1.b) Non-linear model with parallel plate approximation

In order to account for the non-linear effects that the cantilever-driver system exhibits when it vibrates at large amplitudes, a large signal model has been developed. This is a non-linear model, because its validity is not restricted to small vibration amplitudes, but still consider two approximations: i) dynamically reduces the cantilever to a mass-spring system considering the effective mass of the 1st vibration mode and the spring constant of the cantilever; ii) the deflection of the cantilever is considered parallel to the driver, so that the cantilever-driver capacitance changes as a parallel plate capacitance with uniformly changing plate distance.

Assuming this parallel plate capacitance approximation, the cantilever-driver capacitance can be written as function of the geometrical dimensions of the system:

$$C = \frac{\varepsilon_0 lt}{s - z} \tag{13}$$

where z is the deflection of the cantilever towards the driver and ε_0 is the dielectric constant. From the classical Hamiltonian of the system

$$H = \frac{p^2}{2m} + \frac{kz^2}{2} + \int_0^z \frac{D}{m} p dz + \frac{1}{2}\frac{Q_C^2}{C} \tag{14}$$

and the Newton's second law

$$m\ddot{z} = -\nabla H \tag{15}$$

the equation of movement for the deflection of the cantilever can be derived

$$m\ddot{z} + D\dot{z} + kz = \frac{1}{2}V^2 \frac{\varepsilon_0 lt}{(s - z)^2} \tag{16}$$

where $p^2/2m$ is the kinetic energy, m is the effective mass of the cantilever (proportional to the polysilicon density, $\rho_{poly\text{-}Si}$), k is the spring constant which is proportional to the polysilicon Young modulus ($E_{poly\text{-}Si}$), D is the loss energy rate, Q_C is the cantilever charge (assuming that the driver is grounded) and V is the total voltage ($v_{AC}+V_{DC}$) applied between driver and cantilever. A transformation defined by the following equations:

$$I_v = T \cdot \dot{z} \tag{17}$$

$$z = \frac{1}{T}\int_0^t I_v dt \tag{18}$$

$$T \equiv \frac{\varepsilon_0 lt}{s^2} V_R \quad [N/V], \quad where \quad V_R = 1V \tag{19}$$

$$L = \frac{m}{T^2} \tag{20}$$

$$C = \frac{T^2}{k} \tag{21}$$

$$R = \frac{D}{T^2} \tag{22}$$

is used to convert the equation of movement (16), that involves mechanical and electrical magnitudes, in an equivalent equation which only involves electrical magnitudes:

$$L\dot{I}_v + RI_v + \frac{1}{C}\int_0^t I_v dt = \frac{V^2}{2V_R\left(1-\frac{z}{s}\right)^2} \tag{23}$$

The advantage of this new equation is that it decribes the behaviour of the current, I_v, that flows through a series RLC branch and, as a consequence, it can be implemented easily in an electrical circuit simulator like SPICE. An AC or SWEEP analysis can be then performed to get the solution of equation (23), I_v, when the frequency of the AC voltage (v_{AC}) or the value of the DC voltage (V_{DC}) are swept. Using equation (18) the static or dynamic response of the cantilever deflection, z, can be obtained from the current I_v. In conclusion, this is a model which is very convenient to simulate simultaneously electrical and mechanical behaviors and, consequently, to analyze the complete transducer-circuit system.

This model has been validated by fitting their predictions to measurements of the cantilever mechanical frequency response and static deflection, performed by tapping mode AFM. Figure 4.3 shows the model fit to the AFM measured deflections of a polysilicon cantilever, produced by static voltages applied between cantilever and driver ranging from 5 to 40V. Also the model fit to AFM measured frequency response of the mechanical cantilever vibrations is shown in figure 4.4.

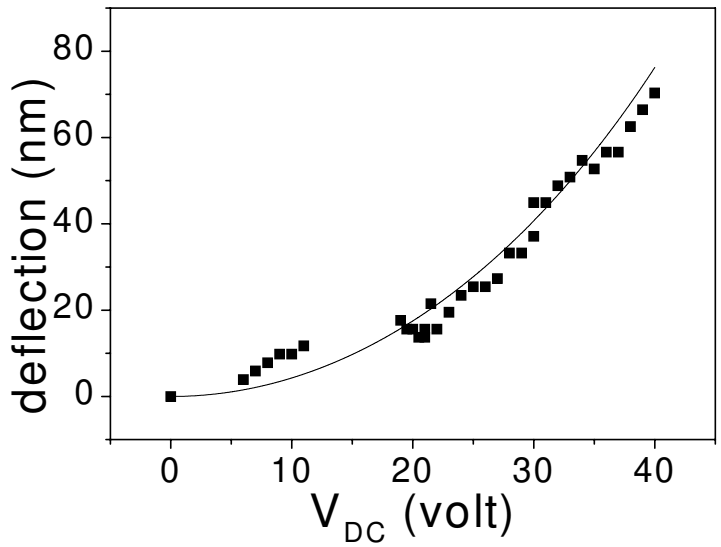


Figure 4.3: *Plot of the measured static cantilever deflection as a function of the applied DC voltage used to bend the cantilever (full squares), and fitting curve of the experimental points obtained from the electromechanically model using the following parameters: l=42μm, w=0.97μm, t=1.8μm, s=1.9μm, $\rho_{poly\text{-}Si}$=2.33 gr/cm^3, $E_{poly\text{-}Si}$=115 GPa.*

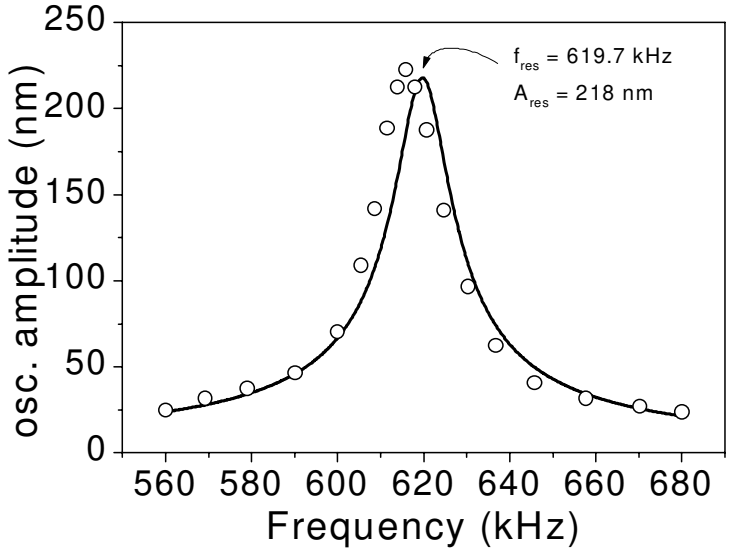


Figure 4.4: *Oscillation amplitude of the cantilever obtained from tapping mode AFM measurements as a function of the AC voltage frequency (open circles). Fit of this experimental points by the electromechanical model using the same parameters specified in figure 4.3 (solid curve).*

4.1.c) Non-linear model with real deflection of the cantilever

A third and more accurate model has been developed in order to better estimate the required dimensions of the cantilever and the polarization voltages for achieving the best sensor performance.

The model proposed is able to carry out static simulation as well as dynamic simulations. A static simulation will consist on applying a *dc* voltage between the cantilever and the driver, and to calculate the end cantilever deflection. On the other hand, in a dynamic simulation the resonant state of the cantilever is calculated when applying *dc* and *ac* voltages to the structure. From these simulations cantilever-driver system electrical static and dynamic properties (snap-in voltage, resonance frequency, output current level) are derived.

In this model the lateral cantilever oscillation is approximated by a spring–mass lumped model system, but it takes into account the real beam deflection in order to calculate the external force applied to the cantilever along its length. The equation of movement is given by:

$$m\ \ddot{z} + D \cdot \dot{z} + k \cdot z = F_{E-ff}(z,t) \tag{24}$$

where m, D and k are the cantilever effective mass, the damping factor and the cantilever equivalent spring constant, as defined before. $F_{E\text{-}ff}$ is the electrostatic force which takes into account the fringing field contribution and the real cantilever bending, and is related with the storage energy (W_C) between the cantilever and the driver through the following equation:

$$F_{E-ff}(z(y)) = -\frac{dW_C}{dz} = \frac{V^2}{2}\frac{dC_{FF}(z(y))}{dz} \tag{25}$$

In the present model, the total capacitance is calculated slicing the cantilever along its length, and considering that each sliced beam creates a plane parallel capacitance with the driver, calculated by:

$$C_{nFF}(z) = \left(\frac{\varepsilon_0 \cdot h}{s} \sum_i \left(\frac{l_i}{1 - z_i / s} \right) \right) \tag{26}$$

where ε_0 is the dielectric constant of the medium (air, vacuum), l_i is the element sliced length, and z_i is the lateral position of each slide with respect to the driver, see figure 4.5. Then, the force without fringing field contribution is given by equation 27:

$$F_E(z,t) = \frac{V(t)^2}{2} \cdot \frac{dC_{nFF}(z)}{dz} = \frac{V(t)^2}{2} \cdot \left(\frac{\varepsilon_0 \cdot h}{s^2} \sum_i \left(\frac{l_i}{\left(1 - z_i(z(t)) / s\right)^2} \right) \right) \tag{27}$$

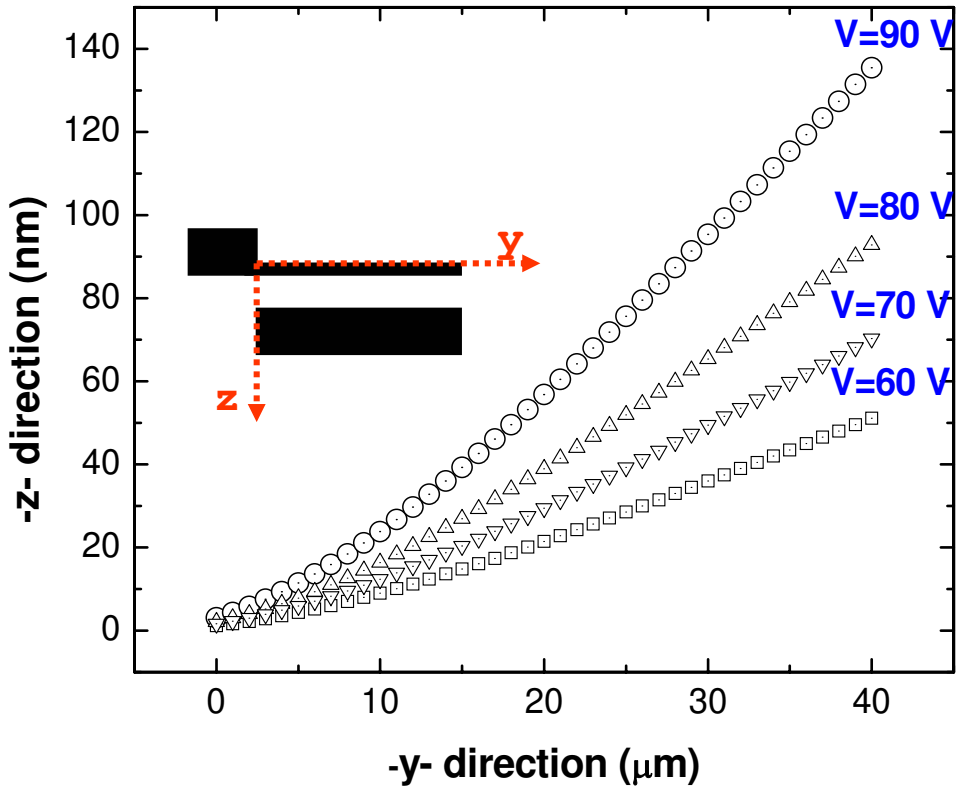


Figure 4.5. *Cantilever real deflection for different voltages applied. The deflection is calculated by a 2D FEM simulator.*

Fringing field contribution to the total capacitance of the cantilever-driver structure is obtained from the semi-empirical formulation developed to determine the fringing field contribution to the capacitance of adjacent lines in a CMOS circuitry. The fringing field component takes into account the cantilever side walls term along the cantilever thinnest dimension (*w* wide side). In

this formulation, a 3D numerical problem is approximated to an analytical equation which only depends on the cantilever-driver geometry. The total force derived is then:

$$F_{E-ff}(z,t) = F_E(z,t)\cdot\left(1+\alpha\left(\frac{s}{h}\right)\left(\frac{w}{s}\right)^{0.222}\right) \tag{28}$$

The fringing field contribution is adjusted to the cantilever-driver structure with the α parameter. Then, this contribution is modeled by a factor that only depends on the geometry. Figure (4.6) shows the resonant current generated in a cantilever-driver structure for two cases, α=0 (no fringing field contribution), and α=0.6. Differences on the resonant current for both cases are observed.

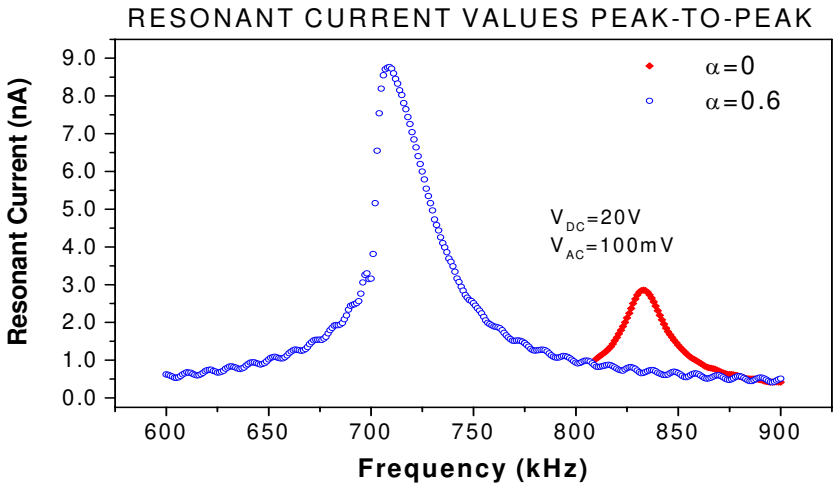


Figure 4.6. *Dynamic simulations of the cantilever-driver system taking into account the fringing field effects due to the finite dimension of the cantilever and the boundary fields*

The model has been validated by experimental measurements. Two different experiments have been developed. On one hand, static measurements involving dc applied voltages and static deflections and on the other hand, dynamic measurements for a given set of *dc* and *ac* voltages involving resonant frequencies and peak-to-peak oscillation values.

In the static measurement case, the *dc* voltage applied was varied from 50V up to 70V, which was enough to determine the cantilever deflection response versus the voltage applied. From these measurements, a response curve representing the free end displacement versus the voltage applied is obtained (figure 4.7), showing the non-linear dependence on the voltage.

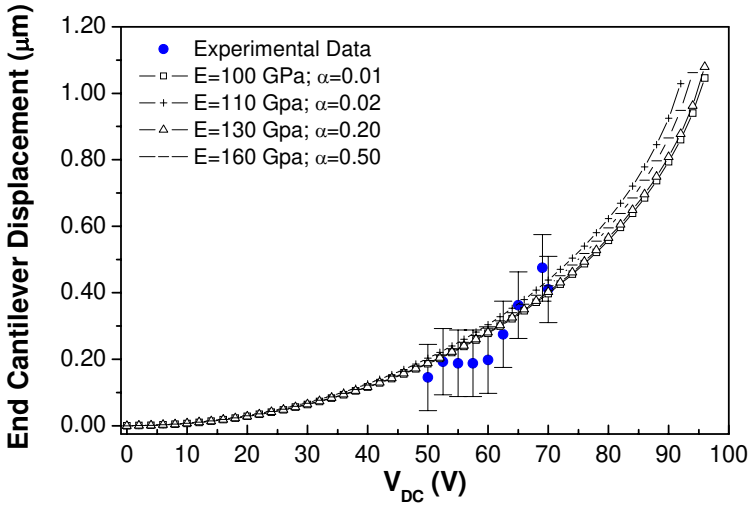


Figure 4.7. *Dynamic simulations of the cantilever-driver system taking into account the fringing field effects due to the finite dimension of the cantilever and the boundary fields*

As it is shown in figure 4.7, several possible sets of parameters (E, ρ and α) fit the experimental points with an error below the experimental uncertainty.

Additional constraints to determine all the fitting parameters have been found on dynamic measurements, which have been carried out for a set of dc and ac voltages. The dc voltage varied on a range between 15 and 35 V, and the ac voltage varied from 10 to 20 V peak-to-peak. From these experiments two magnitudes related to the cantilever-driver transducer have been derived: (a) the peak-to-peak end cantilever displacements and (b) the resonance frequency.

Fitting to experimental peak-to-peak oscillation values will give us an accurate prediction of the resonant current levels generated in a cantilever-driver structure for developing and designing the CMOS circuitry. For each pair of dc and ac voltages, a frequency sweep near the resonance has been performed, and the end cantilever peak-to-peak displacements have been measured for each frequency. From the obtained frequency response the resonant frequency is derived. Figure 4.8 shows the measured and simulated frequency response of the end cantilever displacement around the resonance, for two different voltages set: $V_{DC} = 15V, V_{AC\text{-}PP} = 20V$, and $V_{DC} = 35V, V_{AC\text{-}PP} = 10V$. With these voltage polarizations, linear resonance curves are experimentally observed.

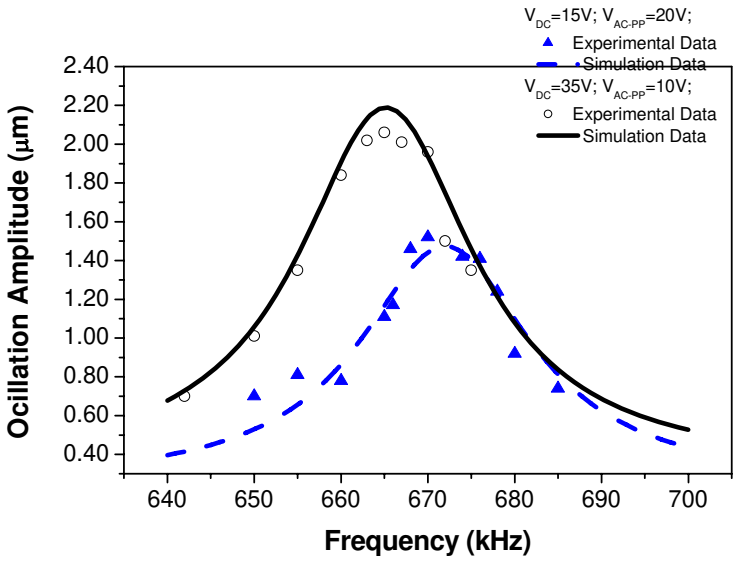


Figure 4.8. *Frequency response of the peak to peak oscillation amplitude for two different voltage polarization conditions: (a) V_{DC}=35V, $V_{AC\text{-}PP}$=10V (open circles) and (b) V_{DC}=15V, $V_{AC\text{-}PP}$=20V (filled triangles). Model fitting curves to the experimental points using E=110·10^{9}Pa, ρ=2.33·10^3 kg·m^{-3} and α=0.02. Error bars are suppressed for graph clarity (value 200nm on amplitude).*

Simulation parameters which fit experimental data are shown in Table 4.2. A good agreement between experimental and simulated data is also observed. Experimental error on the oscillation amplitude is related with the apparent size of a pixel in the captured image using the maximum magnification, which in our case is approximately 200nm.

Mass density, ρ (kg·m^{-3})	Young Modulus, E (Pa)	Fringing field factor, α	Quality Factor, Q
2.33·10^3	**110·10^9**	**0.02**	**40**

Table 4.2. *Simulation parameters for fitting the experimental data.*

After the model validation process, the Young Modulus appears to be a very significant parameter in order to fit the experimental and simulated curves. Then, it was decided to measure this parameter with an Atomic Force Microscopy.

The Young modulus of polysilicon cantilever was obtained by doing measurements with an atomic force microscope. The method is based on the measurement of the deflection of an end loaded cantilever beam, where the load is applied by an AFM probe. Because the value of the AFM cantilever spring constant has to be similar to the value of the cantilever sample spring constant, the experiment was performed with the AFM force applied at different positions along the length cantilever. Once the appropriate distance is obtained, measurements are performed at different positions along the width of the cantilever sample.

The movement of the AFM probe is controlled by a high-precision piezoelectric stage, and its deflection is measured with nanometric accuracy by an optical system composed of a laser diode and a photodiode. With this set-up, the cantilever spring constant could be measured, which in turn, allowed to indirectly derive the material Young modulus. Figure 4.9 shows a typical AFM force curve when the probe makes contact with the beam surface and forces the beam to bend.

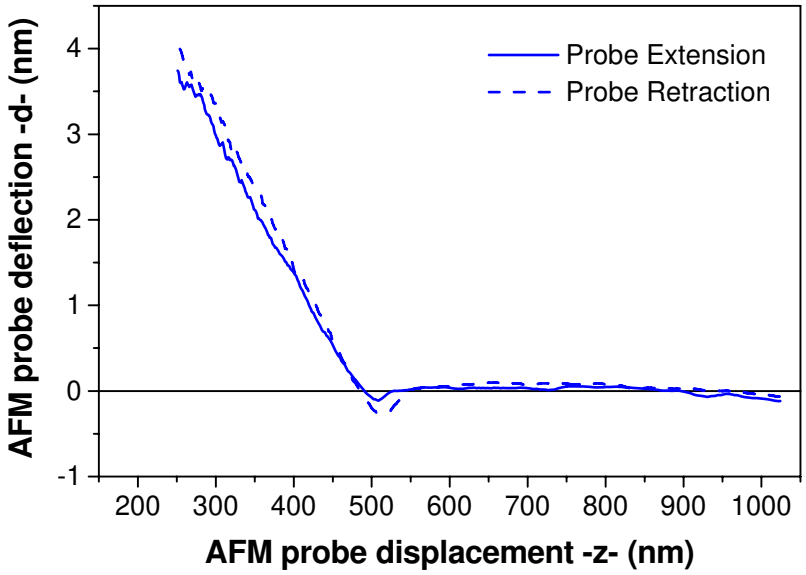


Figure 4.9. *Typical AFM force versus distance curve, where both extension and retraction curves are shown. The slope of the curve is lower than 1, because the sample is also bending.*

The vertical axis is the deflection measured by the AFM photodetector. Horizontal axis represents the vertical AFM cantilever displacement. The slope *A*, obtained from the contact region of the force curve, is used to calculate the material Young modulus of the sample cantilever:

$$E = \frac{4 \cdot l^3}{t^3 \cdot w}\left(\frac{A}{A-1}\right) \cdot k_p \tag{29}$$

Due to the strong dependence on the effective length *l*, i.e the position of the tip when pressing the beam, the experiments were carried out at different positions on the surface of the beam. Results are shown in figure 4.10: in that case, the length was always the same; for each experiment the tip was moving along the cantilever width. From those measurements, the polysilicon Young modulus was determined to be $E = (100 \pm 10) GPa$, which is in good agreement with the Young modulus derived from the fitting.

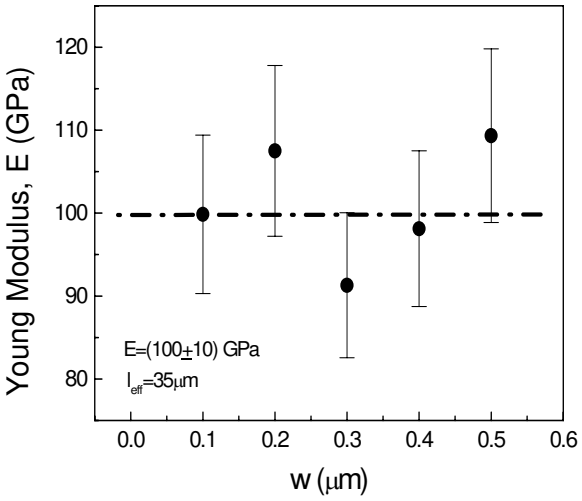


Figure 4.10. *Polysilicon cantilever Young modulus (E) extracted from AFM force curves at the same length of the cantilever but at different lateral positioning along the width of the beam.*

4.2. CMOS VLSI circuit design for the interface and the excitation and read-out of the nano-electromechanical device

Three main aspects have been addressed within this task and following the proposed objectives: a) read-out circuitry, b) added functionality and c) array management.

4.2.a) Read-out circuitry

The purpose of the CMOS circuitry is to detect and amplify the current generated by the cantilever-driver system. This current is a measure of the amplitude of the cantilever oscillation movement, and in consequence, it provides the frequency response of the cantilever (fig. 4.1). This current follows equation (30) where C represents the cantilever-driver capacitance composed by a static capacitance C_p plus a time variable component c that reflects the capacitance variations due to the movement of the cantilever, assuming that the AC voltage will be much smaller that the DC.

$$I_C(t) = \frac{\partial}{\partial t}(C \cdot V) = (C_p + c)\frac{\partial V_{AC}}{\partial t} + (V_{DC} + V_{AC})\frac{\partial c}{\partial t} \approx C_p \frac{\partial V_{AC}}{\partial t} + V_{DC}\frac{\partial c}{\partial t} = I_p + I_d \qquad (30)$$

The first term of this equation is a parasitic current (I_p) since it does not reflect the movement of the cantilever and it is generated due to the AC voltage that it is applied for excitation of the cantilever. The second term, called displacement current (I_d), reflects the oscillation of the cantilever since it depends on the variations of the driver-cantilever capacitance.

Assuming that the tip of the cantilever oscillates according to an harmonic movement, *z(t)*, since it is excited electrostatically by means of an AC voltage signal at a frequency ω, we can found the analytic expressions for the cantilever-driver capacitance (Eq. 31) and its time derivative (Eq. 32).

$$C(t) = C_p + c = \frac{\varepsilon_o l t}{s_o - z(t)} \quad \text{with} \quad z(t) = A_{eff} \sin(\omega t) \tag{14)(31}$$

$$\frac{\partial C}{\partial t} = \frac{\partial C}{\partial z}\frac{\partial z}{\partial t} = \frac{\varepsilon_o l t}{(s_o - z(t))^2} A_{eff}\, \omega \cos(\omega t) \tag{15)(32}$$

The parameter A_{eff} is the effective displacement of the cantilever assuming parallel displacement with respect to the driver. This parameter is calculated from the real amplitude oscillation of the cantilever tip according to $A_{eff}=0.39A$, which takes into account that the cantilever deflection is not exactly linear.

From the last expressions we can evaluate when the displacement current is dominant. Figure 4.10 shows the amplitude of the displacement and parasitic currents versus V_{DC} / V_{AC}, when a cantilever oscillation amplitude of 675 nm is assumed (the gap between cantilever and driver is around 1 μm). The use of high V_{DC} values, as far as the pull-in of the cantilever is avoided, increases the displacement current and in consequence enables an easier detection.

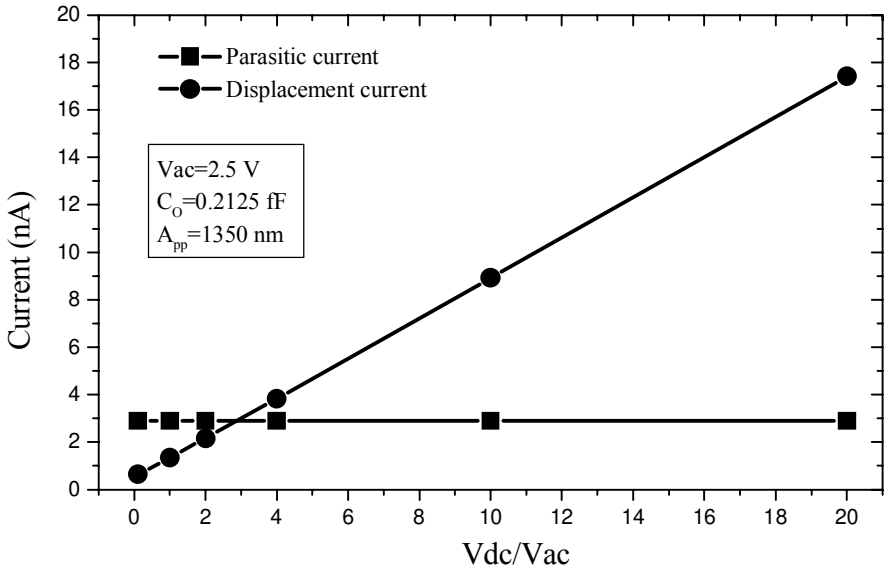


Figure 4.10. *Displacement and parasitic current amplitudes generated by the cantilever-driver system versus the ratio between the DC and AC applied voltages. Cantilever dimensions: l=40μm, s=1μm, w=840 nm and t=600nm. The assumed oscillating amplitude (675nm) corresponds to experimental data when the cantilever is at its resonance. The left hand portion of the figure (when Vdc<Vac) violates the assumption made for calculating the current, but it is shown here for completeness.*

One of the main objectives designing this circuitry has been the reduction of the parasitic capacitance, Cpa in figure 4.2, due to the metal lines that connect the cantilever with the circuit

and the input capacitance of the amplifier. A small value of this parasitic capacitance is required to detect a small current level (20 nA) at the resonance frequency (about 1 MHz) (see Table 4.1). This is addressed in the design of the CMOS circuitry and the interface between the area for the fabrication of the cantilever and the circuitry.

The minimum distance between the cantilever and the circuit is fixed by the CMOS-design rules. As it will be addressed in next section the NEMS system will be integrated with a 2.5 μm CMOS 2-polysilicon 2-metal technology from IMB-CNM[1]. The requirements of the nanofabrication process also increase the number of layers necessary on the area (protection steps), so special care has to be taken in the layout to avoid additional parasitic capacitance. In figure 4.11 the layout of the area where the cantilever is fabricated is shown. The layout provides a stray capacitance in the order of 20 fF (including cantilever capacitance between the structural layer, Poly0, and susbstrate, and metal paths to the circuitry). This capacitance influences the design of the readout circuitry.

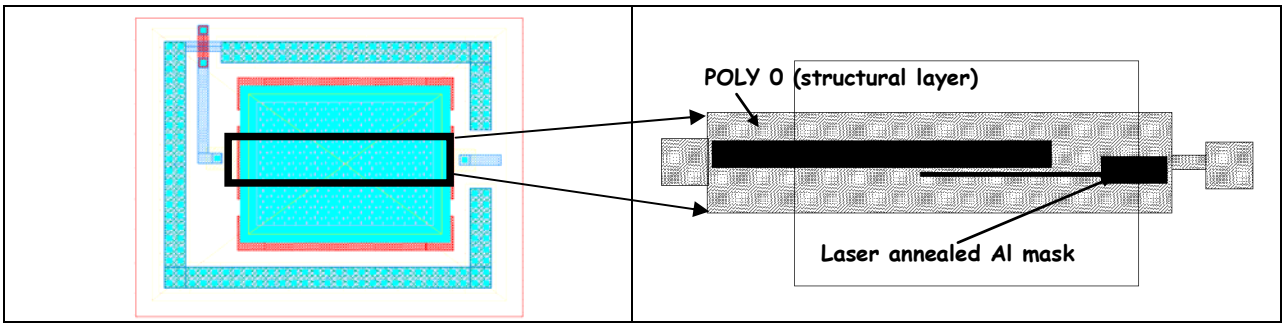


Figure 4.11. *(a) Layout of the area where the cantilever is fabricated (nanoarea). The active area (100μm x 20μm) for nanofabrication has been indicated with a thick line. (b) Layout of the final cantilever-driver system drawn on the nanoarea and which will be fabricated using nanolithographic techniques.*

Two different designs of the read-out circuitry have been implemented to detect the displacement current: (a) Current Amplifier circuits, called CA, based on a transimpedance amplifier and (b) Voltage Amplifiers or Buffering Amplifiers, called BA, based on a capacitive detection method. The two basic requirements for the CMOS circuitry are: (1) it has to be able to detect a low current around 20 nA and (2) the bandwidth has to be larger than 1 MHz.

Current Amplifiers (CA) or transimpedance amplifiers

The Current Amplifiers (CA) or transimpedance amplifiers are based on an operational amplifier with a resistive feedback, commonly called feedback ammeters. The principal advantage of this kind of circuits is the fact that the effect of the parasitic capacitance (Cpa) is negligible by virtually grounding it through the operational amplifier. Also and due to there is not any voltage difference between cantilever and substrate the sticking of the cantilever towards the substrate is avoided. Shunt ammeter configurations do not provide these benefits.

Another requirement of the CA circuits is to provide enough gain to amplify the low current at the resonance frequency. So, a large feedback resistance is necessary. There are two problems to

[1] IMB-CNM: Instituto de Microelectrónica de Barcelona, Centro Nacional de Microelectrónica. http://www.cnm.es

integrate this large resistance: i) the area and ii) the fact that large values of Cpa along with a high value of feedback resistance causes instabilities on the circuit. In addition any external resistance must be avoided, in order not to increase the overall stray capacitance.

Figure 4.12(left) shows one of the designs for the CA circuits. It is based on a T-configuration feedback with a shunt capacitance, *C*. The transfer function between the output voltage, V_{out}, and the current, *i*, at the transimpedance amplifier input, in Laplace domain, is:

$$\frac{V_{out}}{i} = \left(R_1 + \frac{R_2}{1 + R_2 \cdot C \cdot s} \right) \cdot \left(1 + \frac{R_3}{R_4} \right)$$

With this configuration an acceptable gain of almost $2 \cdot 10^6$ V/A is obtained without having to integrate high values of resistance (higher integrated resistance is 175kΩ). The function of the shunt capacitance, C, is to compensate the effect of the input stray capacitance, Cpa, on the circuit stability.

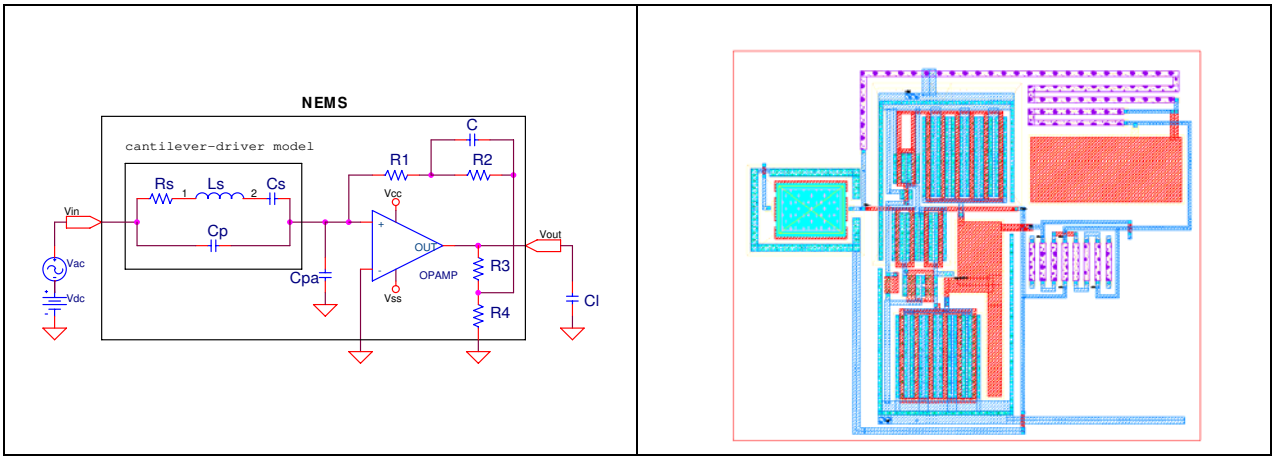
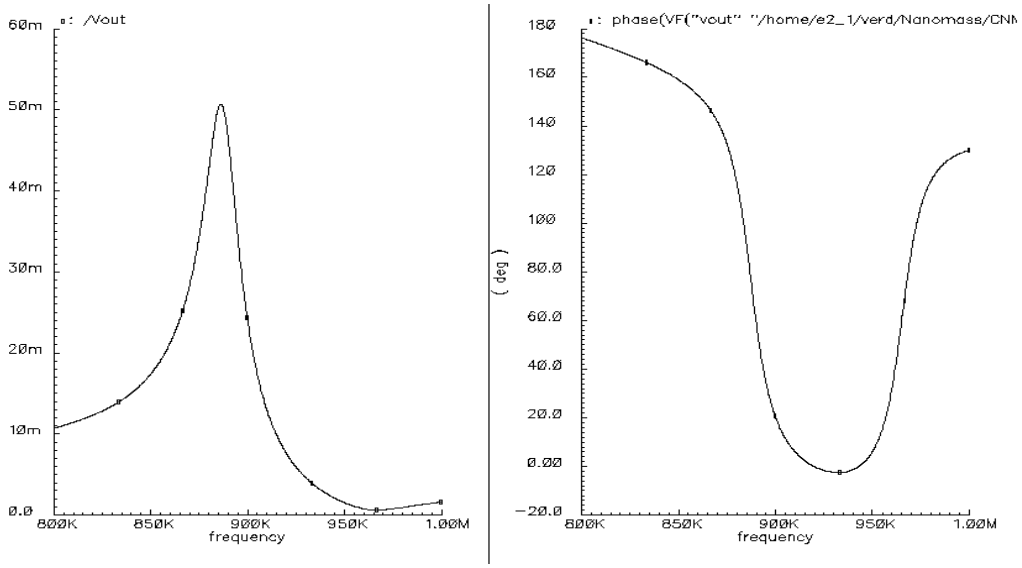


***Figure 4.12**. Schematic diagram of a CA circuit along with the nanotransducer electrical mode (lef), layout of the implemented circuit and nanoarea for cantilever fabrication (right).*

In figure 4.12(right) the layout of the CA circuit is depicted. The operational amplifier used is a simple two-stage amplifier with capacitor compensation. The dynamic characteristics of this operational amplifier are a gain-bandwidth product of 5,64 MHz (for a C_l=30 pF) and a phase margin of 59º. The overall area of the CMOS circuit and the area where the cantilever will be fabricated is 652μm*532μm.

In figure 4.13 the frequency response of the NEMS system from Hspice simulations is shown. The resonance voltage peak is located at 887 kHz and the voltage magnitude is about 50 mV. Further amplification with additional amplifier stages may be externally performed in this case.



magnitude *e* *phase*

Figure 4.13. *Hspice simulation of the frequency response of Vout for the cantilever-CA circuit system. The cantilever resonance frequency is found at 887 kHz.The equivalent electrical model for the cantilever with the parameters of table 4.1 has been used.*

Figure 4.14 is an optical photography of the implemented CA read-out circuitry showing the nanoarea ready for nanoprocessing. In figure 4.15 the electrical characterization CA circuits using a PMOS transistor current source are shown. We can observe in all the experimental curves a small variation on the gain values (corresponding with the frequency response of the amplifier) for different chips on the same wafer and also some variation on the circuit bandwidth for several wafers. Probably, this is because the mismatch effects on the W/L of the PMOS current source and the resistance of the N-well, in accordance to the tolerance provided by the CMOS technology. In all of them the BW is about 900-960 kHz, as expected.

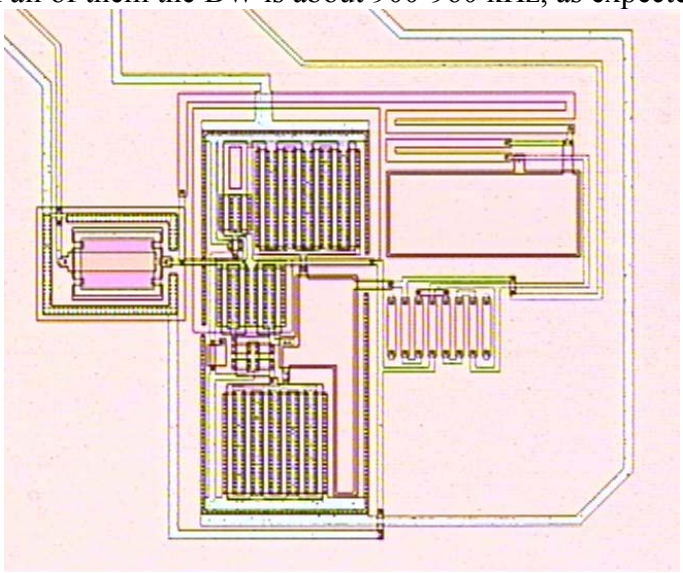


Figure 4.14*. Optical photography of the current amplifier circuit for the read-out of the movement of the cantilever to be fabricated in the nanoarea (specific area on the right of the image).*

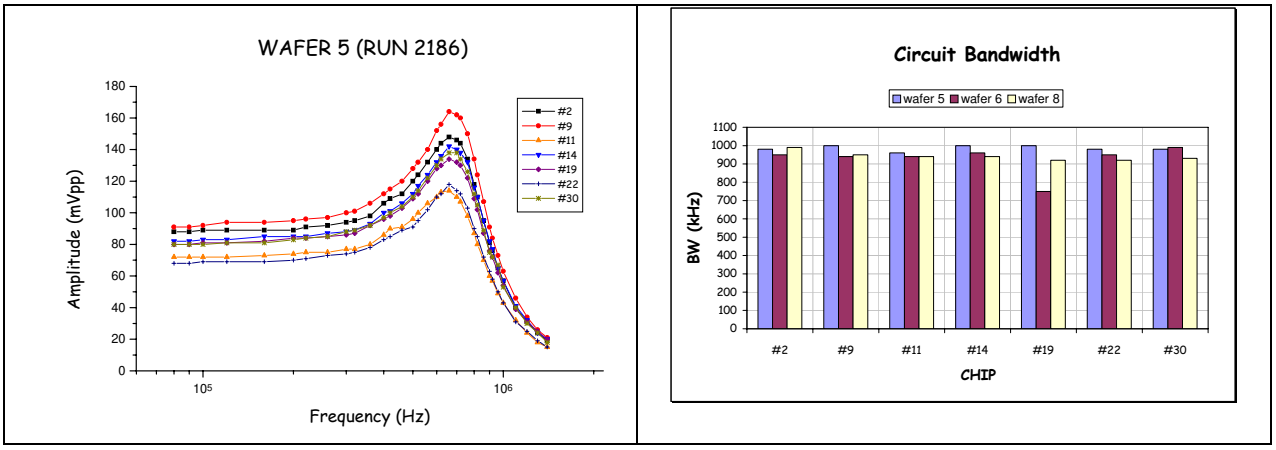


Figure 4.15. (a) *Experimental characterization of the AC circuits for several chips in the same wafer and (b) statistical behaviour of the amplifier bandwidth for different chips and wafers.*

Buffer Amplifiers (BA) or capacitive detection method

The principle of operation of the BA amplifiers is based on the integration of the capacitive current, I_C, by using a capacitor ($C_{pa}=C_{pa1}+C_{pa2}$) and measuring the resulting voltage (V_g in Figure 4.16) by means of a voltage buffer circuit. This non-sampled technique in CMOS technology introduces less noise than resistive or transimpedance methods, since the capacitor does not introduce input-referred current noise.

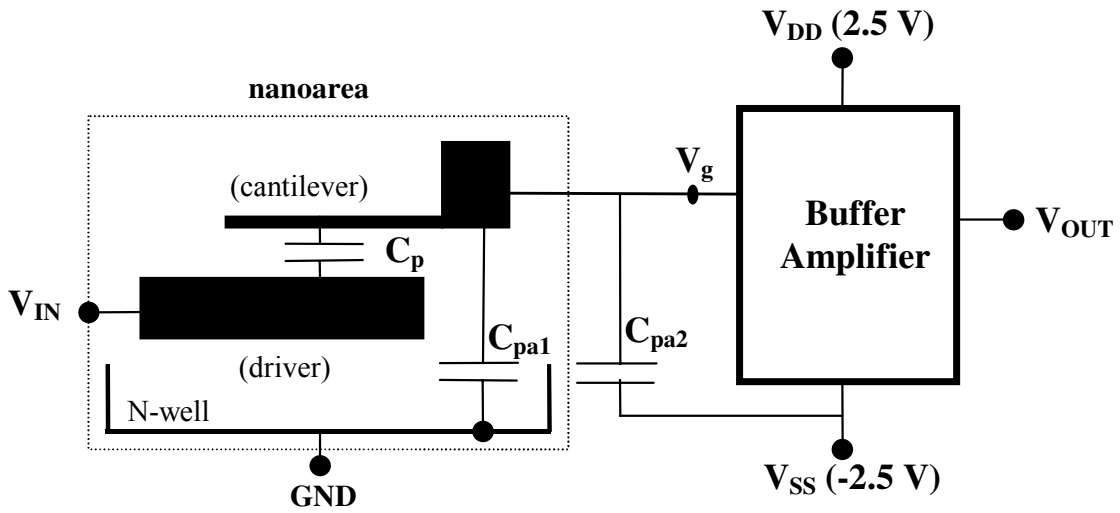


Figure 4.16. *Diagram of the capacitive read-out method used to detect the capacitive current generated in the driver-cantilever interface. The parasitic capacitance C_{pa} (parallel of C_{pa1} and C_{pa2}) is used as the integration capacitor.*

An approximate analytical expression for the amplitude of V_g, is presented in equation (34), where ω is the signal frequency, A is the oscillation amplitude of the cantilever tip and s_o is the gap distance in equilibrium. This equation takes into account that the excitation signal ($V_{in}=V_{DC}+V_{AC}$) does not only drop on the cantilever-driver capacitor but also on the parasitic capacitor, since it is based on a capacitor voltage divider scheme (equation 33).

$$V(C) = V_{in} - V_g = V_{in} \frac{C_{pa}}{C_p + C_{pa}} \tag{33}$$

$$V_g = \frac{I_C}{\omega C_{pa}} \cong \frac{C_p}{C_p + C_{pa}} V_{AC} + 0.39 \frac{C_p}{C_p + C_{pa}} \frac{V_{DC}}{s_o} A = V_P + V_D \tag{34}$$

The parasitic term, V_P, is due to the applied AC voltage and the term corresponding to the cantilever displacement, V_D, is proportional to both the DC voltage and the oscillation amplitude. V_g does not depend on the frequency and it is inversely proportional to the value of C_{pa}. By reducing C_{pa}, the sensitivity of the detection system increases and consequently the capacitive current signal-to-noise ratio at the V_g node improves. Due to the low level of current (few nA) at relatively high resonance frequencies (MHz) and the low value of C_p (0.2fF), the use of integration capacitances in the fF range is compulsory. Consequently we have chosen the small intrinsic capacitance at the V_g node as the integration capacitance.

Figure 4.16 shows that the parasitic capacitance (C_{pa}) can be divided in two components: C_{pa1}, constituted by the cantilever structure and substrate plus the electrical coupling to the cantilever, and C_{pa2} that represents the equivalent input capacitance of the CMOS circuit. The readout circuit design has focused on the minimization of all the parasitic capacitances as well as on getting high impedance at the sense node.

The read-out circuit design is presented in Figure 4.17. It is based on a CMOS voltage amplifier biased as a source-follower (common drain configuration). The voltage at the gate node controls the current of transistor M1, this current is mirrored and amplified through transistors M3 and M4 and finally the voltage across transistor M2 (configured as active load) is measured. This approach minimizes the input capacitance of the circuit because the dominant capacitance is C_{gd} (M1) which in the saturation region is smaller than C_{gs} (M1). Finally a voltage follower has been included for driving the load capacitance C_l, that corresponds to the output pad and electrical test setup.

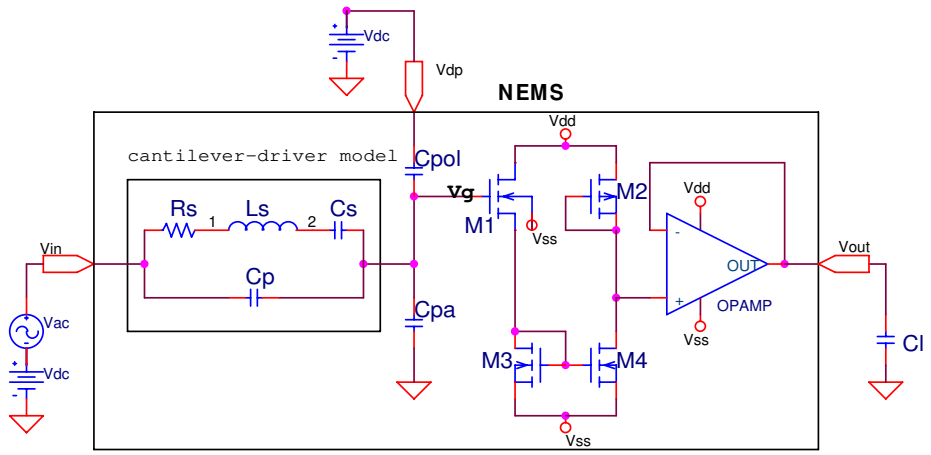


Figure 4.17. *Schematic of a BA circuit along with the nanotransducer electrical model.*

Since V_g is a floating node (no DC path to any fixed voltage), it has to be polarized at the linear region of the amplifier. In this case the optimal value of V_g is around 0 volts (figure 4.18). To guarantee this value, it is necessary to have a tuning circuit for biasing V_g. As it has been previously mentioned, we have to assure that the impedance at the sense node V_g is dominated by C_{pa} since the system has to operate like an integrator. On the other hand, any additional biasing

element (zero-biased diode, MOS device acting as a switch, etc.) connected at the sense node may have undesired effects on the read-out system (basically an increment of the parasitic capacitance C_{pa} and also an increment of the input-referred current noise). In the present work the V_g biasing has been achieved by adding an extra capacitance between the gate and a DC voltage source V_{dp}, C_{pol} in figure 4.17. The value of this capacitance must be high enough to control the biasing of V_g without having to apply high voltages and low enough to not increase the parasitic capacitance (ΔC_{pa}). A good trade-off for this capacitance is in the 1fF range. In figure 19a) an HSPICE simulation shows the effectiveness in polarizing the transistor gate and figure 19b) shows the experimental results of the variation of V_{out} as a function of V_{dp} demonstrating the feasibility to polarize the amplifier with reasonable voltages. Note that experimentally it is not possible to measure the voltage at the gate of the input transistor, V_g.

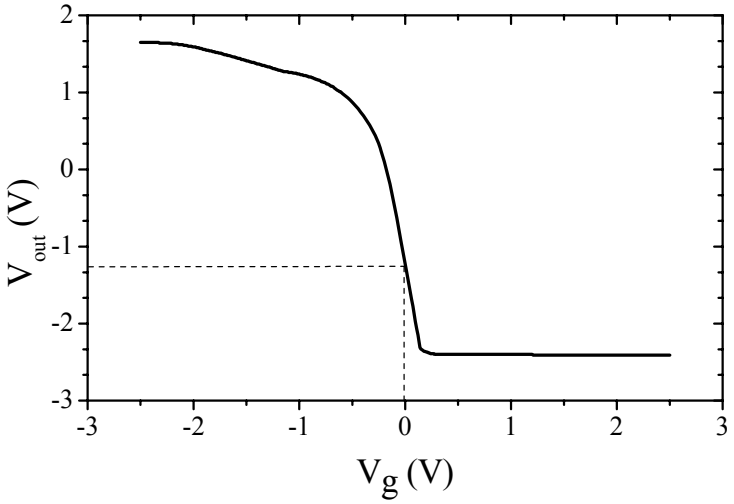
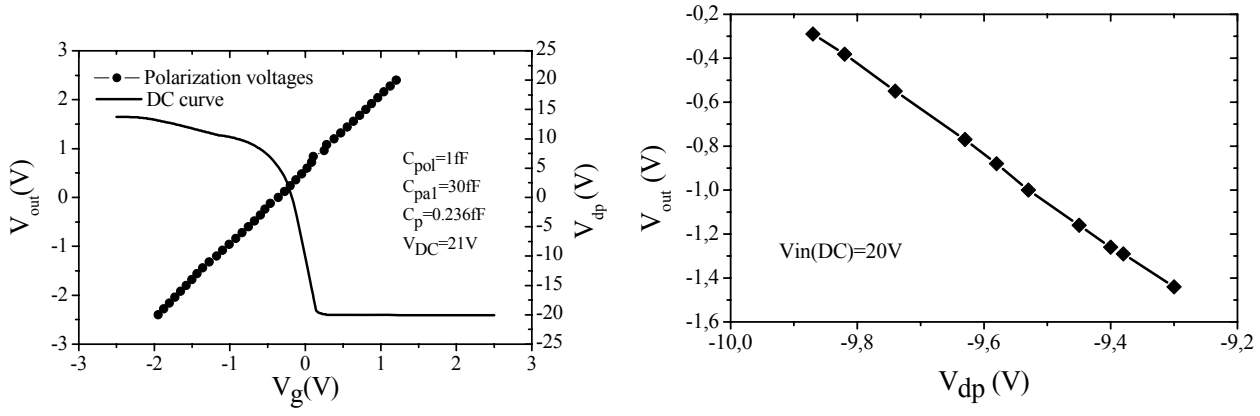


Figure 4.18. *Hspice simulation of the static characteristic of the read-out CMOS circuit. The optimal DC polarization voltage (which corresponds to the maximum gain) is indicated.*

The polarization capacitance is defined in a post-process to the CMOS circuit fabrication using the same nanofabrication methods as used for the cantilever fabrication. By using an interdigitized capacitor configuration, we minimize the increase of the parasitic capacitance due to the increase of the cantilever anchor dimensions.



a ***b***

Figure 4.19. a. *HSPICE simulation of the variation of the gate voltage, V_g, and output voltage,V_{out}, for different polarization voltages, V_{dp}.* ***b.*** *Experimental results of the variation of the output voltage, V_{out}, of the amplifier as a function of different polarization voltages, V_{dp}*

Figure 4.20 shows the layout of the cantilever /driver electrode system together with the additional capacitor in an interdigitized configuration (comb structure). The black area of the layout is defined during the CMOS circuit fabrication and it results in what we have called the 'nano-area', i.e., the area where the nanomechanical device will be fabricated. The final structure (white areas in figure 4.20) is defined as a post-process to the CMOS circuit fabrication using nanolithography and etching processes.

Although the success of V_g polarization has been verified, using a capacitor produces an unstable DC voltage at the sense node due to leakage currents, which in turn produces variations of the bias point. These variations have been detected for a time scale long enough to not affect the measurement of the full frequency spectral resonance of the cantilever. Other strategies for circuit polarization are currently being undertaken, which are based on the use of a very large resistor (zero-biased diode) in a special feedback topology that minimizes the negative effect of the junction diode capacitance on C_{pa}.

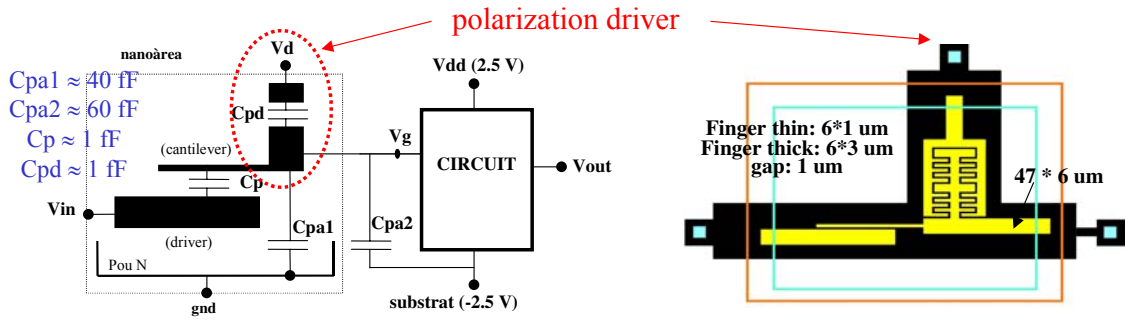
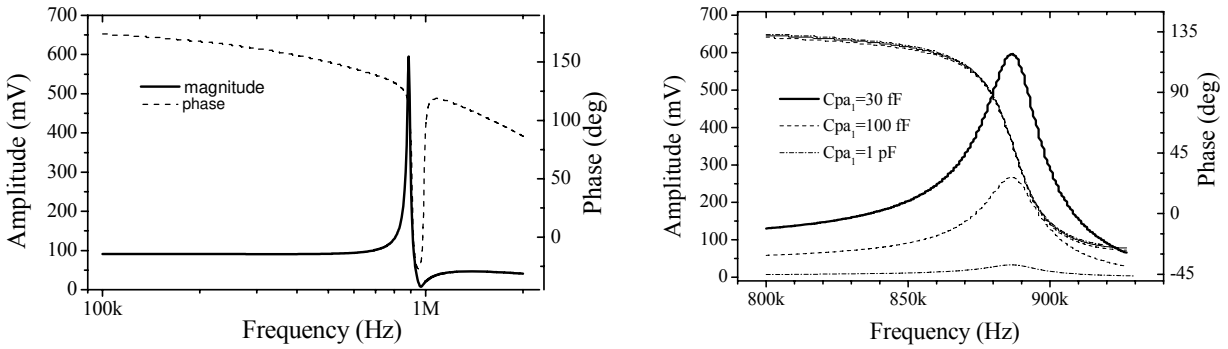


Figure 4.20: *Schematic diagram of the mechanical structure to be fabricated with nanofabrication techniques. Cantilever, driver and comb capacitor for biasing the voltage amplifier are shown.*

In figure 4.21, we show the frequency response of the overall system (mechanical resonator plus the read-out circuit) obtained by HSPICE post-layout electrical simulation. We can observe the resonance peak located at 887 kHz for a cantilever with a length of 40 µm (the rest of the parameters are chosen from table 4.1). Figure 4.21a corresponds to the case of a parasitic capacitance C_{pa1} = 30 fF. The effect of increasing C_{pa} is shown in figure 4.21b, which illustrates the necessity of keeping the parasitic capacitance as small as possible.

Since the estimated stray capacitance for the system (nanoarea and BA circuits) is about 30 fF, it can be stated that buffer amplifiers provide a higher output voltage than CA circuits. In figure 4.22 an optical image of the integrated Buffer Amplifier read-out system is shown. From the experimental characterization shown in figure 4.23, it can be observed that the bandwidth of these circuits is higher than 1 MHz. The only drawback of BA circuits compared with CA circuits is the requirement of biasing V_g at the optimal value (steepest slope). As a consequence, as we have already mentioned, an additional capacitance is needed.



a b

Figure 4.21. a) *Post-layout HSpice simulation of the frequency response for the global system (mechanical resonator plus read-out circuit). A* C_{pa1}*=30 fF has been assumed.* ***b)*** *Post-layout HSpice simulation of the frequency response (amplitude and phase) around the resonance frequency of the electromechanical system for different values of the parasitic capacitances. Note the degradation of the amplitude signal when the parasitic capacitance increases.*

Since the estimated stray capacitance for the system (nanoarea and BA circuits) is about 30 fF, it can be stated that buffer amplifiers provide a higher output voltage than CA circuits. In figure 4.22 an optical image of the integrated Buffer Amplifier read-out system is shown. From the experimental characterization shown in figure 4.23, it can be observed that the bandwidth of these circuits is higher than 1 MHz. The only drawback of BA circuits compared with CA circuits is the requirement of biasing V_g at the optimal value (steepest slope). As a consequence, as we have already mentioned, an additional capacitance is needed.

The final layout of the whole chip that includes both kinds of integrated circuits is shown in figure 4.24. From the experimental characterisation of the designed circuits, its agreement with the simulation results and the electrical characterisation of the resonant cantilevers (see characterization section) through these read-out circuits, the workable reading of these circuits is demonstrated.

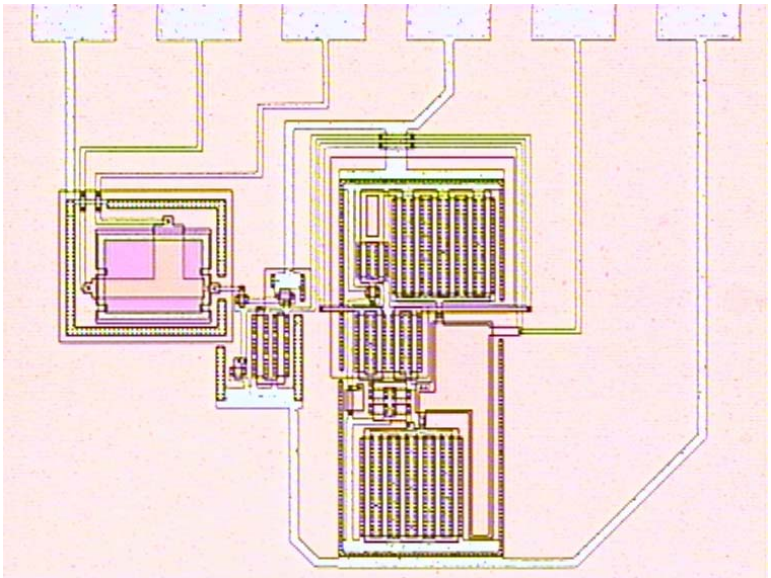


Figure 4.22. *Optical image of the Buffer Amplifier read-out system showing the nanoarea prior to the fabrication of the nanocantilever-driver system.*

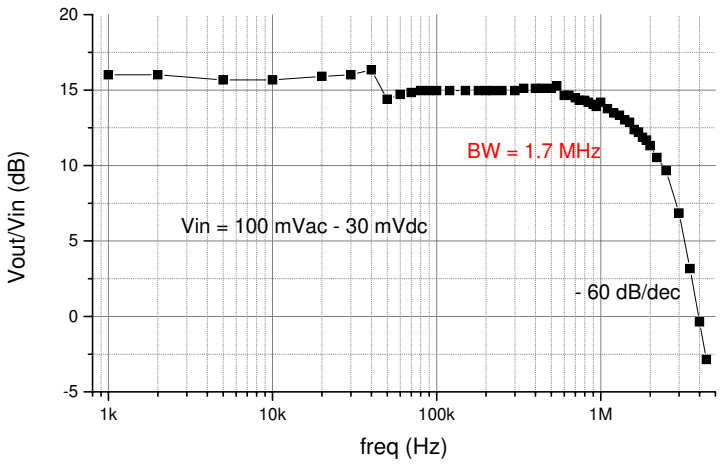


***Figure 4.23**. Result of the electrical test of the dynamic characterization of the buffer amplifier frequency response.*

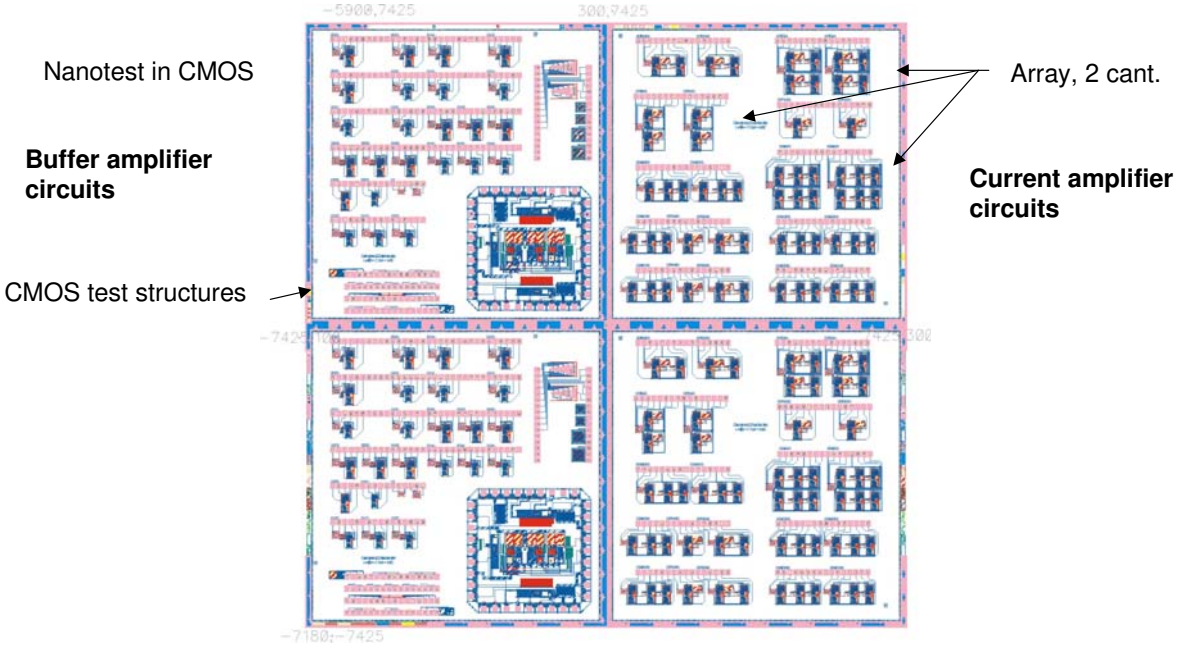


***Figure 4.24:** Layout of* the chip *with 80 circuits for testing* .

4.2.b) Added functionality

Due to the high variation and thus the higher sensitivity on phase in the frequency response of the resonating cantilever, a phase detection circuitry for the on-line characterization of the deposited mass has been designed. A block diagram for this on-line characterization is shown in figure 4.25: V_{out} proportional to new frequency and thus to mass variation.

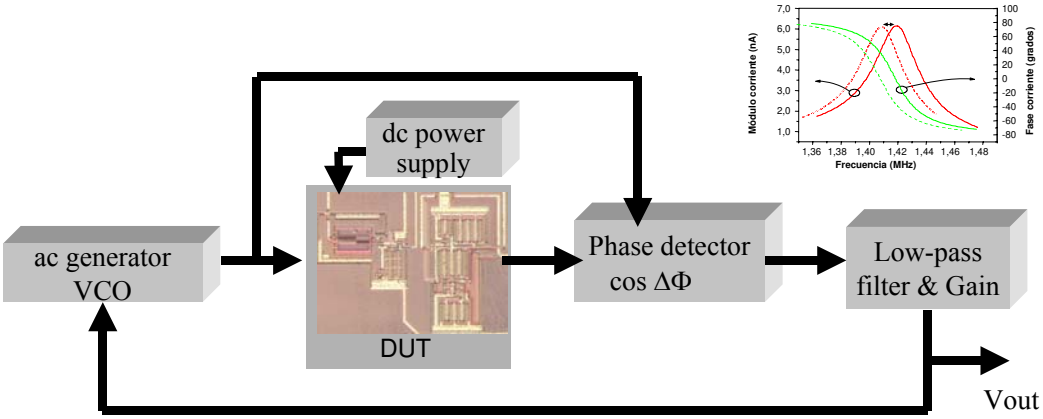


***Figure 4.25**: Block diagram for the real time mass measurement with on-chip circuitry*

The phase detection circuitry designed is based on a digital-edge triggered transitions phase detector (type II phase detectors normally used in Phase Lock Loops). As we are using ac electrical excitation for the resonance of the cantilever a proper conditioning of the signals is needed, so fast analog comparators has been also designed for squaring the ac signal from the generator and also the ac response of the cantilever. In figure 4.26 the experimental electrical test of the phase detector system is shown.

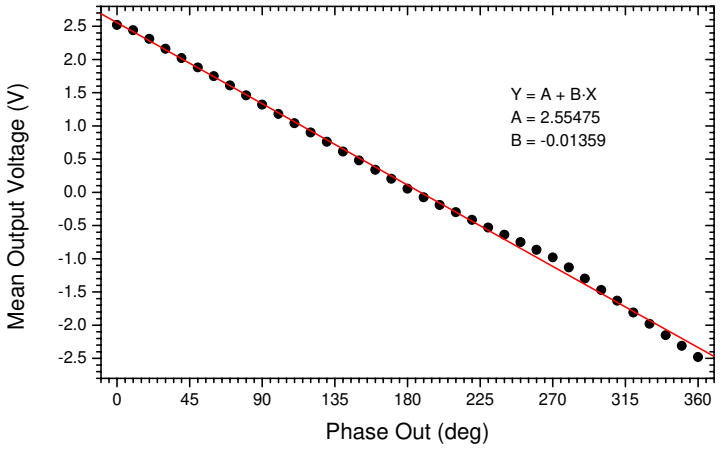


***Figure 4.26.** Electrical characterization of the phase detector circuit implemented with the CNM25 CMOS technology. Mean voltage of one of the output as a function of the phase difference between two sinusoidal signals after squaring with the designed comparators.*

4.2.c) Array management

In order to be able to control an array of 32 cantilevers, it is necessary to use multiplexing techniques and evaluate the parasitic capacitance of the MOS transistors as a switch. Two different configurations have been analyzed (figure 4.27): binary ladder multiplexing and direct multiplexing. Taking into account the electrical characteristics of the MOS transistors of the CNM25 technology[2], and the equivalent model depicted in figure 4.28, we can evaluate both

[2] NMOS transistor with W=L=4.5 μm. Ron (V_{ds} small @ Ids=20 nA) = 5 kΩ. I_{OFF} (V_{ds}=1 V) = 2 pA. C_{ON} (equivalent parasitic capacitance in source or drain in ON-state) = 28 fF. C_{OFF} (equivalent parasitic capacitance in source or drain in OFF-state) = 22 fF. I_{NOISE} (equivalent ac current, BW=2 MHz) = 0.28 nA

configurations (table 4.3). From these results, it is concluded that the binary ladder configuration is the optimum one for this application (the worse parameter is the electrical noise, due to the on resistance of the switch).

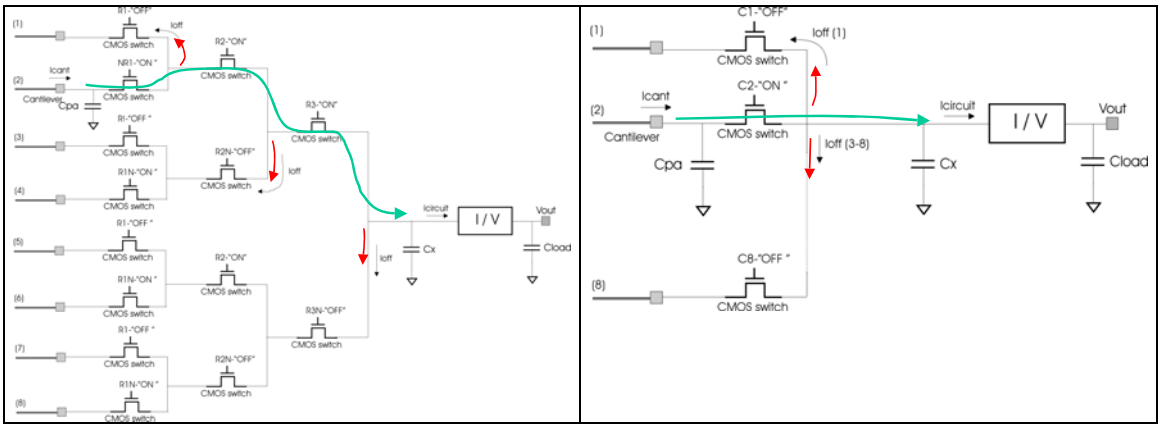


***Figure 4.27**: Multiplexing: a) binary ladder and b) direct*

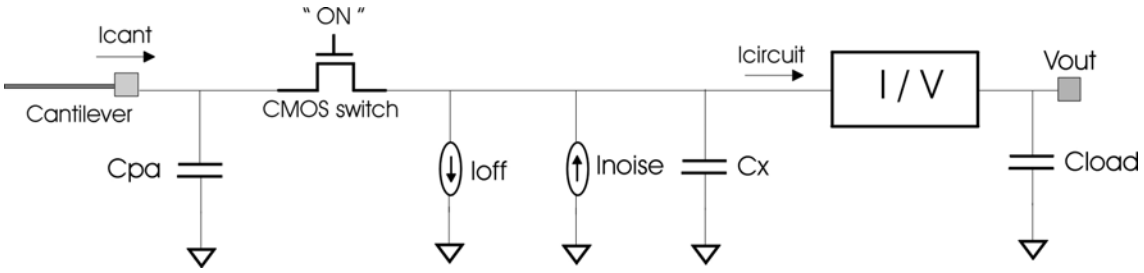


***Figure 4.28:** Equivalent electrical model for evaluation of configurations*

	Without mux.	Ladder mux.	Direct mux.
Cpa	20 fF + Cin (circuit)	48 fF	48 fF
I_{OFF}	0	6 pA (8 cant.) 10 pA (32 cant.)	14 pA (8 cant.) 62 pA (32 cant.)
ΔCx	0	48 fF (all cases)	182 fF (8 cant.) **710 fF** (32 cant.)
i_{NOISE}	0	0.49 nA (8 cant.) 0.63 nA (32 cant.)	0.28 nA (all cases)
I_{PEAK}	170 mVp	160 mVp (32 cant.)	**117.6 mV** (32 cant.)

***Table 4.3:** Evaluation of multiplexing techniques*[3].

[3] Cantilever parameters: s=w=1 μm; l=40 μm; fres=880 kHz; Vdc=21.27 V; Vac=2.364 V. Cload = 30 pF. Hspice simulations from extracted netlist (included layout parasitic capacitances)

According to these results a new chip design has been done to test the feasibility of the management of the array and the circuit improvements for parallel and differential reading. For the control of the multiplexing and in order to minimise the number of external pads, a shift register and a decoder in one of the cases, are used. As an example in figure 4.29 the layout of a 8 cantilevers array with binary ladder multiplexing and with the nanoarea as a whole layer (a) or as 8 individual nanoareas (b) are shown. In figure 4.30 the full layout of this chip is shown. Figure 4.31 shows the optical images of the integrated system for the arrays before the fabrication of the cantilevers.

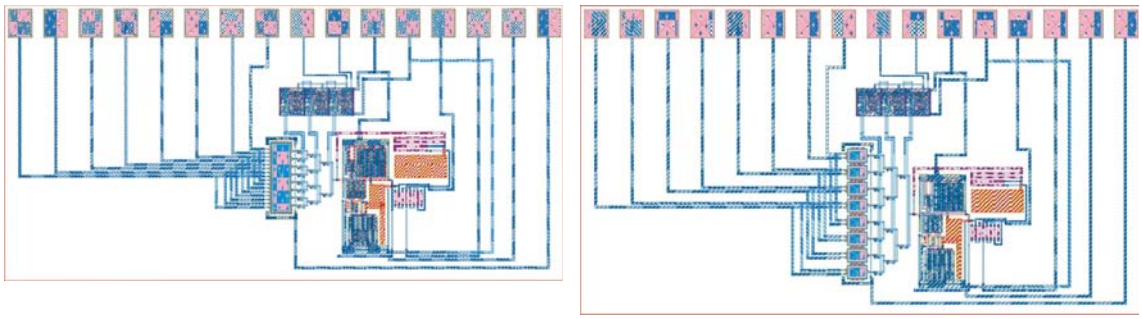


Figure 4.29: *Layout of the 8 cantilevers array with a) same structural layer for the 8 cantilevers and b) 8 individual structural layers.*

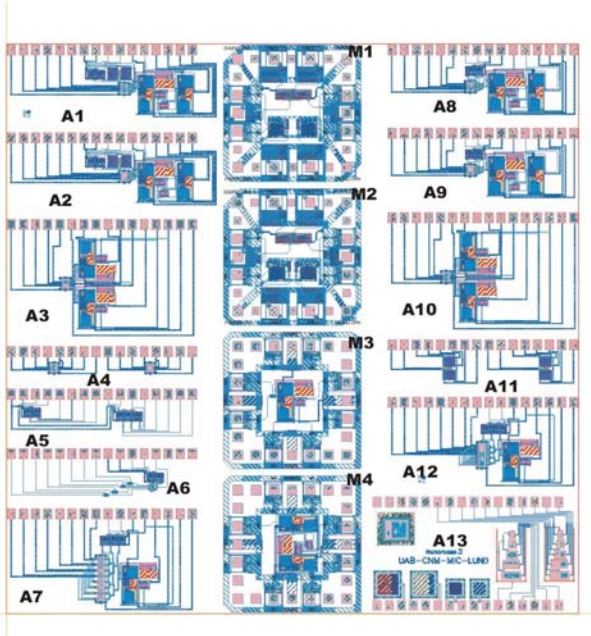


Figure 4.30: *Layout of the complete chip of arrays of cantilevers.*

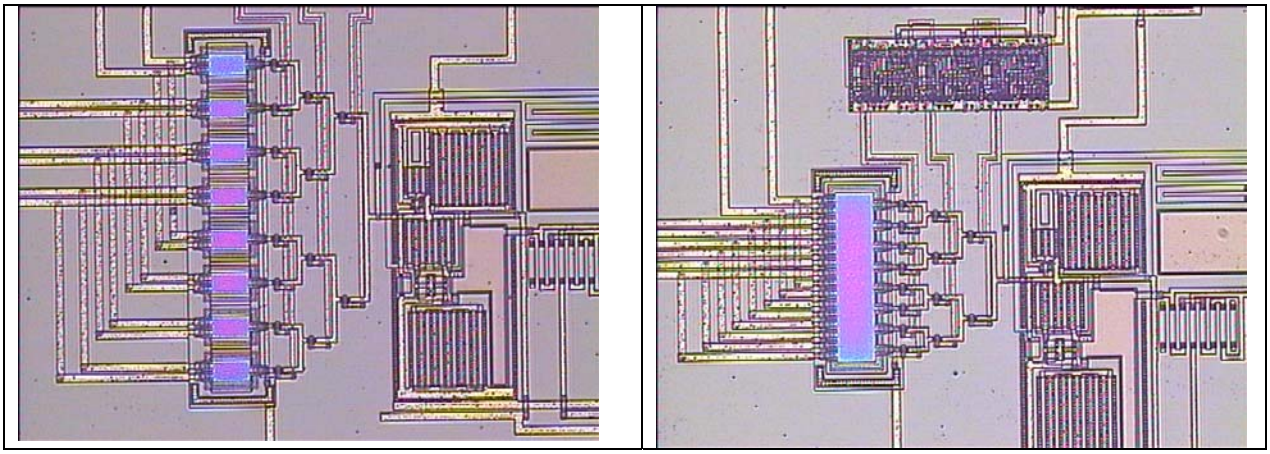


Figure 4.31. *Optical images of the integrated chip for the management of 8 cantilevers (not processed): with individual nanoareas (left) with the same nanoarea (right).*

4.3 Fabrication of sensors with polysilicon nanocantilevers and CMOS circuitry

In this section the full processing for the fabrication of the NEMS system (polysilicon nanocantilevers on the pre-processed CMOS substrates) is explained. The work is divided in the following sections: (a) Technology definition for the compatibilization between CMOS and the nanofabrication processing; (b) CMOS post-processing (preparation of an specific area on the CMOS substrates for the nanoprocessing); (c) Nanofabrication: laser lithography and electron beam lithography for the cantilever definition and needed post-processing steps and (d) compatibility studies after the nanofabrication with the CMOS circuits.

4.3.a) Technology definition for the compatibilization between CMOS and nanofabrication

As we have explained we want to prove the compatibility of standard CMOS processing with the nanofabrication processing. The CMOS technology is the CMOS25 available at CNM. It is a 8 masks CMOS 2,5 μm, 2 poly and 1 or 2 metal levels.

Nanoprocessing consists basically in a surface micromachining technology, where the nanostructure is defined by nanometric capable lithographies (laser, electron beam lithography, NIL or AFM). For the micromachining process, polysilicon is the structural layer and silicon oxide is the sacrificial layer.

The general considerations in order to define the strategy for combining both technologies are summarised below:

- CMOS must not be modified and it must be maintained as a full process
- Nanostructures will be defined as a post-process step

These two general considerations impose the following restrictions in strategy definition:

- Structural and sacrificial layer for nanostructure must be layers already existing in the CMOS process. In consequence there are important limitations in layer characteristics: thickness, doping.
- In the CMOS circuits, a specific "nano-area" must be defined during the CMOS fabrication, with a defined post-process at CNM. The "nano-area" contains the layers used for the nanofabrication process (sacrificial layer-structural layer-thermal isolation oxide layer)
- CMOS circuitry must be protected during nanofabrication
- An alignment methodology must be defined

Election of CMOS layers for nanoprocessing

Structural layer: There are two polysilicon layers that in principle could be used as the structural layer for the nanocantilever fabrication (see figure 4.32).

- Poly0: It is a n^+ polysilicon layer used as the bottom plate of the analog capacitors in the CMOS circuits.
- Poly 1: It is a n^+ polysilicon layer used as a CMOS gate and top plate of the analog capacitors.

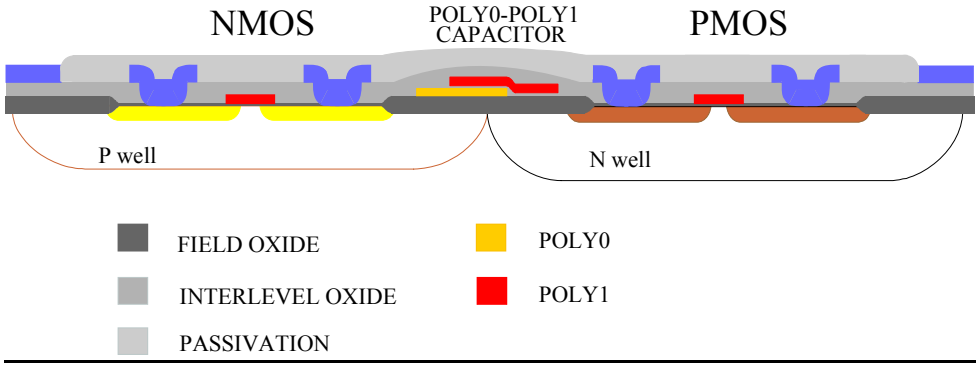


Figure 4.32: *Cross section of the CNM25 CMOS technology. Main layers are depicted.*

Sacrificial layer: The only layer that can be used as sacrificial layer is the 1 μm thick thermally grown field oxide because it is the only thick oxide grown or deposited before the deposition of the polysilicon layer.

Thermal isolation oxide: Different options (Interpoly oxide, Interlevel dielectric, passivation layer, specific thermal isolation oxide) can be considered depending on the polysilicon layer used as structural layer and on process sequence defined for the "nano-area" region.

In standard CMOS process the poly0 layer is 350 nm thick and doped by $POCl_3$. Process conditions for Poly0 can be changed without important effects in the CMOS. Specific changes to adapt poly0 for nanoprocessing can be accepted in the CNM-CMOS25 technology. Furthermore if poly0 is used as structural layer, interpoly oxide can be used as the thermal isolation oxide in the nanoprocessing. The poly1 layer can be used as a protection layer of the structure: field oxide/ poly0/ interpoly oxide, during CMOS processing and can be removed by RIE after CMOS process is completed without any additional mask. As a consequence, this option makes it possible to adapt polysilicon characteristics to nanoprocess requirements. Moreover, the intrinsic oxide for thermal oxidation is protected during the whole CMOS processing by poly1 and CMOS post-process at CNM is greatly simplified. In addition, post-processing is reduced to a polysilicon RIE step without any additional mask.

In order to obtain the conditions for depositing and doping the poly0 layer that structurally matches the needs of the nanoprocess, a polysilicon processing test has been done. The thickness of polysilicon has been established at 600 nm, different conditions for LPCVD deposition and sputtering have been tested, and doping by ion implantation and by $POCl_3$ process have been done. The thermal budget and main parameters of the CMOS process that can affect polysilicon properties have been included in the process in order to have the same conditions than in the final CMOS wafers.

Main results for the different samples are summarised in table 4.4. These samples have been characterized by SEM and AFM for surface roughness characterization. Taking into account

the results of surface roughness, only samples deposited at 580ºC (amorphous as deposited, samples 1610-1 and 1610-2, in table 4.4) are of interest for nanoprocessing.

	Polysilicon				**Interpoly Oxide**
Sample #	Deposition	Doping	Poly0 Thickness (nm)	Sheet Resist. (Ω/sq.)	Tox (nm) (Tencor)
1610-1	LPCVD, 580ºC	Ion Implant.	600	193.3	~ 30
1610-2	LPCVD, 580ºC	$POCl_3$, 950ºC	600	13.8	~ 58
1610-3	LPCVD, 630ºC	$POCl_3$, 950ºC	600	12.7	~ 65
1610-4	LPCVD, 630ºC	$POCl_3$, 950ºC + I.I.	600	12.2	~ 65
1610-5	LPCVD, 630ºC	$POCl_3$, 950ºC	350	27.8	N.A.
1610-6	Sputtering	$POCl_3$, 950ºC	480	136.3	~ 45
1715-1	LPCVD, 580ºC	Ion Implant.	600	162	N.A.

***Table 4.4**. Summary of main results obtained in poly0 process optimisation*

The main structure after the complete CMOS process is summarised in the following table:

Sacrificial layer	Field oxide
Structural layer	Special Poly0 (600 nm thick, LPCVD 580ºC, doped by I.I. or $POCl_3$)
Thermal isolation oxide	Interpoly oxide (thermally grown, ~70 nm)
Protection layer	Poly1

4.3.b) CMOS post-processing (preparation for the nanofabrication)

After the CMOS process is completed post-processing is necessary in order to fabricate the nanocantilevers. The required final structure of this "nano-area" is shown in figure 4.33. Post process can be divided into two differentiated parts:

- CMOS post-process to prepare the nano-area for the nanocantilever fabrication which is done at CNM.
- Nanolithography and post-processing for nanocantilever fabrication which is carried out at MIC and Lund.

The definition of the "nano-area" in the CMOS is schematised in figure 4.34 and summarised in table 4.5. All deposited layers are removed on the nano-area during CMOS process (interlevel oxide, aluminium, passivation) and poly1 acts a protection layer of the nano-area during the etching process. The CMOS post-processing consists of removing the poly1 by RIE. This process will be done without any mask.

Characterisation of CMOS tests structures after poly1 RIE (see figure 4.35) do not show any significant change with respect to the measurements done just after CMOS process.

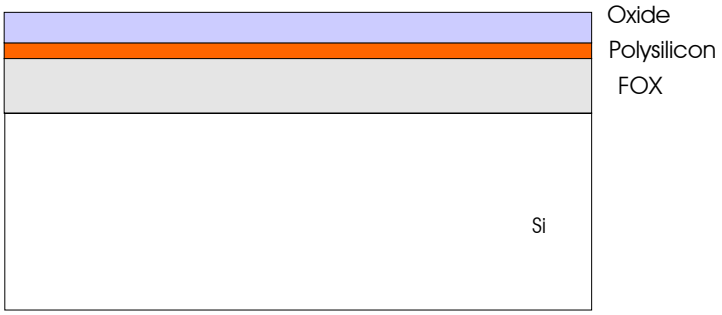


Figure 4.33. *Structure required for the "nano-area" for the fabrication of nanocantilevers*

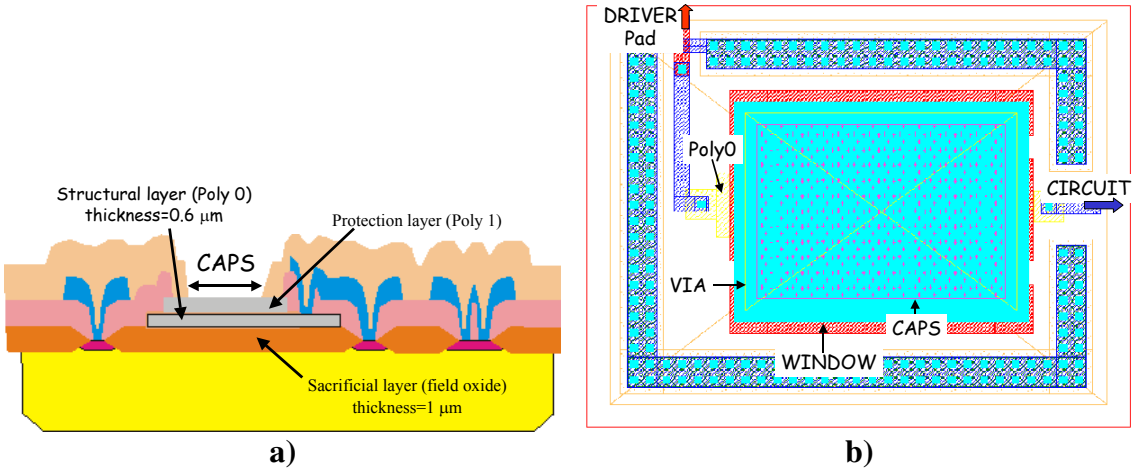


Figure 4.34*. Nano-area structure in the CMOS wafer. (a) cross sectional view, (b) layout*

1. Measurement of electrical CMOS test structures (reported above).
2. Dry etching of Poly1 on top of nanoarea without mask.
3. Measurement of oxide etching during Poly1 removal. (see deliverable#11)
   This is done on a specially designed structure
   Poly1/Gate Oxide/Silicon.
   Results: Initial thickness = 36 nm
   Final thickness = 34 nm
4. Measurement of electrical CMOS test structures.
5. Photolithography. Thick resist, Mask MASS1.
6. Cut the wafer into quarters.
7. One quarter sent to MIC and complete nanoprocessing done.

Table 4.5*: CMOS post-process flow*

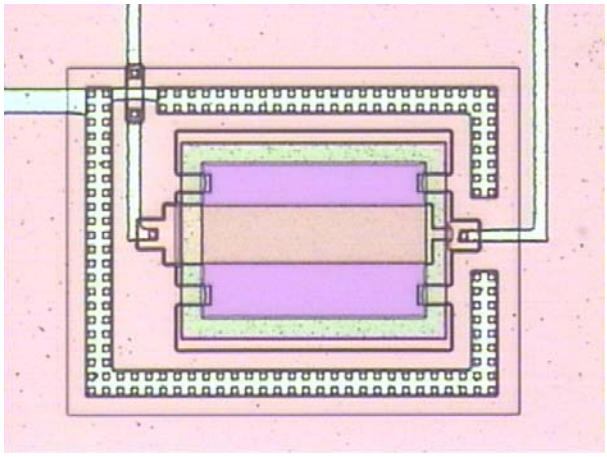


Figure 4.35. *Optical image of a nanoarea after the Poly1 etching. The nanoarea is ready for the nanofabrication. From the image it is clearly seen the Poly0 layer which will be the structural layer fort he cantilever-driver system.*

4.3.c) Nanofabrication: lithography for cantilever definition and post-processing

As we have already explained several nanolithographic techniques have been studied. In this section we explain the two techniques we have used for the fabrication of the polysilicon nanocantilevers on the CMOS substrates: laser lithography and electron beam lithography. Also the needed post-processing to define the cantilever onto the structural layer and to release it from the substrate is presented as the third point of this section.

Laser lithography for cantilever definition

Direct write laser lithography (DWL) has been used for cantilever fabrication at MIC. DWL is a CMOS compatible maskless lithography technique based on localized beam-induced surface modification. The DWL system consists of an argon ion laser, optics that enables the laser beam to be focused to have a spot size of roughly 600 nm and hardware/software controlling the x-y-stage and the A/O modulator, as shown in figure 4.36.

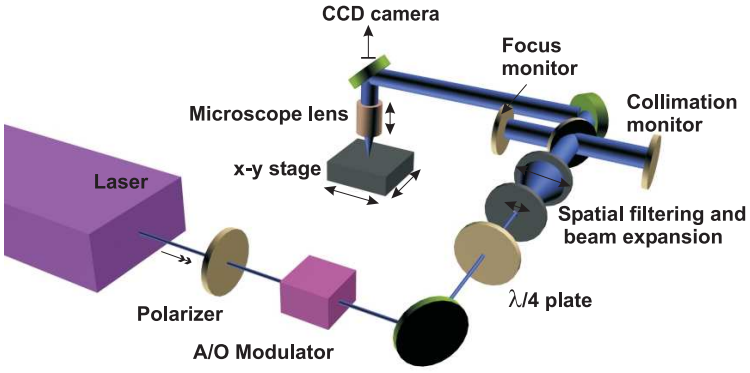


Figure 4.36*: Schematic picture of the laser lithography set-up.*

Two types of DWL have been used: one based on the local annealing of 6-10 nm thin Al films and the other based on local ablation of thin polymer films followed by metal lift-off. Both techniques can be used to define patterns having line widths down to roughly 500 nm over cm^2 areas.

The working principle of DWL based on annealing of Al on CMOS is described in table 4.6 and examples of resulting cantilever structures are shown in figure 4.37.

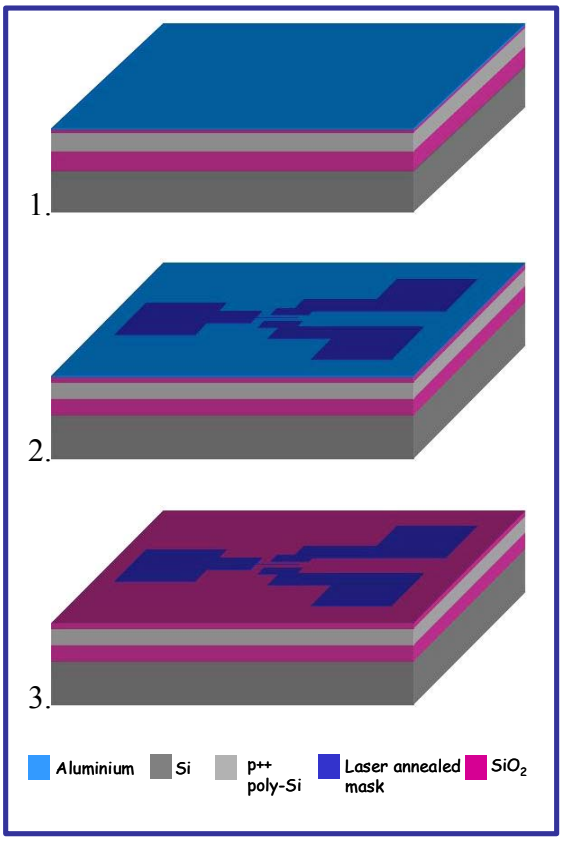
Local Annealing of Al	
1. 6-8 nm of Al is deposited on to the CMOS chip. 2. Local laser annealing is used to define the desired cantilever pattern in the predefined nano-area. The used laser power is roughly 50 mW. 3. The non-annealed Al is removed in a wet etch using H3PO4, for approximately 2 minutes. The resulting Al/Al2O3 pattern is to be used as RIE mask.	

Table 4.6: *DWL annealing of thin Al films.*

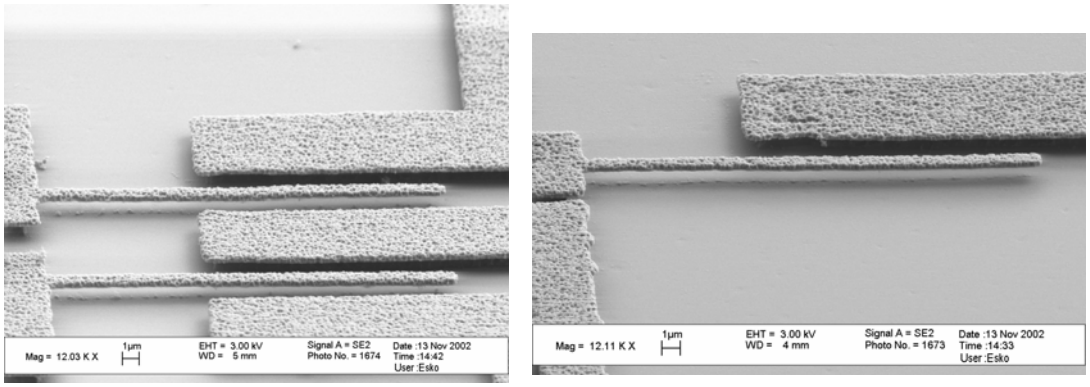


Figure 4.37: *SEM images of poly-Si cantilevers defined by the laser annealing technique on CMOS. The cantilevers are quite porous, this is due to that the Al film used for annealing is only 7 nm thick, which is of the same order of magnitude as the inert poly-Si surface roughness. Hence, this induces small pinholes in the defined Al/Al2O3 pattern reducing its quality as RIE mask.*

However, since the Al thickness is ultra thin (6-10 nm) a high quality RIE mask is extremely difficult to achieve on rough surfaces, which is the case for the poly-Si surface in the nano-area of the CMOS. The optimal Al thickness is typically 6-10 nm, the poly-Si surface roughness is approximately 3-6 nm. It is not possible to increase the thickness of the Al over 10 nm without affecting the line width resolution and the uniformity of the oxidation through the Al film.

Due to the pinholes it is desirable to pattern the CMOS nano-area with thick metal in order to have a RIE mask of higher quality. Therefore, a new DWL technique based on local ablation of a polymer film followed by metal deposition and lift-off has been developed at MIC. The working principle of DWL based on lift-off on CMOS is described in table 4.7.

Laser ablation of thin polymer films

1. The CMOS chip is spin coated with a resist bi-layer consisting of PMMA on top of ZEP (or LOR). The ZEP thickness is approximately 80 nm and it is baked at 160 degrees for 15 min. The thickness of the PMMA is approximately 120 nm ans is baked at 160 degrees for 10 minutes.

2. Laser ablation of the resist bi-layer followed by a short oxygen plasma etch removing any PMMA residues that might be in the trenches. The used laser power is typically 50-200 mW.

3. Development of the bottom ZEP resist using o-xylene, creating a desired lift-off profile.

4. Evaporation of 30 nm of Al.

5. Lift-off.

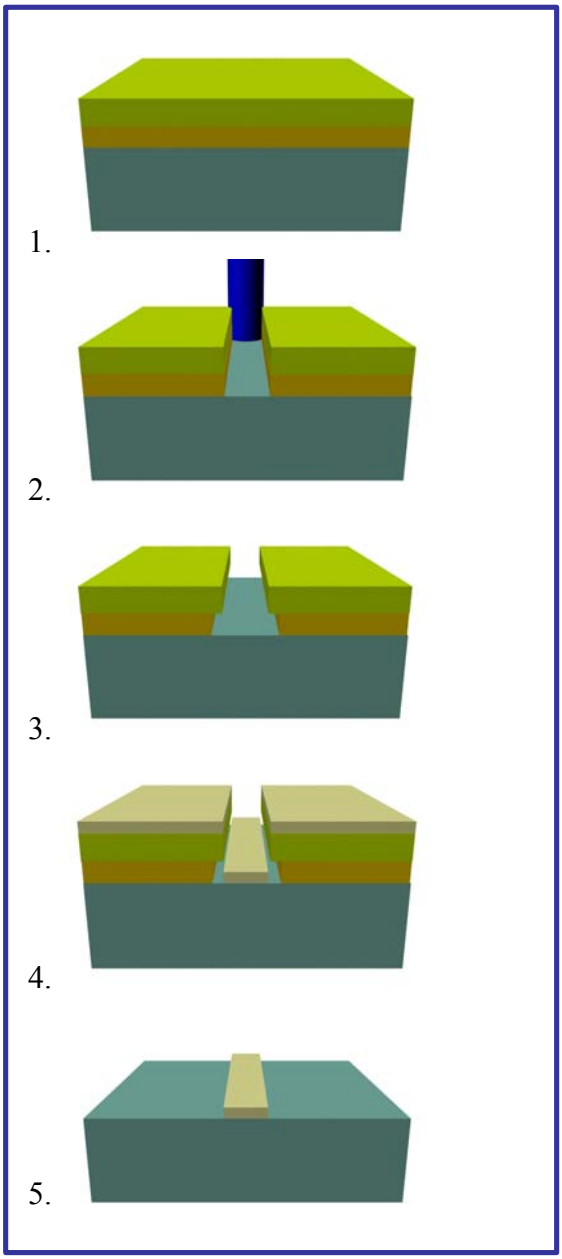


Table 4.7: *Lift-off based DWL.*

We use a bi-layer resist method where differences in dissolution rates makes it possible to create an evaporation-mask in the upper resist layer. The bi-layer consists of a top layer of PMMA and

a bottom layer of ZEP (or LOR). The laser patterning is due to thermal melting and evaporation of the bi-layer, which results in a trench with a gaussian profile, as displayed in the scanning electron microscope (SEM) image in figure 4.38.

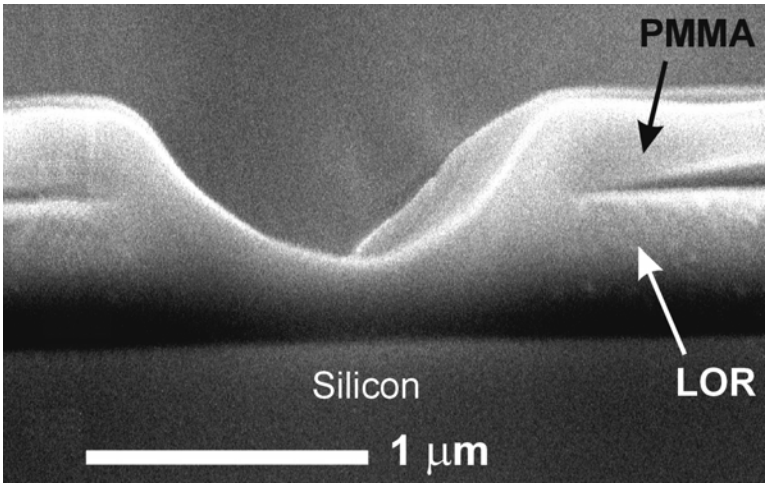


Figure 4.38: *SEM cross-section of a laser lithography written trench in resist bi-layer, consisting of PMMA on LOR, before development of the LOR.*

Hence, the bi-layer is necessary in order to have an undercut of the top resist layer, which is desirable for lift-off processes. The pattern line width can be controlled by varying the laser power, dwell time as well as the thickness composition of the bi-layer. Furthermore, a two-step lift-off process makes the use of ultra sonic agitation unnecessary. Examples of resulting cantilever structures are shown in figure 4.39.

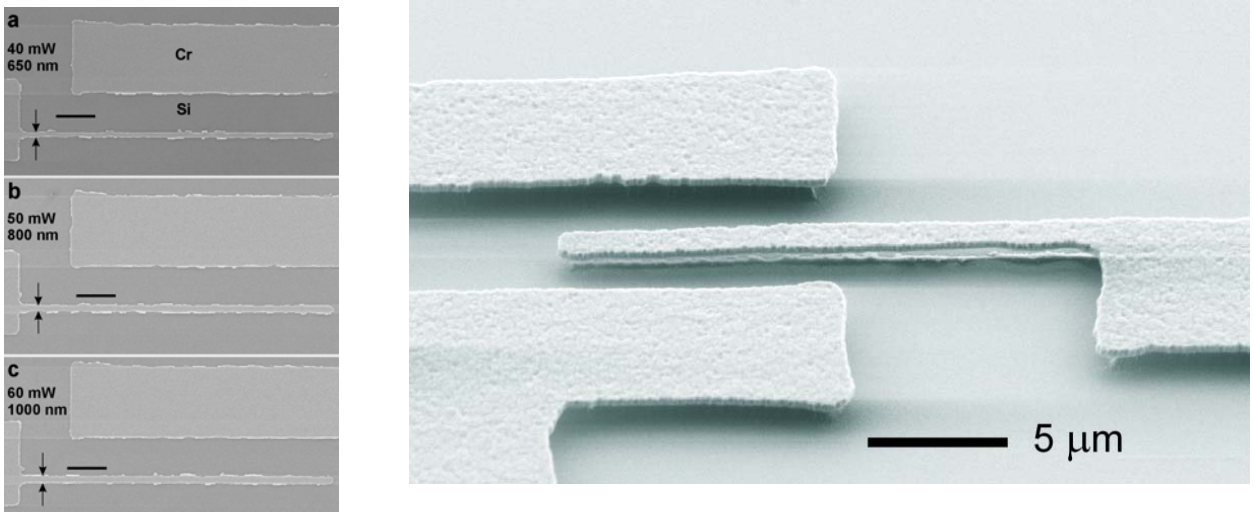


Figure 4.39: *SEM images of defined cantilever structures. (a-c) Cr metal mask after lift-off on poly-Si CMOS, the line width is changed as function of applied laser power and constant dwell time. (d) A fully released poly-Si cantilever on CMOS. The length is 20 μm, the thickness is approximately 400 nm and the width is 900 nm.*

Electron Beam Lithography

Silicon nanocantilevers have been fabricated by using electron beam lithography, (EBL) at Lund, directly on the Polysilicon structural layer and also on the SOI-silicon structural layer with integrated CMOS circuitry.

The chips were washed in acetone and isopropanol (IPA). Two layers of resist were then deposited on to the samples. First, ZEP 520 A7 was spin deposited on the surface using 6000 rpm for 60 s. This gives a layer thickness of approximately 170 nm. The sample was then baked on a hot plate in 160°C for 10 min. After that, PMMA 950 A4 1:1 was spin coated on top at 6000 rpm for 30 s, which gives a layer thickness of 70-80 nm. This was followed by another baking on a hot plate in 160°C for 15 min.

Different cantilever structures have been defined by EBL on the CMOS chips. The structures consist of a cantilever with one or two drivers, and another structure is a cantilever with a corresponding comb-like capacitor required for the biasing of the CMOS circuit. The structures were patterned by EBL using an acceleration voltage of 3kV (see compatibility studies between CMOS and EBL writing below), and a probe current of 20 pA. The exposure dwell time was 4.3 μs. After exposure the samples were developed. The PMMA layer was developed in a MIBK:IPA (1:3) solution for 60 s followed by a rinsing in IPA for 30 s. The ZEP layer was developed using o-xylene for 5min and then IPA for 30 s.

As metal mask for the etching process, aluminum was chosen. A 30 nm thick aluminum layer was thermally evaporated on to the surface. The lift-off process was done by immersing the sample in hot remover S1165 for 5-10 minutes followed by ultra sound for a few seconds. Finally, the samples were rinsed in de-ionized water.

After the lift-off process, an anisotropic reactive ion etching (RIE) was performed to transfer the EBL made pattern to the silicon layer, followed by an etching to fully release the cantilevers. The etching process was performed by MIC in Denmark following the procedure explained in next section.

A major advantage of exposing with low energy electrons is that the electrons will loose most of their energy in the resist layer and thus not reach the underlying substrate and degrade the circuits. A consequence of using low energy electrons, however, is that the sensitivity of the resist will increase and the time for manual alignment of the nanoarea before exposure has to be short. Using low energy EBL a lower resolution is obtained compared to using high-energy electrons (see figure 4.40, where the exposition energy was 35 kV), but the proximity effect, i.e. secondary and backscattered electrons that contribute to the exposure of the resist layer from underneath, is severely suppressed in the low energy case. A consequence of this is that it is possible to have a wider range of exposure doses without loosing much resolution.

In the nanoareas there is an approximately 1.9 μm high step between the poly-Si layer and the protection layer for the circuitry (see figure 4.41). Spin coating with thin resist inevitably produces a thicker bi-layer at the edges of the area for nanofabrication. Using low energy EBL has, in some cases, resulted in poor pattern definition at the edges of the nanoarea since the resist thickness is higher there. In addition, the different nanoareas on the CMOS chips have not exactly the same step height, and therefore the resist thickness at the edges will vary over the chip. Attempts have been made to locally increase the EBL exposure dose at the edges but the results have been inconclusive due to the variation in resist thickness at the edges. Further, since

the circuits are sensitive to the electron beams, an increase in exposure dose might also have an effect on the circuit performance. Therefore, investigations in finding a sufficient dose high enough to pattern the edges were not pursued.

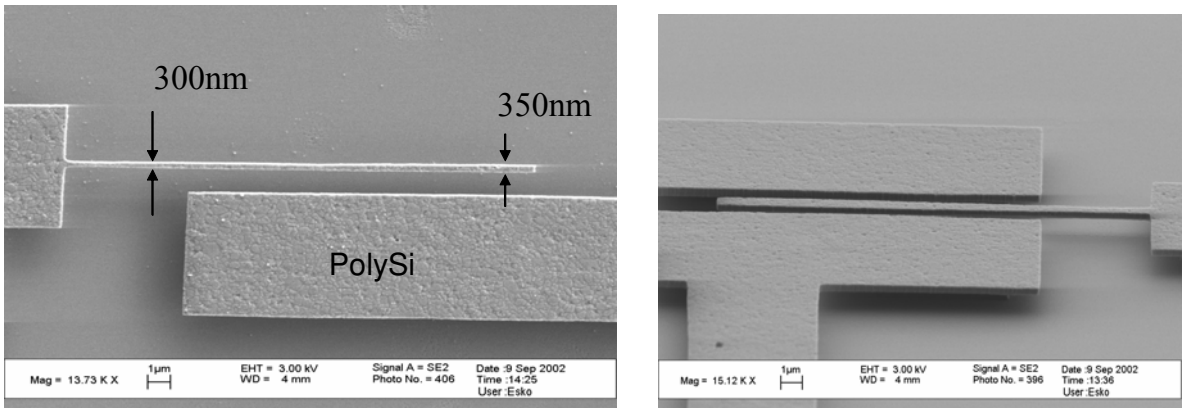


Figure 4.40. *Cantilevers defined by EBL on a nanoarea using a high energy dose of 35 kV.*

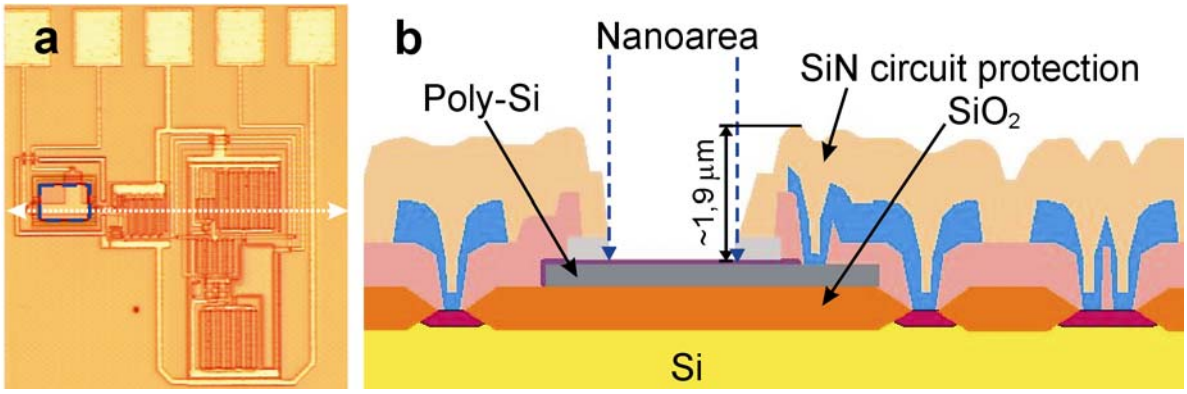


Figure 4.41 *(a) An optical microscope image of a section of a CMOS chip. The white dotted line represents the cross section area. The blue dotted square represents the nanolithography area on a CMOS chip (called the nanoarea in the text). A schematic cross section of the CMOS chip, as shown in (a), is viewed in (b). (b) Cantilevers are defined out of the 600 nm thick poly-Si layer over a 1 µm thick sacrificial SiO_2 layer. The fabrication area lies in a 1.9 µm deep trench and hence spin coating of resist leads to thickness variations in the nanoarea. As a consequence there will be inadequate masking definition at the edges when the exposure dose has not been enough to expose through the thicker resist layer.*

Hence, when using 3 kV electron beam exposure some nanoareas have an insufficient pattern definition at the edges. Unfortunately, it is not possible to detect the poor pattern definition at the edges until after the lift-off process is finished. However, this has been solved by a direct write laser lithography (DWL) technique applied where the masking has been unsatisfactorily, see figure 4.42. The technique, explained in last section, is based on thermally assisted direct laser writing on the resist bi-layer coated chips directly after the EBL exposure. The DWL was used to pattern the structures at the edges without affecting the delicate EBL defined pattern located at the center of the nanoarea. Figures 4.43 and 4.44 show scanning electron microscope images of released cantilevers defined by 3 kV EBL.

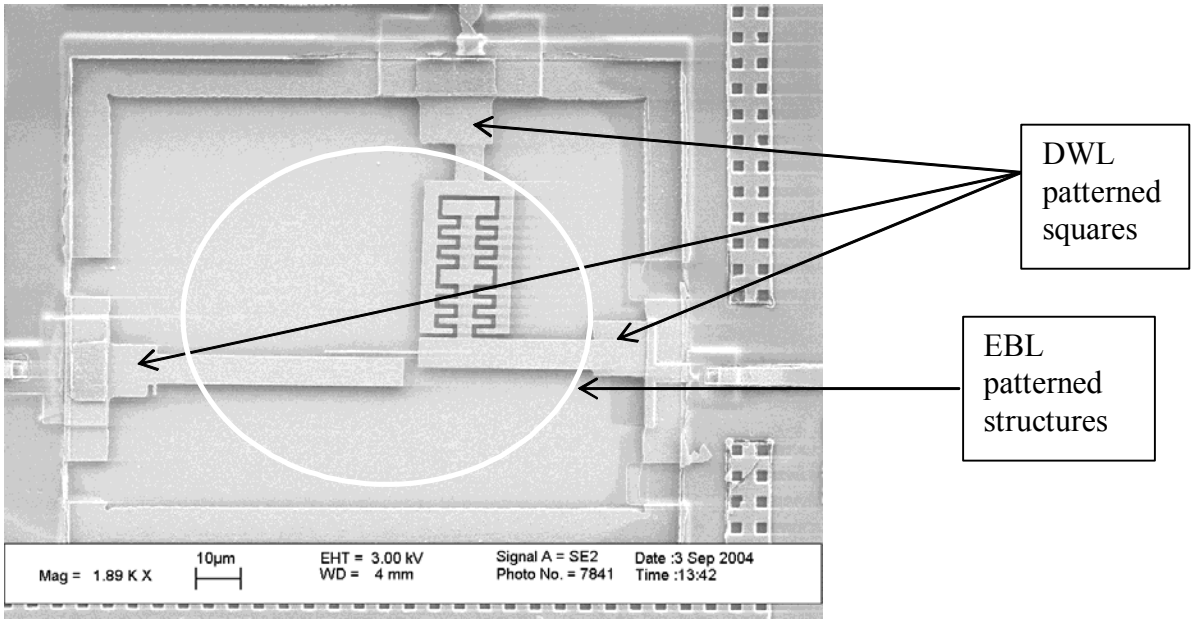


Figure 4.42 *A top view scanning electron microscope picture showing the nanoarea with a released cantilever, the driver and the corresponding comb-like structure. The structures have been patterned by EBL at 3 kV. In order to pattern the structures at the edges, DWL has been applied to insure good connections.*

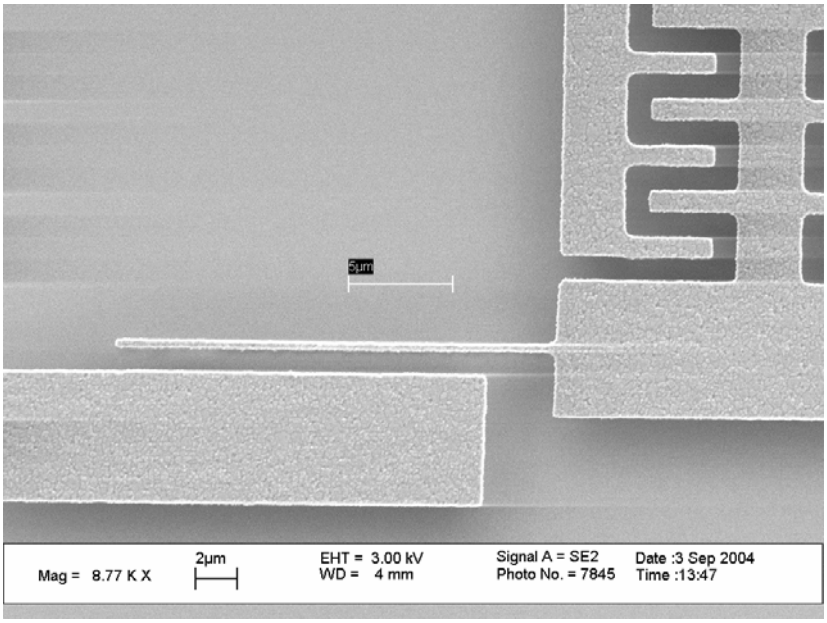


Figure 4.43 *A top view scanning electron microscope image showing a released cantilever. Approximate dimensions of the cantilever are: 420 nm wide, 600 nm thick and 20 µm long. It is clearly seen that patterning with 3 kV EBL generates well-defined structures.*

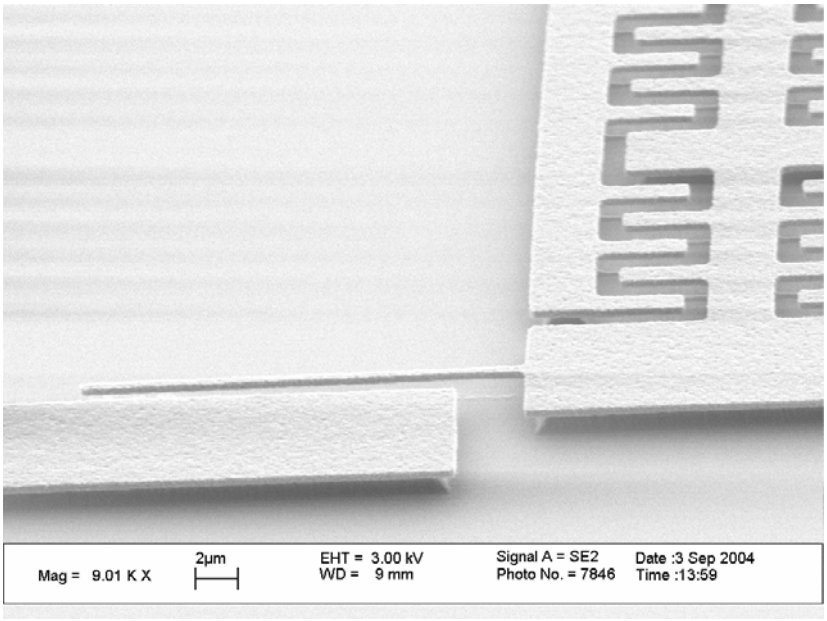


Figure 4.44. *A scanning electron microscope picture, taken at an angle, of a released cantilever suspended 1 µm above the bottom substrate, and the corresponding driver and comb like structure.*

Post-processing after nanolithography definition

Nanofabrication process is summarised in table 4.7. After the nanopatterning in the nano-area using EBL or Laser it is necessary to deposit a protection photoresist layer after the RIE for protecting the CMOS circuitry during sacrificial oxide etching using BHF. A protection mask must be used at MIC and will be a contact mask that must match with the CMOS (using stepper).

Nanofabrication process

1. The CMOS chip is ready for nanoprocessing when the poly1 layer has been removed.
2. Patterning of the nano-area using EBL or DWL.
3. Anisotropic RIE of the poly0 structural layer using SF6:O2 plasma for 8 min.
4. Post processing UVL protection mask for the CMOS circuitry protection. The photoresist is spin-coated to a thickness of 2.5 µm and baked at 120 degrees for 1 min.
5. BHF sacrificial oxide wet etch for 13 min releasing the cantilever structure. This is followed by thorough rinsing in DI-H2O. The water is replaced by acetone and finally photoresist is applied in large amounts until the liquid covering the cantilever is consentrated resist. The CMOS chip is spun at 3000 rpm for 30s and soft baked at 90 degrees for 1 min.
6. The cantilever structures are dry released by oxygen plasma etching of the supportive resist layer for 15 min.

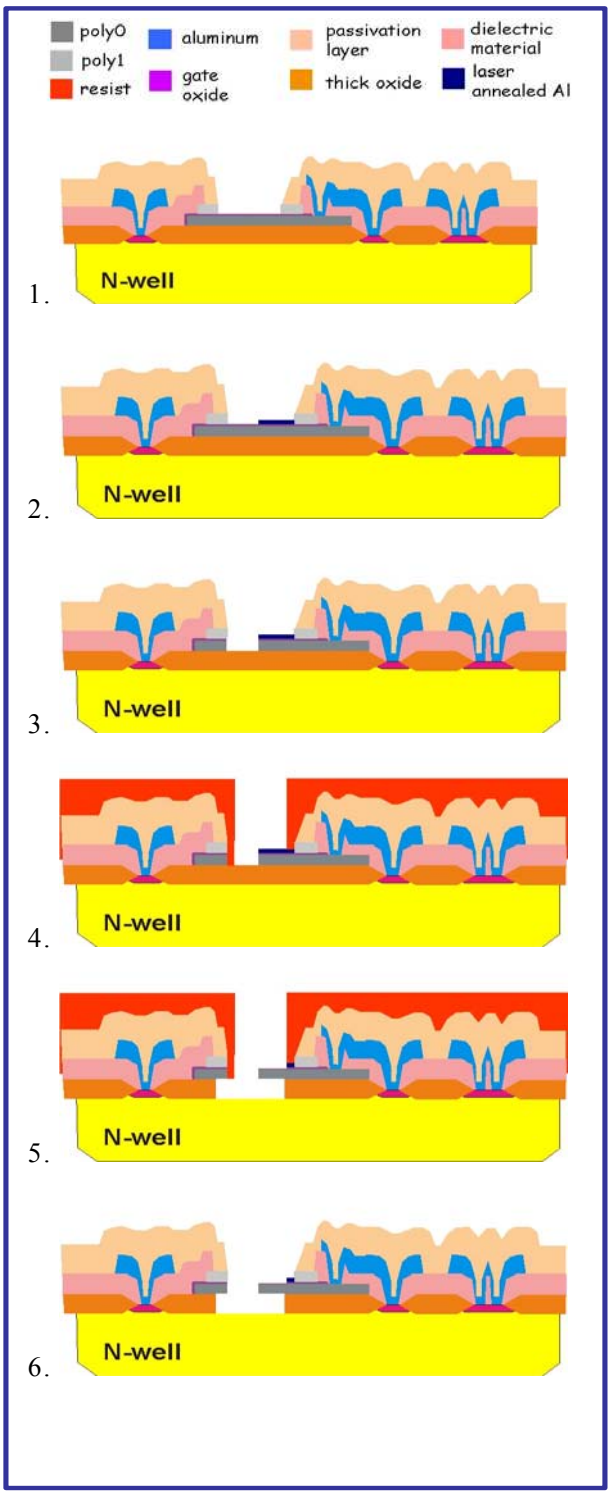


Table 4.7. *Defined post-processing for nanocantilever fabrication.*

4.3.d) Compatibility studies after the nanofabrication with the CMOS circuits

The compatibility study has been made for both kinds of lithography: laser lithography and electron beam lithography.

Compatibility between laser lithography and post-processing with CMOS technology

After nanoprocessing at MIC, CMOS test structures have been measured at CNM, and no significant difference is observed compared with results obtained just after CMOS processing when using laser lithography. In particular, in figure 4.45 threshold voltages for PMOS and NMOS transistors are represented for the measured chips, and no significant difference is observed for these values that were proved to be the most sensitive.

As a conclusion and taking into account the previous results we can conclude that monolithic integration of CMOS circuitry and Nanocantilevers have been successfully achieved with this approach and processing steps.

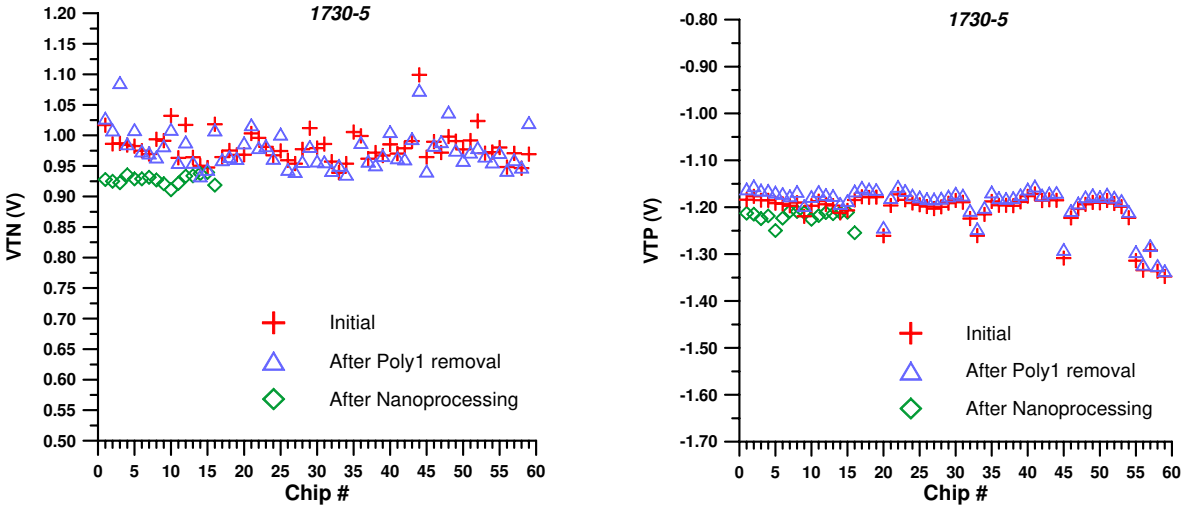


Figure 4.45. *Effect of post-processing on Vth of PMOS and NMOS transistors*

Compatibility between electron beam lithography and post-processing with CMOS technology

In the framework of the Nanomass project, it has been observed that the CMOS circuitry degrades after processing with e-beam lithography, which is used to fabricate the nanocantilever in a polysilicon layer. This layer is electrically connected to the gate of a MOS transistor. The degradation of the CMOS circuitry is such that, in some cases, its performance is not adequate to the specifications of the complete device. In view of these problems, a compatibility study has been carried out at IMB-CNM. In this study the polysilicon layer of the nanoarea has been exposed to the e-beam similarly as in the case of the complete process.

To analyse the effect of the e-beam irradiation on the polysilicon layer which is connected to the gate of a MOS transistor, we use a test structure included in some mask sets specially designed for the Nanomass project. This structure comprises a rectangular polysilicon plate and an NMOS transistor with dimensions: L=4 µm, W=10 µm. In figure 4.46 a photograph of the structure is shown, where the polysilicon plate in the nanoarea is electrically connected by a metal line to the

gate of the transistor, which in turn is electrically accessible through pad number 16. Since the NMOS transistor has the four terminals available, it is possible to measure the complete electrical characteristics.

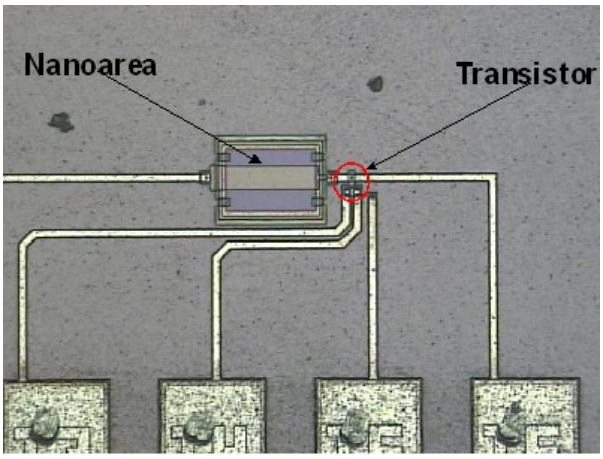


Figure 4.46*. Optical image of the test structure used to study the effect on the MOS transistor.*

The experimental procedure consists of:

- Measurement of the complete electrical characteristics of the NMOS transistors.
- EBL processing of the polysilicon plate in the nanoarea. This process comprises the resist deposition, the e-beam exposure at the selected energy and dose, the deposition of very thin layer of Al (30-40 nm) and finally the lift-off process of the metal layer.
- Measurement of the complete electrical characteristics of the transistors after EBL.
- Comparison of characteristics before and after EBL processing.

The acceleration voltages of the e-beam that have been analysed are:

- 4 kV, 15 kV and 35 kV, for the samples processed at Lund University, where a converted JSM 6400 SEM with LaB6 cathode has been used.
- 10 kV for the samples processed at IMB-CNM, using a Leo 1530 of Gemini with an Elphy Plus of Raith.

It should be noted that the EBL processes at Lund University and at IMB-CNM are rather different since different equipments are used. This has led to the use of a higher dose in the 10kV exposures carried out at IMB-CNM, as compared to the doses used at Lund University. In addition, the e-beam exposure procedure is rather different in each case particularly the elapsed times involved. Further to that, the EBL process not being optimized at IMB-CNM, has resulted in patterns that would be useless for further processing. Despite all these differences and for the purpose of this investigation, we will consider the results corresponding to the samples processed at IMB-CNM as indicative of the damage caused by e-beam processing at 10 kV.

The electrical characterisation of the NMOS transistor has been carried out by measuring the complete set of curves corresponding to:

- Drain-source current v. Drain-source voltage (I_{ds}-V_{ds}) at different Gate-source voltages (V_{gs}) and at a bulk-source voltage (V_{bs}) of 0 V.
- Drain-source current v. Gate-source voltage (I_{ds}-V_{gs}) at different Bulk-source voltages (V_{bs}) and at a fixed Drain-source voltage (V_{ds}) of 100 mV.

One example of NMOS transistor characteristics for two of the EBL processing conditions (4kV and 35kV) is shown in the following figures, together with a photograph of the processed nanoarea.

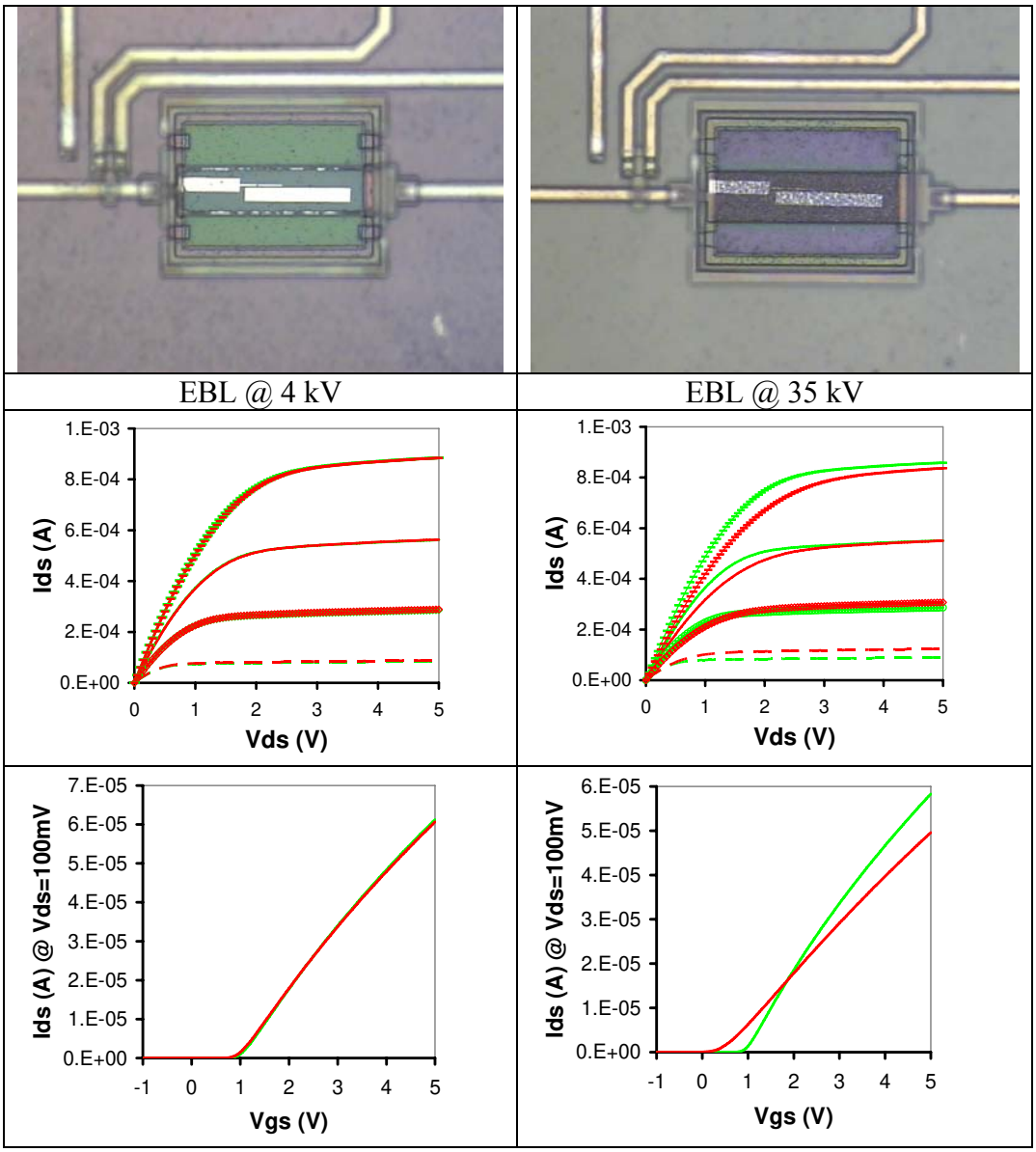


Figure 4.47. *Optical image and electrical curves for the NMOS transistor when different exposition energies for the EBL process have been used (Green before EBL, Red after EBL exposition).*

In order to quantify the information that these curves are giving, four parameters have been considered:

- Threshold Voltage, V_{th}
- Drain current at the linear regime, I_{dlin}
- Drain current at the saturation regime, I_{dsat}
- Maximum of the transconductance, G_{mmax}

These parameters have been obtained as follows:

V_{th}: V_{gs} @ $I_{ds}=10^{-7}$ A, $V_{ds}=0.1V$, $V_{bs}=0V$
I_{dlin}: I_{ds} @ $V_{gs}=5V$, $V_{ds}=0.1V$, $V_{bs}=0V$
I_{dsat}: I_{ds} @ $V_{gs}=V_{ds}=5V$, $V_{bs}=0V$

G_{mmax}: Maximum of G_m, where $G_m=dI_{ds}/dV_{gs}$ @ $V_{ds}=0.1V$, $V_{bs}=0V$

The results obtained for the 5 processed samples at the same conditions are summarized in the figure 4.48.

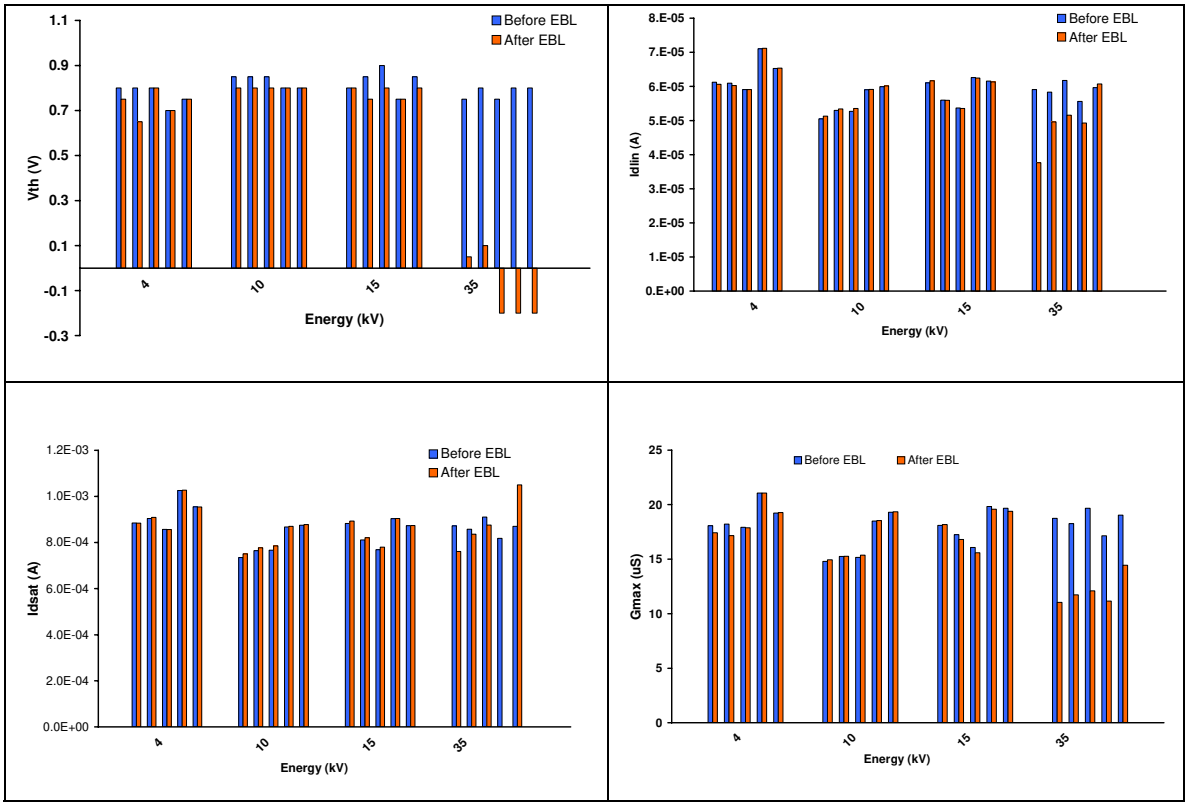


Figure 4.48. *Main electrical parameters for the five EBL processed samples*

In view of these results we can conclude that:

- EBL processing for the nanocantilever of the devices of the Nanomass project, leads to a degradation of the NMOS transistor characteristics when the EBL is carried out at an e-beam acceleration voltage of 35 kV. The most severe degradation corresponds to **a shift of the threshold voltage to negative values of the order of 0.9 V and a reduction of the maximum of the transconductance of the order of 40%**. A reduction of I_{dlin} of a 15% is also observed whereas there is a lower effect in I_{dsat}.

- When EBL is carried out at acceleration voltages lower than 15 kV, most of the differences are within the tolerances for the CMOS technology used and, as a consequence, the EBL processing would not lead to a degradation of the circuit performance.

From these results it is clear that, as far as the Nanomass devices are concerned, EBL processing for the fabrication of the nanocantilever in the polysilicon layer electrically connected to the first transistor of the circuitry should be carried out at acceleration voltages of 15 kV or lower.

4.4 Fabrication of sensors with crystalline silicon nanocantilevers and CMOS on SOI substrates

In order to fabricate nanocantilevers with monocrystalline silicon as structural material, it has been proposed to use SOI wafers as a substrate where nanoareas have been defined. The nanocantilever will be fabricated in the nanoareas, which basically are formed by the top silicon layer of the SOI layer (the structural layer) on the buried oxide layer (the sacrificial layer). The CMOS is fabricated in the bulk silicon wafer. In this way we can adjust the thickness of the silicon structural layer and the sacrificial layer independently of the CMOS technology, and the CMOS technology is also independent of the SOI substrate. In figure 4.49 a scheme of the proposed structure is shown.

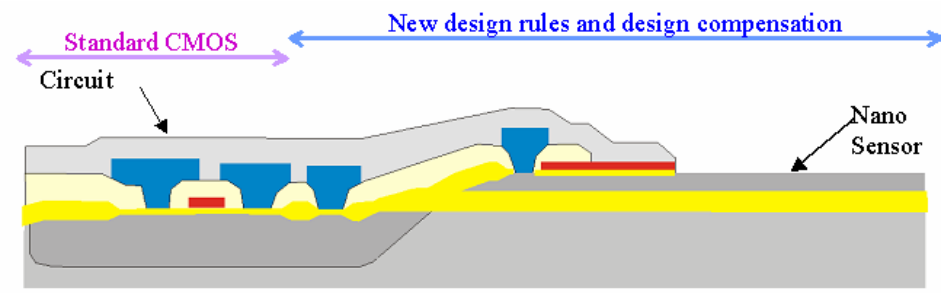


Figure 4.49. *SOI-CMOS nanoarea description*

The objective of this approach is to improve the lateral resolution achieved with the polysilicon cantilevers. As it has been shown in last section, the granular structure of the polysilicon layer makes difficult to obtain cantilevers with widths smaller than 300 nm. Also the established mechanical properties of the crystalline Silicon (Young Module, Hardness…) make it an ideal material for structural layer. To achieve these aims, bulk CMOS technology is combined with nanofabrication on Silicon using SOI wafers.

In this section we will explain the following items: a) Technology definition for defining nanoareas in the SOI-silicon layer electrically connected to standard CMOS fabricated on the silicon substrate of a SOI wafer; b) CMOS test results of the processed SOI wafers; c) nanofabrication results.

4.4.a) Technology process for defining nanoareas in the SOI-silicon layer electrically connected to standard CMOS fabricated on the silicon substrate of a SOI wafer

In order to obtain the nanoareas the initial substrates are SOI wafers with pre-defined Si and SiO_2 thicknesses. A pre-process is necessary for the definition of the nanoareas and the preparation of the substrate where standard CMOS will be fabricated.

The SOI substrates that have been used are BESOI wafers provided by Shin-Etsu, with 1,3µm thick SOI-silicon layer and with 1µm thick buried oxide. The CMOS standard technology is the CMOS CNM25 2P, 2M, from IMB-CNM (the same we have used for the polysilicon cantilevers approach). The study of the compatibilization of this CMOS technology with SOI substrate, using SOI-silicon as structural layers for NEMS fabrication, is done taken into account that for

the transducer fabrication electron-beam, laser and AFM (atomic force microscope) lithography will be used.

On the SOI wafer will be defined two kind of regions: (i) SOI islands, where the nanodevice will be fabricated (regions called nanoareas); and (ii) regions where the SOI silicon layer and the buried oxide one are removed. On these regions the CMOS process will take place. A remarkable issue to take into account in this process is that the CMOS characteristics have to be kept unaltered.

Figure 4.49 shows a schematic cross section of the desired structure: CMOS region on bulk silicon, the SOI structured region for the fabrication of the nanoresonator-driver systems and a smooth transition region between both regions to allow a good electrical connection.

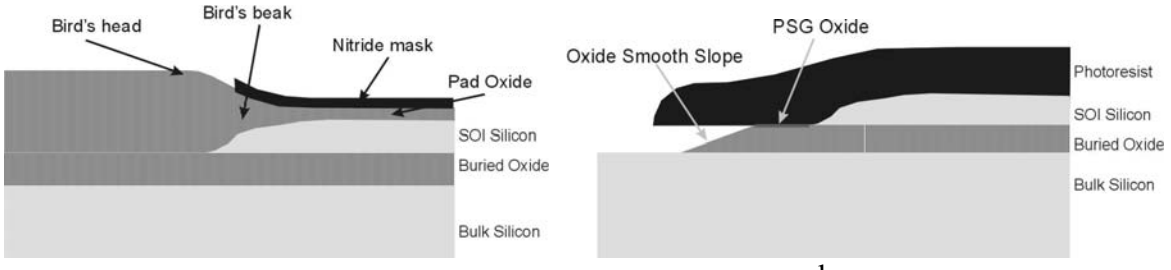
We decide to use a process based on a LOCal Oxidation of Silicon (LOCOS) to obtain the required slope for the smooth silicon transition. With this oxidation process the obtained slope on silicon is very similar to a hyperbolic tangent slope. To make this local oxidation first a pad oxide is grown on all the surface, afterwards a nitride mask is used to define the transition limit and then the oxidation takes place. Due to the thick silicon layer to be oxidized, the process is done in two steps: oxidizing the silicon, and etching the silicon oxide, two times.

As the silicon layer thickness is nominally 1,3 μm and for each 1 μm oxidation it is consumed 0.44 μm of silicon, it is compulsory to grow 2.95μm oxide to consume all the silicon layer. The used wafers have a wide silicon thickness dispersion (variations around 0.5μm on the same wafer and 0.8μm in the batch were the specifications provided by the foundry). The maximum thickness of the used wafer has to be used to calculate the required oxide growing.

The length of the bird's beak becomes bigger with the thickness of the pad oxide, but this dependence is only significant for thickness lower than 400Å. A 500Å thick pad oxide is used as a compromise between a thick oxide to allow the bird's beak formation and a thin oxide to not consume the SOI silicon from the nanoarea. The process is done at 1100ºC, thus a bird's beak length of 0,75μm is expected.

The nitride layer thickness used is the thinner that can last during all the oxidation process. Thicker layer will produce higher surface stresses due to the volume expansion during oxidation and it is never recommended. The used nitride thickness is 1800Å.

Figure 4.50 shows the schematic final stage of this process, before the oxide etching.



a b

Figure 4.50. *Schematic for the definition of the silicon slope (a) and the oxide slope (b)*

The oxide smooth transition is obtained using the different etch rates between PSG and thermal oxide. A thin layer (1000Å) of PSG (Phosphorus Silicon Glass) is deposit on top of the buried

oxide. As the etch rate of PSG oxide is seven times higher than the thermal buried oxide, the etch on the surface parallel direction is seven times faster than in the normal direction. Using a resist mask, a smooth oxide slope is achieved. In figure 4.51 the profiles obtained for both slopes are shown.

After establishing the process to define the two regions (nanoarea and standard CMOS area) the minima distances defining the areas and the transitions has to be determined. The process to test the design rules for defining the nanoareas is done using the same lithography system used for the standard CMOS CNM25 process consisting of a stepper; specifically model Nikon NRS-150.SG7E. It is known that this stepper focuses just on a focal plane and uses as reference the center of the chip, so the chip is design maintaining its center free of islands. This assures that the CMOS CNM25 is kept unaltered as standard process.

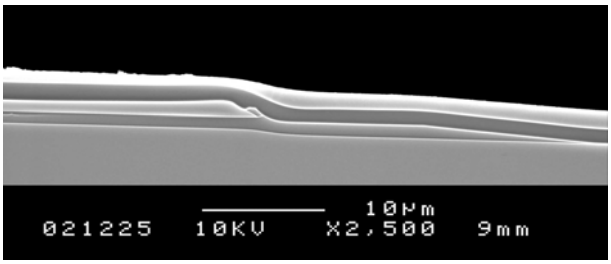


Figure 4.51. *SEM image of the SOI wafer cross section showing the obtained steps for the silicon and the silicon oxide*

As result of the performed tests the new design rules summarized are:

- The center of the chip has to be free of nanofabrication areas with SOI structure.
- The minimum distance between mask defining the smooth slope is 30 µm
- Around the transition 6µm separation have to be considered in the new design rules
- Minimum width for metal lines in the transition and on top of the SOI region is 5 µm.
- Minimum separation distance between metal lines is 5 µm.

Following the above design rules for the transition regions, the CMOS circuitry is designed. The same circuits described in section 4.2.b have been used. Figure 4.52 shows a layout of the designed chip. The central region is free of nanofabrication areas with SOI structure. In figure 4.53 an optical image of the integrated chip with the defined SOI nanoarea and read-out circuit is shown.

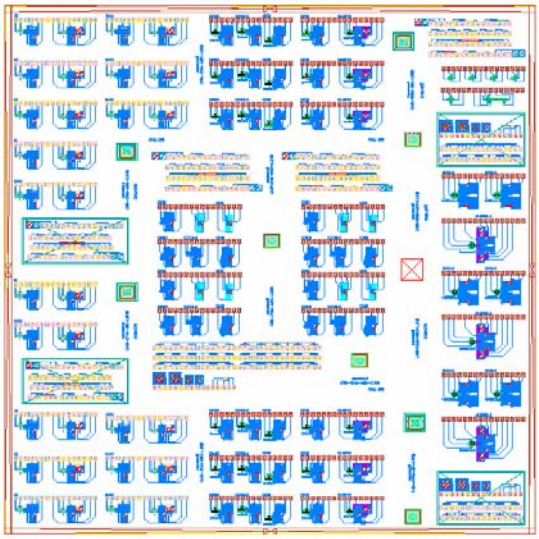
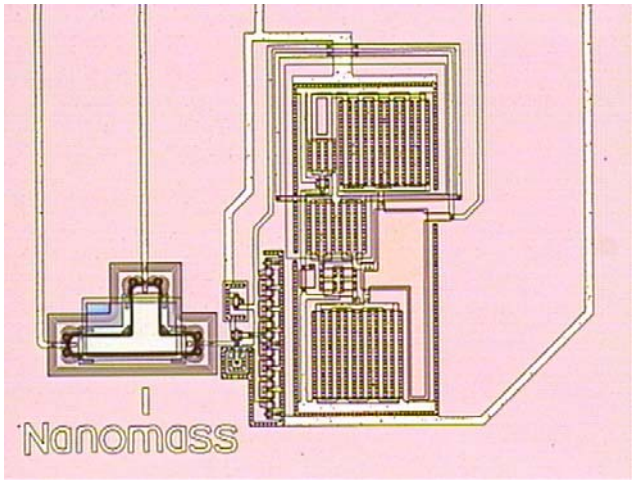


Figure 4.52*. Chip layout of CMOS with nanofabrication defined regions on SOI wafers*



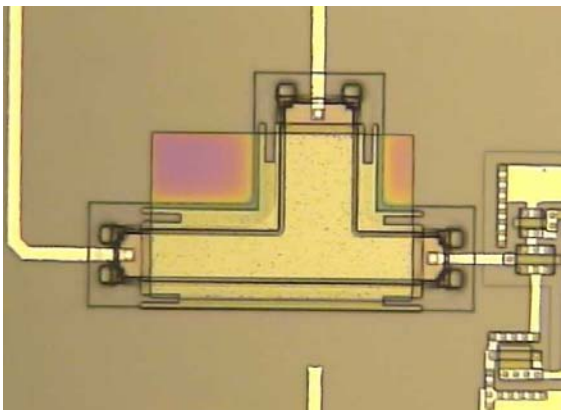


Figure 4.53. *Optical images of the nanoarea and the CMOS read-out circuit integrated on a SOI wafer. The nanoarea (closer view on the right) is formed by the top silicon layer of the SOI layer (the structural layer for the cantilever) on the buried oxide layer (the sacrificial layer for releasing the cantilever from the substrates)*

4.4.b) CMOS test results of the processed SOI wafers

After completing the full process, the CMOS test structures have been fully measured with the standard procedure established at IMB-CNM. All the parameters are under specifications and a high yield has been obtained. Any significant difference is appreciated between SOI substrates and standard test wafers. As an example, and due to the threshold voltages for P and N transistor are the most relevant parameters of a technology for the circuit design we shown the obtained measurements for these parameters in figure 4.54. Further the electrical specifications of the CMOS VLSI circuitry have been also measured. Figure 4.55 shows an example of the obtained results, which corresponds with the expected ones. The conclusion of this electrical test is that CMOS CNM25 technology is not affected by the use of a silicon substrate coming from a SOI wafer as it was expected.

Wafer identification	**VTN30** (mean) V	**VTP30** (mean) V
2380-1, SOI	0.994399	-0.746823
2380-2, SOI	0.969006	-0.787515
2380-3, SOI	0.968066	-0.755677
2380-4, standard CMOS	1.03602	-0.812213
2399-1, SOI	1.00098	-0.719551
2399-3, SOI	1.01859	-0.714842
2399-4, SOI	0.974159	-0.802612
2399-5, SOI	1.00361	-0.772477
2399-6, SOI	1.07912	-0.700756
2399-7, standard CMOS	0.999127	-0.775001

Figure 4.54. *Threshold voltages for n and p transistors.*

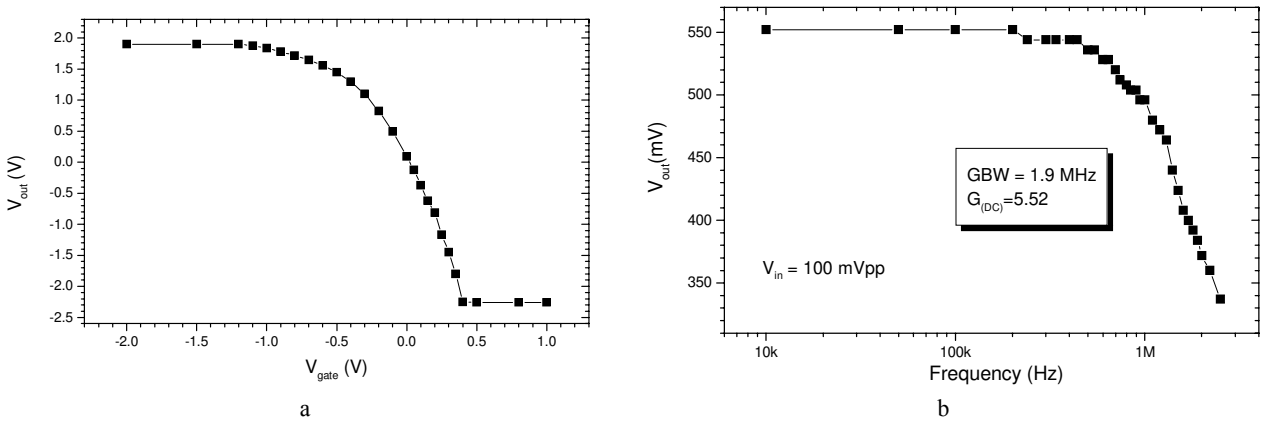


Figure 4.55. *Electrical response of a Buffer Amplifier: (a) Static biasing polarization of the circuit. (b) Frequency response for the same circuit (only magnitude)*

The electrical characterization of the processed CMOS chips on SOI substrates indicates the compatibilization between the integration of SOI-nanoareas with the CMOS circuitry. Both the CMOS test structures and the designed read-out circuits give the expected results. As a conclusion, we can state that SOI nanoareas have been integrated with standard CMOS process for the fabrication of integrated nanocantilevers in monocrystalline silicon as structural material and read-out CMOS circuits. Pre-processing for nanoareas definition has no significant influence in CMOS parameters and in the obtained yield.

As a final remark, the technology developed, SOI nano-areas integrated with standard CMOS can be of interest for the fabrication of other inetegrated nano/microstructures.

4.4.c) Nanofabrication results on the SOI processed wafers

Electron beam lithography (EBL) as well as atomic force microscope lithography has been used to fabricate crystalline silicon cantilevers on the integrated nanoareas of the pre-processed CMOS SOI wafers. The processing for the fabrication (EBL or AFM lithography and post-processing) is the same we have reported in section 4.3. For both lithographic techniques a combination with laser lithography has been needed. As expected, the width of the cantilevers fabricated using crystal silicon instead of polysilicon is smaller than for the polysilicon approach (widths between 215 nm and 285 nm have been achieved). In Figure 4.56 an example of silicon cantilevers fabricated on the SOI-CMOS chip using EBL is shown.

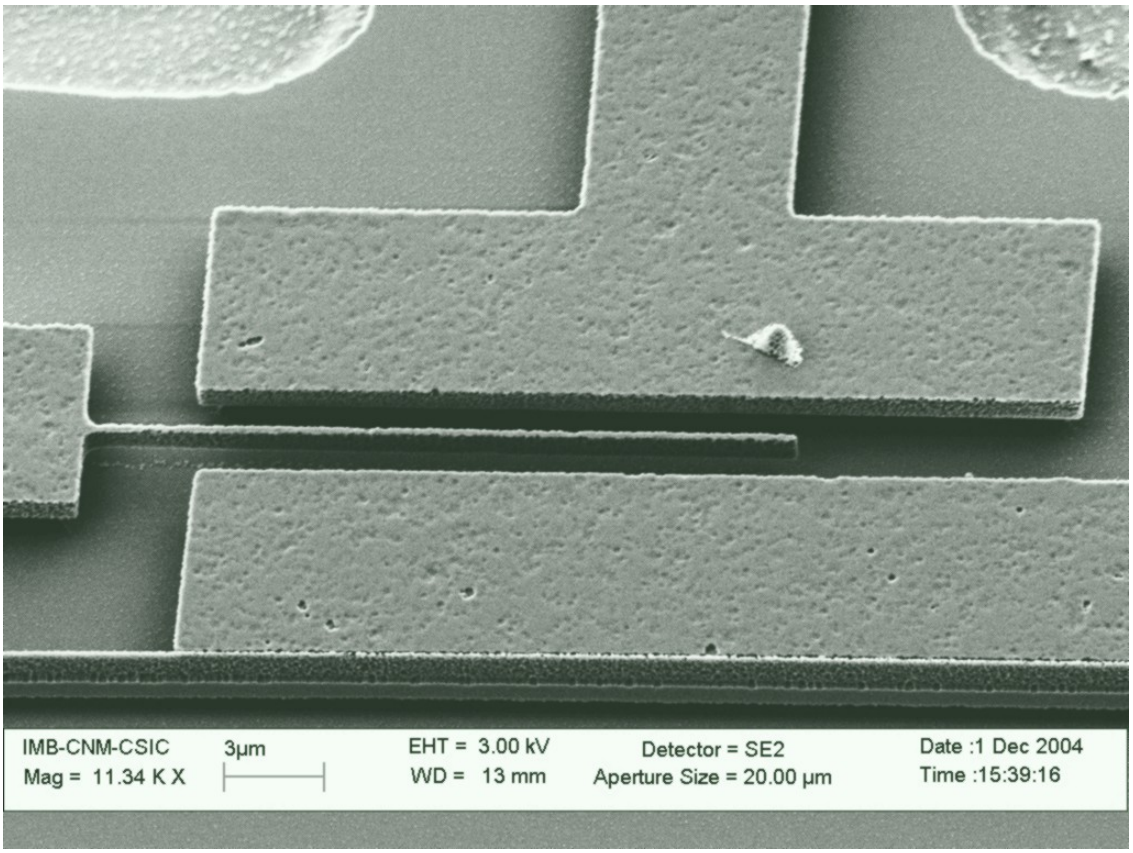


Figure 4.56. *SEM image of an EBL processed silicon cantilever on the SOI-CMOS chip.*

Also by AFM (Atomic Force Microscope) lithography resonators with higher resolution have been defined. This technique cannot be used on polysilicon due to the granular structure of this material. Next figure shows the fabrication process from which a sub-200 nm cantilever has been obtained (figure 4.57).

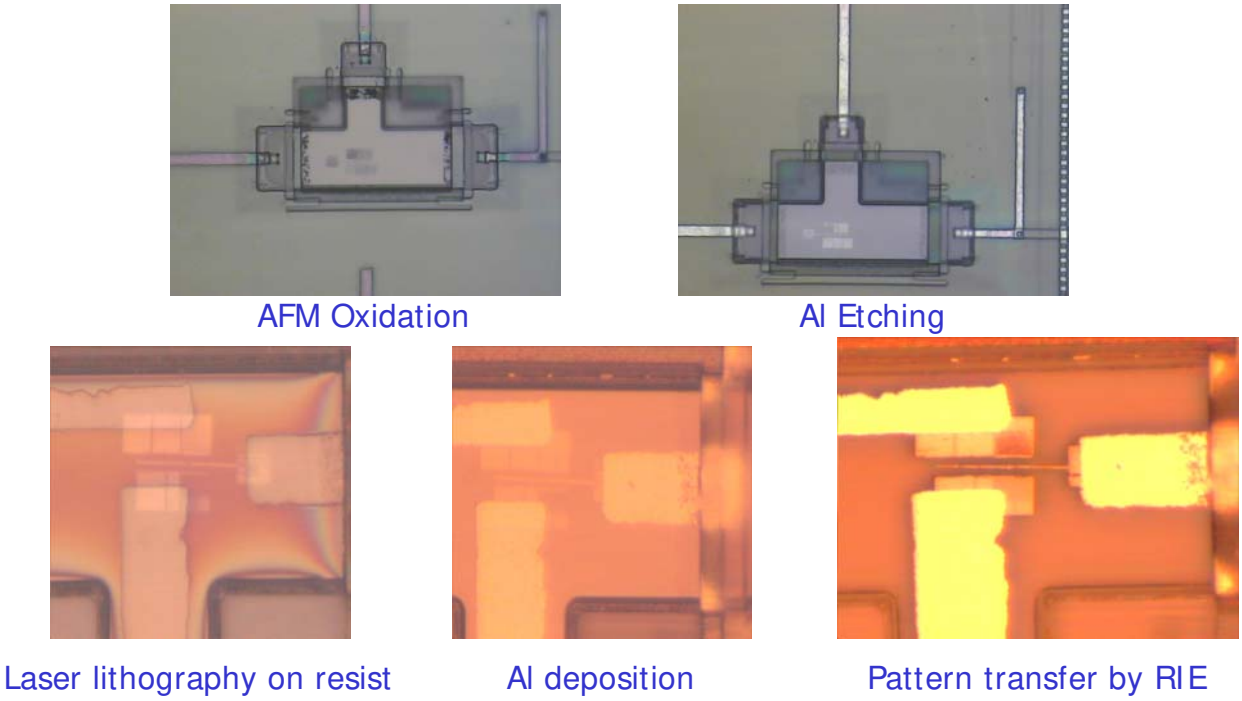


Figure 4.57. *Optical images obtained for the different process steps of the AFM fabrication of cantilevers. First an 8 nm thick Aluminum layer is deposit on the region. It is oxidized locally by AFM. Then the Aluminum is etched selectively. Aluminum oxide will be used as mask. By laser the contacts between the driver/cantilever and circuits contacts are defined. Aluminum is deposit by liftoff. Then by RIE the pattern is transferred. Finally the structure is realised by HF wet etching.*

4.5 Fabrication of nanocantilevers using nanoimprint lithography on CMOS substrates

Several methods have been shown to be able to produce cantilever structures on CMOS chips i.e. EBL, AFM lithography and laser lithography. However, these are all serial and this would be a considerable limitation for industry production. NIL is inherently a parallel process. The objective here is to show that is possible to use nanoimprint lithography on a pre-processed CMOS chip.

4.5.a) Stamp

In our standard stamp manufacturing process we use thermally oxidized Si 1" wafers, with an oxide layer thickness of 300 to 800nm. Electron beam lithography (EBL) and a metal lift-off process defines the stamp pattern and creates an etch mask for the consequent reactive ion etching (RIE), yielding a structure height of 100 to 400nm. After this we apply an anti-sticking monolayer (F13-TCS) on the surface of the stamp by CVD and the stamp is ready to use.

Due to the fact that we choose an optical alignment method several problems arose in the stamp manufacturing process. We wanted to keep the general scheme of production, which led us to the following issues.

- SiO2 is not conductive and has to be modified in order for the EBL to able to generate a pattern.
- Unknown etch rates for the possible transparent materials i.e. glass, fused silica and SiN.
- Due to the topographical nature of the CMOS-chips the stamp needed a structure height of 1.5microns, something never previously done at the department.
- Unknown properties during imprint.

The problems are listed in process order. However, we decided to start our experiments in step two, since the first problem is common to all possible stamp material choices.

Etching experiments

To start with it was clear that the etch speed we used for standard stamps was to slow. This process would give unreasonable etching times or the etch mask would be sputtered away resulting in a defect stamp. Unfortunately glass and SiN turned out to etch even slower, effectively at 1/3 of the etch rate of SiO2.

As a consequence we decided to use fused silica and experimented with the etching parameters to find a process with higher speed and a lower sputtering effect on the mask. This was not successful. The highest possible stamp structure is about 600nm.

In the final solution we use a mesa defined by EBL and etched by HF. The mesa height is about 2μm. The isotropic nature of the wet etch is not a problem since the mesa can be oversized. On top of this mesa the cantilever structure is defined by a second EBL exposure and etched by RIE to a height of 400nm.

EBL on Fused Silica

Doing EBL on a 1mm thick non-conductive sample is not possible. Several possible solutions were considered. Such as buried metal under plasma enhanced chemical vapour deposited (PECVD) SiN, this failed due to the low etch rate of SiN. Practical experiments with metal on fused silica were performed. The process flow for making the stamp is as follows.

- Evaporate a thin Chromium (Cr) layer on the SiO2 1" stamp.
- Do EBL with a negative resist mrL 6000.1 XP (from Microresist Technology). To define the mesa structure
- Use the EBL defined polymer structure as an etch mask to etch away all the surrounding Cr.
- Use O2 plasma to remove the polymer etch mask.
- Etch out mesa using buffered HF
- Evaporate a thin Chromium (Cr) layer on the SiO2 1" stamp.
- Do EBL with a negative resist mrL 6000.1 XP (Microresist Technology). To define cantilever structure.
- Use O2 plasma to remove the polymer etch mask.
- Use RIE to etch out the final cantilever stamp.
- Cr-etch to remove the etch mask.

Mark well that in the whole stamp making process these EBL steps are done twice, once for the mesa and once for the cantilever.

There are focusing problems in the EBL especially for the cantilever structure, since this need to be aligned on the mesa, which is approximately 2microns high. The dose in exposing the resist is becomes highly sensitive to the thickness of the metal. The Cr wet-etch results in jagged edges which will lead to uneven stamp structures.

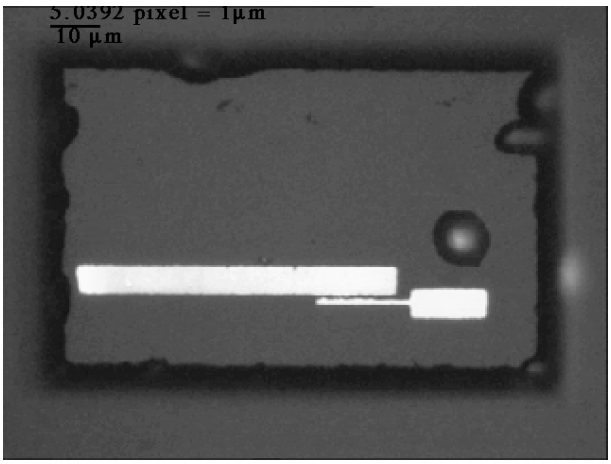


***Figure 4.58**. Image shows cantilever and driver on mesa.*

Structure height and imprinting

The extreme structure height required in this case was solved using a mesa. The imprinting problems will be discussed in the imprint chapter.

4.5.b) Alignment

The alignment is made ex-situ in a Karl Suss (KS) contact mask alignment machine. It features micrometer screws and microscope with 50 and 200 times magnification. The precision is in the micrometer range.

Some minor hardware modification has been done. An alignment process has been developed, which include e.g. transport from the KS to the NIL machine.

4.5.c) Imprinting

Our standard lift-off imprint process is based on a double-layer off polymers, PMMA on LOR. The thickness of this layer is about 200nm. In this case it was decided to start the imprint experiments using much thicker polymers since the combination of a 1mm fused silica stamp and topographically structured sample was an entirely new imprinting challenge for us. It was assessed that the thicker polymer would increase the rate of success of getting pattern transfer and it would also protect the stamp against possible particles. Several interesting aspects have been noted.

- It is possible to get pattern transfer to the polymer.
- Fused silica stamps are very rigid and same-sized stamps and samples are all but impossible to separate (not a problem in this case).
- Since the stamp is rigid and the chips fairly small there are problems accommodating particle defects or uneven substrates.
- Somehow metal particles are deposited from the sample to the stamp
- Heating of the fused silica stamp is slower than the standard silicon stamps. This might affect the viscosity of the polymers on the sample.
- The stamp has been imprinted more than 30 times, without breaking.

Successful pattern transfer to the polymer have been achieved several times, unfortunately the mesa will affect the polymer around the cantilever and driver. The reason for this is not yet entirely understood.

Figure 4.59. *Cantilever and driver in nanoarea after imprint.*

4.5.d) Post Processing

The functionality of our lift-off process has been proven with Cr and Al on flat Si substrates. The cantilever/driver structures themselves do not constitute any problem.

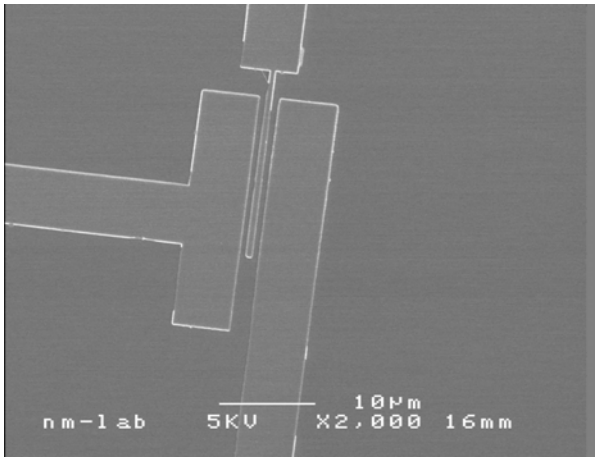


Figure 4.60. *Cantilever and driver in Al on Si after lift-off.*

Development and metal evaporation on the chips has been attempted. No metal remained on the sample after lift-off.

4.5.e) Conclusions

Each process step works individually. Measures are being taken to further improve all of them. Limiting right now is stamp manufacturing. It takes a long time to make a stamp and the success rate is low.

4.6. Electrical characterization of the fabricated NEMS sensors

In this section the electrical characterization of the three demonstrators of the NEMS systems are provided. The NEMS sensors consist on an electromechanical device, in particular a resonant cantilever, excited and detected through a dedicated CMOS VLSI read-out circuit. In the three cases the resonant devices are polysilicon nanocantilevers: a) fabricated using laser lithography; b) fabricated using low energy EBL combined with laser lithography and c) arrays of cantilevers fabricated using optical lithography.

4.6.a) NEMS sensor with cantilevers fabricated using laser lithography

The electrical characterization of the oscillating movement of a polysilicon resonant cantilever through the integrated CMOS circuits is described in this section. In this demonstrator, the cantilever has been fabricated using laser lithography. In figure 4.61 an optical image of the fabricated sensor is shown. The dimensions of the cantilever are: length, l=40 μm; width w=840 nm; thickness, t=600 nm and gap spacing s=1.3 μm. In this case the CMOS read-out circuit follows the voltage amplifier scheme (see explanation on section 4.2 of this report).

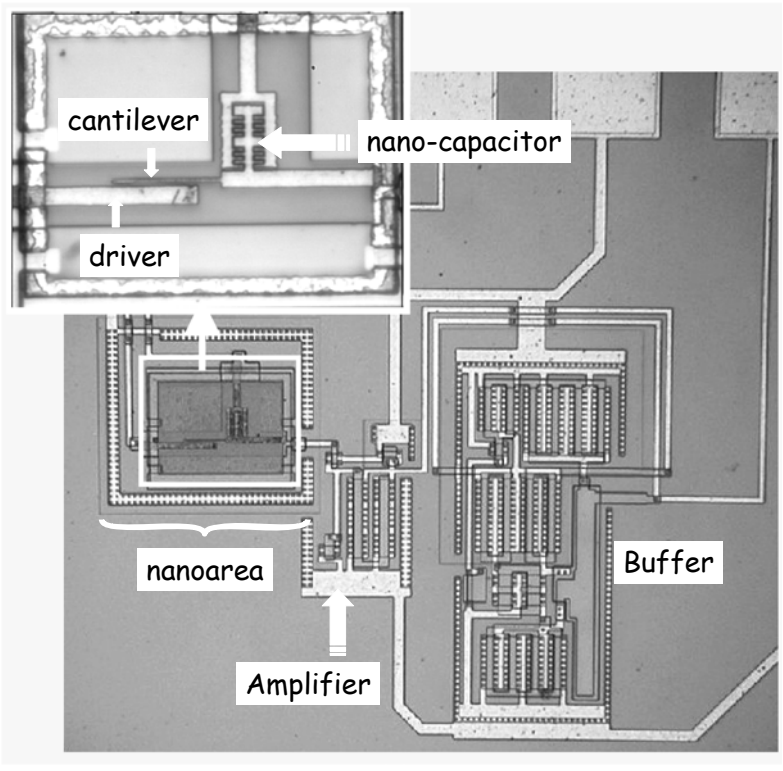
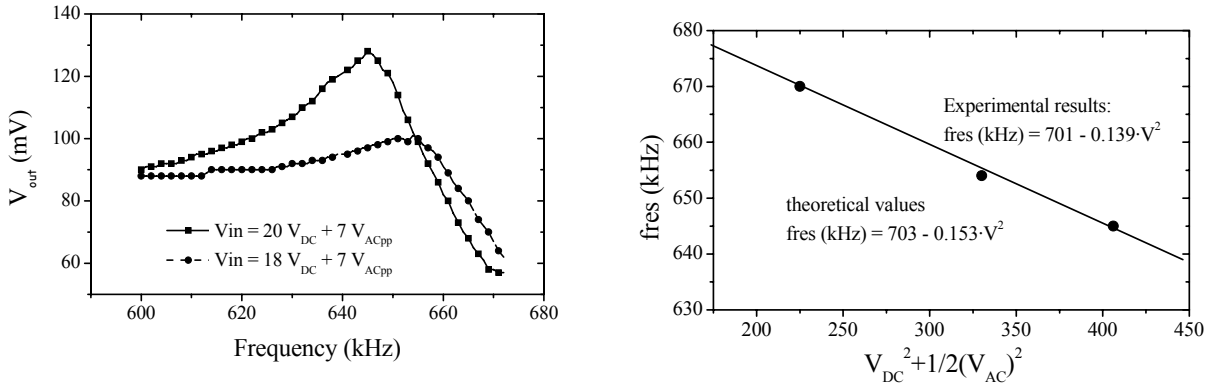


Figure 4.61. *Optical images of the nanomechanical resonator integrated monolithically with the CMOS voltage amplifier. The large image shows the CMOS circuit and the area where the nanomechanical device is fabricated. The inset ia a zoom image of it, where it can be better appreciated the cantilever, the driver and the integrated capacitor for proper circuit polarization. The dimensions of the cantilever are: length, l=40 μm; width w=840 nm; thickness, t=600 nm and gap spacing s=1.3 μm.*

The electrical magnitude of the frequency response of the nanoelectromechanical system is presented in figure 62a. These two curves have been obtained by applying an AC voltage of $7V_{pp}$ and a DC voltage of 18V and 20V to the driver. The peak of the curves corresponds to the mechanical resonance of the cantilever as it has been corroborated by the simultaneous inspection with an optical microscope.



a b

Figure 4.62 a). *Electrical characterization of the global system (CMOS voltage amplifier circuit plus electromechanical transducer) corresponding to the system shown in figure 21 for two different DC voltages (V_{dc}).* ***b).*** *Experimental dependence of the resonance frequency with the applied voltage. The points corresponds to three experimental resonance frequencies (two of them corresponding to figure 13a) and the straight line to the linear fit.*

Figure 62a shows that the resonance peak is larger and shifted to a lower frequency when increasing the DC voltage. When applying a higher DC voltage the force between the driver and cantilever increases, increasing the oscillation amplitude of the cantilever and thereby the voltage output. Also, the increase in electrostatic force decreases the effective spring constant of the cantilever and thus decreases the cantilever resonance frequency. An analytical expression of the dependence of the resonance frequency on the DC voltage is:

$$f(V) = f_o - \left(\frac{2 f_o \varepsilon_o l^4}{E w^3 s^3} \right) V^2 \qquad \text{(Hz)} \qquad (35)$$

Since we use both DC and AC voltage, $V^2 = V_{dc}^2 + 1/2(V_{ac}^2)$ in this case. Figure 4.62b shows the experimental (dots) dependence of the resonance frequency together with the linear fit curve. From the dimensions of the cantilever and using the equations from the electromechanical model explained in section 4.1, we find that the theoretical value of the natural resonance frequency (V_{dc} =0) is 703 kHz. This is approximately the same value as obtained from the experimental results, shown in figure 4.62b. From these results, we obtain that the theoretical sensitivity of this cantilever is $34 \cdot 10^{-18}$ g/Hz, which is an extremely high sensitivity for punctual mass detection. In terms of distributed mass detection, the sensitivity is $12 \cdot 10^{-13}$ g/Hz/cm^2 which is comparable to quartz microbalances. By further decreasing the dimensions of the cantilever, this sensitivity can be improved.

The final resolution of the cantilever will depend on the minimum change of frequency that the system will be able to detect. Along with factors like electrical and thermomechanical noise, this

is limited by the value of the Q-factor. The Q-factor of the cantilever depends strongly on the environment where the measurements are performed. In this case, the experimental results have been obtained in air. For both curves we have obtained a Q-factor ≈ 21. This value is increased when working in vacuum, as we will show in next section, or by using feedback specific techniques.

First, we can evaluate the minimum change of frequency due to the electrical noise for our integrated read-out circuit. A simple and rough estimation of the change of the transducer output, V_{out}, close to the resonance can be expressed as the ratio between the maximum voltage at the resonance and the second-order system frequency bandwidth (equation 36). Taking into account the definition of the quality factor, Q, we obtain the following expression:

$$\partial V_{out} / \partial f \approx \frac{V_{\max}}{\Delta f} = \frac{QV_{\max}}{f_o} \tag{36}$$

From this expression, the variation of frequency as a function of the SNR (signal-to-noise ratio) of the read-out system at the resonance can be obtained (equation 37):

$$\delta f \approx \frac{f_o}{Q}\frac{\delta V_{out}}{V_{\max}} \approx \frac{f_o}{Q}\frac{1}{SNR} \tag{37}$$

From the values of the simulated electrical noise and the bandwidth of our read-out system (250 nV/$\sqrt{Hz}$ and 1 kHz, respectively), the SNR ≅ 84dB. Consequently, from equation 37, the minimum measurable frequency change is $\delta f \approx 1.9$ Hz. In this case, the mass sensitivity with the integrated system will be below 65 attograms.

Second we have evaluated the effect of V_g polarization which induces DC voltage instabilities at the sense node, which in turn produces variations of the bias point. We have experimentally obtained that the DC variation at the output of the circuit is in the order of 5 mV in the time framework of the experiment. Taking into account that the experimental gain of the circuit (buffer amplifier) is 4.85, the Vg variation voltage will account for 1 mV. The frequency stability evaluation can be derived from the frequency dependence with the applied voltage (figure 4.62b and equation 38).

$$f_{res}(kHz) = 701 - 0{,}139V^2 \tag{38}$$

According to this dependence, and taking into account the DC voltage applied in this experimental data (Vdc=18V), the frequency stability will be Δf=5 Hz (calculated from equation 39) which is in the same range than the thermomechanical noise inherent to mechanical devices and constitutes the major source of noise in our system

$$\delta f_{res}(kHz) = 2 \cdot 0.139 \cdot V_{dc}\delta V \tag{39}$$

From the AC value of V_{out} at 600 kHz, when the cantilever is out of resonance, we can estimate the value of the total parasitic capacitance C_{pa} by assuming a simple AC capacitive voltage divider formed by C_{pa} and the static capacitance C_p (equation 33). The value of V_g is the value of $V_{out}(AC)$ (90mV$_{pp}$) divided by the gain (G_{amp}) of the circuit at 600 kHz. This gain has been determined experimentally from the frequency response of this readout circuit and it is found to be 4.85 (at 600 kHz). Thus, we obtain a value of V_g = 18.6 mV$_{pp}$. The value of V_g cannot be tested directly because any external connection would introduce an additional parasitic capacitance. However, we know the value of C_p calculated from the dimensions obtained by the optical inspection of the fabricated cantilever, which is around 122 aF (note that for this

evaluation the coupling length of the cantilever is 30 μm). With these values and knowing that $V_{in}(AC)$ is 7 V_{pp}, we obtain a value of C_{pa} = 46 fF. This is in good accordance with the expected value. From this result and taking into account equation (34), we are able to evaluate the amplitude of the cantilever movement at the resonance ($\approx$250 nm). Finally from this amplitude and assuming a linear deflection of the cantilever, we can also evaluate the variation of the static capacitance (C_p) due to the cantilever movement, ($\Delta C \approx 40$ aF). These results validate the overall circuit design and fabrication process that we have chosen to fabricate the mass sensor, and the success of the combination of a nanomechanical device and a CMOS circuit.

4.6.b) NEMS sensor with cantilevers fabricated using low energy e-beam lithography

The electrical characterization of the oscillation of nanocantilevers fabricated using EBL and measured through the integrated CMOS circuit are described in this section. The EBL process has been made using low dose energy for the irradiation of the resist, decreasing the degradation of the CMOS circuits (see further details in section 4.3 dedicated to the fabrication of the cantilevers).

Figure 4.63 shows optical images of a PolySi resonating cantilever while the electrical characterization is performed. In figure 4.63a, the cantilever is excited with a frequency smaller than its resonance, so that there is no movement of the tip of the cantilever. On the other hand, as it is shown in figure 4.63b, the cantilever is oscillating because the frequency of the excitation signal is closer to its resonance. The dimensions of this polysilicon cantilever are: length=23 μm, width=400 nm and thickness= 600 nm.

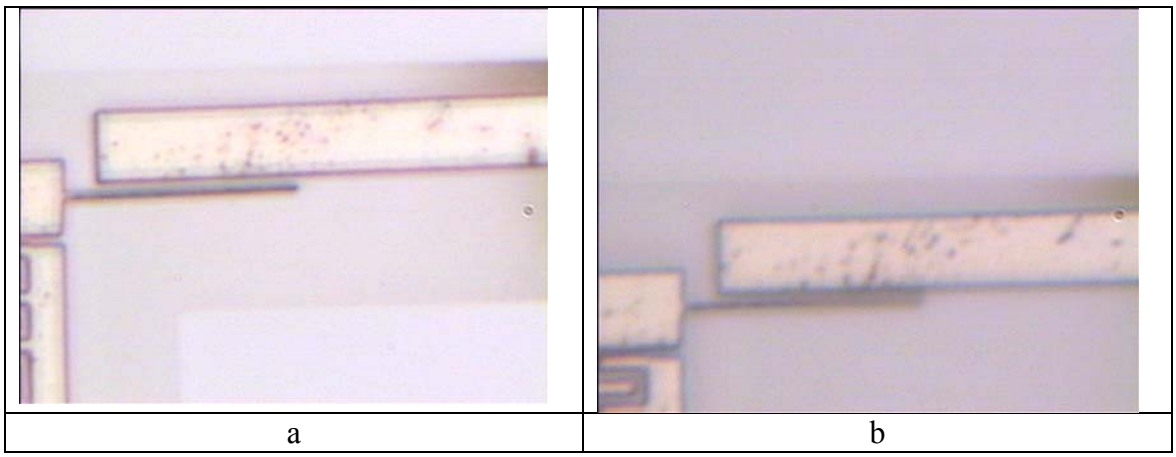


Figure 4.63 *Optical images of: a) the non-oscillating cantilever while applying 18Vdc and 5Vac@700 kHz and b) closed view of the oscillating cantilever while applying 18Vdc and 5Vac@830 kHz. Dimensions of the cantilever (by AFM characterization) are: length=23 μm, width=400 nm and thickness= 600 nm.*

Figure 4.64(a) shows the on-chip voltage (gain amplitude and phase) response of a resonating cantilever having a width of 420 nm, a thickness approximately of 600 nm and a length of 20 μm (see figure 4.43 in section 4.3.c of this report for an image of this cantilever). The theoretical resonance frequency of this system is approximately 1.407 MHz, and the theoretical mass resolution, $\partial m/\partial f$, is 17 ag/Hz using a Young's modulus value of 160 GPa. The cantilever is driven by 5.5 V AC peak-to-peak to induce the oscillation. Simultaneously, a DC voltage is applied, which allows detecting the displacement current, and in this way the oscillation of the

cantilever is translated into an electrical signal. A set of curves is acquired at different values of a DC voltage: from 14 V to 7 V DC (figure 4.64(b)).

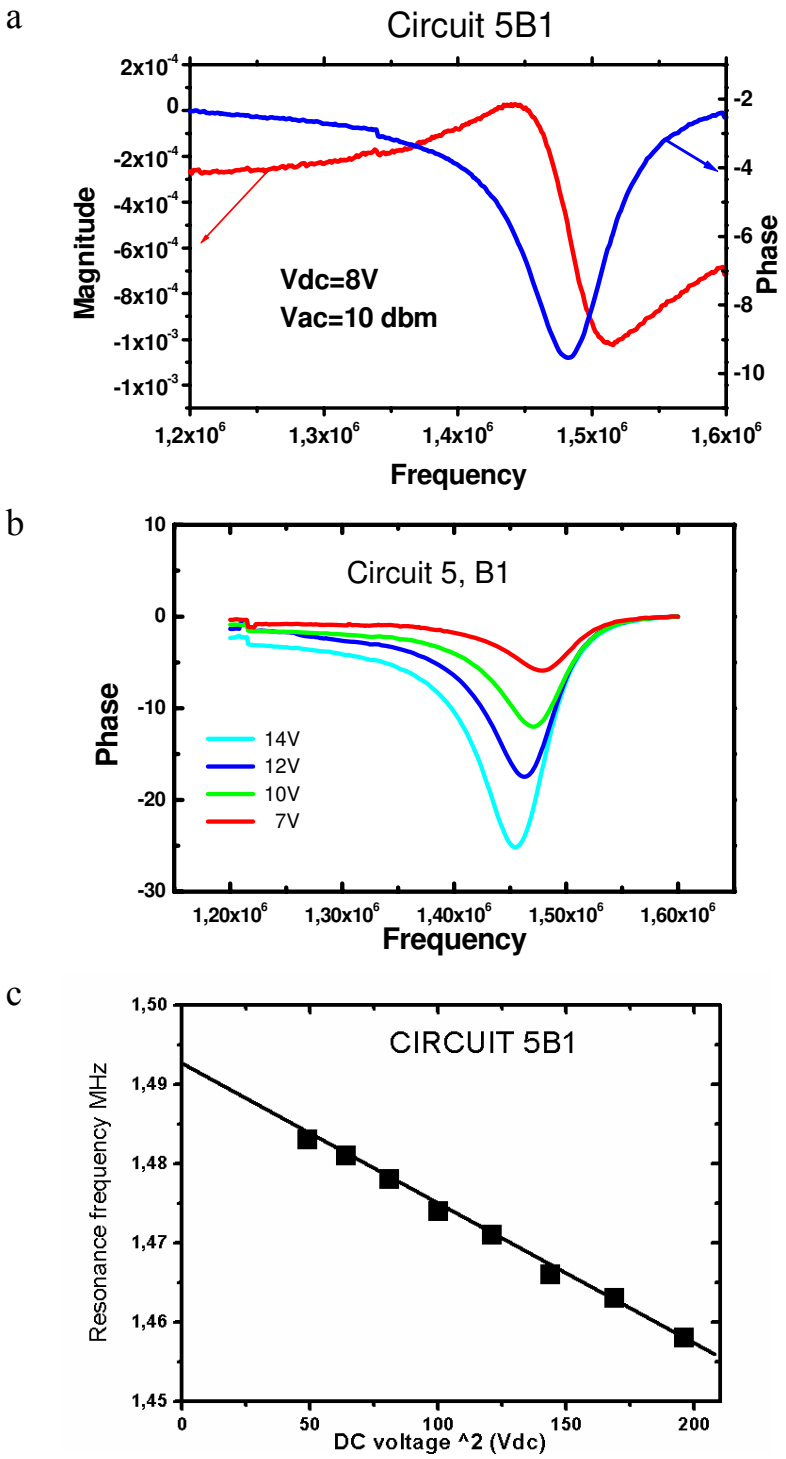


Figure 4.64. *Electrical characterization of a resonating cantilever with a width of 420 nm, a thickness approximately of 600 nm and a length of 20 µm obtained through the integrated CMOS circuit. (a) Magnitude and phase around the resonance frequency. (b) Phase versus frequency for different applied voltages. (c) Resonant frequency versus the squared applied voltages. A clear fitting between the experimental 0 bias resonance frequency extrapolated from the different experimental data and the theoretical natural resonance frequency is obtained.*

The decrease in resonance frequency when increasing the DC voltage is due to electrostatic damping. Figure 4.64(c) shows the dependence of resonance frequency with voltage. The extrapolation of the curve to a 0 V DC voltage indicates a free resonance frequency of the cantilever of 1.492 MHz, in accordance with the theoretical estimation of 1.407 MHz. From the figures, the quality factor of the resonance curve is about 11, which is due to air damping since the electrical characterization was performed in air.

4.6.c) MEMS sensor with Arrays of cantilevers fabricated using optical lithography

In this section we describe the electrical characterization results obtained on cantilever arrays fabricated on polysilicon CMOS substrates. Some examples of these arrays are shown in Figure 4.65: a) array of 4 cantilevers, b) detail of two cantilevers, c) array of 8 cantilevers fabricated within the same nanoarea and d) detail of an array of 8 cantilevers with independent nanoarea for each.

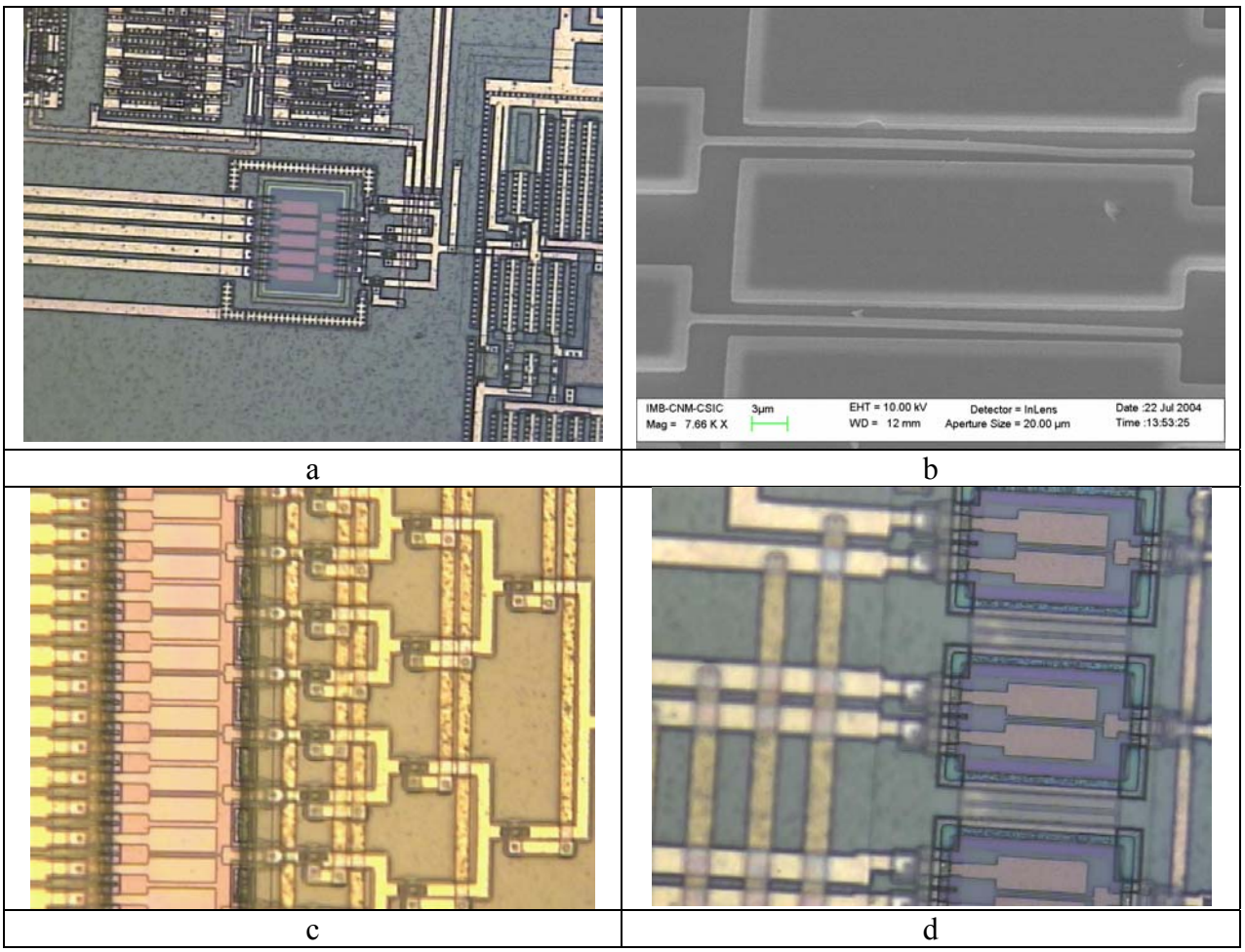


Figure 4.65. *Examples of the fabricated arrays of cantilevers monolithically integrated with the CMOS circuit. (a, c, d) are optical images, while b) is a scanning electron microscopy in which it can be appreciated that the edge of the cantilevers are still stuck onto the substrates. Prior to the electrical measurements these cantilevers are unstuck with the aid of an atomic force microscope.*

The results obtained with these devices can be classified in two groups:

1) Simultaneous excitation and detection of two cantilevers of a 4-elements array through the CMOS readout circuit.
2) Digital controlled selection of the connection between an 8-elements array and a single CMOS readout circuit.

Multiple excitation and detection

Figure 4.66 shows the device where multiple excitation and detection of cantilever array components has been obtained. Such devices consist on an array of 4 cantilevers with detection through a driver electrode connected to CMOS circuitry. In this case, two independent readout circuits are used to detect the resonance of a group of two cantilevers. The upper circuit is connected to the two upper cantilevers and the lower circuit to the lower part cantilevers.

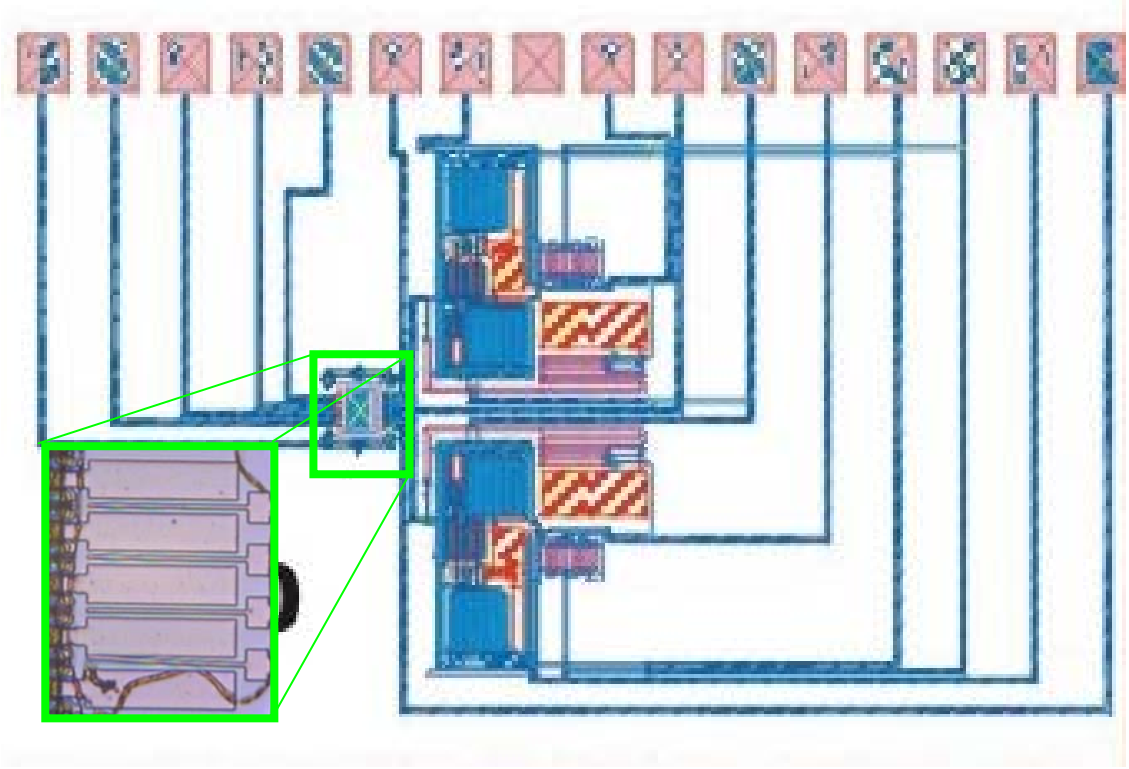


Fig. 4.66: *Layout of a 4-cantilevers array with double CMOS readout circuitry. In the left bottom side, an optical image of the array shows the 4 cantilevers and the excitation and reading electrodes.*

In figure 4.67 the electrical signal (phase and magnitude) obtained at the output of the CMOS circuit of fig 4.67 device is shown. Both curves corresponds to the frequency response around the resonance of the 2nd (cantilever #1) and 3rd (cantilever #2) cantilevers (from top) of figure 4.66 array. The resonance of cantilever #1 is detected through the upper circuit and the one of cantilever #2 through the lower circuit. Although dimensions of cantilevers are identical from design (50 μm long, 1.4 μm wide, and 600 nm thick) , and polarization conditions are also the same, process mismatch can be the responsible of a 11 kHz difference on the resonance frequency. In this case the CMOS read-out circuits are the current amplifiers described in section 4.2.

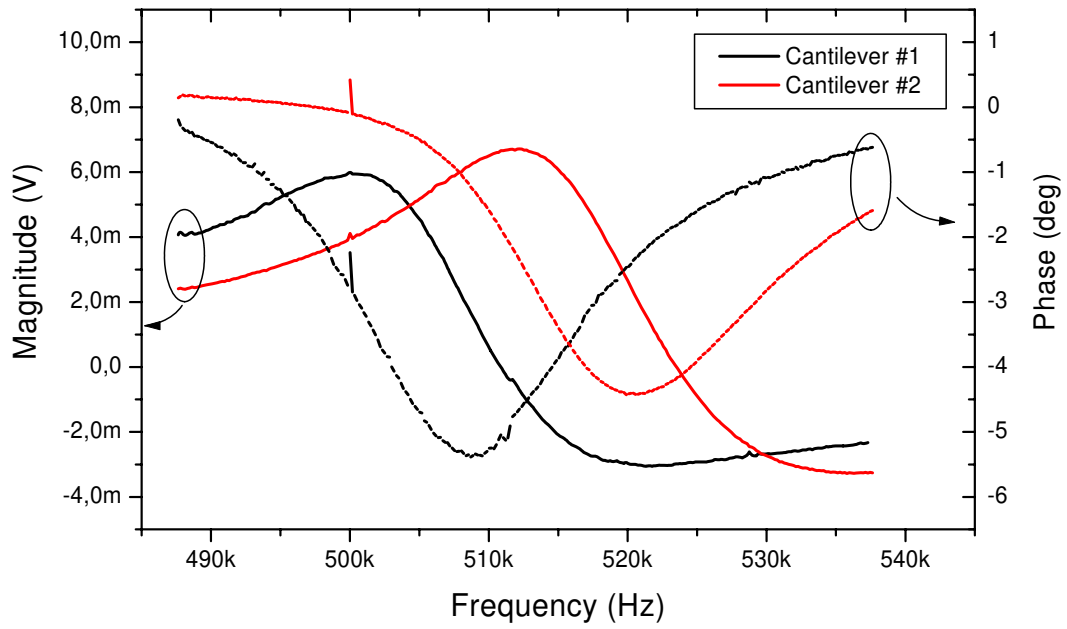


Fig. 4.67 *Electrical signal obtained at the output of two independent CMOS readout circuits, corresponding to the frequency response around the mechanical resonance of two cantilevers of a 4-components array (figure 26). Resonance frequency is at 501 kHz for cantilever 1 and at 512 kHz for cantilever 2. Polarization conditions are for both cantilevers Vdc=18 V and Vac=9 Vpp.*

Device shown in figure 4.68 consists on an 8 components array, connected through a digital controlled switching interface to a single CMOS readout circuit. This device has been selected to study the stray coupling of an excited but not connected cantilever to the circuit output.

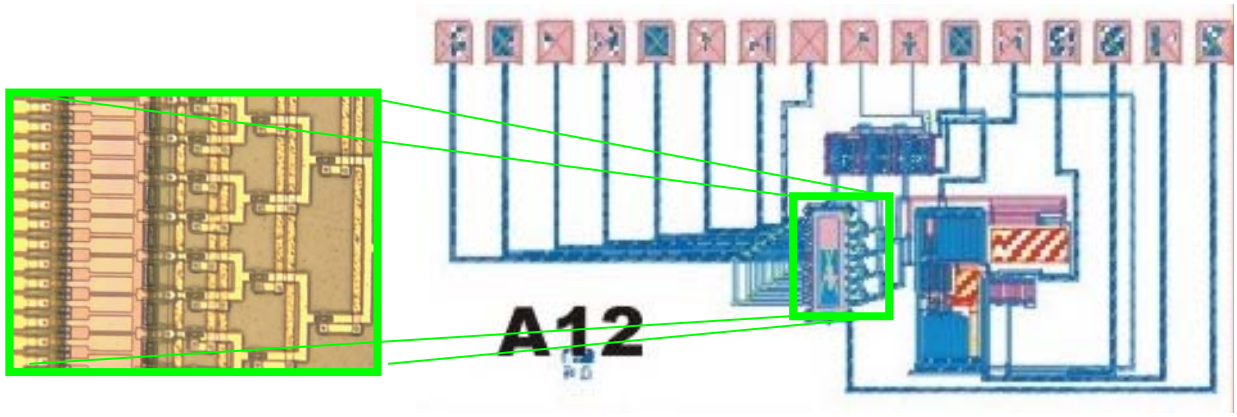


Fig. 4.68: *Layout of an 8-cantilevers array with single CMOS readout circuitry, with digital multiplexing control for sinlgle array component detection. In the left side, an optical image of the array of 8 cantilevers is shown.*

In table 4.8 the ouput level of the CMOS circuit of figure 4.68 is summarized at the 8 different switching states, when only cantilevers 4 and 8 are excited with a 500 kHz and Vac=1.98 Vpp signal. As it is shown in the table, only when the circuit is connected to the excited components of the array, the output signal is maximum (around 12mVpp). In the rest of cases, a parasitic signal of around 8.5mVpp is detected coming from not directly connected cantilevers 4 and 8.

Digital trol Code	Cantilever	Vout (mVpp)	Excitation
000	1	8.2	NO
001	2	8.2	NO
010	3	8.6	NO
011	4	12.8	YES
100	5	8.4	NO
101	6	8.4	NO
110	7	8.6	NO
111	8	12.0	YES

Table 4.8 *Output voltage level of an 8-cantilevers single CMOS read circuit device, with digital controlled selection interface of the reading cantilever. Only cantilevers 4 and 8 are excited with a 1.98Vpp signal at 500 kHz.*

4.7. Mass measurements performed with the system on chip NEMS sensors

In this section the experiments and results to evaluate the functional performance of the sensors under different environmental conditions and for mass sensitivity evaluation are presented. The experiments have been performed with the Polysilicon cantilevers fabricated on pre-processed CMOS circuits. The electrical excitation and read-out have been performed with the on-chip integrated circuitry. In the first part of the section the characterization of the performance of the sensor under different electrical and environmental conditions are described. In the second part of the report we will describe the experiments on mass detection performed to demonstrate the ability of the Nanomass sensors to detect mass in the atto-femtogram range

In order to enable best possible characterization of the performance of fabricated nanocantilever mass sensors a chamber has been built at MIC. The chamber enables control of pressure (1 bar-0,01 mbar), temperature (20^{o}C-200 ^{o}C) and furthermore it is possible to insert gases at controlled flow rates. Also biomolecules that initially are in liquid state can be inserted into the chamber by injecting the liquid solution using an syringe. Molecules can also be placed in an externally connected glass manifold, in which a transition into gas phase can be achieved by heating the molecules above their boiling temperature. Hence, the chamber will also enable biochemical detection with high control of molecular content, evaporation quality and reproducible conditions. Figure 4.69 shows images of the measurement chamber in the laboratory.

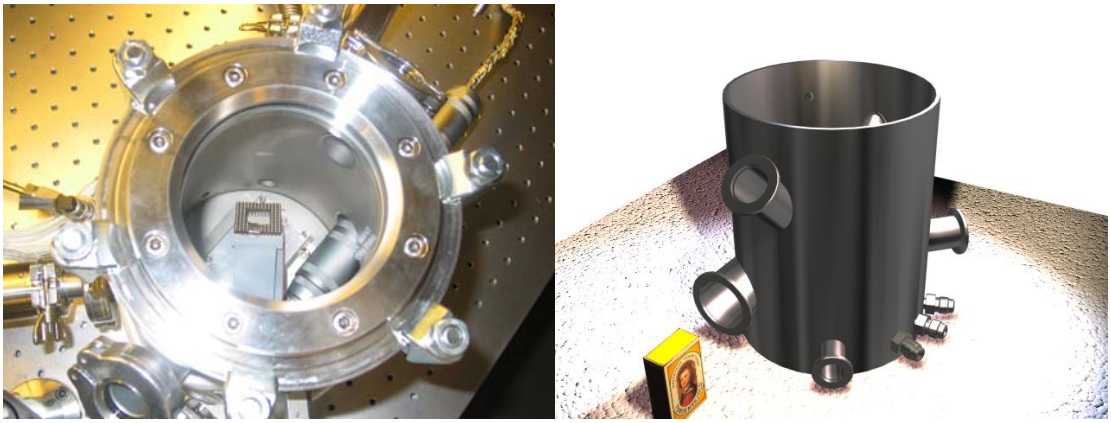


Fig. 4.69*. (Left) Image of the interior of the measurement chamber. The pin-grid holder is visible in the middle of the chamber. (Right) A schematic 3D image of the chamber is displayed.*

Electrical connections are made by wire bonding the CMOS chips to a ceramic chip holder that is placed on a ceramic pin-grid mounted inside the measurement chamber. A gain-phase analyser has been used to detect the electrical signal from the CMOS.

To study the behaviour of the resonance frequency of the resonators under different ambient conditions, resonator structures have been characterized in this chamber. The main result is related with the dependence on the Q-factor of the resonator on the ambient pressure. In figure 4.70 the estimated quality factor (Q-factor), obtained through the on-chip read out CMOS circuit, is displayed as a function of pressure as well as DC voltage. The quality factor dependence on the pressure shows a log-log dependence. As seen using high DC voltages at low pressure decreases the Q-factor. This is due to electrostatic damping of the cantilever as it is bent closer to the driving electrode as a DC voltage is applied. A quality factor of approximately 5000 is determined at 0.4 mbar and 1 V_{DC}. The quality factor is reduced to 30 at ambient conditions.

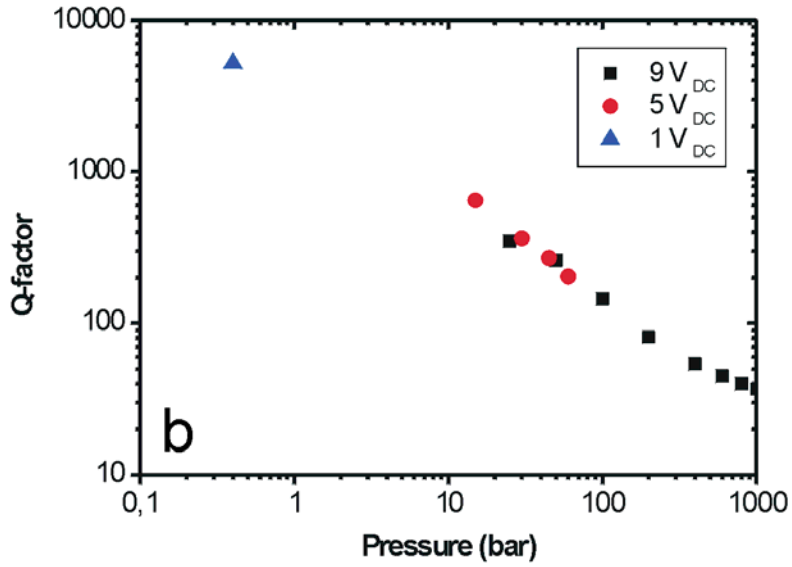


Figure 4.70. *Quality factor dependence on the pressure for a Poly-Si cantilever (see figure 4.43) having a width of 420 nm, a thickness of 600 nm and a length of 20 μm, defined by combined low energy EBL and DWL. A quality factor of approximately 5000 is determined at 0.4 mbar and 1* V_{DC}.

In order to characterize the performance of the mass sensor in air point masses were placed at the endpoint of the cantilever. Single glycerine drops were placed selectively on the cantilever using an STM-tip. The deposited glycerin drop had a diameter of approximately 500 nm. Giving a hemispherical volume and $\rho = 1{,}26 \cdot 10^6$ g/m^3 the weight of the glycerine drop was estimated to be 41 fg. Figure 4.72 shows the on-chip read-out before and after the controlled positioning of a single glycerin drop on the end point of the resonator (optical images in figure 4.71). An AC voltage of 6 V_{pp} and a DC voltage of 14 V were applied to a 20 μm long, 400 nm wide and 600 nm thick nanoresonator, similar to the one in figure 4.43. A resonant frequency of 1,432 MHz was measured before the deposition of the glycerin bead. Directly after the deposition of the drop a frequency shift of 14,8 kHz was measured in air. From the frequency shift an added mass of 50 fg is calculated, which is close to the estimated mass of the glycerine drop of 41 fg. Hence, the mass resolution of the system is approximately 3 ag/Hz.

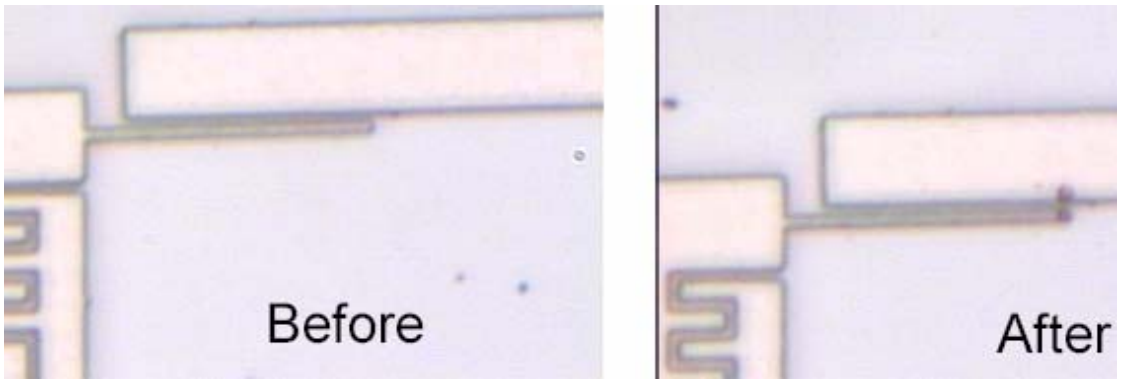


Figure 4.71*.Optical images of the cantilever-driver system before and after the deposition of two glycerin beads: one at the end point of the cantilever and the other is on the counter electrode and did not affect the measurements*

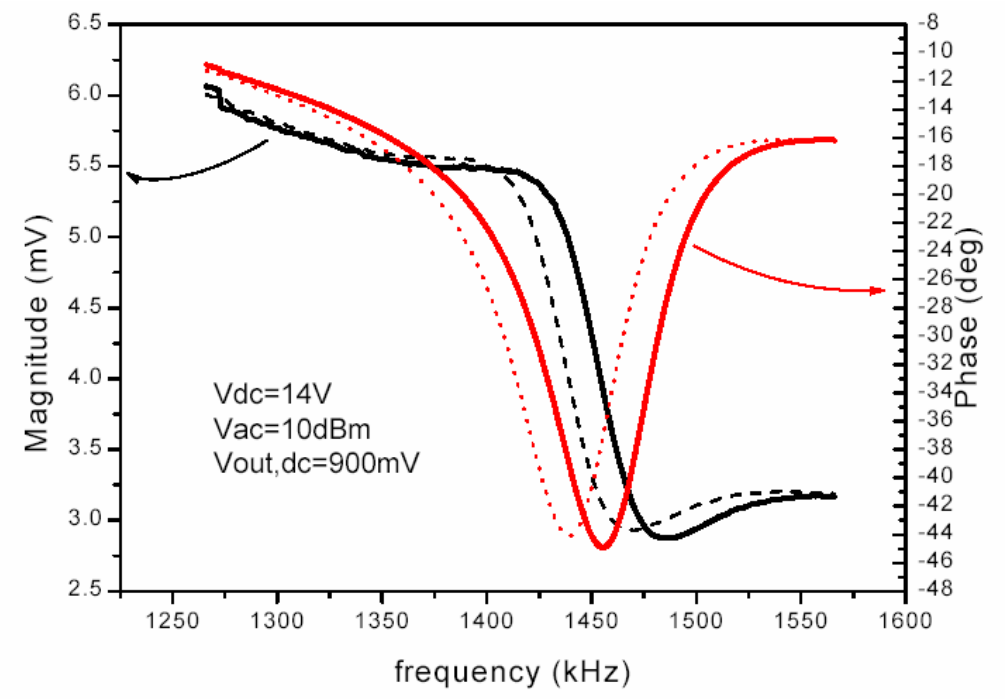


Figure 4.72. *The diagram shows the CMOS electrical resonance signal for a poly-Si cantilever before (solid line) and after the deposition of the glycerin bead. The cantilever is 20 μm long, 400 nm wide and 600 nm thick. It was excited into resonance by applying 6* $V_{peak\text{-}peak}$ *AC and 14 V DC.*

5. Deliverables and references

5.1 Deliverables

All details on technical information have been reported on a set of 23 deliverables. Contents of each deliverable are summarized in this section. The following table indicates the delivery project month, the type of deliverable and its security level.

Del. no.	Del. name	Delivery (proj.month)	Del. type	Security
0	**Dissemination and Use plan**	6	R	CO
1	**Application forecast 1:** Expected applications of phase I devices	6	R	CO
2	**Technology definition for SOI substrates**	12	R	CO
3	**Characterization released cantilevers:** Fabrication of metal cantilevers	12	R	CO
4	**Fabrication of nanocantilevers by e-beam**	12	R	CO
5	**Periodic progress report of first year**	12	R	CO
6	**Demonstrator sensor 1:** Sensor fabricated with polysilicon cantilevers	12	D	CO
7	**Application forecast 2:** Update of deliverable 1	18	R	CO
8	**Fabrication of nanocantilevers by NIL**	18	R	CO
9	**Validation of nanocantilever fabrication by EBL**	18	R	CO
10	**Mid term report**	18	R	CO
11	**Evaluation electroplating technology**	20	R	CO
12	**Periodic progress report of second year**	24	R	CO
13	**Functional evaluation of demonstrator 1:** Sensor fabricated with polysilicon cantilevers	24	R	CO
14	**Circuit electrical characterization 2:** Circuit electrical characterizartion of CMOS on SOI substrates	24	R	CO
15	**Demonstrator sensor 4 :** Sensor fabricated using electroplating	24	D	CO
16	**Functional evaluation for demonstrator 4**	30	R	CO
17	**Combination CMOS with NIL**	30	R	CO
18	**Demonstrator Sensor 2:** Sensor fabricated using SOI substrates	30	R (initially D)	CO

19	**Circuit electrical characterization 3**	32	R	CO
20	**Demonstrator sensor 3:** Sensor fabricated using NIL	33	D	CO
21	**Functional Evaluation for demonstrator 2:** Sensor fabricated on SOI substrates	36	R	CO
22	**Report on industrialization**	36	R	CO
23	**Final report, summary**	36	R	CO

R: report
D: demonstrator
CO: Confidential

Due to different reasons, deliverables numbered 15, 16, 19, 20 and 21 has not been completed. In the case of metal cantilevers, D15 and D16, after the first review of the project, it was decided to focalize the efforts on the silicon approach as structural layer. In the case of D19 and D20, due to the technological problems between the nanoimprint lithography and the pre-processed CMOS substrates, the results to be reported on these deliverables were not achieved. Finally the functional evaluation of the performance of the sensors has been concentrated on the sensors with polysilicon cantilevers, thus D21 has not been also provided.

Following a brief summary of the main contents of each of the deliverables is provided.

Deliverable 1. ***Report on application forecast***

This deliverable explains a set of possible application of the devices. In this deliverable, the expected sensitivity of the devices are compared with that of Q-microbalance, and from this comparison, a set of expected applications is presented. These expected applications will influence the specifications and design of the first set of sensors based on phase-1 approach.

Deliverable 2. ***CMOS Technology Definition for SOI Substrates***

On this report it is summarised the study of the possibilities to integrate the silicon nanosensor and the CMOS circuitry on a SOI wafer. The goal is to fabricate cantilevers on crystalline silicon, using the SOI layer of the wafer as the structural layer and placing the CMOS integrated circuitry on the bulk silicon of the same wafer, as a usual standard run. The silicon oxide by one hand is used as insulator, by the other is used as a sacrificial layer which will be etch to release the cantilever from the substrate. The main point of this development is to keep unaltered the characteristics of the CMOS process, or to introduce small changes.

Deliverable 3. ***Metal Cantilevers***

In this report the first trial to obtain metal cantilevers for being integrated with the CMOS circuitry is explained. The studied process sequence with the main results, some theoretical considerations about different metals and finally the future considerations are reported.

Deliverable 4. ***Fabrication of nanocantilevers using electron beam nanolithography***

In this report the nanocantilevers fabrication using electron beam lithography is explained. The first structures were defined on both silicon (100) and on poly-silicon samples with pre-fabricated CMOS circuits. The process for the fabrication were developed where different resists were used as well as different exposure times. This resulted in a working concept which is explained in this deliverable.

Deliverable 5. ***Periodic progress report of first year***

The main result of the first year Nanomass II project (deliverable written after accomplishing the 9th month) was the electrical characterisation of a resonating nanocantilever through the CMOS integrated circuit. A workable NEMS system was obtained and in this way, Demonstrator 1 for testing and study the functionality of the sensor was available.

Deliverable 7. ***Report on application forecast 2***

This deliverable explains a set of possible application of the devices. Expected applications will influence the design of demonstratores D2 and D4. The present deliverable is organized as an update of deliverable 1: Report on application forecast 1 (issued on June 1st, 2002). Only new applications are highlighted (in red). Rest of applications is still valid. The strategy to validate applications described in deliverable 1 consisted on the experimental evaluation of sensitivity achieved. Due to the delay in WP1 and WP7, this validation has not been performed yet.

Compared to deliverable 1, the following elements have been added:

- A collaborative relation with a partner from ATOMS project, EPFL (Prof. Juergen Brugger) has been established. As an outcome of this relation, the application of NANOMASS sensor for characterization of nanostencil lithography has been proposed.
- CNM will sign a cooperative research agreement with BDC/EPSON for the development of Si/ressonators + IC monolithic devices. Technological advances within NANOMASS project are expected to be applied.

For the evaluation of the expected sensitivity of the devices are compared with that of Q-microbalance, and from this comparison, a set of expected applications are presented.

Deliverable 8. ***Fabrication of nanocantilevers by Nanoimprint lithography***

The process flow for the fabrication with Nanoimprint lithography of metal nanocantilevers in one inch Si wafers with native oxide is explained in this deliverable. The required layout for the cantilever and the driver has been obtained with different metals (Al and a combination of Au and Cr). Although the width of the Al cantilever is 200 nm, they bent due to the superficial stress.

Deliverable 9. ***Validation of nanocantilever fabrication by EBL***

Nanocantilevers have been fabricated by using electron beam lithography, (EBL), directly on CMOS chips. The process for the cleaning of, and resist depositing on the CMOS chips prior to EBL exposure is the same as reported in deliverable 4. The circuit performance of the chips, which were exposed with high-energy electron beams, turned out to be significantly affected (see annex 1 in this deliverable). The high-energy electrons severely damaged the circuits, and no signal could be detected from these circuits even after annealing the chips. The reason for this behavior and how to prevent it is currently studied at the CNM in Barcelona. In order to minimize the damage of the circuits, exposures using low energy EBL were made, and the accelerating voltage was decreased to 3kV. Chips with tested circuits were then exposed with low energy electron beams and after the lift-off process the circuits were measured again. A slight degradation in the circuit performance could be detected but the performance was restored after an annealing step of the processed chip.

Deliverable 10. ***Mid Term Report***

The main results of the first 18 months of the Nanomass II project have been: (i) the electrical characterisation of a resonating nanocantilever through the CMOS integrated circuit (Demonstrator 1: NEMS-CMOS system), (ii) the fabrication of nanocantilevers using both AFM and EBL lithography techniques on the CMOS pre-processed substrates, (iii) the procedure to use SOI wafers for the CMOS fabrication and the nanoarea definition, (iv) the fabrication of metal cantilevers by a lift-off technique using UV lithography for defining the resist mold and also by nanoimprint techniques. Some of these results have been fully described in deliverables 2, 3, 4 and 5 (periodic progress report of first year), 8, 9 and 11.

One of the main problems dealing with the cantilever fabrication, as it was highlighted during the first review of the Nanomass project, was the **sticktion of the cantilever** with either the driver or the substrate. During this second year of project we have tried to solve this problem. Along with these, other preliminary results coming from the other workpackages have been obtained. They are explained in this deliverable.

Deliverable 11. ***Evaluation of metal cantilevers***

Through a theoretical evaluation, it seemed that Al was the best choice of metal which could be used to fabricate metal cantilevers. The fabrication of Al cantilevers was described and the results have been shown, proving that cantilever under 500nm in width and 100nm in thickness can be fabricated on a wafer scale level.

In the future thicker cantilevers need to be fabricated. The problem is to fabricate a high aspect ratio resist mold, which can be used for lift-off. Several ideas are being pursued, such as using multi-layer resists.

Characterization of the cantilevers revealed that the Q-factor is poor, which is probably due to bad clamping of the cantilever. This is seen in the light that the cantilever was actuated in

vertical resonance, which was the original idea of the device. Actuating the cantilever laterally should increase the Q-factor, but this still needs to be investigated.

Finally, preliminary mass measurements have shown that these 100nm thick cantilevers have a very high mass sensitivity, which proves that Al cantilevers can compete with Si.

Deliverable 12. ***Periodic progress report of second year***

During this second year of the Project, the main results of the Nanomass II project have been: (i) the electrical characterisation of a resonating nanocantilever defined by Electron Beam Lithography on a CMOS integrated circuit, (ii) the integration of CMOS circuits on the SOI wafers using the bulk Si as substrate for the CMOS , (iii) the development of stamps for nanoimprinting lithography on CMOS (layouts for required dimensions, widths around 100 nm, and alignment capabilities for the CMOS pre-processed wafers).

Deliverable 13. ***Functional evaluation for Demonstrator 1***

In this report the experiments and results to evaluate the functional performance of the sensors under different environmental conditions and for several applications are presented. The experiments have been performed with the Polysilicon cantilevers fabricated on pre-processed CMOS circuits. The electrical excitation and read-out have been performed with the on-chip integrated circuitry. In the first part of the report the characterization of the performance of the sensor under different electrical and environmental conditions are described. In the second part of the report we will describe the experiments on mass detection performed to demonstrate the ability of the Nanomass sensors to detect mass in the atto-femtogram range.

Deliverable 14. ***Circuit electrical characterization of CMOS on SOI substrates***

In this report the electrical characterization of the CMOS test structures and of the read-out circuits of the CMOS process on SOI substrates are presented. The process flow for the nanoareas fabrication have been previously described in Deliverable 2 "*CMOS technology definition for SOI substrates*" and the first results of the compatibilization of the CMOS layers on the SOI substrate and the definition of the sensors have been described in Deliverable 10 (annex 4) "*Fabrication of sensor using SOI substrates"*.

Deliverable 17. ***Combination CMOS with Nanoimprint lithography (NIL)***

Several methods have been shown to be able to produce cantilever structures on CMOS chips i.e. EBL, AFM lithography and laser lithography. However, these are all serial and this would be a considerable limitation for industry production. NIL is inherently a parallel process. The objective here is to show that is possible to use nanoimprint lithography on a pre-processed CMOS chip. The stamp processing with fused silica, the alignment between the stamp and the CMOS and the imprinting process itself are explained in this deliverable. As a conclusion it can be stated that each process step works individually and that the limiting process right now is stamp manufacturing. It takes a long time to make a stamp and the success rate is low.

Deliverable 18. ***Demonstrator sensor 2***

In this deliverable, it is reported the integration of the silicon nanocantilever with the CMOS circuitry on a SOI wafer. The approach to obtain silicon nanocantilevers is to fabricate cantilevers on crystalline silicon using the SOI layer of the wafer as the structural layer and the CMOS integrated circuitry placed on the bulk silicon of the same wafer, as a usual standard run.

In this report, first a short reference of the SOI nanoarea fabrication process is included. Then the characteristics of the resonator nanofabrication are shown. Third problems due to an unexpected short-circuit between the nanoarea electrodes are analyzed and solved. Although the final sensor has been fabricated this one can not be presented as the demonstrator because of the short circuit between electrodes. In this deliverable the origin of these short-circuits will be explained and a solution will be proposed and proved. A new set of sensors without short circuits is under fabrication.

Deliverable 22. ***Report on industrialization***

In this report three main aspects were discussed: first results relevant for industrialization; second, a route to industrialization (which includes a Technology roadmap for the combination of nano-processing with CMOS) and third, the industrial collaborations established and derived from the Nanomass project.

Deliverable 23. ***Periodic Progress Report of third year***

During this third year of the Project, the main objective of the project has been achieved. A functional characterization of nanocantilevers integrated with CMOS circuit operating as mass sensors have been characterized. A mass resolution of 3 ag/Hz has been obtained with a a 20 μm long, 500 nm wide and 600 nm thick polysilicon cantilever fabricated on a post-processed CMOS substrate by EBL and laser lithography. The measurement has been performed in air, and a glycerine bead has been used as deposited mass. With this result, we have proved the functionality of the Nanomass approach in which a nanoresonator is electrically excited and its movement is electrically characterized with a dedicated CMOS read-out circuit integrated monolithically with the resonator.

Next the main activities developed within this third year of the Nanomass II project are summarized:

- Fabrication of polysilicon and silicon nanocantilevers on CMOS substrates using low energy exposed EBL combined with direct write laser lithography on resist
- Electrical characterisation of resonating polysilicon nanocantilevers defined on CMOS substrates with the integrated read-out circuit
- Study of the compatibility of the EBL processing with the CMOS fabrication according to the Nanomass approach
- Definition of cantilevers on the CMOS substrates by NIL using quartz stamps.
- Establishment of a methodology for a controllable mass deposition on the cantilevers through latex beads in air
- Development of a specific gas chamber for functionalization of the cantilevers and the electrical characterization of the change of resonance “in situ”

5.2 References

Articles

[1] G. Abadal, Z.J. Davis, B. Helbo, X. Borrisé, R. Ruiz, A. Boisen, F. Campabadal, J. Esteve, E.Figueras, F.Pérez-Murano, N. Barniol
Electromechanical model of a resonating nano-cantilever based sensor for high resolution and high sensitivity mass detection
Nanotechnology. Vol 12, pp 100-104. (2001).

[2] Authors: Nanomass consortium.
Nanomass project: smart NEMS system for high sensitivity mass detection
Phantoms Newsletter, July/September 2002, issues 7/8, Pp. 4-8 (2002).

[3] Z.J.Davis, G.Abadal, B.Helbo, O.Hansen, F.Campabadal, F.Pérez-Murano, J.Esteve, E.Figueras, J.Verd, N.Barniol, A.Boisen
Monolithic integration of mass sensing nano-cantilevers with CMOS circuitry
Sensors and Actuators A, Volume 105, pp. 311-319, (2003).

[4] G.Abadal, Z.J.Davis, X.Borrisé, O.Hansen, A.Boisen, N.Barniol, F.Pérez-Murano, F.Serra.
Atomic Force Microscope characterization of a resonating nanocantilever.
Ultramicroscopy, vol 97/1-4 pp 127 - 133, (2003)

[5] Z.J.Davis, G.Abadal, O.Hansen, X.Borrisé, N.Barniol, F.Pérez-Murano, A.Boisen
AFM lithography of aluminium for fabrication of nanomechanical systems
Ultramicroscopy, vol 97/1-4 pp 467 - 472, (2003)

[6] F. Pérez-Murano, C. Martín, H. Kuramochi, H. Yokoyama, N. Barniol, J.A. Dagata.
Measuring electrical current during scanning probe oxidation.
Applied Physics Letters, Volume 82 (18): 3086-3088 (2003)

[7] S. G. Nilsson, E.-L. Sarwe, and L. Montelius, "Fabrication and mechanical characterization of ultrashort nanocantilevers", Appl. Phys. Lett. 83, 990, (2003).

[8] S. G. Nilsson, X. Borrisé, and L. Montelius, "Size effect on Young's modulus of thin chromium cantilevers", Appl. Phys. Lett. To be published October 18 (2004).

[9] E Forsén, S G Nilsson, P Carlberg, G Abadal, F Pérez-Murano, J Esteve, J Montserrat, E Figueras, F Campabadal, J Verd, L Montelius, N Barniol and A Boisen, "Fabrication of cantilever based mass sensors integrated with CMOS using direct write laser lithography on resist", Nanotechnology 15 (2004) 628-633

[10] E. Forsén, Z. Davis, M. Dong, S.G. Nilsson, L. Montelius and A. Boisen, "Dry release of suspended nanostructures", Microelectronic Engineering 73–74 (2004) 487–490

[11] E. Forsen, P. Carlberg, L. Montelius and A. Boisen, "Laser lithography on resist bi-layer for nanoelectromechanical systems prototyping", Microelectronic Engineering 73–74 (2004) 491–495

[12] Ramona Mateiu, Zachary Davis, Dorte N. Madsen, Kristian Mulhave, Peter Boggild, Anne-Marie Rassmusen, M. Brorson, Claus J.H. Jacobsen, Anja Boisen,"An approach to a multi walled carbon nanotube based mass sensor", Microelectronic Engineering 73–74 (2004) 670–674

[13] M.Villarroya, F.Pérez-Murano, C.Martín, Z.Davis, A.Boisen, J.Esteve, E.Figueras, J,Montserrat, N.Barniol. "AFM lithography for the definition of nanometre scale gaps: application to the fabrication of cantilever-based sensor with electrochemical current detection". Nanotechnology, 15, pp. 771-776, (2004).

[14] J. Teva, G. Abadal, Z.J. Davis, J. Verd, X. Borrisé, A. Boisen, F. Pérez-Murano, N. Barniol
On the electromechanical modelling of a resonating nano-cantilever based transducer.
Ultramicroscopy, 100, pp. 225-232, (2004)

[15] J.Verd, G.Abadal, J.Teva, M.Villarroya, A.Uranga, X.Borrisé, F.Campabadal, J.Esteve, E.Figueras, F.Pérez-Murano, Z.Davis, E.Forsen, A.Boisen, N.Barniol.
Design, fabrication and characterization of a sub-microelectromechanical resonator with monolithically integrated CMOS readout circuit . IEEE Journal of Microelectromechanical Systems (accepted, to be published in 2005)

[16] S. Ghatnekar-Nilsson, E. Forsén, G. Abadal, J. Verd, N. Barniol, F. Pérez.Murano, J. Esteve, A. Boisen, L. Montelius, *Resonators with integrated CMOS circuitry for mass sensing applications, fabricated with electron beam lithography.* Accepted for publication in Nanotechnology.

Conferences

G.Abadal, F.Pérez-Murano, Z.Davis, B.Helbo ,X.Borrisé, A.Boisen, O.Hansen, N.Barniol
Non-linear static and dynamic behaviour of an electrostatically excited nanocantilever: electrical modelization and AFM characterization.
9th MEL-ARI/NID Workshop. Catania (Italy), 6-8 febrero 2001.

Z. J. Davis, G. Abadal, B. Helbo, O. Hansen, F. Campabadal, F. Pérez-Murano, J. Esteve, E. Figueras, R. Ruiz, N. Barniol, A. Boisen
High mass and spatial resolution mass sensor based on resonating nano-cantilevers integrated with cmos circuitry
11th International Conference on Solid State Sensors and Actuators & XV Eurosensors Transducers'01&Eurosensors. Munich (Alemania), 10-14 Junio 2001

F. Pérez-Murano, N. Barniol, G. Abadal, A. Boisen, Z. J. Davis, J. Esteve, F. Campabadal, E. Figueras
NANOMASS: Towards a smart mass nanosensor.
8th MELARI/NID workshop. Wuzburg (Alemania). 4-6 Julio 2001.

Z. J. Davis, G. Abadal, B. Helbo, O. Hansen, F. Campabadal, F. Pérez-Murano, J. Esteve, E. Figueras, J. Verd, N. Barniol, A. Boisen
High mass and spatial resolution mass sensor based on resonating nano-cantilevers integrated with CMOS circuitry
SPM'01 International conference. Vancouver (Canadá). 15-20 Julio 2001.

G.Abadal, Z.J.Davis, B.Helbo, , A.Boisen, J.Verd, F.Pérez-Murano, N.Barniol, F.Campabadal, J.Esteve, E.Figueras.
Fabrication of a complete nanoelectromechanical system for mass detection with atto-gram resolution through a CMOS compatible micro-nanotechnology process.
Micro & Nano Engineering MNE'2001. Pp. 80-81. Grenoble (France). 16-19 September 2001.

G.Abadal, N.Barniol, X.Borrisé, F.pérez-Murano, R.Ruiz, J.Verd, A.Boisen, Z.Davis, B.Helbo, O.Hansen, F.Campabadal, J.Esteve, E.Figueras, L.Fonseca.
A mass sensor with attogram sensitivity using resonating nanocantilevers
1st PHANTOMS (IST-Nanoelectronics Network) Workshop. pp. 40-41. Grenoble. (France). 20-21 September 2001.

E.Figueras, F.Campabadal, F. Pérez-Murano, J. Esteve, Z. J. Davis, G. Abadal, B. Helbo, O. Hansen, N. Barniol and A. Boisen
Polysilicon layer for cmos-compatible nanoresonators
Microscopy, Barcelona 2001. 3-7 September 2001.

M.Villarroya, E.Figueras, J.Esteve, F.Campabadal, F.Pérez-Murano, N.Barniol
Compatibilization of nanoprocessing with CMOS circuitry on SOI substrate for NEMS applications.
10th MEL-ARI/NID Workshop. Helsinky (Finland), 1-3 July 2002.

J.Verd, M.Villarroya, G.Abadal, X.Borrisé, F.Pérez-Murano, N.Barniol.
CMOS circuitry for on-chip read-out of a resonating nanometer-scale cantilever
XVII Conference on Design of Circuits and Integrated Systems. DCIS'02. Santander (España), 19-22 de November 2002.

N.Barniol, G.Abadal, X.Borrisé, F.Pérez-Murano, J.Verd, M.Villarroya, Z.Davis, A.Boisen, F.Campabadal, E.Figueras, J.Esteve, J.Montserrat, S.G.Nilson, I.Maximov, E-L.Sarwe, L.Montelius.
A mass sensor with attogram resolution using resonating nanocantilevers
7th International Conference on nanometer-scale science an technology + 21st European Conference on Surface Science, Nano-7/ECOSS21. Pp. 58. Malmö (Suecia), 24-28 de Junio 2002.

N.Barniol, G.Abadal, X.Borrisé, F.Pérez-Murano, J.Verd, M.Villarroya, Z.Davis, A.Boisen, F.Campabadal, E.Figueras, J.Esteve, J.Montserrat, S.G.Nilson, I.Maximov, E-L.Sarwe, L.Montelius.
Nanoelectromechanical system for ultra high sensitivity mass detection
Trends in Nanotechnology, TNT'2002. Celebrado en Santiago de Compostela (España) 9-13 de September 2002.

F.Pérez-Murano, N.Barniol, G.Abadal, X.Borrisé, J.Verd, M.Villarroya, Z.Davis, A.Boisen, F.Campabadal, E.Figueras, J.Esteve, J.Montserrat, S.G.Nilsson, I.Maximov, E-L-Sarwe, L.Montelius
Nanoelectromechanical system for high sensitivity mass detection.
Micro- and Nanoengineering International Conference, MNE'2002. p. 270-271. Lugano (Switzerland) 16-19 de september 2002.

F.Pérez-Murano, Z.Davis, J.Montserrat, G.Abadal, X.Borrisé, O.Hansen, A.Boisen, N.Barniol
Nanopatterning by AFM nano-oxidation of thin aluminum layers as a tool for the prototyping of nanoelectromechanical systems.
Micro- and Nanoengineering International Conference, MNE'2002. p. 272-273. Lugano (Switzerland) 16-19 de september 2002.

Z.Davis, G.Abadal, E.Forsen, O.Hansen, F.Campabadal, E.Figueras, J.Esteve, J.Verd, F.Pérez-Murano, X.Borrisé, S.G.Nilsson, I.Maximov, L.Montelius, N.Barniol, A.Boisen.
Nanocantilever based mass sensor integrated with CMOS circuitry
The 12th International Conference on Solid-State Sensors, Actuators and Microsystems, Transducers'03. Boston, Massachussets (EEUU). 8-12 junio de 2003.

J.Teva, G.Abadal, X.Jordà, X.Borrisé, Z.Davis, N.Barniol
Resonating cantilever mass sensor with mechanical on-plane excitation
SPIE's First International Symposium on Microtechnologies ofr the New Millenium 2003. Mas Palomas (Gran Canaria), Spain. 19-21 de mayo 2003

J.Teva, G.Abadal, Z.Davis, J.Verd, X.Borrisé, A.Boisen, F.Pérez-Murano, N.Barniol
On the electromechanical modelling of a resonating nano-cantilever based mass-sensor
Oxford 2003: Scanning Probe Microscopy, Sensors and Nanostructures. Oxford (Inglaterra), del 23 al 26 de mayo de 2003.

J.Teva, G.Abadal, Z.Davis, X.Borrisé, A.Boisen, F.Pérez-Murano, N.Barniol
Electromechanical model validation of a resonating nano-cantilever based mass sensor.
12th MEL-ARI/NID Workshop. Cork (Ireland). 23-25 junio de 2003.

J.Teva, G. Abadal, Z. Davis , J. Verd, X. Borrisé, A. Boisen, F. Pérez-Murano, N. Barniol
Electromechanical model of an AFM-characterized resonating nano-scale cantilever
Trends in Nanotechnology TNT'2003, Salamanca (España) 15-19 september 2003.

M.Villarroya, F. Pérez-Murano, C.Martín, Z.Davis, A.Boisen, J. Esteve, E.Figueras, J.Montserrat, N. Barniol.
Cantilever-based-sensor with electrochemical current detection
Trends in Nanotechnology TNT'2003, Salamanca (España) 15-19 september 2003.

M.Villarroya, F. Pérez-Murano, C.Martín, Z.Davis, A.Boisen, J. Esteve, E.Figueras, J.Montserrat, N. Barniol.
Cantilever based biosensor for electrochemical detection using AFM lithography to define nanometric electrodes separation.
Micro- and Nanoengineering International Conference, MNE'2003. Cambridge (United Kingdom). 22-25 September 2003.

E. Forsén, P. Carlberg, L. Montelius and A. Boisen, "*NEMS prototyping using laser lithography*", Proceeding of MNE 2003, p 310-311 (Cambridge, UK, 2003)

E. Forsén, Z. Davis, M. Dong, S.G. Nilsson, L. Montelius and A. Boisen, "*Dry release of suspended nanostructures*", Proceeding of MNE 2003, p 312-313 (Cambridge, UK, 2003)

E. Forsén, P. Carlberg, L. Montelius and Anja Boisen, "*Lift-Off by Local Laser Lithography for Stamp Manufacturing*", Proceeding of NNT 2003, p25 (Boston, US, 2003)

Ramona Mateiu, Zachary Davis, Dorte N. Madsen, Kristian Mølhave, Peter Bøggild, Anne-Marie Rassmusen, M. Brorson, Claus J.H. Jacobsen, Anja Boisen,"*An approach to a multi walled carbon nanotube based mass sensor*", Proceeding of MNE 2003, pp. 26-27 (Cambridge, UK, 2003)

P. Carlberg, S. G. Nilsson, X. Borrisé, L. Montelius, *"Nanoimprint lithography defined cantilevers for integration on CMOS chips",* Micro- and Nanoengineering International Conference, MNE'2003. Cambridge (United Kingdom). 22-25 September 2003.

P. Carlberg, S. G. Nilsson, L. Montelius, *"Nanoimprint lithography defined cantilevers for integration on CMOS chips",* Conference on Nanoimprint and Nanoprint Technology, Boston MA USA, 3-5 December 2003.

M.Villarroya, E. Figueras, F. Pérez-Murano, F. Campabadal, J. Esteve, N. Barniol
SOI-Silicon as structural layer for NEMS applications
SPIE's First International Symposium on Microtechnologies of the New Millenium 2003. Mas Palomas (Gran Canaria), Spain. 19-21 may 2003

Jordi Teva, Cristina Martín, Gabriel Abadal, Francesc Pérez-Murano, Núria Barniol[1]
Characterization of silicon cantilevers for nanosensing applications
First Workshop of Nanospain. San Sebastian (Spain). March 2004

Esko Forsén, Sara G Nilsson, Gabriel Abadal, Francesc Pérez-Murano, Jaume Esteve, Josep Montserrat, Eduard Figueras, Francesca Campabadal, Jaume Verd, Lars Montelius, Nuria Barniol and Anja Boisen
Electron beam lithography based fabrication of nanocantilever mass sensors systems on pre-processed CMOS
Micro- and Nanoengineering International Conference, MNE'2004. Rotterdam (Netherlands). September 2004

G. Abadal, J. Teva, J. Esteve, F. Pérez-Murano, N. Barniol
A method for mass detection testing in the femto-gram range of micro/nano-cantilever based mass sensors
Micro- and Nanoengineering International Conference, MNE'2004. Rotterdam (Netherlands). September 2004

Esko Forsén, Sara G Nilsson, Gabriel Abadal, Francesc P Murano, Jaume Esteve, Josep Montserrat, Eduard Figueras, Francesca Campabadal, Jaume V Martorell, Lars Montelius, Nuria Barniol and Anja Boisen,
Nanocantilever based mass sensors integrated with CMOS"
EuroSensors, , Roma (Italy). pp 702. September 2004

E. Forsén, G. Abadal, S. G. Nilsson, J. Verd, R. Sandberg, W. Svendsen, J. Teva, F. Peréz-Murano, J. Esteve, E. Figueras, F. Campabadal, L. Montelius, N. Barniol, and A. Boisen
Fully Integrated Nanoresonator System with Attogram/Hz Mass Resolution
MEMS'2005, to be presented. January'05

6. Potential impact of project results

In this section a qualitative assessment of the project achievements and the potential impact of the project results in a collective way are presented. The section has been divided in several points to better emphasize the potential impact. In the first section the impact in the area on Nanoelectromechanical systems is addressed. In the second section the main results of the Nanomass approach for having a mass sensor device are explained. The third section is devoted to explain the new specific technological processes which have emerged during the course of the project and which can be applied to the development of other kind of micro/nano systems. Finally in section fourth some aspects concerning the circuit design for having a full system on chip composed by an electromechanical device and its read-out are addressed.

6.1 Impact in the area of Nanoelectromechanical systems (NEMS)

The main outcome of NANOMASS project is that it has been demonstrated the possibility to combine novel nanofabrication methods with standard CMOS technology. For the first time, a nanomechanical device has been integrated monolithically within a CMOS circuit, and its functional operation has been confirmed. In the framework of the project, we have been constraint to the fabrication of a mass sensor This first demonstrator should trigger that other groups (including the groups that form the NANOMASS consortium) will tackle the challenge to develop systems that combine the advantage of the nano dimensions (more sensitivity, higher operation frequency) with the possibilities of CMOS technology (mass production, signal processing).

A future application that is currently being addressed is the monolithic integration of nanomechanical resonators with CMOS circuits for developing high frequency oscillators for implementing low power consumption telecommunication systems. The gain with respect to the current solution (use of external, non integrated oscillators) will be higher Q-factors, lower power consumption and requirement of less physical space. Methods and processes developed under NANOMASS form the base to fabricate these systems. Other foreseeable applications will be in the field of (bio)chemical sensors and smart AFM probes.

6.2 Noteworthy results as mass sensor device

Next table quantitatively describes the best values for the different parameters that characterize the performance of the devices fabricated during the course of the project.

In the operation as a mass sensing device, the following partial aspects have been demonstrated, which were not obvious at the beginning of the project:

1. Electrostatic excitation and capacitive read-out is a powerful method to implement a resonant mass sensor device, with subsequent advantages as density of integration, easiness to implement and spatial resolution.
2. Integration of the cantilever with the CMOS circuit allows to use capacitive detection because of the reduction in the parasitic capacitance
3. Sensitivity in the attogram regime has been demonstrated. Even better mass sensitivity is expected to be obtained at lower operation pressures.

4. High quality factors (25.000) for the resonating cantilevers can be achieved, even with the same polysilicon than the one used for the CMOS circuit fabrication as the structural material of the cantilever
5. Simultaneous detection of the oscillation of the cantilever from an array of cantilevers has been achieved.

Parameter	**Experimental value obtained**	**Expected in near future**
Sensitivity	3 ag/Hz (in air)	1 ag or better. (lower pressure, smaller cantilever)
Q factor	5.000 (0.4 mbar)	In progress testing the Quality Factor at lower pressure
Smaller dimensions for CMOS integrated cantilever	Length = 20 μm Width = 200 nm Thickness 600 nm	Length = 10 μm Width = 100 nm Thickness 600 nm
Smaller dimensions for CMOS integrated cantilever with electrical read-out	Length = 20 μm Width = 300 nm Thickness 600 nm	Length = 10 μm Width = 100 nm Thickness 600 nm
Number of cantilevers per array	8	16
Resonant frequency	1.5 MHz	10 MHz (with sub-micron CMOS technologies)

At present, the most employed devices to detect small quantities of mass are the quartz microbalances. State-of-the-art mass sensitivity for a quartz microbalance is 10^{-10} gr/cm^2. NANOMASS sensors are more sensitive in terms of absolute mass detection and almost as sensitive in terms of mass detection per unit area:

Assuming a **punctual mass detection at the end of the cantilever**:

	l (μm)	**t (μm)**	**w (μm)**	**Sensitivity (gr/Hz)**
NANOMASS SENSOR	20	0.6	0.42	$3\ 10^{-18}$
QUARTZ MICROBALANCE				Non applicable

Assuming **distributed mass detection along all the cantilever** :

	l (μm)	**t (μm)**	**w (μm)**	**Sensitivity (gr/Hz)**
NANOMASS SENSOR	20	0.6	0.42	$1.1 \cdot 10^{-10}$
NANOMASS SENSOR	4	0.6	0.4	$2.4 \cdot 10^{-11}$
QUARTZ MICROBALANCE				10^{-10}

For the mass detection per unit area, Nanomass sensor has the additional advantage of larger integration and on chip signal processing that would allow multiple detections and differential reading which can improve the functionality of the system. In addition, Nanomass strategy can be further exploited in the future by reducing the dimensions and using higher resonance frequency which would leed to higher sensitivity.

6.3 Technology development

A bunch of new specific technological processes have emerged during the course of the project, most of which can be applied to the development of other kind of micro/nano systems.

Two approaches have been tested for combining the fabrication of nanomechanical devices with the fabrication of the CMOS circuits. Each of the approaches have certain features that deserve to be highlighted.

Approach 1:
Use of standard layer of the CMOS circuit as the structural layer of the cantilever

- The area where the cantilever is going to be fabricated ('nanoarea') is defined during the fabrication of the CMOS circuit
- When using the CNM-CMOS technology, the cantilever is fabricated using the lower polysilicon layer
- The 'nanoarea' is protected during the fabrication of the CMOS circuit with a protective layer (top polysilicon layer). This ensures to keep a good surface conditioning.
- The protective layer is enough to store and transport the chips and wafers before the definition of the cantilever (not need for extra-passivation in the nano-area)
- Roughness and polycrystalline structure of the polysilicon allows to define nanomechanical devices with sub-400 nm resolution.

Approach 2:
Use of SOI as starting wafer for the fabrication of the system

- The area where the cantilever is going to be fabricated ('nanoarea') is defined before beginning the fabrication of the CMOS circuit
- The SOI layer is the structural layer for the cantilever
- The CNM-CMOS technology is not modified, the CMOS circuit is fabricated in the lower silicon (silicon substrate of the SOI wafer)
- The 'nanoarea' is protected during the fabrication of the CMOS circuit with a protective layer (top polysilicon layer of the CMOS circuit). This ensures to keep a good surface conditioning. The protective layer is enough to store and transport the chips and wafers before the definition of the cantilever (not need for extra-passivation in the nano-area)
- Roughness and crystalline structure of the polysilicon allows to define nanomechanical devices with sub-200 nm resolution.

For both approaches, the cantilever is defined (using nanolithography methods) after finalizing the CMOS circuit fabrication (post-processing). Integrated cantilevers have been successfully defined following both approaches. At the moment of writing this report, electrical detection of the cantilever oscillation was only achieved for the polysilicon approach, due to a problem in the design of the 'nanoarea' at the SOI approach. This problem has been solved by adding an additional post-processing step. Next table summarizes advantages and disadvantages for each approach:

Approach	Advantages	Disadvantages
Polysilicon as structural layer	• Standard CMOS can be used • Easiness for contacting the cantilever with the circuit • Less processing steps	• High surface roughness limits minimum dimensions of the cantilever • Worse mechanical properties (Young modulus and Quality factor)
Crystalline silicon as structural layer	• Lower surface roughness allows to define structure with smaller features • Better mechanical properties (Young modulus and Quality factor)	• Non standard CMOS • Difficulties for contacting the CMOS circuit with the cantilever • More processing steps • More expensive

In addition, nanolithography and post-processing methods have been adapted for:

a) dealing with the requirements that the CMOS prefabrication presents (surface topography)
b) avoiding the damage of the CMOS circuit

Optimization of post-processing methods includes nanolithography for defining the width and length of the cantilever, reactive ion etching for transferring the pattern to the structural layer and under-etching of the oxide to release the cantilever. In the following, the main conclusions obtained with the different classes of nanolithographic processes are detailed, although an important effort has also been devoted to the other processes. The conclusions will be equally valid when attempting the fabrication of other sort of nanosystems.

Nanolithography Techniques

The following lithographic methods have been applied for defining the cantilevers on CMOS substrates.

Lithography	Characteristics	Polysilicon approach	SOI approach
Laser lithography	Laser lithography on thin aluminum layers. Resolution 600 nm. Not damage to CMOS circuit. Good alignment.	Yes	No
Electron-beam lithography (EBL)	Use of double e-beam resist and metal lift-off. Resolution: 200 nm. At 35 keV, good edge definition but damage to CMOS. At 3 kEV, bad edge definition but not damage to CMOS. Good alignment.	Yes	Yes
Laser on resist (DWL)	Use of laser to define holes on e-beam sensitive resist. Resolution: 800 nm. No damage to CMOS. Not enough resolution for comb capacitor. Good alignment.	Yes	No
EBL+DWL	Electron beam lithography at 3 keV plus laser on resist for edge definition. NO damage to CMOS circuit. Good alignment.	Yes	Yes

AFM + DWL	AFM nano-oxidation of thin aluminum layers. AFM defines cantilevers and driver electrode. DWL completes fabrication. NO damage to CMOS circuit. Good alignment.	No	Yes
Nanoimprint lithography (NIL)	Dedicated stamps due to nanoarea topography. Double layer NIL resists plus lift-off. Difficult alignment, but solved. Final resolution not tested. Damage to CMOS not tested.	No	Yes

After comparing the different approaches, following conclusions have been obtained:

a) Combined EBL (3 keV) +DWL provides the best fabrication performance
b) AFM lithography will provide ultimate resolution, at expenses of a very low throughput
c) NIL has a lot of potential for achieving high throughput. A complete device has not been fabricated.

6.4 Main aspects concerning CMOS circuit design and operation

The purpose of the read-out circuit is to detect the capacitive current since this is a measure of the oscillation amplitude of the cantilever, and in consequence, it will allow to obtain the frequency response of the cantilever. Electrostatic transduction in the nano-size regime needs the minimization of the parasitic capacitance since the magnitude of the current to detect is proportional to the coupling capacity between the cantilever and the driver (smaller than 10^{-18} F).

The circuit activity ha been focused to three main areas: To avoid introduction of noise by the circuit, to minimize parasitic capacitance, to amplify the signal at the resonant frequency and to manage the cantilever arrays. The design of the circuits has been based on new electromechanical models of the electrostatically driven cantilever, which have been generated within the project. Further activities of monolithic integration of nanomechanical devices within CMOS may take the know-how generated here as the starting point.

Within the course of the project, the main results in this area can be summarized as:

a) Modelization of the cantilever-driver electromechanical behavior and definition of equivalent electrical models useful for the circuit design
b) Definition of a amplification scheme based on voltage amplifiers, that provides good frequency response without adding electrical noise neither parasitic capacitance
c) Definition of methods to manage arrays of cantilevers without adding significant extra parasitic capacitance to the system.

In the Nanomass project we have designed a capacitive method to sense the cantilever oscillation. This is the best analog current-sensing method for low-noise applications. In fact, sampled or switched capacitor circuits are widely used in capacitive sensors since they are more insensitive to the parasitic capacitances, besides synchronous modulation/demodulation techniques improve the signal-to-noise ratio by means of flicker noise suppression. Nevertheless, this type of circuits is not used in applications where the sensing signal frequency is relatively

high (>100kHz). They are used commonly in DC sensors like accelerometers and they are not valid for our system.

The principle of operation of our developed read-out circuitry is based on the integration of the capacitive current by using a capacitor and measuring the resulting voltage by means of a voltage buffer circuit. This method maximises the S/N ratio since the capacitance does not introduce input-referred noise at the sense node. The noise of the read-out system is dominated by the buffer circuit.

The characteristics of the developed circuit are: a) low input capacitance achieved by using a source-follower input stage and using the intrinsic capacitance (input capacitance of the circuit, cantilever-substrate capacitance and the interconnection to the circuit) as the integration capacitor; b) gain very closed to 1 in order to minimize the Miller effect of the parasitic capacitance; c) the existence of a DC polarization point and d) capability of loading high capacitances (@30 pF) in a relative high BW (@50 MHz). This read-out system improves the sensitivity of other referenced works where the bias element becomes a limit on the detection sensitivity because the sense node capacitance is increased by this element: directly or by miller effect.

As a conclusion we can state that this new architecture constitutes a circuit improvement for being used for other sensory applications in which the reduction of parasitic capacitance and noise is a must.

7. Future outlook

NANOMASS project has demonstrated the feasibility of fabricating nanosystems based on the combination of nanomechanical devices and CMOS circuits. During the development of the project, the partners have generated a bunch of new technological processes and know-how that they aim to exploit in the future.

It is clear that within the next few years more and more efforts will be done to meet the demands envisaged from the ITRS-roadmap, .i.e. to be able to make functional circuits employing structures having dimensions in the few nm-scale. Clearly, such demands and challenges will, at least initially, be solved by integration of nanoscaled devices and/or structures together with standard CMOS-fabricated structures. In this context, our consortium has been exploring this domain, and to the best of our knowledge, it seems at present, besides our work, to be a rather unexplored field of science. This fact puts us in a beneficial position, enabling us as a consortium to become a key player if we manage to play with skill and care. Hence, this strength is also our largest challenge and as a group therefore also our weakest point since we need to keep together although the specific project is no longer active. However, some partners in Nanomass already work together in various ways in other EU-programs, such as the IP NaPa and NoE nano2life, so we do have rather good chances to keep up the relations and improving the results although no specific project is running. Likewise, we have to exercise great care when, as individual partners, we are approaching different possible companies that are longing for getting access to our expertise in the nano-CMOS hybrid world. We have to stick together in order to build our "brand" as the expert node in hybrid CMOS-nano technology, But we will only manage doing this if we all keep together. It is maybe unnecessary to point out but of course the expertise and knowledge that we have acquired as a group during these years will be of value not only in the mass sensing area but also in all other kind of semiconductor areas where a combinational approach is important.

7.1 NANOMASS follow-up in near future

In the following, some examples of the nearest steps to undertake are described:

1. The experience acquired from the results obtained in the NANOMASS project has originated the collaboration between the groups of CNM and UAB with the EPSON Company for a collaborative project for the development of new electromechanical elements for high frequency telecommunication applications. This project is fully financed by EPSON (Title of collaborative project: *R434: Towards a 434MHz Monolithic N/MEMS-CMOS Resonator*).

2. CNM is applying the combination strategy of CMOS and nanofabrication developed in NANOMASS in the framework of the FP6 Integrated project *'Emerging nanofabrication methods, (NaPa)'*. In NaPa nanostencil lithography is explored as an alternative to nanoimprint lithography for the parallel patterning approach.

3. Also in NaPa, Nanomass sensors are expected to be used in characterizing metal deposition through nanostencil.

4. The four partners have agreed to continue a collaborative work within the next months to perform more experiments of mass sensitivity or technology.

7.2 Technology roadmap for the combination of nano-processing with CMOS

As a result of the experience gained during the course of the NANOMASS project, a technological roadmap that addresses critical aspects of the combination between nanofabrication and CMOS has been issued (detailed in *deliverable 22, Report to industrialization*), which is summarized below

a. Use of standards layers of CMOS technology

Using standard layers of the CMOS technology has the following benefits:

- It allows the monolithically integration of the nanomechanical device
- It simplifies the interconnection of the nanomechanical device with the CMOS circuit
- The developments can be exported to different CMOS technologies
- Cheapest approach when mass production is required

However, it presents also some difficulties/drawbacks:

- Properties of the structural layers of the nanomechanical devices may not be the optimal (not the best material, not the best thickness)
- Patterning and processing of the mechanical structure is usually more difficult when it is integrated in a CMOS circuit

Two alternatives to the use of standard CMOS layers exist: i) deposition of additional layers but keeping monolithic integration, ii) hybrid integration, i.e., separated fabrication of nanomechanical devices and CMOS circuit, and afterward interconnection. Both approaches have advantages and disadvantages compared to NANOMASS approach, which are summarized in the following table:

Approach	Advantages	Disadvantages
NANOMASS: Standard CMOS layers	- Monolithically integration - Simplifies interconnection - Easily exportable - Cheapest approach for mass production	- Not the best material properties for the structural layer - Difficult post-processing
Deposition of additional layers	- Monolithical integration - Better materials properties	- Difficult interconnection - Difficult post-processing - More expensive
Heterogeneous	- Better materials properties	- Difficult interconnection (specially

integration	- Easier fabrication of nanomechanical device - More flexibility for combination	to avoid parasitic capacitance) - More expensive

In conclusion, for industrialization, the use of standard CMOS layers is the preferred approach when the materials properties of these layers are good enough for the applications. This can not be the case when very high resonance frequency is needed. Then, our suggestion would be:

i) To use heterogeneous integration when parasitic capacitances are not critical. (as it is explored for example by IBM in the Millipede project)

ii) Deposition of additional layers/materials (for example, piezoelectric materials or carbon nanotubes). In this case, an additional effort is required for the interconnection with the CMOS circuit. Both approaches are currently under exploration: CNM for piezoelectric materials and MIC for carbon nanotubes.

b. Use of other CMOS technologies

During the NANOMASS project, the CMOS technology employed was the CNM-CMOS technology. The reason to choose this technology was that it was available 'in-house', and it was very convenient for experimentation: cost of the processes was not very high, and the CMOS process could be slightly modified to improve the structural layers. However, the CNM CMOS technology will not be adequate for many future applications when higher resonance frequencies are required.

Advanced sub-micronic CMOS technologies would allow to pattern the nanomechanical device simultaneously to the fabrication of the CMOS circuit. This would be an advantage in terms of throughput and fabrication. In order to corroborate this assumption, some prototypes have been fabricated using a 0.35 microns CMOS technology from Austria Microsystems (AMS). As preliminary results metal cantilevers (600 nm width, 925 nm thick and 10 mm length and natural resonant frequencies of 5 MHz) have been excited and measured with the integrated read-out circuitry.

c. Nanopatterning methods

During the Nanomass project, the following lithography methods for the definition of the cantilever have been checked: AFM lithography, laser lithography, electron-beam lithography and Nanoimprint lithography. AFM lithography and laser lithography are at present not feasible to use for industrial applications because of its extremely low throughput. In the following table, we present advantages and disadvantages of the other two methods together with UV optical lithography.

Method	**Characteristics**			**Problems**
	Resolution	**Throughput**	**Mask Cost**	
UV Optical lithography	400 nm	Several wafer/ hour	Low	Low resolution
e-beam lithography (High energy)	200 nm	Several chips / hour	N/A	Damage of CMOS circuits
e-beam lithography (low energy)	400 nm	Several chips / hour	N/A	Bad definition of edges requires combination with other techniques
Nanoimprint lithography	100 nm	Several wafers / hour	Medium	Topography of circuit

In consequence, industrialization feasibility should rely on UV optical lithography for cases where lateral dimensions of the mechanical structures are not below 400 nm. EUV lithography could allow obtaining lower dimensions, but with a very high cost of mask fabrication. For smaller dimensions, Nanoimprint Lithography is adequate.

d. Additional post-processing

The technology for the additional post-processing is solved in a chip basis. However it implies an increase of cost. Wafer based post-processing should be developed and characterized in terms of reliability and cost.

When evaluating the additional cost due to post-processing, assuming a wafer based post-processing and chip providing to final users, at least the following processes have to be added after the nanolithography:

- Reactive ion etching (except if the mechanical device is defined during the CMOS process)
- Under-etching for release of the mechanical structure
- Dicing
- Anti sticking layer / functionalization (depending on the application)
- Packaging

Packaging has not been addressed during the development of the project because it will be application dependent.

7.3 Mass sensing applications

Functional testing of the devices is still underway at the moment of writing the present report. However, a set of applications areas has been defined, as it is described in the table below:

Area	Example of application	Description	NANOMASS pros and cons
Mapping a spatial distributions of molecules or atoms (in vacuum)	Evaporation systems (metal, molecular, MBE)	Detection of small flux of atoms or molecules under vacuum conditions. Operation as a local mass sensor	Nanomass presents better sensitivity, nanometer spatial resolution and easiness to implement arrays spatially distributed sensors
	Atom beam lithography		
Vaccum/environmental detector	Gas detection Vacuum detection	By detecting the outgassing or absorption of molecules (using appropriated coating layers), the vacuum could be measured with high sensitivity. Alternatively, use as a gas detector for ultrahigh sensitivity measurements (artificial nose)	Expected sensitivity better than existing gas and vacuum detectors.
			Functionalization of the cantilevers is difficult and it has not been addressed yet
Bio(chemical) sensing	DNA chips Biochemical analysis	The sensitivity of the device is high enough to study **single**	Very good sensitivity Arrays easy to implement

	Environmental analysis	**molecular** interactions. The cantilever needs to be functionalized with an appropriate ‘detector film’,	Liquid operation is not possible. Functionalization of the cantilevers is difficult and it has not been addressed yet.