

1-1-2018

Doped And Chemically Transformed Transition Metal Dichalcogenides (tmdcs) For Two-Dimensional (2d) Electronics

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**DOPED AND CHEMICALLY TRANSFORMED TRANSITION METAL
DICALCOGENIDES (TMDCS) FOR TWO-DIMENSIONAL (2D)
ELECTRONICS**

by

SAGAR PRASAD PAUDEL

DISSERTATION

Submitted to the Graduate School

of Wayne State University,

Detroit, Michigan

in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

2018

MAJOR: PHYSICS

Approved By:

Advisor

Date

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2018

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DEDICATION

Dedicated to my parents

JivaNath Padhya and Numala Kumari Sharma.

ACKNOWLEDGEMENTS

A lot of people helped and motivated me in my PhD journey. I would like to express my deepest gratitude to all the people who helped and inspired me directly and indirectly in this journey.

I want to thank Wayne State University, Department of Physics & Astronomy for providing me an opportunity to join the department. It is my good fortune to get an opportunity to work with Dr. Zhixian Zhou. I would like to thank him for his expertise guidance, unlimited patience and generous help. I am thankful to Late Prof. Gaven Lawes for giving me a chance to join his lab. Unfortunately, he is no more with us, but the lesson he taught, guidance he provided in short period of time is lifelong lesson for me.

My sincere thank goes to the dissertation committee members: Dr. Boris Nadgorny, Dr. Ashis Mukhopadhyay and Dr. Mark Ming- Cheng Cheng for their highly advice and help. I am grateful to all the teachers who taught me and helped me to understand the fundamentals of physics. I would also like to thank Prof. Ratna Naik and Prof. Jogindra Wadehra for guidance and help.

It is impossible to list name of all the people who have given me help, encouragement, advice and well wishes during this period. I wish to express my sincere thanks to all my friends who help me directly or indirectly to achieve my goal. Special thank goes to Dr. Bhim Chamlagain, Dr. Madusanka Perera, Dr. Hsun Jen Chuang (Ben) for helping me in lab during my starting days. I would like to thank Dr. Qingsong Cui, Mr. Bill Funk and Mr. Dan Durisin from ECE for the help during this journey. I am also thankful to friends Prakash Thapa, Ramesh Tripathi, Ek Adhikari, Nabin Poudyal, Niraj Shrestha, Shiva Pokhrel, Shambhu Pokhrel, Gobin Acharya, Sushil pageni and my current lab mates Arthur, Kraig and Upendra.

Last but not the least, I would like to dedicate this work to my parents who always stood by me in every run of life. I would be nowhere without their support and belief in me. I am grateful to my wife Meena for her support, patience and motivation and to my son Suyog, who brought a lot of happiness in our life.

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LIST OF ABBREVIATIONS

TMDC: Transition Metal Dichalcogenide

2D: Two-dimensional

FET: Field-Effect Transistor

h-BN: hexagonal Boron Nitride

SiO₂: Silicon dioxide

Al₂O₃: Aluminum oxide

TaS₂: Tantalum di-sulfide

TiS₂: Titanium di-sulfide

Ta₂O₅: Tantalum pentoxide

TiO₂: Titanium dioxide

MoS₂: Molybdenum di-sulfide

MoSe₂: Molybdenum di-selenide

HfO₂: Hafnium oxide

HfSe₂: Hafnium di-selenide

WSe₂: Tungsten di-selenide

BP: Black phosphorus

Si: silicon

SEM: Scanning electron microscope

AFM: Atomic force microscope

CVD: Chemical vapor deposition

ALD: Atomic layer deposition

NPGS: Nano patterning generation system

PMMA: Polymethyl methacrylate

vdW: van der Waals

HSQ: Hydrogen silsesquioxane

IPA: Isopropanol

DFT: Density functional theory

STM: Scanning tunneling microscope

STS: Scanning tunneling spectroscopy

MIBK: Methyl isobutylketone

MEK: Methyl ethyl ketone

SS: Subthreshold swing

PDMS: Poly-dimethylsiloxane

RT: room temperature

MIT: Metal insulator transition

SB: Schottky barrier

CMOS: Complementary metal-oxide semiconductor

XPS: X-ray photoelectron spectroscopy

EDS: Energy dispersive spectroscopy

UHV: ultra-high vacuum

BTBT: Band to band tunneling

SCTD: Surface Charge Transfer Doping

CHAPTER 1: INTRODUCTION

In 1904, Jon Ambrose Fleming invented the first Vacuum tube that worked as a rectifier to convert AC into DC current, which marked the beginning of the age of electronics. In 1907, Lee De Forest invented the triode, consisting of two electrodes - anode & cathode and one control grid to amplify weak signals. The cathode was heated, to generate the electrons and the control grid was used to control the flow of electrons to the anode. Thus, the output of the tube could be controlled by the grid current. The first computer was made up of these vacuum tubes. However, these vacuum tubes were not efficient as electronic switches. The vacuum tubes were big in size, needed large amount of the power and gave off large amount of heat. The search for the alternatives of these vacuum tubes led the world towards the modern age of electronics. With the invention of Silicon based transistors, the world witnessed the huge progress in the field of electronics. In 1954, first Silicon transistor was developed at Bell laboratories by controlling the doping of single Silicon crystal while grown from molten Silicon¹. In 1955, the doping process was refined by using diffusion of donor and acceptor impurities in single Silicon crystal². The continuous process of improvement and development is going on until the present. After the invention of Silicon chip in the late 1950s, the number of transistors in a chip has doubled almost every 18 months³. Now, a microprocessor can contain more than two billion transistors. The performance of the chip has been improved with less power consumption and reduced cost. This became possible because of the scalability of Si-based transistor alongside the improvement in speed and energy consumption. These benefits led to the rise of personal computers and mobile computing technologies such as laptops, smart phones etc. However, the scaling down of Si transistor cannot go indefinitely. Transistors are already so small, further shrinking them would compromise the performance of the device. As the traditional scaling of Si transistors is about to reach its limit, suitable alternative

candidate is required to carry the progress of electronics further. In this regard, atomically thin two-dimensional (2D) materials are sought as a post-silicon alternative. These 2D materials exhibit excellent electronic and optoelectronic properties, mechanical flexibility and stability^{4–8}. Furthermore, these 2D materials have wide range of applications from Electronics, Optoelectronics, Spintronics, Valleytronics to bio-sensors.

1.1 Two Dimensional (2D) Materials

Two dimensional materials received significant attention because of their atomically thin nature, which makes the scaling possible without giving rise to the detrimental short channel effects. Furthermore, these materials provide an unique platform for several interesting features like exquisite valley physics, excitonic effects, strain induced phase transition effects, efficient quantum mechanical tunneling etc⁹. Since the successful isolation and study of the Graphene¹⁰, 2D materials have attracted a lot of interest. Two dimensional materials is even projected as a post-silicon alternative⁴. In two dimensional layered materials, the electrons in a plane are bounded by strong covalent force, whereas, the layers are connected by weak inter layer van der Waals (vdW) force. This weak vdW force enables the mechanical exfoliation of atomically thin sheets and allows for the formation of different heterostructures vdW assembly. The absence of dangling bonds ensures the high-quality interface and low charge traps across the interface. Graphene is the most studied 2D material.

1.1.1 Graphene

Graphene is a monolayer chain of carbon, packed into hexagonal honeycomb lattice (shown in figure 1.1). The covalent bond within a plane is strong, while the different layers are held together by weak vdW force. Graphene has high mobility ($>50,000 \text{ cm}^2/\text{Vs}$ at room temperature^{11,12}) and is thermally stable. It has wide area of applications from electronics, spintronics to

bio-sensing. But, the absence of intrinsic band gap overshadowed its high mobility and small quantum capacitance^{13–15}. Due to the absence of band gap, it is not possible to use graphene in logic devices where the device must act like a switch. Due to the zero-band gap, we cannot get low off current to consider it as an off state. Engineering a band gap in Graphene suffered by severe mobility degradation, or required high bias voltages^{16,17}. This limitation of the graphene encouraged the scientific community to look for other two-dimensional materials, which have nearly graphene like properties along with an intrinsic band gap.

1.1.2 Transition Metal Dichalcogenides (TMDCs)

Besides Graphene, a group of 2D materials called Transition metal Dichalcogenides (TMDCs) have been studied heavily, because of the graphene like properties alongside the inherent bandgap they possess. TMDCs offer inherent band gap with good electronic properties, mechanical flexibility, and chemical & thermal stability. TMDCs have layered structure in the form MX_2 , where M refers to metal (eg. Mo, W, Re, Ta, Ti etc.) and X, the chalcogen (eg. S, Se, Te). MX_2 crystals are hexagonally packed with stacking layers of X-M-X. TMDCs possess strong covalent bonds between metal and chalcogen atoms within a layer and those layers are held together by weak vdW force. TMDCs possess dangling bond free surface which helps to minimize the performance degradation due to interface states¹⁸. Recent studies showed the wide area of application of TMDCs for low energy devices, digital electronics & optoelectronics^{19–21}. A lot of studies have done, which resulted in theories for electron-phonon scattering in TMDCs like MoS_2 and WS_2 . Also, strongly correlated electron phenomena such as charge density waves and superconductivity was explored for group V TMDCs like TaS_2 , NbSe_2 ²². TMDCs based on Groups V and VI metals (eg. V, Nb, Ta, Cr, Mo, W etc.) are the most heavily studied due to the diverse permutations of stable compounds and electronic behavior²³. Furthermore, TMDCs can be prepared at the wafer

scale using different deposition techniques like CVD, ALD etc. This increases the practical application prospect of the TMDCs²⁴.

1.1.2.1 Semi-conducting TMDCs

The high charge carrier mobilities and presence of inherent band gap that enables large switching ratios in field-effect transistors (FETs) have made semiconducting TMDCs, specifically MoS₂, WS₂, and WSe₂ attractive materials for electronic devices^{4,19,25,26}. Furthermore, successful large-scale growth and the stability increase their prospects for practical applications. TMDCs possess indirect band gap at bulk state, but the band gap converts to the direct in monolayer limit. This indirect to direct bandgap conversion is important especially in optoelectronic applications like light emitting diode (LED). TMDCs also represent an interesting platform for fundamental studies of light-matter interactions, optoelectronics, and nano-photonics²⁷⁻³¹. Figure 1.2 shows the hexagonal structure of TMDCs. Figure 1.2b gives the top view of the structure.

1.1.2.1.1 MoS₂

MoS₂ is the most studied 2D TMDCs material. MoS₂ is found in nature and is used as a lubricant because of its lubricating property. MoS₂ has three different structural phases: i) 2H-phase, which has hexagonal symmetry and semiconducting properties, ii) 1T-phase having tetragonal symmetry and metallic properties and iii) 3R-phased MoS₂ with rhombohedral symmetry which has semiconducting properties like 2H-phased MoS₂.

Semiconducting MoS₂ has indirect band gap with 1.2 eV in bulk state that changes into the direct band gap of 1.8 eV in monolayer due to quantum confinement⁵. Monolayer MoS₂ FET showed the mobility in the range of 0.1-10 cm²V⁻¹s⁻¹^{32,33}. But, the phonon-scattering room-temperature mobility for bulk MoS₂ was reported 200-500 cm²V⁻¹s⁻¹³⁴. With HfO₂ as high K dielectric for the top gate the mobility of the MoS₂ was found to be about 200 cm²V⁻¹s⁻¹³².

1.1.2.2 Metallic TMDCs

Layered sulfides of Group IV (i.e., Ti, Hf, and Zr) also possess interesting semi-metallic and semiconducting behavior, but they suffer from a high propensity for non-stoichiometric structure due to the low energy barriers for intercalation of metal atoms. Group V and VII TMDCs are mostly studied for many-body phenomena such as 1T TaS₂ for gate-tunable charge density waves and 1T' ReS₂ for linear anisotropy in electrical and optical properties^{5,23,32,35–37}.

Unlike semi-conducting TMDCs, metallic TMDCs are prone to oxidation in presence of air. TMDCs like TaS₂, TiS₂, HfS₂, HfSe₂ surface reacts to air and displace the chalcogenide atoms with oxygen atoms at the atom sites to form oxides. This property of these TMDCs is particularly useful to form atomically flat two-dimensional High K dielectrics.

1.1.3 Transport Properties and Device applications of TMDCs

Transport properties of 2D semiconductor shows wide variation depending up on the materials, type of charge carriers and dielectric used. Studies showed the exceptional electronic properties of graphene based on the unique band structure including the observation of ambipolar behavior and high mobility exceeding $15000\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ at room temperature with ballistic transport, and shows quantum Hall effect^{10,38}. In case of MoS₂, the mobility values of monolayer and multilayer MoS₂ devices on SiO₂ reported by multiple groups were substantially below the Hall mobility of bulk MoS₂ ($100 - 200\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)^{32,39,40}. Bao et. al. reported ambipolar multilayer MoS₂ with two terminal field-effect mobility attained to $470\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ at room temperature on PMMA⁴¹. S. L. Li et.al. presented thickness dependent interfacial charge scattering of MoS₂ FET and showed the improvement of field effect mobility with increase of thickness by suppressing the Coulomb scattering originated from SiO₂ surface and MoS₂ /SiO₂ interfaces⁴². Different efforts to modify the SiO₂ surface, using high-k dielectric such as HfO₂, Al₂O₃ and h-BN encapsulation have been done

for graphene and TMDCs field effect transistor but the mobility values never reached to theoretical phonon limited mobility^{12,39,43–46}, which indicates the carrier mobility of 2D channel materials is limited by extrinsic scattering from charged impurities at the channel/substrate interface and charge traps in dielectric, substrate surface roughness, and remote surface optical phonons originating from substrate.

A good transistor layer material should have high enough charge carrier mobility for on state current and fast operation of transistor. The layered materials should have reasonable band gap to maintain enough on/off current for the operation of transistor by electrostatically switching on and off state. On the other hand, sharp switching characteristic is equally important to allow high degree of electrostatic control over devices. Flexibility and transparency are also important characteristics for future electronics. Two-dimensional TMDCs such as MoS₂ and others offer an important advantage when compared with traditional bulk electronic materials: their sub-nanometer thickness. Coupled with a bandgap typically in the 1–2 eV range can result in high on/off ratios, the extreme thinness of TMDCs allows more efficient control over switching and can help to reduce short-channel effects and power dissipation. To achieve these ideal properties, selection of channel materials and dielectric materials is exceptionally important. In addition, devices structures, designs and modification are also important to optimize and modify the 2D thin layer transistor devices properties.

1.1.4 Optoelectronic Properties of TMDCs

TMDCs have indirect bandgap at multilayer structure, which converts to direct band gap in monolayer⁴⁷. This transition from indirect to direct band gap is quite important as it increases the quantum yield. The direct band gap increases the probability of electron-hole pair generation resulting in better light absorption. The band gaps of the few layered TMDCs depends on the

number of layers^{48,49}, which allows the absorption of light of different wavelengths. The stacked heterostructure of TMDCs further allows light absorption from wide range of wavelength⁵⁰. The direct band gap monolayer TMDCs exhibit unique properties like strong photoluminescence(PL)⁴⁷, high absorption in the visible range⁵¹, valley polarization^{52,53}, and strongly bound and charged excitons^{54–56}. Photodetectors made of Monolayer MoS₂ displayed strong photoresponsivity of 880 AW⁻¹⁵⁷. The built in electric field of TMDCs is useful to separate photo generated electron-hole pairs. Also, strong exciton energies have been reported for monolayer TMDCs due to the strong coulomb interactions^{54–56}.

1.1.6 Challenges of TMDCs

The channel of 2D materials is thin which needs substrate to support and for the investigation of its properties we must make electrical connections using metal electrodes. The contact metal form barrier with semiconductor channel of 2D materials and the dielectric on substrate plays important role to determine the channel properties of the thin 2D materials. To enhance the performance of MoS₂ (or in general, TMDC channel materials) MOSFET, there are several issues that needs to be resolved⁵⁸:

- Proper doping of the TMDCs
- Metal-semiconductor contact effect
- High K dielectric integration

1.1.7 Doping TMDCs

The success of conventional Si-semiconductor relies on the ability to achieve ohmic contacts through substitutional/impurity doping profiles for electron (n-type) and hole (p-type) injection respectively. The doping for conventional semiconductors is developed for years and is in excellent condition, but for 2D channel the doping method is still in early phase. In absence of

effective doping schemes, early 2D FETs relied on the use of elemental metals with different work functions for carrier injection into the respective bands of 2D channel. There has been some progress in the doping of 2D materials now. Doping in TMDCs has been realized from the impurities used for bulk crystal growth, ambient interaction with intrinsic defects, interaction with substrate impurities, adsorption of metals or charge transferring molecules^{44,59–63}. Chalcogen substitution and direct substitution of transition metal have also been demonstrated^{64,65}. Some studies doped bulk TMDCs using vapor transport methods but to get monolayers mechanical exfoliation had to be done^{66,67}. Mn doping in MoS₂ has been realized using chemical vapor deposition on inert substrate⁶⁸. Suh et al. (2014) researched niobium (Nb) doping on MoS₂ as a p-type⁶⁹. Nb atoms are doped on MoS₂ at the substitutional sites, leading to a degenerating hole density of around $3 \times 10^{19} \text{ cm}^{-3}$. Lin et al. (2014) demonstrated the doping of rhenium (Re) and gold (Au) on monolayer MoS₂ via CVT growth⁶⁶.

Some of these doping methods may be selectively apply to limited areas through lithography processes, they still may damage the channel through ion impacts. None of these methods have applied to degenerately dope the contact area of the 2D materials. Since doping happens during the growth of the crystal, it is impossible to dope selective area. But, we can use these degenerately doped 2D material along with undoped channel for various applications like *p-n* junction or 2D-2D contacts.

1.1.8 Metal-Semiconductor Contact

The main problem with TMDCs electronic devices is the contact as it often fails to form ohmic contact with the electrode metal. The mismatch in work function between TMDCs channel and the electrode metal forms a barrier at the metal semiconductor interface. With Ti (work function of 4.33 eV) as electrode metal, few layer MoS₂ shows strong electron conduction, while p-

type transport is not observed due to the formation of large Schottky barrier (SB) at the interface. In case of WSe₂ FET, ambipolar behavior is seen when contacted with Ti metal. As the fermi level of WSe₂ lies at the middle of the band gap, a relatively small SB forms for both n-type and p-type conduction allowing both n-type and p-type conduction. Fig. 1.3 shows the barrier formation at metal-semiconductor interface for MoS₂ and WSe₂ with three different metals. As shown in 1.3(a) for MoS₂-metal contact, fermi level of the metal is close to the conduction band of MoS₂ forming small barrier for electron conduction and very large barrier for hole conduction. For WSe₂, fermi level of metal lies close to the middle of the band gap forming significant barrier for both electron and hole conduction. This explains the n-type behavior of MOS₂ and ambipolar conduction in WSe₂.

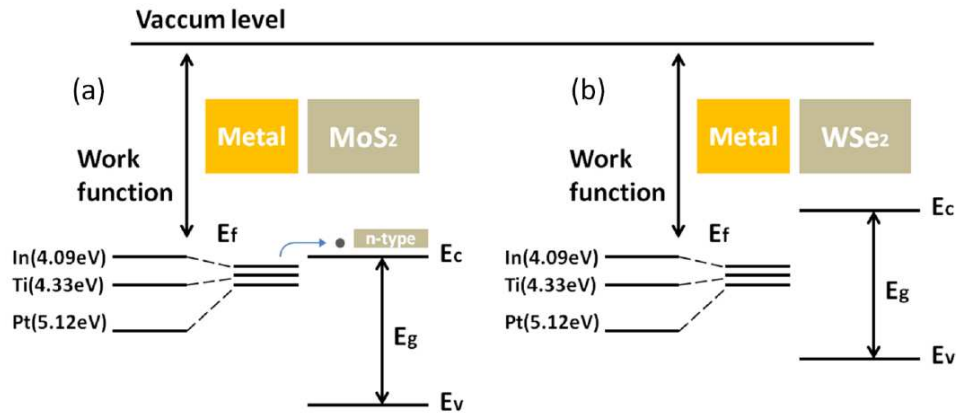


Figure 1. 1. Schematic diagram of the barrier formation at metal-semiconductor interface⁷⁰. Three metals with different work functions are shown, (a) Metal-MoS₂ interface, fermi level of the metal is close to the conduction band allowing n-type transport and (b) Metal-WSe₂ interface, fermi levels of metals are close to the middle of the band gap, forming barrier for both type of conduction.

Low resistive ohmic contacts are essential for FETs. However, semiconductors with large band gap have trouble in formation of ohmic contact with metal electrodes. There are few ways to deal with the problem. Firstly, low resistance ohmic contact can be achieved between metal and semiconductor by suitable choice of metal electrode. For n-type semiconductor like MoS₂, small

work function metal forms ohmic contact. In such case the fermi level of the metal lies close to the conduction band of the semiconductor allowing almost zero barrier. However, the work function of commonly used metal is over 4 eV (Ti, Al) or 5 eV (Pd, Ni). In addition to the small work function, the metal should highly conductive as well as thermally & chemically stable. Ca has low work function (2.9 eV) but oxidizes easily leading to degradation in performance. It is difficult to find the low work function metal satisfying the conditions. Similarly, for p-type semiconductor like WSe₂, work function of the metal should be large so that the fermi level of the metal aligns close to the valence band of the semi-conductor allowing the formation of low barrier. This is equally difficult to find such metal. Although, high work function metals made good contacts with monolayer WSe₂, SB has not been eliminated completely⁷¹. Another way to deal with the problem is to make Schottky junctions narrow, so that the tunneling current defines the contact resistance. Using large ionized impurity doping in semiconductor, the SB height can be decreased and low contact resistance can be achieved⁷². But due to the 2D nature of TMDCs, any attempt to dope it results in deterioration of channel.

1.1.9 Contact Engineering

Low resistance ohmic contacts between a metal and a semiconductor can be achieved either by a) lowering the SB height by suitable choice of contact metals or by b) degenerately doping the contact area. In subsections below, we are going to discuss both methods in detail:

1.1.9.1 Lowering Schottky Barrier height

Low work function metals like scandium (Sc) have been shown low Schottky barrier height and low resistance in MoS₂ FETs. However, because of the fermi level pinning, the range for the barrier adjustment is small and only applicable if pinning location is close to the band edge. If depinning is complete, ohmic contacts can be obtained easily for all TMDCs by selecting a metal

with the fermi level lying above the conduction band or below the valence band for *n*-type or *p*-type FETs. Although the origin of the fermi level is not understood fully, it is at least partially dependent on metal-semiconductor interactions which induce states within the bandgap near the interface^{73,74}. Thus, if an ultra-thin layer of insulator is used to separate metal and semiconductor, the insulator attenuates the metal electron wave function before penetrating the 2D semiconductor, reduces the density of induced states, which prevents fermi level to moving from charge neutrality level⁷⁵. The dipole formed at the interface also help to decrease the SB height. However, the insulator layer increases the tunneling barrier for the carrier injection. The specific contact resistivity of MoS₂ channel was found to be reduced in 2-3 orders by the insertion of 1.5 nm Ta₂O₅ layer due to the reduction in SB height from ~95meV to ~30 meV⁷⁵. But as the thickness of the insulator is increased the resistivity is also found to be increased monotonically.

Local hybridization of 2D semiconductor under metal electrodes also can provide an alternative way to ensure low resistive ohmic contacts. This can be done by using a strongly interacting metal and semi-conductor through covalent bonding. The strong covalent bonding of Mo contacts with monolayer MoS₂ has significantly reduced the SB height and improved contact resistance⁷⁵. In contrary, the covalent bonding between MoS₂ and metals like Ti, Ni etc. results in higher contact resistance⁷⁶.

Another approach to reduce SB height is by transforming the 2D semi-conductor underneath the contacts into metal by phase engineering. About 60 -70% area of monolayer MoS₂ converted from semiconducting 2H phase to metallic 1T phase on immersed in n-butyl lithium. The n-butyl lithium donates charge to MOS₂, converting it to 1T state. The 1T MoS₂ under contact forms sharp boundary with 2H channel and eliminates the SB, improving the contact resistance values as low as 200 $\Omega\mu\text{m}$ ^{77,78}.

Edge contacts are also a favorable option over top contacts for lowering SB heights because of favorable in-plane carrier injection with a high degree of covalency and small tunnel barrier^{79,80}. As each layer can form edge contact, charge can be efficiently injected deep into 2D materials. Edge contacts are beneficial for scaling purposes as well as no overlap region is required. However, the fabrication of edge contacts is not easy with current techniques.

1.1.9.2 Doping of Contacts

Although different doping methods are studied over the years to achieve low resistance ohmic contacts for 2D TMDCs material, most of these methods suffer from the lack of air or thermal stability. Furthermore, selective area doping is not possible as in the case of Si-based FETs. In Si-based devices heavy ion implantation doping of the source and drain area forms highly transparent barrier free contacts with the metal. But in case of TMDCs channel, due to the 2D nature of the material it is not possible without compromising the structural integrity of the channel. In section below, we will discuss the methods that have been used to dope the contacts for 2D TMDCs channel.

1.1.9.2.1 Ionic liquid gating

In this approach to improve the contacts of MoS₂ FETs, Ionic Liquid (IL) gating is used, which forms an electric double layer with high capacitance at MoS₂/metal interface. As a result, IL gated MoS₂ FETs demonstrate high tunneling efficiency and thus low contact resistance due to the strong band-bending occurring at MoS₂/metal interface.

1.1.9.2.2 Low resistance Graphene contacts tuned by double layer Ionic liquid

In this approach, Graphene has been used as a tunable electrode material to achieve low resistance ohmic contacts for ultrathin channel of TMDCs. Because of the large band gap of TMDCs material, large range tunability is required in order to achieve true ohmic contacts for both

n-type and *p*-type conduction. In this method, the large electric double layer (EDL) capacitance of Ionic liquid (IL) tunes the carrier density of graphene and forms low resistance contacts with the TMDC channel. An ionic liquid gate induces high carrier density in graphene in the order of 10^{14} cm^{-2} , which is an order more than using a conventional solid-state gate dielectric⁷¹.

1.1.9.2.3 2D-2D contact electrode

One of the useful advantage of 2D TMDCs is the ability to form heterostructures by stacking different materials in vdW assembly. Since TMDCs do not possess dangling bonds they form ultraclean and sharp interfaces. Thin layers of MoS_2 and WSe_2 have been stacked in vdW assembly to form atomically thin *p-n* junction^{84–87}. The built-in potential in these thin atomic *p-n* junction is dropped across vdW gap due to the absence of obvious depletion region as in the case of bulk *p-n* junctions. The charge transport across the junction is dominated by the tunneling current through the vdW gap. This results in fast charge transfer across the junction, which is verified by recent findings of strong photocurrents and quenching of photoluminescence signals in study of $\text{MoS}_2/\text{WSe}_2$ *p-n* junctions. Low resistance ohmic contacts have been observed for both electron and hole transport for WSe_2 FETs using substitutionally doped 2D contacts.

1.1.10 High K Di-electric Integration

In past few decades, we experienced a heavy reduction in dimension of electronic devices. This reduction in the size of devices is achieved by reducing the size of key components of those circuits: The 'MOSFET'. This reduction in dimension allows the integration of a large number of transistors on a chip, enabling higher speed and reduced cost. The scaling of MOSFET follows the famous Moore's Law⁸⁸. As shown in figure 2, Moore's law predicts exponential increase of transistors density on a chip.

The scaling of MOSFET results to smaller devices in smaller area, consumption of less power and decrease in cost per transistor. But, this downscaling of MOSFET cannot go forever, as it is limited by short channel effect. Short channel effect depends up on the thickness and dielectric constant of the used dielectric. Gate oxide thickness must be reduced as channel length is reduced in order to avoid short channel effects⁸⁹. As a thickness of SiO₂ gate insulators is reduced to few atomic layers, charge carriers can flow through the gate dielectric by a quantum tunneling mechanism^{90,91}. This mechanism involves the tunneling of charge carriers through a trapezoidal energy barrier⁹². It is seen that the tunneling probability increases exponentially as the thickness of SiO₂ layer decreases^{90,92}. In addition to the gate leakage current, the reduction in width of gate oxide also causes a reduction in the ON/OFF ratios⁸⁹.

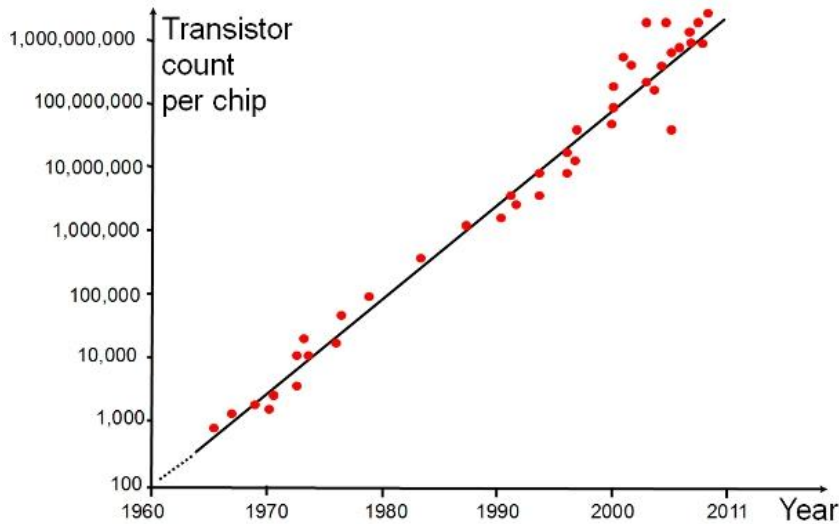


Figure 1. 2. Graphical representation of Moore's law⁹³.

During the operation of MOSFETs, charge carriers flow through the device resulting the generation of defects in SiO₂/ Si interface⁹⁴⁻⁹⁶. When a critical density of defect is reached, breakdown of the gate layer occurs, resulting in the failure of the device⁹⁷⁻⁹⁹. The SiO₂ thickness limit was found to be 2.2 nm at room temperature and 2.8 nm at 150° C^{94,97}.

1.1.11 High-K Dielectrics

The electrostatic control of the channel by the gate is achieved through capacitive coupling between the gate and channel region through the gate dielectric. Scaling requires reduction in the depth of source and drain regions by the same factor as the gate length, as this would require less control over channel. As the capacitance of the system depends inversely on the thickness of the dielectric, this can also be done by decreasing the thickness of the dielectric. The inefficiency of SiO₂ to decrease further as per device scaling required the replacement of the insulator with high K (Dielectric Strength) dielectric oxides⁹⁷, to increase its thickness and thus preventing the charge carriers from tunneling while retaining the electronic properties of SiO₂ layer. The metal oxide semiconductor structure in MOSFET acts like a parallel plate capacitor. The capacitance of the structure is given as,

$$C = \frac{A\epsilon_r\epsilon_0}{t_{ox}}$$

Where, A is the capacitor area, ϵ_r is the relative dielectric constant of the material, ϵ_0 , the permittivity of free space ($8.85 \times 10^{-12} \text{ Fm}^{-1}$), and t_{ox} is the gate oxide thickness.

As SiO₂ has approached its limit, an alternative way to increase capacitance is to use an insulator with higher relative dielectric constant than SiO₂ ($\kappa = 3.9$ for SiO₂). Then we can use the thicker gate layer and hopefully can reduce the leakage current and improve the reliability of the gate dielectric. The thickness of hig- κ dielectric is usually expressed in terms of equivalent oxide thickness (t_{eq}). The equivalent oxide thickness of a material is defined as the thickness of SiO₂ layer that would be required to achieve the same capacitance density as the high K material in consideration,

$$\frac{t_{eq}}{\epsilon_{r,SiO2}} = \frac{t_{high\kappa}}{\epsilon_{r,high\kappa}}$$

Where, $t_{\text{high } \kappa}$ and $\epsilon_{r,\text{high } \kappa}$ are the thickness and dielectric constant of high κ dielectric material. Recently, a lot of efforts have focused to investigate high- κ gate dielectrics^{98–105}. The equivalent oxide thickness is found to be 1.1 nm (for $\text{Al}_x\text{Zr}_{1-x}\text{O}_2$ layer). Also, the leakage current is reduced by several orders of magnitude. High- κ dielectric seemed to be resolving the scaling problem of SiO_2 , but the high κ dielectric material, which could replace SiO_2 as a gate dielectric should satisfy few requirements¹⁰⁶:

- thermal stability
- preventing the formation of thick interfacial low- κ dielectric layer
- low density of intrinsic defects at Si interface
- sufficient gate dielectric lifetime
- sufficiently large energy band gap, to reduce leakage current

1.1.11.1 Possible Candidates

The hexagonal boron nitride (hBN) is an excellent choice for the substrate as it is atomically smooth and have low interface traps but the low dielectric constant limited its use in form of dielectric in FET devices. There are several high- κ dielectrics, which have been studied for replacing SiO_2 . A list of dielectrics and their properties is given in table 1.1.

The most likely high κ dielectrics as a replacement of SiO_2 are zirconium dioxide (ZrO_2)¹⁰⁷, hafnium dioxide (HfO_2 ^{108,109}), aluminium oxide (Al_2O_3 ¹¹⁰), titanium dioxide (TiO_2 ¹¹¹), tantalum pentoxide (Ta_2O_5 ^{112,113}) etc. The oxide film growth of the dielectric thin films is critical as extremely reliable high quality thin dielectric films are required. Several thin film growth techniques have been used such as thermal evaporation, atomic layer deposition (ALD), chemical vapor deposition (CVD), pulsed laser deposition (PLD), and molecular beam epitaxy (MBE)^{114–118}.

Table 1 Some physical parameters of high- κ dielectrics and heterostructures with Si and Ge

Material	Dielectric constant (κ)	Band gap E_G (eV)	Band offset ΔE_C (eV) to Si	Band offset ΔE_C (eV) to Ge	Crystal structure
SiO ₂	3.9	8.9	3.2		Amorphous
Al ₂ O ₃	9	8.7	2.8	2.6 [24]	Amorphous
Si ₃ N ₄					Amorphous
TiO ₂	80–100	3.5	1.2		Tetragonal
Ta ₂ O ₅	26	4.5	1–1.5		Orthorhombic
HfO ₂	25	5.7	1.4	2.0 \pm 0.1 [25]	Monoclinic, tetragonal, cubic
ZrO ₂	25	7.8	1.5		Monoclinic, tetragonal, cubic
La ₂ O ₃	30	4.3	2.3	2.56 [24]	Hexagonal, cubic
Y ₂ O ₃	15	5.6	2.3	2.56 [24]	Cubic
Gd ₂ O ₃	24 \pm 2 [6]			2.44 [24]	
MgO	9.8 [7]	7.3 [7]			Cubic
Er ₂ O ₃	14.4 [8]	7.5 [8]	3.5 [8]		
Nd ₂ O ₃		5.8 [9]	2.2 [9]		
PrO ₂	25 [10]	3–4 [10]	>1 [10]		Cubic
CeO ₂	52 [11], 26 [12]	4.5 [12]			
LaAlO ₃	26 [13]	6.0 [10]		2.2 [24]	
ZrSiO ₄					Amorphous
HfSiO ₄				2.2 [24]	Amorphous
(Dy ₂ O ₃)	14	4.8			

Table 1. 1. List of High K dielectrics ⁸⁹

1.1.11.2 Challenges with High K Dielectric Integration of TMDCs

For the enhancement of the device, TMD as channel, the growth of conformal, uniform high K dielectric is necessary. The high K dielectric integration study so far has been based on different growth methods (CVD, ALD, PLD, MBE, etc.). With these complex growth methods, the interface has always been issue. ALD is supposed to be more reliable deposition in case of TMDs. McDonnell et. al., (2013) deposited of HfO₂ on the MoS₂ surface using Atomic layer deposition (ALD) method¹¹⁹, and found that the ALD on MoS₂ was not uniform. They could not detect covalent bonding between the HfO₂ and MoS₂. In another study, when 15-17 nm HfO₂ is deposited by ALD, island type growth was observed resulting in non-uniform films¹²⁰. In their study, Lembke et al., (2015) found that, due to the absence of out of plane covalent functional group in MoS₂, surface functionalization is needed to fabricate scaled two-dimensional layered devices using ALD⁸. The problem of high K dielectric integration of TMDCs has not been resolved yet. In

this dissertation, we will discuss a new approach to form atomically thin High K dielectric from thermal oxidation of the semi-metallic TMDCs.

1.2 Scope of the Study

This dissertation is focused on developing new methods to fabricate TMDC based 2D electronic devices such as p - n junction diodes and FETs. We can divide this work into two parts: i) 2D p - n junction diodes and ii) High K dielectric integration in 2D electronics. In first part, we fabricated 2D p - n junction diodes (homo/hetero structures) using heavily p -doped (Nb-MoS₂) and slightly n -doped (MoS₂/WSe₂) semiconducting TMDCs. Chapter 3 describes in detail the fabrication and characterization of atomically thin p - n junction diodes made from 2D TMDCs. In the second part, we developed a new approach to achieve ultrathin high K dielectric using thermal oxidation process. We chemically transformed the metallic TMDCs into their oxides, characterized them and used them as a dielectric material in FETs with semiconducting TMDCs as the channel. In Chapter 4, we successfully converted TaS₂ into Ta₂O₅ using thermal oxidation process and used as a high K dielectric in MoS₂ FETs. We followed the same method of oxidation for another metallic semiconductor in Chapter 5, where we successfully converted HfSe₂ into HfO₂ and measured the dielectric constant and the leakage current. Further characterization of chemically converted HfO₂ and its potential application in FETs is described in Future works section.

CHAPTER 2: EXPERIMENTAL METHODS

This dissertation is focused on the study of two-dimensional materials. During the period of this dissertation, we studied different devices including 2D-2D p - n junction diodes, Metal Insulator Metal junction diodes, Field effect transistors etc., based on two-dimensional semiconductors and ultrathin dielectrics converted from 2D semiconductors along with Graphene and hexagonal Boron Nitride (h-BN). We fabricated those devices and characterized to understand them. In this chapter, we will discuss in detail about the fabrication process of the devices that we studied and the techniques used to characterize them. This chapter is divided into two parts; in the first part, we will discuss about the device fabrication and in the second part we will talk about the characterization technique.

2.1 Device Fabrication

Our study mostly used the two-dimensional materials as a channel or dielectric material for the purpose of device fabrication. We used Si/SiO₂ as the substrate for device fabrication. We cleaned the substrate with Acetone, Isopropanol (IPA) and Deionized (DI) subsequently in ultrasonic bath. After cleaning, the substrate is annealed in ULVAC MILA-5000 annealing tool. We used the mechanical cleavage technique to exfoliate the few-layer samples on low residue scotch tape from the bulk sample and transferred to the substrate. After assembling the required structure of the device, we defined electrodes on the device with the help of e-beam lithography, and finally deposited metal on those electrodes to make electrical connections. The sections below will explain each step of the fabrication in detail.

2.1.1 Crystal synthesis

WSe₂, Nb-WSe₂ and Nb-MoS₂ crystals were synthesized by chemical vapour transport using iodine as the transport agent. MoS₂, Graphite and hBN crystals were purchased from manufacturers SPI Supplies and 2D semiconductor supplies. All TMDC crystals were synthesized by chemical vapour transport using iodine as a transport agent. For our study, high-quality single crystals were provided by Dr David Mandrus' group at the University of Tennessee. In case of doped samples, 0.5% of Niobium (Rhenium) was used as substituent atoms for p-doping (n-doping)⁶⁹.

2.1.2 Substrate preparation

We used degenerately doped silicon substrate with 270 nm thick oxide layer with prefabricated gold alignments, as a substrate. We first cleaned the substrate by sonicating it in acetone for 20 minutes followed by sonicating in Isopropanol (IPA) for another 20 minutes. acetone helps to remove organic polar residues, while Isopropanol helps to remove non-polar residues. Both acetone and IPA evaporates at a faster rate and in the process may redeposit remnants. In the end, we cleaned the substrate with deionized (DI) water to completely wash out those residues and then dried by the jet of inert gas (N₂/Ar). After cleaning the substrate, we examined them under optical microscope to ensure the condition of the substrate. The substrate having residue on it, or without alignment marks, or having some other problems were eliminated. The well dried substrate was then further cleaned by annealing in vacuum. Annealing of the substrate helps to remove the organic residues and moisture absorbed at the surface of the substrate from the atmosphere. We used ULVAC MILA-5000 annealing tool to anneal the substrate. The substrate were then annealed at 600° C for 10 minutes with passing forming gas for 2 minutes, when temperature of the substrate just reaches 600° C.



Figure 2. 1. ULVAC MILA-5000 annealer.

2.1.3 Sample Preparation

Two-dimensional layered materials are strongly bounded in the plane by a covalent bond, but the inter-layer attraction is weak due to the presence of long-range van der Waals force. Due to the weak interlayer attraction, the layers can be peeled off easily. We used mechanical cleavage method¹⁰ to exfoliate few layers TMDCs material on scotch tape. For this, we took a small bulk crystal of the material and peeled off the layers repeatedly for several times until we get sample thinned to few layers. We then transferred the samples to the substrate in different ways per the need. The different methods we used to transfer sample to substrates are explained below:

2.1.3.1 Exfoliation on substrate

Most of the time, we transferred the exfoliated sample on cleaned Si/SiO₂ substrate directly. We placed the substrate on the scotch tape with the alignment side of the substrate over the sample and pressed gently for few minutes. This will transfer the sample from scotch tape to the substrate. Then we examined the substrate under the optical microscope and located thin uniform samples based on colour contrast. To get the exact information about thickness and uniformity, we did AFM characterization later.

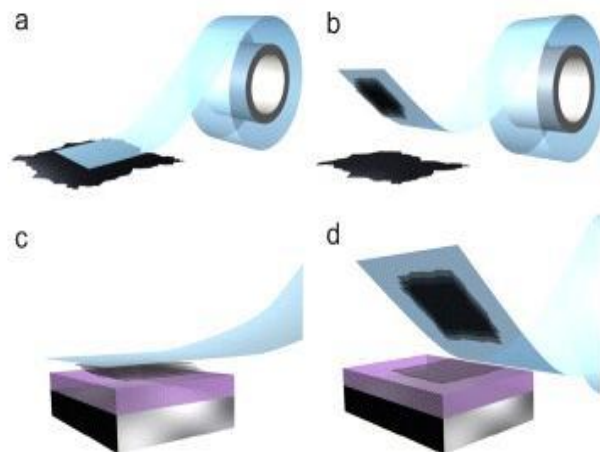


Figure 2. 2. Schematic diagram representing mechanical exfoliation of two-dimensional TMDCs sample. a) a small portion of bulk material is taken on the scotch tape b) peel off repeatedly the sample until we get few layers thick c) after getting few layers thick sample, scotch tape is stamped over the substrate and pressed uniformly for few minutes d) scotch tape is gently removed, samples are now attached to the substrate.

2.1.3.2 PDMS assisted transfer

When we need to transfer one 2D sample over another, we cannot use direct exfoliation to the substrate method. In such cases, we used PDMS assisted transfer method. PDMS is a Silicon-based organic polymer, known for its viscoelastic properties. PDMS can be used as an elastic stamp to transfer samples of nanometer dimension. The PDMS patches were prepared from SYLGARD 184 SILICONE ELASTOMER kit. It has two parts: Elastomer base, and curing agent as shown in Fig. 2.3.

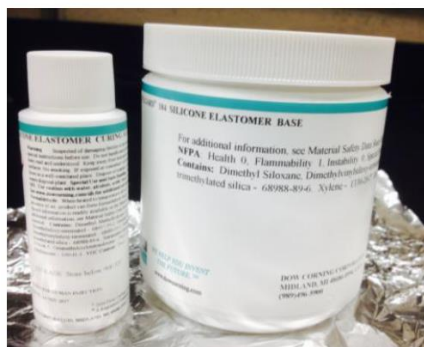


Figure 2. 3. Sylgard 184 silicone curing agent and elastomer (respectively from left to right). A mixture of these two is spin coated and baked to prepare PDMS polymer.

A mixture of 184 silicone elastomer and curing agent with the weight ratio of 10:1 is thoroughly mixed and the mixture is placed in a vacuum chamber for 20 minutes to remove air bubbles from the mixture. For one batch, we mixed 7 gm of elastomer with 0.7 gm of the curing agent. After 20 minutes in vacuum, the mixture is spin coated onto a clean polished 4 inches silicon wafer at a spin rate of 350 rpm for 35sec. The thickness of PDMS was approximately 300-500 μ m. We placed the coated wafer onto a hot plate to bake at 80°C for 30 minutes in air and left another 30 minutes to cool down¹²¹. As the PDMS patch is prepared on the wafer, we cut down the patch into small pieces for the ease of handling.

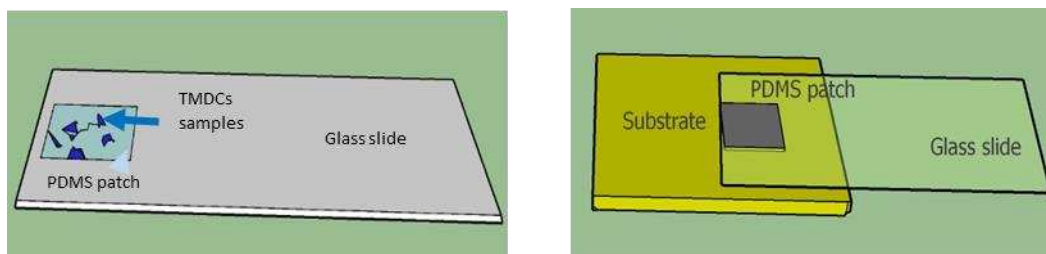


Figure 2. 4. Schematic diagram showing the process of dry transfer Sample transfer using DMS layer a) PDMS patch with the sample is put on the glass slide b) With the help of micromanipulator, the sample is transferred to the substrate.

We placed small patches of PDMS above the exfoliated layer of the sample on scotch tape, this would transfer the sample from scotch tape to the PDMS patch. We located the sample under an optical microscope and transferred to the precise location with the help of micromanipulator. After transfer, we annealed the substrate at 250° C for 30 minutes in vacuum to remove any residue introduced during the transfer and increase the attachment.

2.1.3.3 PC pickup

Another method, we extensively used for sample transfer is PC pickup method. This method enables to transfer sample which is already on the substrate, to the precise location of another substrate. This method is very useful when you needed thinner samples to transfer. Usu-

ally, the sample exfoliated on PDMS are thicker than those exfoliated on the substrate. We prepared PC solution by dissolving 0.18 gm Polycarbonate (PC) on 3 gm of Chloroform uniformly. We applied a layer of PC on the substrate and kept a patch of PDMS covering the sample containing a portion of the substrate. We carefully removed the PC layer from the substrate except the area covered by the PDMS patch. We scratched along the edge of PDMS and applied Deionized (DI) water. The substrate surface being hydrophobic, DI water helps to pick up the sample from the substrate. Then, we carefully picked up PDMS along with the PC layer containing the sample. We transferred the sample to the desired location with the help of micromanipulator. For this method, we applied heat after touching down to melt the PC layer. Then the substrate was immersed in chloroform for 10-15 minutes to remove PC layer. The substrate was then blow dried with inert gas jet and annealed at 250° C for 30 minutes in vacuum.

2.1.4 Thermal Oxidation

Some of our projects are based on the thermal oxidation of TMDCs material. We used the heating method to oxidize TaS₂ (HfSe₂). We heated the TaS₂ (HfSe₂) of different thickness for a different period. We monitored the change in colour contrast and thickness of the sample. After few trials, we realized, for TaS₂ (HfSe₂) heating at 300° C for 3 hours is sufficient to convert it to oxide. We exfoliated sample on the substrate and located them with the help of an optical microscope. We heated the substrate with the sample in it to 300° C for 3 hours in ambient condition. The sample was characterized by AFM before and after heating. Figure 2.5 shows an optical image of the sample before and after heating. Figure 2.5a shows the TaS₂ sample immediately after exfoliation. The sample is then heated on a hot plate for 3 hours at 300° C. Figure 2.5b is the image of the same sample after oxidation. Significant change in color contrast of the sample is seen due to the phase change of the sample. This fact is supported by TEM, XPS characterization as well.

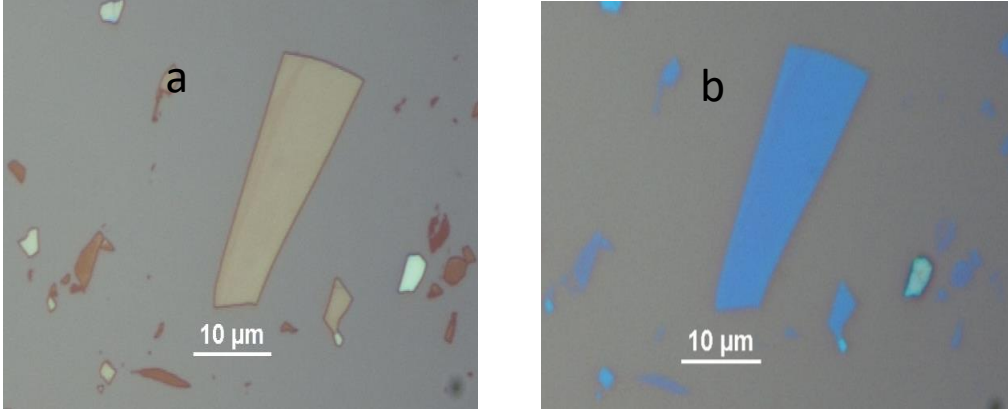


Figure 2. 5. Thermal oxidation of TaS₂. a) TaS₂ sample immediately after exfoliation b) Thermally oxidized TaS₂ after heating on a hot plate at 300° C for 3 hours.

2.1.5 Electrode Fabrication

To measure the electrical properties of the device, we fabricated the electrodes on the sample to make electric connections. The fabrication process involves several steps: coating resist, designing electrodes, printing those designs on the resist, removing resist from the selective area, metal deposition and finally lift off metal from the area except the electrodes. These steps are explained in detail below:

2.1.5.1 PMMA coating

Polymethyl methacrylate (PMMA) is a polymeric material that is commonly used for various imaging and non-imaging microelectronic applications. It is used as a positive resist for e-beam lithography. Upon exposed with an electron beam, the polymer chain will be broken. That broken chain will be easily dissolved in developer solution exposing the area to deposit metal on. In this way, we can selectively choose the area and deposit metal for electrode fabrication. The substrate was spin-coated with 2 layers of 495A4 PMMA followed by a single layer of 950A2 PMMA at 4500 rpm. Each coating layer was followed by baking the substrate on a hot plate at 180° C for 5 minutes. The thickness of 3 layers of PMMA was 360 nm.

2.1.5.2 Electrode design and E-beam lithography

We used Nano-pattern generation system (NPGS) AUTOCAD software to draw the electrode pattern that needed to write on the sample. With the help of the optical image, we defined the area of the sample, to be written electrode upon. We used the graph, generated using NPGS, to write electrodes on the substrate by e-beam lithography. E-beam lithography uses an electron beam to write a specific pattern on the substrate as directed by the design provided. Although e-beam lithography system is slow and little costly, it has already been commonly used in semiconductor industry for patterning a smaller feature size. The dedicated e-beam lithography instruments are expensive. Alternatively, SEM with dedicated e-beam writing column provides the solution at moderate pricing. Figure 2.6 shows the SEM system with the dedicated e-beam writing column attached to it.

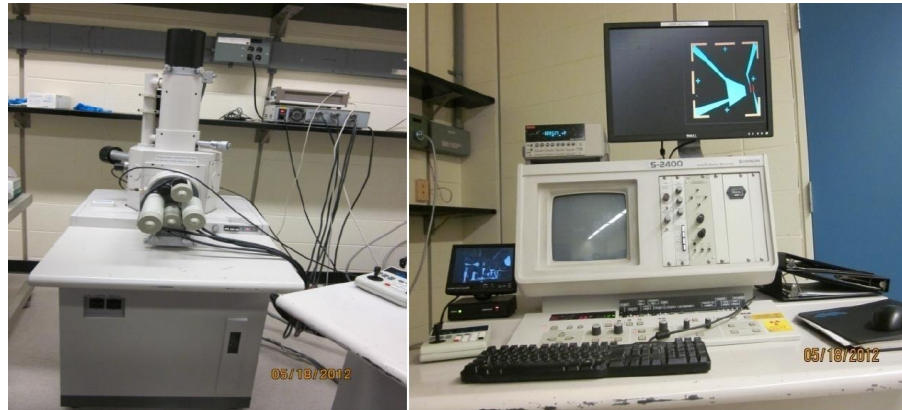


Figure 2. 6. Hitachi S-2400 Scanning Electron Microscope attached with E-beam writing column. It has the maximum accelerating voltage of 25 KV.

We used Hitachi S-2400 SEM system equipped with dedicated e-beam writing column to write the lithography patterns. In an SEM, a highly focused beam of electrons emitting from an electron gun travels through a vacuum and are guided by electromagnetic lenses. The electrons beam hit the substrate surface coated by polymer and interact with it to break its bond. The polymer area which is interacted with electrons beam is easily soluble in organic solvent. We optimized the

SEM by adjusting beam current, fine focus with minimizing astigmatism of the focused electron beam and aligning the alignment marks on the substrate. We used the area dose of $350 \mu\text{C}/\text{cm}^2$ and line dose $15 \mu\text{C}/\text{cm}$ to write the pattern. When electron beam hits a certain area of the substrate, the polymer chain of the PMMA covering that area will be broken, which reacts with the developer solution and dissolves in the solution exposing the area. After e-beam writing is done, the substrate was dipped in MIBK/MEK developer solution for 1 minute to dissolve the broken loose PMMA particles and open the specific design electrodes. Figure 2.7 shows the e-beam pattern written on a substrate.

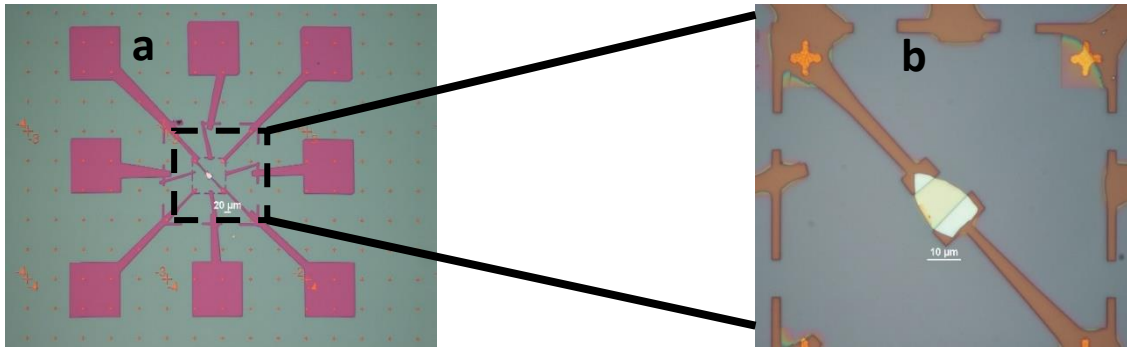


Figure 2. 7. Optical image of a device showing e-beam pattern a) at 10X magnification b) at 100X magnification. The pattern was developed in MIBK/MKE developer solution for 1 minute after e-beam writing.

2.1.5.3 Metal Deposition

We used BJD-1800 metal evaporator (shown in figure 2.8) to evaporate the metals to tailor the electrodes. The substrate was adjusted horizontally in BJD chamber. The chamber pumped down to the pressure of $\sim 10^{-6}$ torr and deposited metal electrodes with sufficient slow deposition rate. The metal deposition was done by evaporating the metal normal to the substrate without rotation for easy lift-off. E-beam with proper frequency and current to hit the targets metals (contained in crucible) and get the metal evaporated to deposited on the target areas. For the electrodes, we deposited 5 nm of Ti followed by 45 nm of Au at the deposition rate of $1 \text{ \AA}/\text{sec}$.



Figure 2. 8. BJD 1800 e-beam metal evaporator.

2.1.5.4 Lift-off

During metal deposition, the whole area of the substrate will be covered with the metal, so we should remove the metal from all the area except the electrodes before characterizing the device. This process is called lift-off. For lift-off, the substrate would be dipped in acetone. Acetone reacts with the PMMA layer and dissolves it. The bottom layer of PMMA easily dissolves in acetone than the upper layer making it easy for Acetone to undercut the metal deposited in the unnecessary area and make it free to float. In short time all metal except deposited on the pattern created by e-beam would be removed. Figure 2.9 shows the optical image of a device after lift-off.

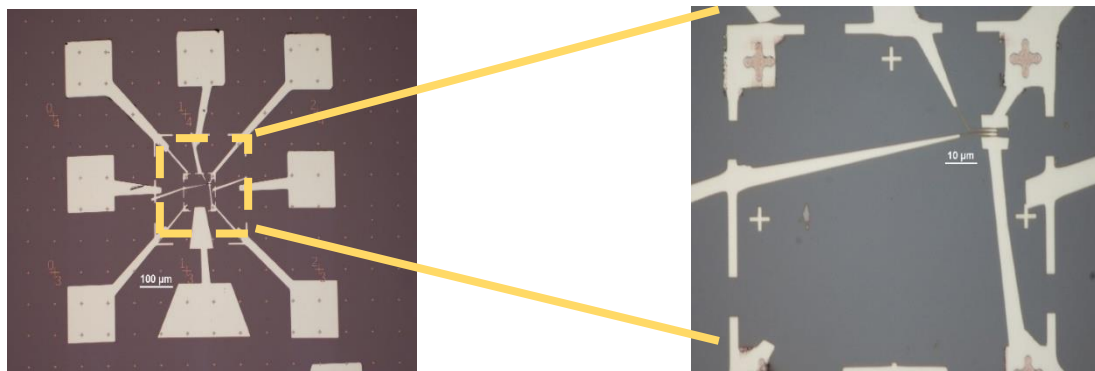


Figure 2. 9. Optical image of a device after lift-off. The substrate was dipped in acetone for 5-10 minutes to lift-off the metal

Figure 2.10 shows the flowchart of the whole process of the electrode fabrication.

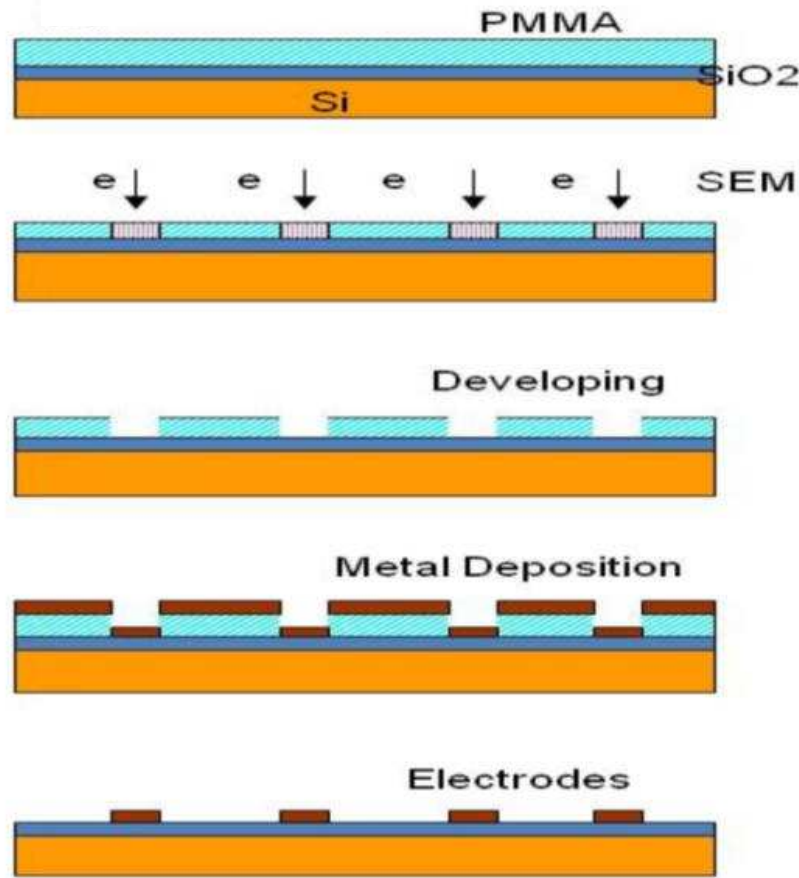


Figure 2. 10. Flowchart of the electrode fabrication. a) 2/3 layers of PMMA spin coating followed by baking at 180°C for 5 minutes after each layer coating, b) writing pattern on the substrate using electron-beam, c) developing the lithography pattern by dipping the substrate in the developer solution. The cut-out parts are the pattern designed to deposit metal on to form the electrodes, d) depositing Ti/Au:5nm/45nm on the substrate, e) removing the metal from all the area except the electrodes by dipping the substrate in acetone.

2.2 Characterization Techniques

In order to study the various characteristics of the two-dimensional TMDCs material, we used different characterization tools. Initially, we used Optical and Atomic Force Microscope to get the information about their shape, size and topography. We fabricated the devices of those materials and then carried out the Electrical characterization. In this section, we will discuss in detail about the characterization techniques we used in this work.

2.2.1 Optical microscope

An optical microscope uses visible light to magnify objects for observation. It uses a small and spherical objective lens which has a shorter focal length and another longer focal length lens called eyepiece. The object is placed near to objective lens and observes through the eyepiece. The microscope brings an object's image into focus at a close distance within the tube by objective lens and eyepiece magnifies the image. Aside from a light source, a microscope also has a condenser which focuses light from the source to a small, bright spot of the specimen. It has fixed eyepieces and interchangeable objective lenses with different magnification. It can magnify incredibly small areas or object when the objective lenses are changed from flat with low magnification lenses to rounder with high magnification ones. The image quality seen by using an optical microscope is assessed based on brightness, resolution and contrast. The optical microscope shows different contrast for different thickness 2D materials. The TMDs flake and other 2D flakes transfer on the substrate is observed under optical microscope to identify rough thickness of the better flakes. The optical microscope is used to estimate the thickness and identify the cleanness and uniformity of the sample.



Figure 2. 11. Optical microscope

2.2.2 Atomic Force Microscope (AFM)

AFM is a kind of scanning probe microscope. A sharp probe called tip is moved close to the surface of sample under study in non-contact mode. The tip is connected to a cantilever. The tip scans across the sample surface and comes into force of interactions. As the cantilever is displaced by its interactions with the surface, the reflection of the laser beam will be displaced on the surface of the photodiode and the image is constructed. The surface topography is fully determined by the interacting forces during scan. AFM can measure a roughness of a sample surface, help to determine shape & the dimensions of sample, identify atoms at a surface, evaluate an interaction between a specific atom and its neighboring atoms, distinguish change in physical properties arisen from a change in an atomic arrangement through the atomic manipulation, help to distinguish cancer cells and normal cells based on a hardness of cells, evaluate an interaction between a specific cell and its neighboring cells in a competitive culture system. The identified better sample flakes under optical microscope is characterized by noncontact mode XE-70 atomic force microscope (AFM). The surface topography of AFM image is analysed to determine the dimensions (length, width, thickness etc.), surface cleanness and surface roughness of the identified sample. XEI image processing software is used to process the AFM image. The surface smoothness is compare by root mean square value of PSD.

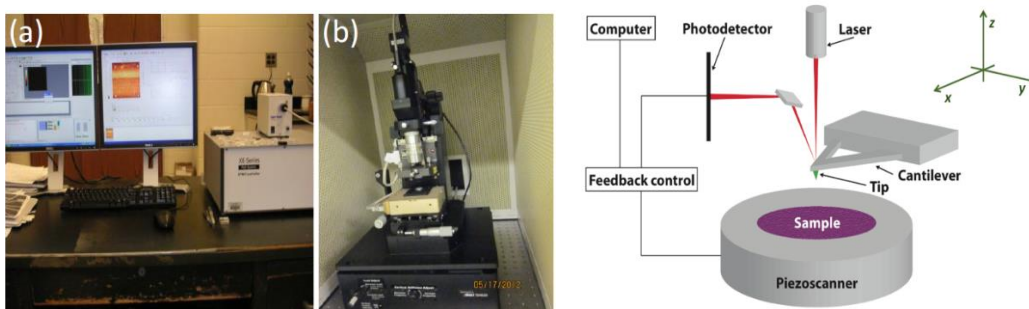


Figure 2. 12. AFM setup (a) & (b). Schematic diagram of AFM working principle.

2.2.3 Electrical Characterization

To measure the electrical properties of the device, we used Keithley 4200 Semiconductor parameter analyzer. The device after defined Ti/Au electrodes is kept in Lakeshore cryogenic probe station and pumps it overnight to reach the pressure down to $\sim 1 \times 10^{-6}$ torr. The Keithley 4200 parameter analyzer is used to characterize its electrical properties at different temperatures varying from 77K to 300 K by using liquid nitrogen. Mainly we measured the current voltage relationship and gate voltage dependence for the field effect transistors.

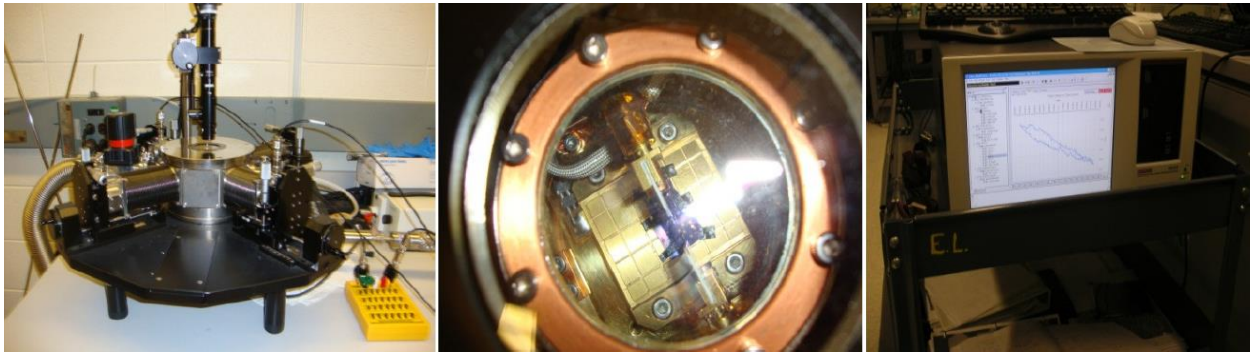


Figure 2. 13. Lakeshore cryogenic probe station for low temperature measurement system

2.2.4 Capacitance Voltage (C-V) measurement

We used HP 4284A precision LCR meter for our C-V measurements. HP 4284A precision LCR meter measures two components of the complex parameters at the same time of a measurement cycle. The primary measurement parameters are: absolute value of impedance ($|Z|$), absolute value of admittance ($|Y|$), inductance (L), capacitance (C), resistance (R), conductance (G) and the secondary measurement parameters are: dissipation factor (D), quality factor (Q), equivalent series resistance (RS), equivalent parallel resistance (RP), reactance (X), susceptance (B), phase angle (θ). The HP 4284A precision LCR meter is used to measure the capacitance of the dielectric used to fabricate devices. It has frequency range from 20 Hz to 1 MHz with different mode of measurements. MIM junction was designed by sandwiching dielectric between two metal electrodes. Capacitance was measured with sweeping the bias voltage at different frequencies level by applying

low AC system voltage (50 mV to 100 mV). The capacitance is measured in Cp:D configuration to minimize the parasitic capacitance effects. To measure the capacitance more precisely, the recorded measure value was set at least average of 8 consecutive measurements.

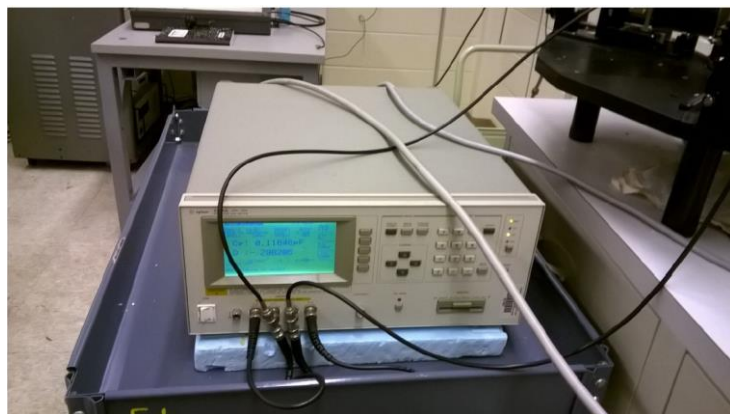


Figure 2. 14. Alignment 4284A precision LCR meter

2.2.5 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) measurement was performed using a Kratos Axis Ultra XPS system with a monochromatic Al source. The samples were mechanically exfoliated from bulk crystals right before XPS measurement and then immediately inserted into the XPS chamber to avoid oxidation. Pass energy of 20 eV with 0.1 eV scanning step was used for photoelectron detection. The C 1s reference line at the binding energy of 284.6 eV was used to calibrate the charging effect.

CHAPTER 3: GATE-TUNABLE *P-N* JUNCTIONS FORMED BETWEEN DEGENERATELY *P*-DOPED AND UNDOPED TMDCS

3.1 Background and Motivation

Semi-conductor *p-n* junctions are the basic building blocks of electronic and optoelectronic devices^{122–124}. These devices are heavily used in applications ranging from rectifying diodes, frequency mixing diodes, tunneling diodes, light emitting diodes to laser diodes^{125–127}. In conventional *p-n* junction diodes, there exists a charge-carrier depletion region on both sides of junction generating built in potential. Carrier transport across the junction occurs by the diffusion and drift processes. Recently, layered materials with strong in-plane chemical bonds and weak out-of-plane bonds have attracted much attention for Nano-electronic applications^{38,128–130}. Their excellent electronic and optoelectronic properties along with their flexibilities allow for their use in high-performance nanodevices, such as tunneling transistors¹³¹, photodetectors^{132–134}, photo responsive memory devices¹³⁵, light-emitting devices¹³⁶, and Integrated circuits^{137,138}. With the discovery of these two-dimensional material, it is now possible to fabricate a junction diode at ultimate thickness. Lack of the dangling bond on the surface of these 2D materials made it possible to create high quality heterointerfaces^{50,139}. The availability of materials with different band gaps and work functions helps for the band engineering of these stacked structures.

Heterostructures based on bulk materials have covalent bonding at the interface that pins the band offsets at the tunneling interface, irrespective of doping level or bias voltage unless an insulator is inserted between. But in case of two dimensional vdW assembly, potential can be dropped across the vdW gap, allowing the bands of the two material components of freely move with respect to each other at the junction by the applied drain voltage or electrostatic doping by the two gates¹⁴⁰. vdW assembly provides a new degree of freedom in terms of modulation of the

band structure to form atomically sharp vertically stacked heterojunction¹³¹. Recently, heterostructures based on graphene, hBN and TMDCs have been studied extensively. Studies showed the feasibility of vertical tunneling of electrons in vdW heterostructures, but due to the lack of intrinsic band gap in graphene, tunnel devices cannot be turned off. Few studies focused on MoS₂/WSe₂ heterostructures. Artificially stacked MoS₂/WSe₂ heterostructures exhibit gate controlled rectification diode behavior^{84,141}. However, these heterostructures showed the saturation in reverse bias tunneling current and forward bias current, because of the parasitic resistance of the contacts, especially for WSe₂¹⁴¹. The reverse current in these devices has been largely limited by a lateral depletion region instead of the true vertical junction because of the inadequate doping of at least one of the constituent^{69,124}. To realize the intrinsic properties of TMDC-based *p-n* junction, it is necessary to use heavily doped TMDCs to form *p-n* junctions, so that low-resistance ohmic contacts can be achieved. Electrostatic gating can be used to induce high carrier concentration in the n-type (or p-type) semiconductor forming the *p-n* junction, which unavoidably leads to the carrier depletion in p-type (or n-type) semiconductor and consequently a substantial Schottky barrier at one of the contacts. In our study, we fabricated the vdW assembly *p-n* junction consisting of degenerately *p*-doped TMDC layer and undoped MoS₂. The electron concentration in undoped MoS₂ can be modulated by a gate voltage for a large range without affecting the hole concentration in the degenerately *p*-doped TMDC layer. For homojunction structure, we used Nb-doped MoS₂ with the undoped MoS₂ and for heterostructure we used the Nb-doped Wse₂ with undoped MoS₂.

3.2 Results and Discussion

For the study of homojunction and heterojunction *p-n* junction diodes, all the samples were prepared using mechanical cleavage method¹⁰. Undoped MoS₂ crystal were purchased from SPI Supplies and Nb-doped Mos₂ and WSe₂ crystals were synthesized by chemical vapor transport

using iodine as the transport agent. 0.5% of Nb was used as substituent atoms for p-doping. The undoped MoS₂ samples were exfoliated directly on the substrate, while doped WSe₂/MoS₂ were exfoliated on PDMS and transferred using dry transfer process. For heterojunction diode, Nb-doped WSe₂ were stacked over undoped MoS₂, exfoliated on the substrate. Similarly, for homojunction diode, Nb-doped MoS₂ were stacked over undoped MoS₂. After each transfer the substrate was annealed in vacuum for 30 minutes at 250° C.

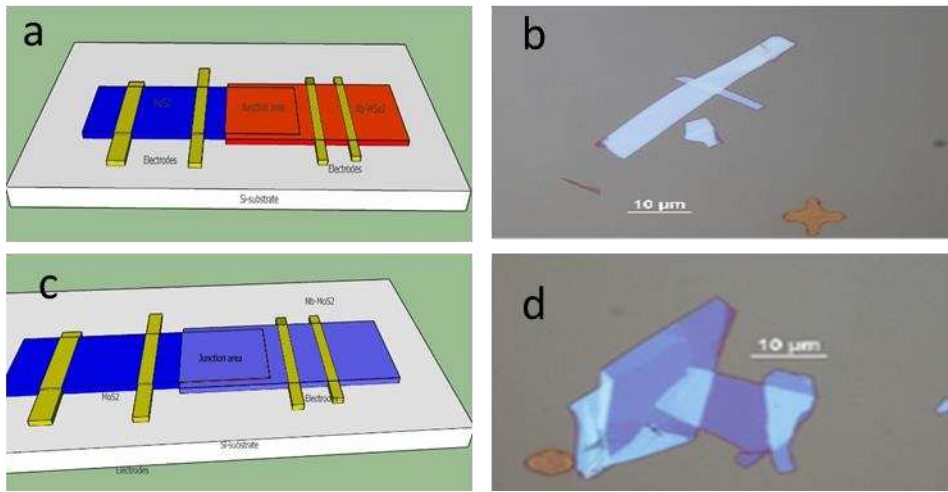


Figure 3. 1. a) Schematic diagram & b) optical micrograph of the heterojunction *p-n* junction diode, Nb-doped WSe₂ is stacked on the top of undoped MoS₂; c) Schematic diagram & d) optical micrograph of the homojunction *p-n* junction diode, Nb-doped MoS₂ is stacked on the top of undoped MoS₂. The overlap area between the doped and undoped sample constitute the *p-n* junction diode.

The samples were characterized using AFM before and after making devices and were found atomically smooth and pristine. Non-contact mode Park System XE-70 atomic force microscope (AFM) was used to study the surface characteristics of the sample.

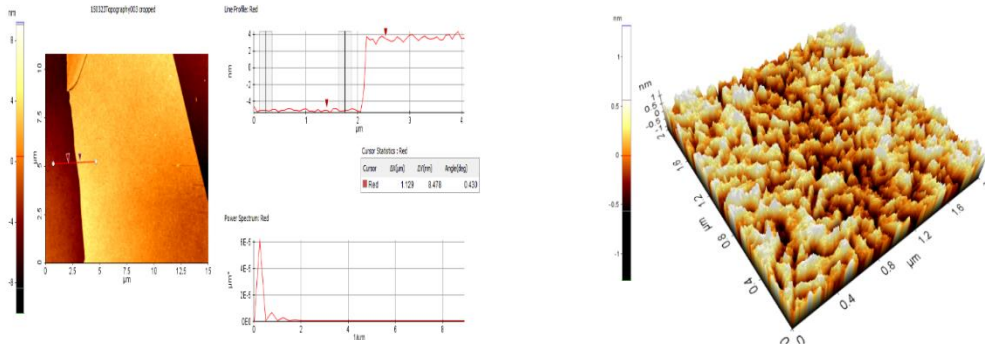


Figure 3. 2. AFM image of undoped MoS₂. a) Thickness measurement, the thickness of the sample is shown 8.5 nm, b) 3-dimensional view of the 2μm X 2μm area scan of the same sample

Figure 3.2 shows an AFM image of the undoped MoS₂ sample used to fabricate the device. The thicknesses of the samples were ranging from 6 nm to 12 nm. The peaks and dips seen in image 3.2b represent the non-uniformity present at the surface. Non-uniformities may arise due to several reasons such as presence of some residue from the scotch tape during exfoliation, residue trapped between the substrate and the sample and so on. We do annealing to remove the residue. It helps to decrease the non-uniformities but cannot eliminate it entirely. The root mean square fluctuation is seen in the order of hundreds of pm ensuring the atomic smoothness and pristine surface.

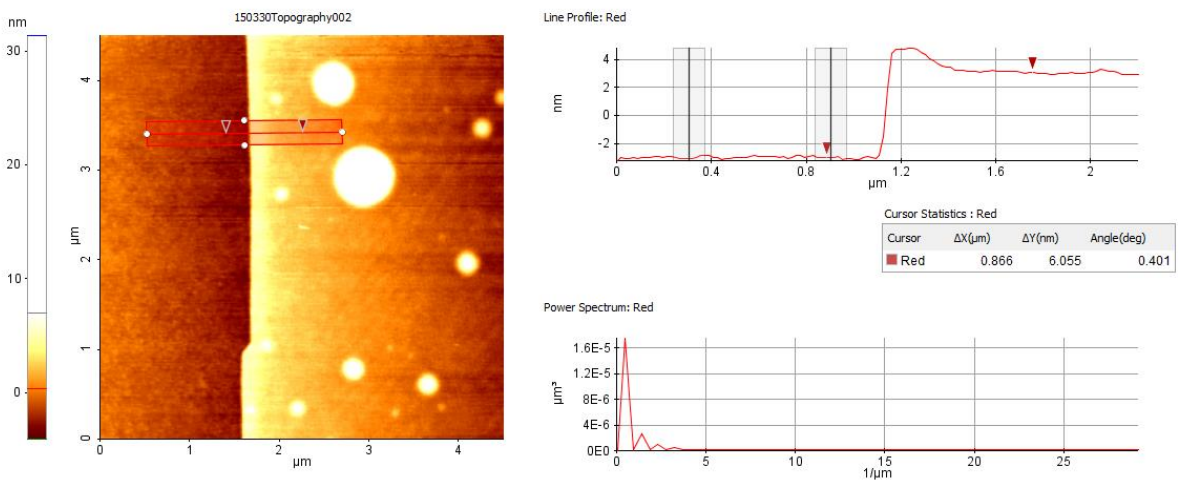


Figure 3. 3. AFM image of vertically stacked heterojunction diode.

The doped samples were stacked on the top of undoped MoS₂ using PDMS assisted dry transfer technique. After transfer, the substrate was annealed at 250° C for 30 minutes and again imaged using AFM. Figure 3.3 shows the AFM image of a vertically stacked device. We saw similar bubbles when we scanned the junctions after transfer second layer over MoS₂. Besides the bubbles, the overall junction area looks clean as seen in figure 3.3.

To measure the electric properties, electrodes were fabricated for the electrical connections. Nanometer Pattern Generation System (NPGS) was used to design the electrodes pattern. Two layers of 495-A4 and one layer of 950-A2 electron resist polymer Polymethylmethacrylate (PMMA) were spin-coated followed by 180° C baking on the hotplate for 5 mins after coating of each layer. Scanning electron microscope (Hitachi S-2400) with EBL attachment was used to write electrodes pattern. After e-beam lithography, the substrate was soaked in the mixture of MIBK and MEK for 70 seconds to develop the e-beam written electrodes. For the deposition of metal on electrodes, BJD-1800 e-beam metal evaporator was used. The substrate with electrode pattern after e-beam lithography was fixed on the hood of the metal evaporator. 5nm titanium (Ti) and 50 nm gold (Au) were deposited at ultrahigh vacuum (about 10^{-7} Torr) with deposition rate 1 \AA/s .

To measure the electrical properties, the devices were kept in cryogenic probe station (Lakeshore Cryogenic probe station) under ultrahigh vacuum ($\sim 10^{-6}$ to 10^{-7} torr). The electrical transport properties of the devices were measured by Keithley 4200 semiconductor parameter analyzer at room temperature (297 K).

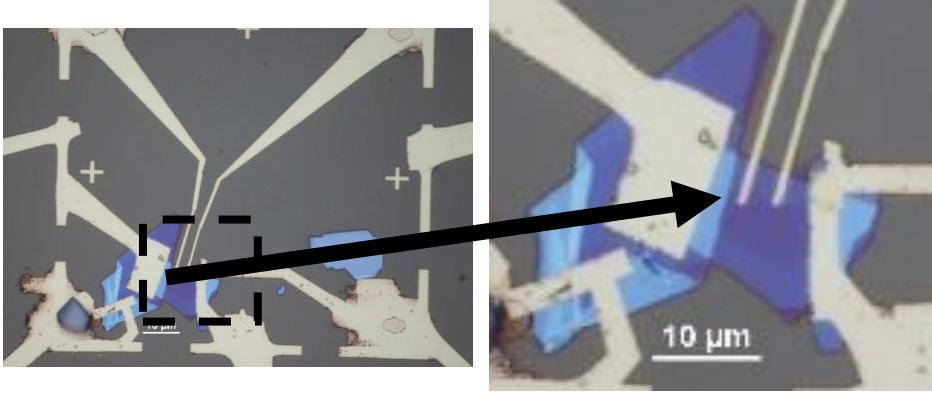


Figure 3. 4. Optical micrograph of homojunction p - n junction diode.

Figure 3.4 shows the optical micrograph of the homostructure p - n junction diode. The homo-junction structures were prepared by transferring the Nb-doped MoS₂ over undoped MoS₂. The overlap region of Nb-doped MoS₂ and undoped MoS₂ constitute the p - n junction. A pair of electrodes were fabricated on both doped and undoped samples to measure the electrical properties of respective samples separately. For the junction, drain bias was always applied to the doped MoS₂, while the undoped MoS₂ was connected to the source terminal.

The I-V measurement of the doped Nb-MoS₂ contact is shown in figure 3.5. The measurement was done by sweeping the drain voltage from 0 V to -0.1 V at back gate voltages from 0 V to -60 V at the step of 20V. The output characteristics of the Nb-doped MoS₂ show negligible gate dependence, indicating that the Nb-doped MoS₂ is degenerately doped.

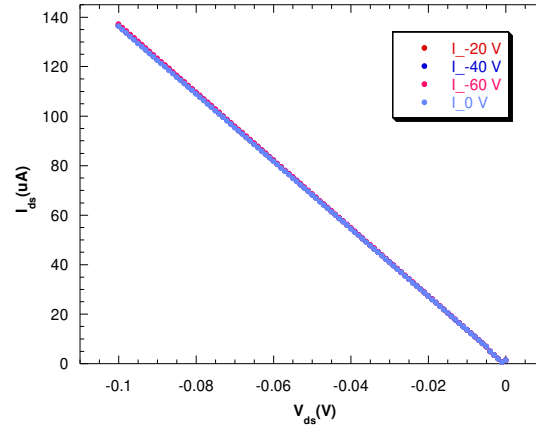


Figure 3. 5. I-V characteristic of Nb-doped MoS₂ contact on homojunction *p-n* diode.

The characterization of the undoped MoS₂ is shown in figure 3.6. Figure 3.6a shows the transfer curve of the undoped sample. The drain current was measured at the bias voltage of 100 mV by sweeping the back-gate voltage from 0 V to 60 V. It clearly shows the n-type behaviour of the undoped MoS₂.

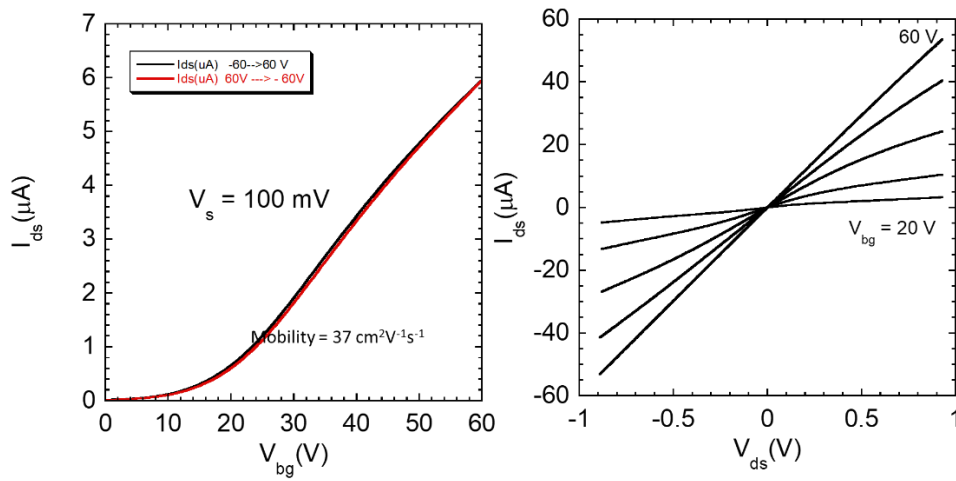


Figure 3. 6. a) Transfer characteristics and b) I-V characteristics of the undoped MoS₂ sample.

The channel seems to be turned on around 10 V. As the back-gate voltage is increased, current increased correspondingly. For large back gate voltage, more electrons would be energetically favourable to cross the Schottky barrier across the metal-semiconductor interface, increases the drain current. The transfer curve at higher back gate voltage is linear. Which is supported by the I-V curve on figure 3.6b. We measured the drain current by sweeping the drain voltage from -1 V to 1 V at different gate voltages from 20 V to 60 V. As we increased the back-gate voltage beyond threshold voltage, the curve is linear indicating that the metal contacts are forming an ohmic contact with the MoS₂ at higher back gate voltage. The current is not limited in undoped MoS₂ by the Schottky barrier at higher back gate voltage.

Now, we measured the electrical properties of the *p-n* junction using one electrode on the Nb-doped MoS₂ and another electrode on undoped MoS₂. Drain bias was applied to the Nb-doped MoS₂ and undoped MoS₂ was connected to the source terminal. As shown in figure 3.7a, the *p-n* junction clearly shows the rectification behaviour. The ratio of the current at 1V to the current at -1V (forward current to the reverse current) for the back-gate voltage of 20 V is ~ 50. The current is increasing with the increase in back gate voltage due to the electrostatic modulation of the carrier density. At the back-gate voltage of 60 V, the current at 1V forward bias is less than 15 μ A. As we mentioned before, doped MoS₂ is independent of the gate voltage and degenerately doped and undoped MoS₂ is also forming an ohmic contact for high back gate voltage. Comparing the current for the same bias at a same back-gate voltage for the doped MoS₂, undoped MoS₂ and the *p-n* junction, it seems that the current is limited by the rectification behaviour of the junction. I-V characteristic of the homostructure *p-n* junction diode is plotted in semi-log scale in figure 3.7b.

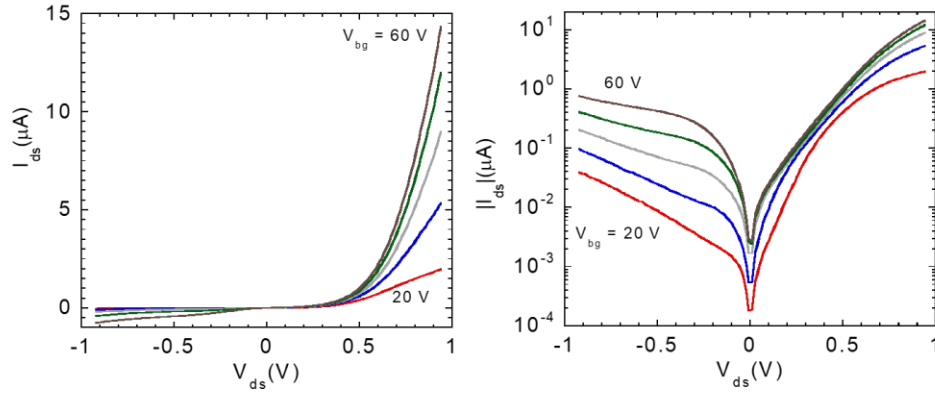


Figure 3. 7. a) I-V characteristics of homojunction p - n junction diode consisting of Nb-doped MoS₂ as p -type and undoped MoS₂ as an n -type semiconductor, b) I-V characteristics of the diode in semi-log scale.

During forward bias, the current increases exponentially with the drain voltage given by the equation,

$$I_{D(forward)} = I_s(e^{\frac{V_D}{nV_T}} - 1)$$

Where I_D is the diode current, I_s is the reverse bias saturation current, V_D is the voltage across the diode, n is the ideality factor and V_T is the thermal voltage¹⁴². As V_{ds} increases, that shifts the band of doped MoS₂ down to lower the interface barrier height. Hence, the electrons in the conduction band of undoped MoS₂ and holes in the valence band of p -doped MoS₂ can overcome the interface barrier. For higher V_{ds} , the barrier height further decreases and the number of carriers crossing the barrier increases giving rise to a large current. This is a thermionic emission process. Figure 3.8c and 3.8d shows the band diagram of p - n junction diode in forward biasing condition.

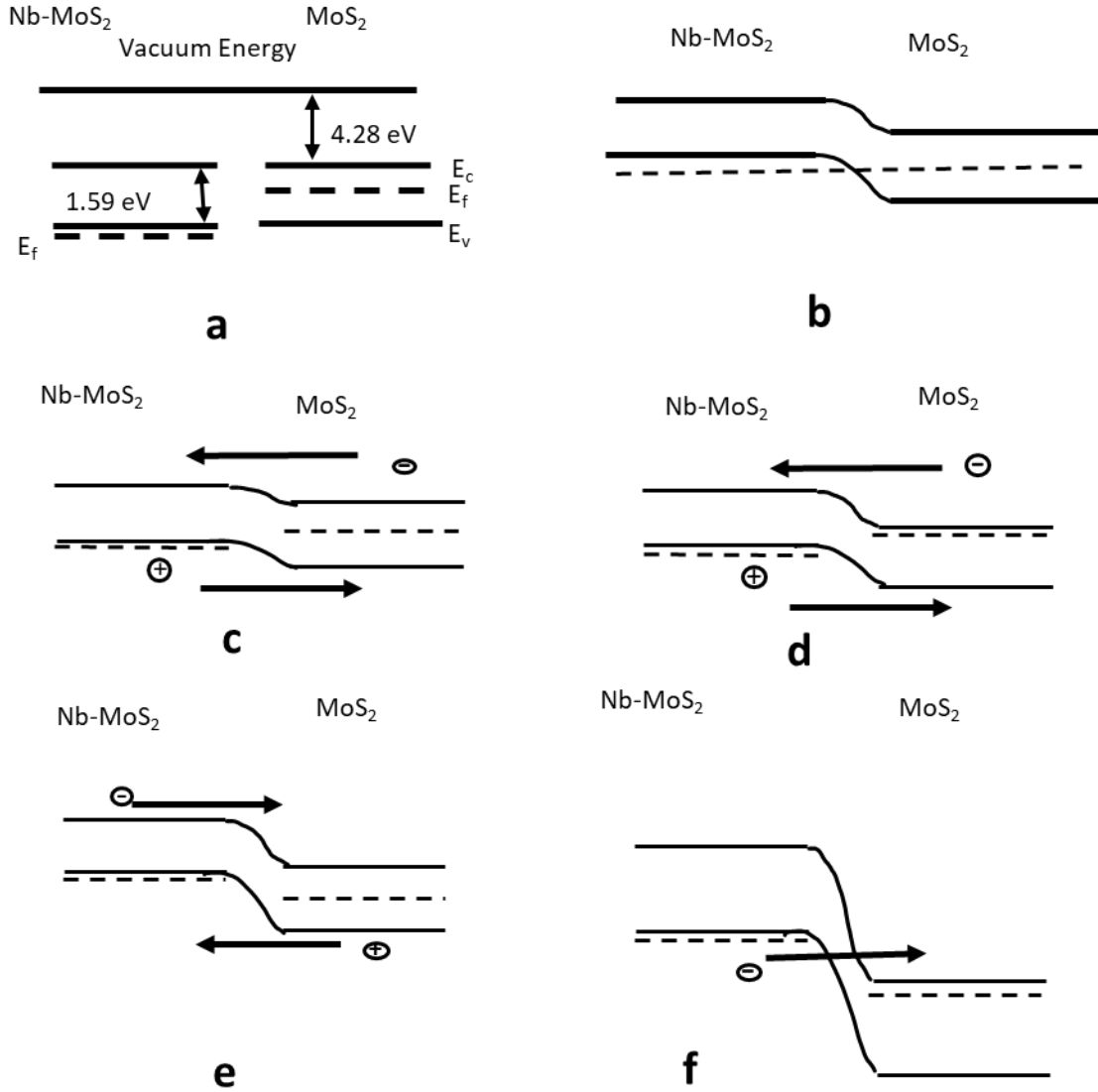


Figure 3. 8. Band diagram of Nb-MoS₂/MoS₂ homojunction *p-n* diode. a) when two semiconductors are not in contact b) in an equilibrium condition, Fermi levels are lined up. c) forward bias at low gate voltage. Due to the forward bias, the interface barrier height is decreased increasing the current. d) forward bias at large voltage. Due to large gate voltage electrostatic doping of the semiconductor increases the carrier concentration in both sides increasing the current. e) reverse bias at low gate voltage. The interface barrier height is increased due to the depletion of the carrier and the conduction is solely due to the minority charge carriers. f) reverse bias at large gate voltage. The large gate voltage dopes the channel electrostatically bringing the conduction band of n-side at the energy level below the valence band of p-side giving rise to band to band tunneling current.

At forward bias and low gate voltage (figure 3.8c), the barrier height decreases due to the applied bias giving rise to the forward current. Forward current is dominated by recombination

current. As gate voltage is increased (figure 3.8d), electrostatic doping of the channel increases and more carriers are able to recombine. As a result, current increases as shown in figure 3.7.

The reverse current is dominated by the minority charge carriers at low gate voltages (low electron concentrations in MoS₂). At small V_{gs} , the Fermi level of the heavily p-doped MoS₂ lies in the band gap of the undoped MoS₂, in which case the tunneling of the electron from the valence band of the heavily *p*-doped MoS₂ to the conduction band of the lightly n-doped MoS₂ is prohibited and the conduction is only due to the drift of minority carriers (figure 3.8e). For larger V_{gs} , the electron concentration on the n-side increases due to the electrostatic doping while the hole concentration on the p-side remains nearly unchanged, leading to a finite overlap of the valence band of the Nb-MoS₂ and the conduction band of the MoS₂. Now the electrons in the valence band of Nb-MoS₂ can tunnel to the conduction band of the MoS₂ giving rise to the band to band tunnelling (BTBT) current (figure 3.8f). Reverse current is dominated by the BTBT current.

The relation of forward and reverse current with the back-gate voltage is further evaluated by plotting forward and reverse current against the back-gate voltage. The current at large forward bias varies linearly (figure 3.9a) with the back-gate voltage, suggesting that it is limited by the series resistance of MoS₂ between the p-n junction and the metal contact to MoS₂. On the other hand, the reverse current increases exponentially with the gate voltage. The tunnelling probability of an electron is proportional to the exponential of the inverse of tunnelling barrier width given by the expression,

$$T(E) = \exp \left[-\frac{2W \sqrt{2m^* (qV_D - E)}}{\hbar} \right]$$

Where W is the tunnelling barrier width, m^* is the effective mass of the electron, $qV_D - E$ represents the tunnelling barrier height for an electron of energy E , \hbar is the reduced Planck's constant¹²⁹. This result indicates that the barrier width decreases linearly with the increase of back-gate voltage giving exponential rise in current.

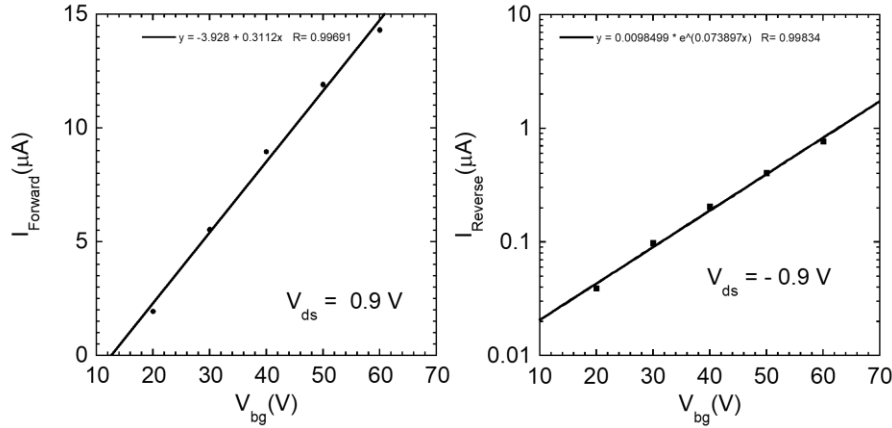


Figure 3. 9. Forward (a) and reverse (b) current of homojunction p - n diode as a function of back-gate voltage. Forward current showed a linear relationship with back-gate voltage, while reverse current increased exponentially with back-gate voltage.

The measurement on the heterostructure p - n junction diodes closely agrees with the result for homojunction diodes. Figure 3.10 shows the I-V characteristics measurement of the device.

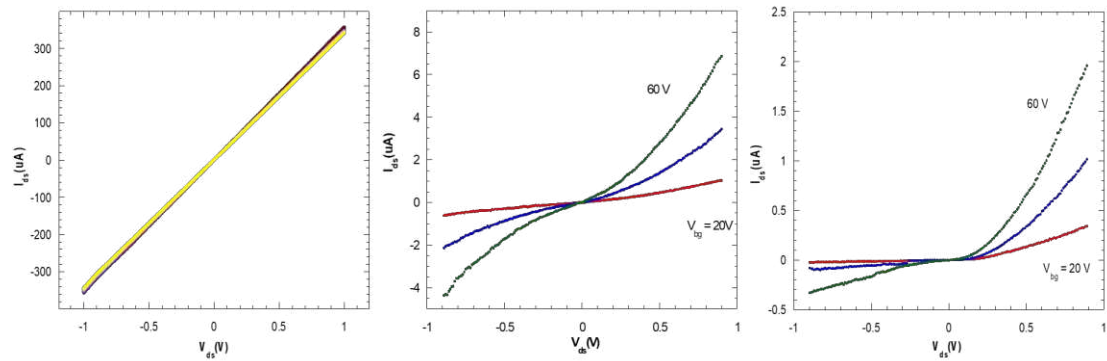


Figure 3. 10. a) I-V characteristics of doped WSe_2 sample b) I-V characteristics of undoped MoS_2 sample c) I-V characteristics of heterostructure p - n junction diode.

Figure 3.10a represents the I-V characteristics of the doped WSe₂ sample. As shown from the plot, Nb-doped WSe₂ is degenerately doped p-type semiconductor. The I-V measurement was done at different gate voltages from -60 V to 60 V and found no dependence on gate voltage. Figure 3.10b is the I-V plot for the undoped MoS₂ sample. The channel seems to be turned on around 20 V indicating the n-type behavior of the sample. At large back-gate voltages I-V curve are linear indicating ohmic contact with the metal electrodes. Figure 3.10c displays the I-V plot of the heterostructure *p-n* junction diode. The diode shows the gate dependent rectification behavior. This is due to the modulation of carrier density by the electrostatic gating. On comparing the I-V characteristics of doped WSe₂, undoped MoS₂ and the diode it is clear that the effect of the lateral part in limiting current is nominal for the back-gate voltage greater than 20 V. The current is limited by the vertical junction. The I-V characteristics of the *p-n* junction diode is plotted on semi-log scale in figure 3.11a.

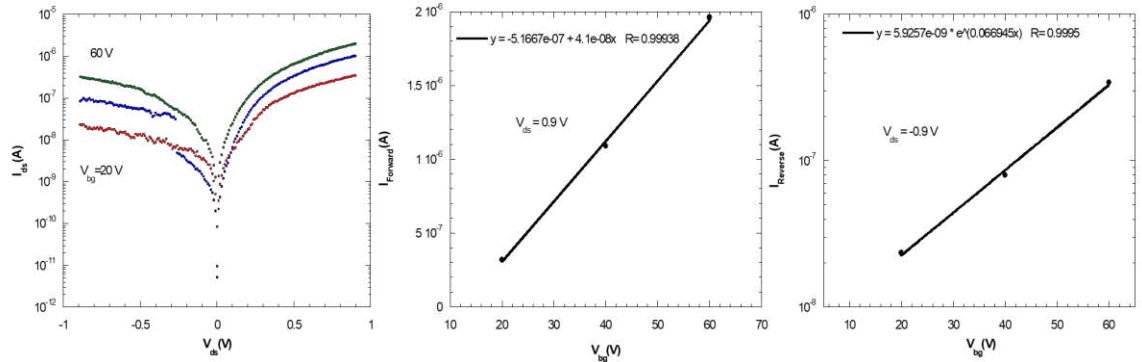


Figure 3. 11. a) I-V characteristics of heterostructure *p-n* junction diode in semi-log scale, b) forward diode current as a function of back gate voltage c) reverse diode current as a function of back gate voltage.

As in the case of homo-structure *p-n* junction diode, the forward current of the diode is linearly dependent on the gate voltage (figure 3.11b) and the reverse current is exponentially dependent (figure 3.11c), indicating recombination dominated forward current and the tunneling

dominated reverse current. The difference in the magnitude of the current in heterostructure can be attributed to the differences in band alignments between the WSe₂ and MoS₂ samples.

3.3 Summary

In summary, we fabricated two-dimensional p - n junction diodes using van der Waal assembly method. We fabricated and characterized both the homo-structure as well as the hetero-structure diodes. The diodes displayed the gate tuned rectification behavior. Forward current is found to be dominated by thermal emission and is linearly dependent on gate voltage. Whereas, the reverse current is dominated by the band to band tunneling current and exponentially increases with the back-gate voltage.

CHAPTER 4: THERMALLY OXIDIZED 2D TAs₂ AS HIGH-K DIELECTRIC FOR MOS₂ FETS

4.1 Background and Motivation

Layered transition metal dichalcogenides (TMDCs) such as MoS₂, MoSe₂, and WSe₂ have recently emerged as promising post-silicon electronic materials because they have not only demonstrated a multitude of graphene-like properties desirable for flexible electronics including a relatively high carrier mobility, mechanical flexibility, and chemical and thermal stability, but also offer the significant advantage of a substantial band gap essential for low-power digital electronics.¹⁻⁶ In addition, pristine surfaces of TMDCs are free of dangling bonds, which reduces surface roughness scattering and interface traps. Recent experimental and theoretical studies have shown that the mobility of monolayer and multilayer TMDCs such as MoS₂ and MoSe₂ is strongly affected by their dielectric environment and the quality of the interface between the channel and dielectric/substrate.⁷⁻¹¹ Ultraclean hexagonal boron nitride (h-BN) is an ideal substrate/dielectric material in preserving the intrinsic mobility of MoS₂ because it has atomically flat surfaces absent of dangling bonds, and is nearly free of charged impurities and charge traps.^{12, 13} However, h-BN has a relatively low dielectric constant of 3-4, while high- κ dielectrics are needed to optimize the electrostatic control of the channel and minimize operation voltage.¹⁴⁻¹⁶

In silicon-based electronics, atomic layer deposition (ALD) has been widely used to integrate high- κ gate dielectrics such as Al₂O₃ and HfO₂ with atomically controlled thickness and uniformity. However, the lack of out-of-plane covalent bonds or functional groups on pristine TMD surfaces imposes a significant challenge for high- κ dielectric integration in top-gated TMDC devices because ALD requires chemical groups such as hydroxyl groups on the channel surfaces to form conformal and uniform interface layers.¹⁷⁻²⁰ To overcome this challenge, Liu *et al.* have significantly lowered the ALD temperature to grow Al₂O₃ films on MoS₂.²¹ However, the coverage

and uniformity of Al_2O_3 thin films grown by low-temperature ALD are intricately affected by multiple growth parameters such as pulsing and purging times, process pressure, and cleanliness of the MoS_2 surface, leading to poor reproducibility.²² For instance, a small amount of organic and solvent residues on the TMDC surfaces have been found to drastically influence the ALD nuclear behaviour during the initial stage of deposition.²³ In addition, ALD dielectric films grown at low temperatures tend to contain a substantial amount of impurities such as OH and C residues.^{24, 25} A variety of surface functionalization methods such as oxygen plasma and ozone have been used to improve the smoothness and uniformity of ALD grown high- κ dielectrics on TMDCs.^{22, 26, 27} However, highly reactive oxygen plasma and ozone tend to degrade the electrical properties of monolayer and few-layer TMDCs through surface oxidation and the introduction of defect states. To date, it remains a major challenge to grow highly uniform, atomically smooth and ultrathin high- κ dielectrics on TMDC surfaces while preserving the intrinsic channel properties of pristine TMDC channels.

In this chapter, we present a new strategy to integrate high- κ dielectric into MoS_2 field-effect transistors through the mechanical assembly of Ta_2O_5 chemically transformed from 2D TaS_2 . In contrast to relatively inert semiconducting TMDs such as MoS_2 , MoSe_2 and WSe_2 , metallic TMDCs such as TaS_2 are prone to surface oxidation in ambient environment.²⁸⁻³⁰ At elevated temperatures, monolayer and multilayer TaS_2 can be chemically transformed into atomically flat, spatially uniform and nearly defect-free Ta_2O_5 insulator via thermal oxidation, as recently demonstrated by the authors.³¹ In this work, we have systematically characterized the dielectric properties of Ta_2O_5 thermally oxidized from TaS_2 by capacitance-voltage measurement, yielding a thickness independent high dielectric constant of $\kappa \sim 15.5$. MoS_2 FETs fabricated using thermally oxidized thin Ta_2O_5 as gate dielectric show nearly hysteresis-free transfer characteristics, suggesting high

interface quality. Furthermore, this new approach enables us to assemble high-quality Ta₂O₅ dielectric on top of pristine MoS₂ channels to form top-gated FETs, while circumventing the constraints of ALD methods. MoS₂ FETs with the thermal Ta₂O₅ top-gate dielectric demonstrate a current on/off ratio of $\sim 10^6$, a high field-effect mobility $> 60 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, and a near ideal subthreshold swing (SS) of $\sim 61 \text{ mV/dec}$ at room temperature, along with pronounced drain-current saturation in their output characteristics. The impressive performance of the MoS₂ FETs can be attributed to the atomically flat, spatially uniform, and nearly charge-trap free high- κ Ta₂O₅ dielectric synthesized by thermal oxidation of TaS₂, which forms an ultraclean interface with the MoS₂ channel.

4.2 Results and discussion

To chemically transform TaS₂ 2D metal into Ta₂O₅ high- κ dielectric, TaS₂ flakes were first mechanically exfoliated on SiO₂/Si substrate and subsequently oxidized by heating on a hot plate at 300°C for 3 hours in air. The chemical transformation of TaS₂ into Ta₂O₅ was confirmed by X-ray photoelectron spectroscopy (XPS). X-ray photoelectron spectroscopy (XPS) measurement was performed using a Kratos Axis Ultra XPS system with a monochromatic Al source. Because TaS₂ is sensitive to air, the samples were mechanically exfoliated from bulk crystals right before XPS measurement and then immediately inserted into the XPS chamber to avoid oxidation unless specified otherwise in the manuscript. Pass energy of 20 eV with 0.1 eV scanning step was used for photoelectron detection. The C 1s reference line at the binding energy of 284.6 eV was used to calibrate the charging effect.

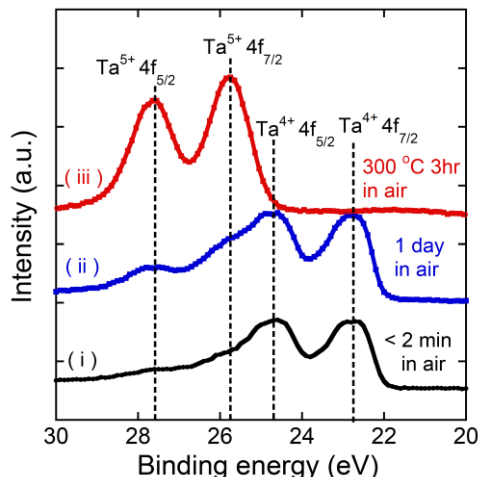


Figure 4. 1. XPS of exfoliated TaS₂ flakes measured within 2 min of ambient exposure, after 1 day of ambient exposure, and after 3hr of hotplate heating at 300°C in air.

Figure 4.1 shows Ta 4f core level XPS spectra of multilayer TaS₂ flakes that are (i) freshly exfoliated (inserted into the XPS chamber within 1-2 minutes of exfoliation), (ii) exposed in ambient environment for one day, and (iii) heated at 300°C in ambient air for 3 hrs. The freshly exfoliated TaS₂ flakes exhibit two well-defined peaks at binding energies of 22.8 eV and 24.7 eV, corresponding to the Ta⁴⁺ 4f_{7/2} and Ta⁴⁺ 4f_{5/2} doublet of TaS₂. After exposed to ambient air for a day, the TaS₂ flakes exhibit two additional weak peaks at slightly higher binding energies, suggesting partial oxidation of TaS₂ surfaces. After the TaS₂ flakes were heated to 300°C for 3 hours in air, the Ta⁴⁺ doublet of TaS₂ completely disappears, while the weak peaks develop into two distinct peaks at binding energies of 25.7 eV and 27.6 eV, corresponding to the Ta⁵⁺ 4f_{7/2} and Ta⁵⁺ 4f_{5/2} doublet of Ta₂O₅.³²⁻³⁵

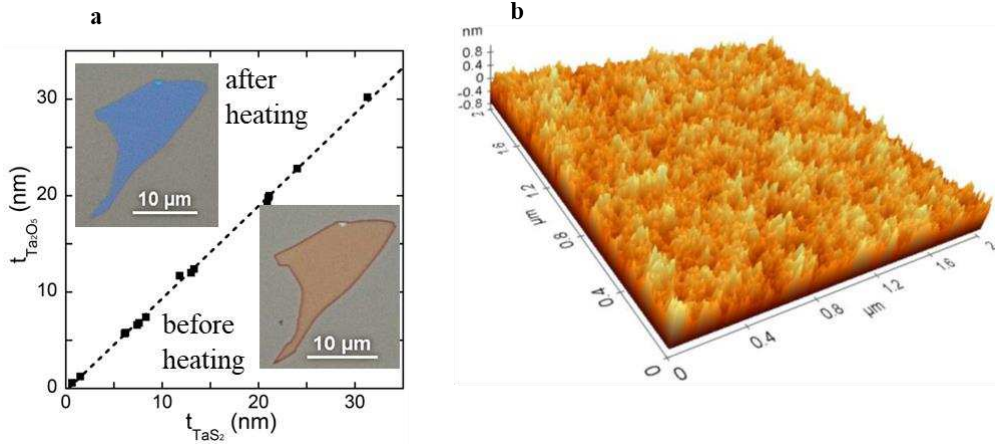


Figure 4. 2. (a) Thicknesses of mechanically exfoliated TaS₂ before and after 3hr of heating at 300°C in air as determined by AFM. The insets show optical micrographs of a typical TaS₂ flake on SiO₂ before (bottom right) and after heating at 300°C in air (top left). (b) AFM surface topography of a Ta₂O₅ flake converted from a corresponding TaS₂.

The chemical transformation of TaS₂ into Ta₂O₅ is also clearly manifested in the form of color change. The lower-right and upper-left insets of figure 3a present the optical micrographs of a ~ 12 nm multilayer TaS₂ sample before and after thermal oxidation (which chemically transforms TaS₂ to Ta₂O₅). While the sample geometry and lateral dimensions remain nearly unchanged throughout the chemical transformation, the sample thickness measured by AFM systematically decreases by ~4% upon thermal oxidation independent of initial sample thickness as shown in Figure 4.2a, indicating that thermal oxidation occurs throughout the entire sample. Because about 25% volume decrease would be expected if the TaS₂ was transformed into crystalline Ta₂O₅, the 4% thickness reduction (with nearly unchanged lateral dimensions) observed here suggests that the Ta₂O₅ has significantly lower density than crystalline Ta₂O₅ and is likely amorphous.^{36, 37} The non-crystalline structure of our Ta₂O₅ with relatively low density allows the oxygen in air to diffuse deep into the sample and achieve uniform and thorough thermal oxidation. In spite of the chemical and structural transformation, the Ta₂O₅ flakes display very low root-mean-square (RMS) surface roughness. Figure 4.2b shows a representative AFM topographic image acquired

on a ~ 12 nm thick Ta_2O_5 synthesized by thermal oxidation yielding an RMS roughness of 0.17 nm, which is comparable to that of TMDCs.³⁸ Such a low RMS roughness in the thermal Ta_2O_5 is essential for the formation of high quality interface with MoS_2 and other TMDC channel materials.

To extract the dielectric constant of the Ta_2O_5 synthesized by thermal oxidation, we fabricated capacitors consisting of an ultrathin Ta_2O_5 dielectric layer sandwiched between the top and bottom metal electrodes as schematically illustrated in Figure 4.3a. First, bottom electrodes consisting of 10 nm of platinum (Pt) with 5 nm of titanium (Ti) adhesion layer were patterned on Si substrates with 290 nm of thermal oxide using electron beam lithography followed by electron beam deposition and lift-off. Next, TaS_2 flakes were produced by mechanical exfoliation of commercial available TaS_2 crystals on Poly-dimethylsiloxane (PDMS) stamps and subsequently transferred on top of the Pt electrodes using a dry transfer method.³⁹ The TaS_2 flakes were then thermally oxidized to Ta_2O_5 by heating on a hotplate at 300°C for 3 hours in ambient air. Finally, top electrodes were fabricated by e-beam lithography and electron beam deposition of 10 nm Ti and 30 nm Au. The area of each metal-insulator-metal capacitor is defined by the area of the Ta_2O_5 dielectric in the overlap region between each top electrode and the bottom electrode. The C - V measurements were carried out at room temperature using an Agilent 4284A Precision LCR Meter inside a Lakeshore TTPX probe station.

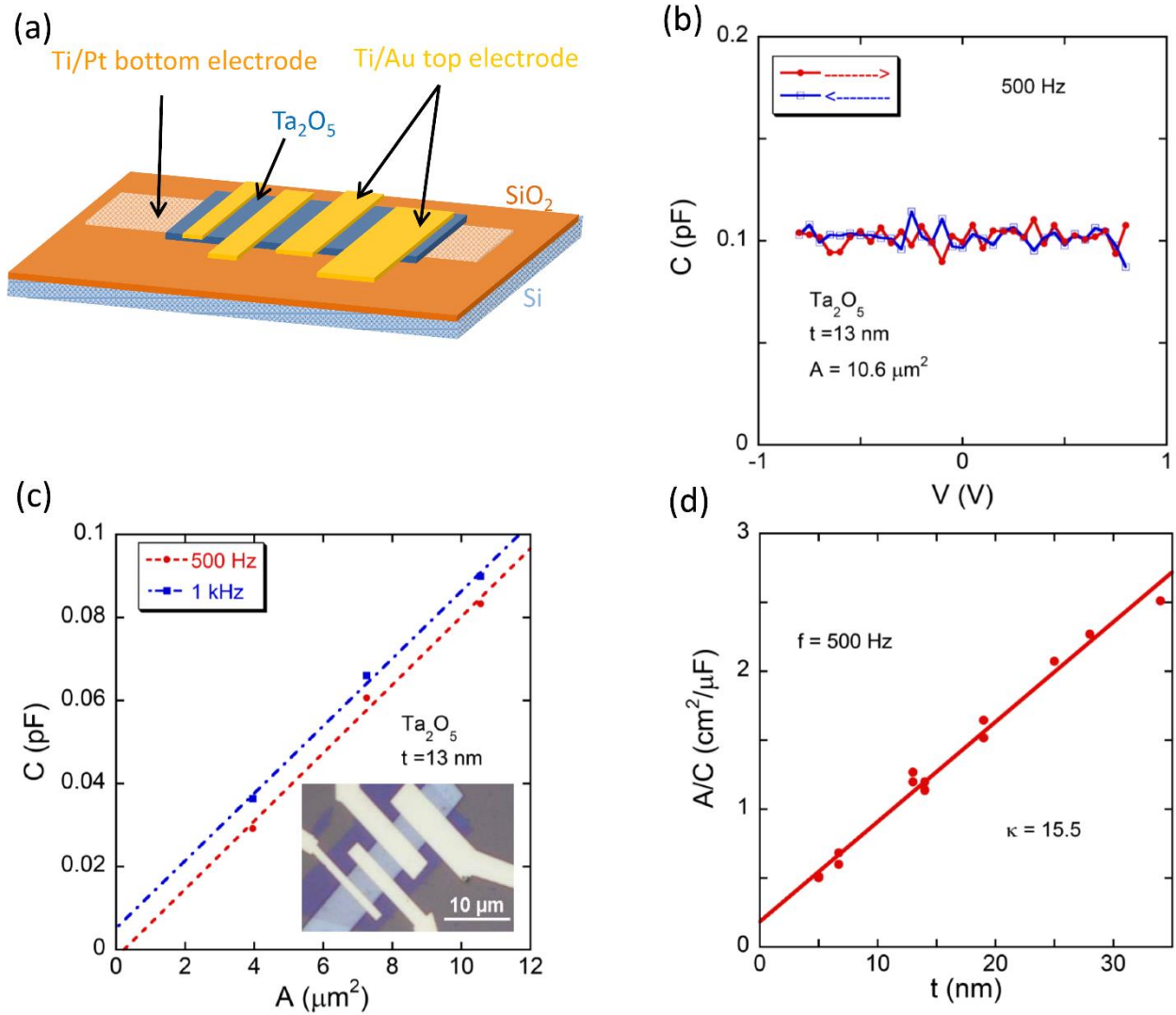


Figure 4. 3. (a) Schematic illustration of capacitors consisting of a thin Ta₂O₅ dielectric sandwiched between Pt and Ti/Au metal electrodes (b) Capacitance *vs.* voltage for a capacitor comprising a 13 nm thick Ta₂O₅ dielectric as the voltage is swept along both negative and positive directions. (c) Capacitance as a function of the area for three capacitors with the same Ta₂O₅ dielectric thickness (13 nm) measured at two different frequencies (500 Hz and 1 kHz). Inset: an optical image of the corresponding capacitors. (d) *A/C vs.* thickness of Ta₂O₅. The inverse of the slope of the plot gives the dielectric constant of Ta₂O₅ based on the parallel plate capacitor model:

$$\frac{C}{A} = \frac{\epsilon_0 \kappa}{t}$$

Figure 4.3b shows the capacitance as a function of the applied DC bias voltage (*C-V*) of a capacitor with a 13 nm thick Ta₂O₅ dielectric measured by applying a 500 Hz and 50 mV AC

excitation voltage. The nearly voltage independent capacitance shows negligible hysteresis, indicating that the Ta₂O₅ dielectric is of high quality because charge traps in the dielectric and at the interfaces usually introduce non-negligible hysteresis. To exclude the background capacitance (e.g. the cable capacitance), we plot the total capacitance as a function of the area for capacitors fabricated using the same piece of Ta₂O₅ with uniform thickness, as shown in figure 4.3c. From a linear fit to the capacitance *vs.* area data, capacitance per unit area (C/A) of the capacitors with different Ta₂O₅ dielectric thicknesses is determined. The near zero intercept of the linear fit in figure 4c indicates negligible background capacitance. The dielectric constant can be calculated using the parallel capacitor model: $\frac{C}{A} = \frac{\epsilon_0 \kappa}{t}$, where ϵ_0 is the permittivity of the free space, and κ and t are the dielectric constant and thickness of the Ta₂O₅, respectively. Figure 4.3d shows that the inverse of capacitance per unit area (A/C) is linearly proportional to the thickness (t) for various Ta₂O₅ thicknesses ranging from 5 to 33 nm, indicating that the dielectric constant of the Ta₂O₅ is thickness independent. This finding provides further evidence that multilayer TaS₂ samples have been uniformly transformed into Ta₂O₅. From the slope of the linear fit, we extract a dielectric constant of ~ 15.5 , which is consistent with the κ reported for amorphous Ta₂O₅.⁴⁰ It is worth noting that the dielectric constant of our thermal Ta₂O₅ is about 4 times larger than that of SiO₂ (3.9) and h-BN (3 - 4).

To further evaluate the quality of the thermally oxidized Ta₂O₅ as a high- κ dielectric for 2D electronics, we first fabricated MoS₂ FETs with an ultrathin Ta₂O₅ dielectric and a multilayer graphene (M-Gr) gate as schematically shown in Figure 4.4a. Here we choose multilayer graphene as the gate because it not only has atomically smooth surfaces but also is compatible with the fabrication of 2D flexible electronics in the future. To fabricate MoS₂ FETs with Ta₂O₅ gate dielectric and graphite bottom gate, thin graphite flakes were first mechanically exfoliated and

transferred onto Si/SiO₂ substrates as bottom gates. Subsequently, multilayer TaS₂ flakes were produced by mechanical exfoliation from commercially available TaS₂ crystals on PDMS stamps and subsequently transferred onto top of the graphite gates using a home-built precision transfer stage. The substrates were then heated at 300°C for 3 hrs in ambient environment to chemically transform TaS₂ to Ta₂O₅. The oxidized flakes were further characterized by optical microscope and XE-70 non-contact mode atomic force microscopy (AFM). Next, few-layer MoS₂ flakes were exfoliated on PDMS stamp and transferred onto the Ta₂O₅/graphite gate stack. Finally, drain/source electrodes and electrical contacts to the graphite gate were fabricated by e-beam lithography and electron beam deposition of 5 nm of Ti and 40 nm of Au followed by acetone lift-off. Figure 4.4b presents a micrograph of a representative MoS₂ FET consisting of a 7.0 nm thick MoS₂ channel, a 6.5 nm thick Ta₂O₅ dielectric and a multilayer graphene back gate. Figure 5c shows the output characteristics of the MoS₂ device depicted in Figure 4.4b. In the low V_{ds} region, the I - V characteristics are linear, indicating near ohmic contacts. At high drain/source voltages, the device exhibits apparent current saturation partially due to the channel pinch-off, suggesting effective gate coupling. Figure 4.4d presents room-temperature transfer characteristics of the device measured at $V_{ds} = 100$ mV. The MoS₂ device exhibits n -type behavior with a current on/off ratio exceeding 10^5 , where the off current is limited by the leak current as shown in Figure 4.4d.

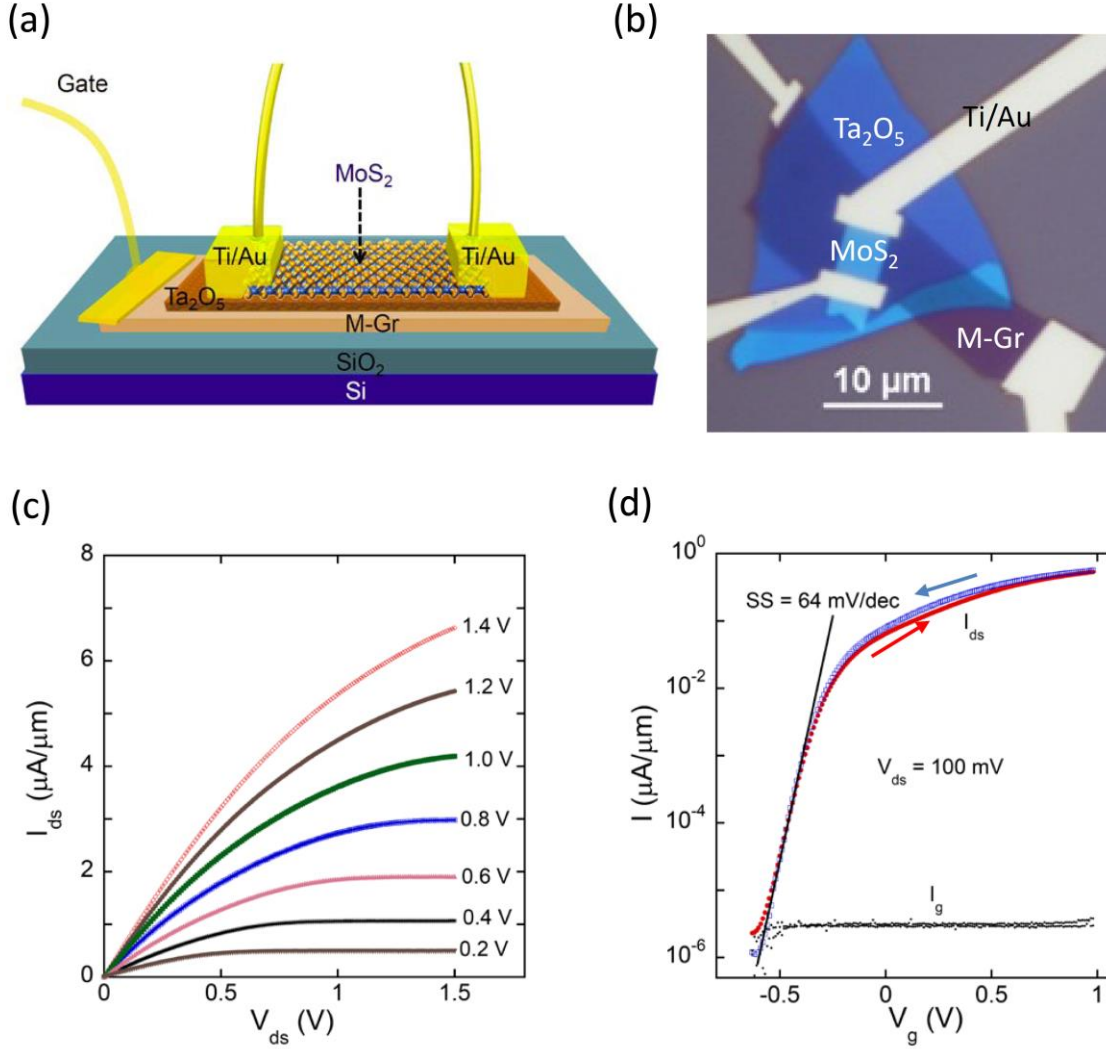


Figure 4. 4. (a) Schematic illustration of a MoS₂ FET device with Ta₂O₅ dielectric and multilayer-graphene (M-Gr) bottom gate. (b) Optical image of a typical bottom-gated MoS₂ FET device with Ta₂O₅ dielectric. (c) Output characteristics of the MoS₂ device shown in (b). (d) Transfer characteristics of the same MoS₂ FET device along with the gate leakage current. Red color represents the positive sweep direction and the blue color represents the negative sweep direction of the gate voltage.

In spite of the ultrathin layer thickness (6.5 nm) and relatively small band gap of Ta₂O₅ (3.8-5.3 eV) as a dielectric, the gate leak current is rather low, suggesting that the thermally oxidized Ta₂O₅ is highly uniform with very low density of pinholes. We expect that the gate-leak current can be significantly reduced by using high- κ dielectrics with a larger bandgap such as

HfO₂. Similar to metallic TaS₂, HfSe₂ is also prone to oxidation in air (similar to TaS₂) in spite of the fact that it is a semiconductor with a bulk band-gap comparable to that of bulk MoS₂.^{41, 42} We envision that 2D HfSe₂ can be relatively straightforwardly transformed to ultrathin HfO₂ high- κ dielectric and integrated into FETs with semiconducting TMDC channel materials such as MoS₂ by mechanical assembly. The on-current can be increased through contact engineering to further improve the on/off ratio and overall device performance.⁴³ The transfer characteristics measured with opposite gate sweep directions show negligible hysteresis, indicating low charge trap density at the channel/dielectric interface. The subthreshold swing of the device (~ 64 mV/dec) approaches the theoretical limit of $\frac{kT}{e} \ln(10) = 60$ mV/dec at $T = 300$ K, which can be attributed to the large gate capacitance of the ultrathin Ta₂O₅ high- κ dielectric and high interface quality. A relatively low interface trap density of $D_{it} = 1.2 \times 10^{12}$ cm⁻²eV⁻¹ is calculated from the following equations:

$$SS = \left(1 + \frac{C_{it}}{C_{ox}}\right) \times kT \times \ln(10)/e \quad (1)$$

$$D_{it} = C_{it}/e \quad (2)$$

Here C_{it} and C_{ox} are the interfacial and oxide capacitances, respectively.

For practical application of MoS₂ as a channel material in integrated circuits, top-gated MoS₂ FETs with high- κ gate dielectric are needed to individually control each device. A significant advantage of this approach to integrating high- κ dielectrics in 2D electronics is that it circumvents a major challenge encountered in the ALD growth of high- κ dielectrics on TMDs due to the lack of dangling bonds on semiconducting TMDC surfaces. To fabricate the devices, mechanically exfoliated multilayer TaS₂ flakes were dry-transferred on top of mechanically exfoliated M-Gr flakes serving as gate electrodes, and subsequently thermally oxidized to Ta₂O₅. Next, a selected few-layer MoS₂ channel was placed on top of the Ta₂O₅/M-Gr stack also by dry-transfer.⁴³ Finally,

drain, source and gate contacts were fabricated by electron beam lithography and subsequent deposition of 5 nm Ti and 40 nm Au. Figure 4.5a schematically shows a few-layer MoS₂ FET with Ta₂O₅ as top-gate dielectric. To fabricate the devices, ultrathin flakes of Ta₂O₅ were produced by thermal oxidation of mechanically exfoliated TaS₂ multilayers on Si substrate at 300°C in air, and subsequently transferred onto mechanically exfoliated few-layer MoS₂ on degenerately doped Si substrate with 290 nm thermal oxide. Both the drain/source and top-gate electrodes were then fabricated by EBL and e-beam deposition of 5 nm Ti and 40 nm Au. Figure 4.5b shows an optical micrograph of a representative top-gated MoS₂ FET, which consists of a 6.5 nm thick MoS₂ channel and 31 nm thick Ta₂O₅ gate dielectric. As shown in Figure 4.5c, the output characteristics of the device show linear behavior at low V_{ds} and current saturation at high V_{ds} , similar to the MoS₂ devices with Ta₂O₅ bottom-gate dielectric. Here a constant back-gate voltage of 60 V is applied to reduce the contact resistance and turn on the under-lapped regions between the drain/source electrodes and top-gate electrode. Figure 4.5d shows room temperature transfer characteristics of the same device measured at $V_{ds} = 100$ mV by sweeping the top-gate voltage at a fixed back-gate voltage of 60 V. The transfer curve exhibits a nearly ideal SS of 61 mV/dec in spite of the relatively thick (31 nm) Ta₂O₅ gate dielectric, indicating nearly trap-free channel/dielectric interface. The current on/off ratio approaches 10^6 , which can be further enhanced by increasing the on-current through the reduction of series resistance. It is worth noting that the drain current starts to saturate at $V_{tg} \sim 0$ V, which is mainly caused by the reduction of the effective gate voltage (V_{tg_eff}) due to the presence of a significant series resistance from the drain/source contacts and the under-lapped regions given by $V_{tg_eff} = V_{tg} - R_s I_{ds}$, where V_{tg} is the applied top-gate voltage, and R_s is the sum of metal/MoS₂ contact resistance and the resistance of the under-lapped regions.⁴⁴ The presence of a substantial R_s may also partially contribute to the current saturation in the output characteristics

because the effective drain-source bias voltage given by $V_{ds_eff} = V_{ds} - 2R_s I_{ds}$ is also reduced at high I_{ds} .

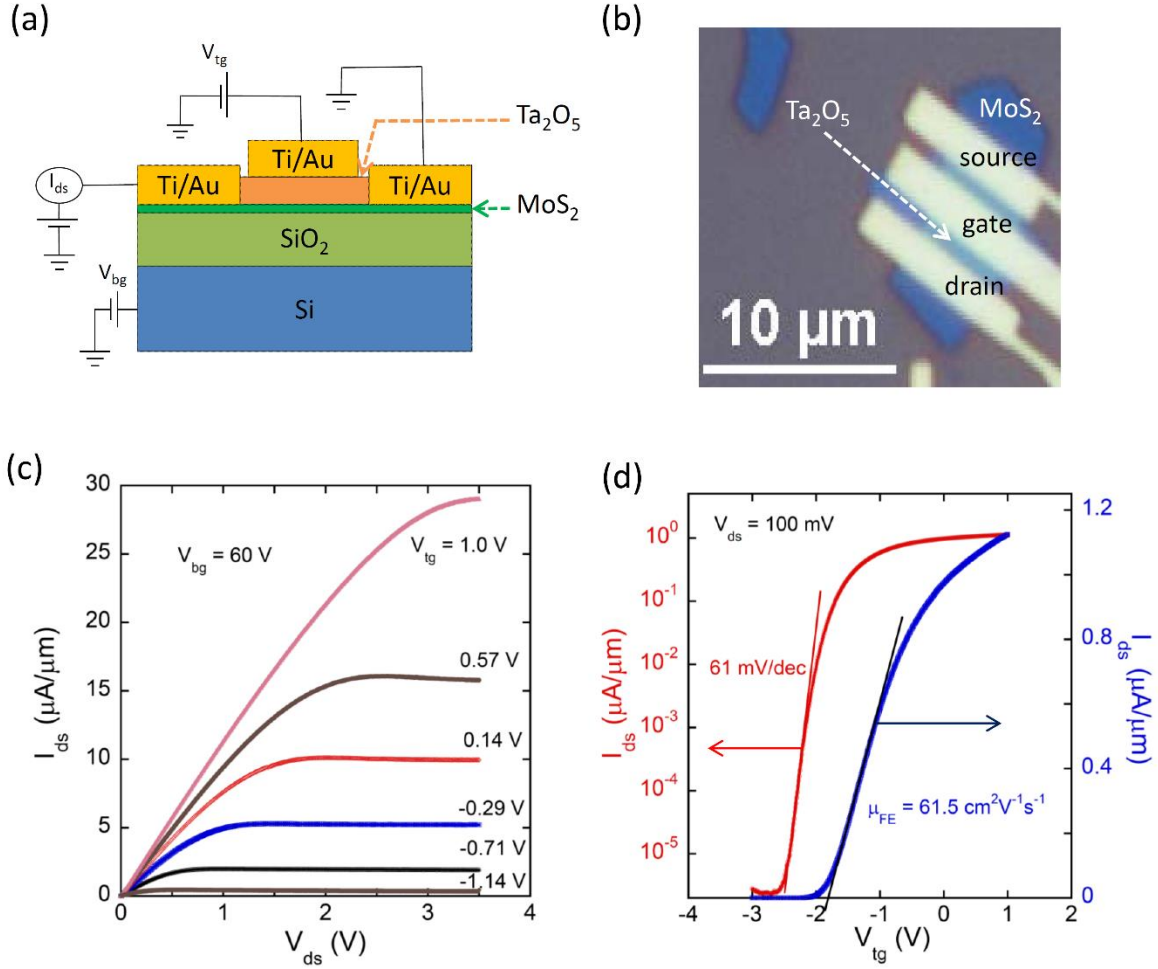


Figure 4. 5. (a) Cross-sectional view of a MoS₂ FET device with Ta₂O₅ dielectric and metal top gate. (b) Optical image of a MoS₂ FET device with Ta₂O₅ top-gate dielectric. (c) Output characteristics of the MoS₂ device in (b). (d) Transfer characteristics of the same MoS₂ FET device plotted both in semi-log and linear scales.

As shown in Figure 4.5d, a field-effect mobility of $\mu_{FE} \approx 61.5\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ is extracted from the linear region of the transfer curve using the expression $\mu_{FE} = \frac{L}{W} \times \frac{dI_{ds}}{dV_{tg}} \times \frac{1}{C_{tg}} \times \frac{1}{V_{ds}}$. Here L is the channel length directly underneath the metal gate because the under-lapped regions are not tunable by the top-gate. Inclusion of the under-lapped areas in the calculations would overestimate

the field-effect mobility. The field-effect mobility observed in our top-gated MoS₂ FETs is comparable to the highest room-temperature mobility values for top-gated MoS₂ devices with high- κ dielectric, further indicating low density of trap states in the thermally oxidized Ta₂O₅ dielectric and at the channel/dielectric interface.

4.3 Summary

In summary, we have demonstrated integration of ultrathin Ta₂O₅ chemically transformed from 2D TaS₂ in both bottom-gated and top-gated MoS₂ FETs as a high- κ gate dielectric. These devices show desirable FET characteristics such as a high on/off ratio, absence of hysteresis, a nearly ideal subthreshold swing, and a relatively high mobility, indicating high dielectric and interface quality. The newly developed dielectric integration strategy via chemical transformation of 2D materials to high- κ dielectrics in conjunction with polymer-based dry transfer techniques overcomes a significant challenge of dielectric integration in semiconducting TMDC devices, and is applicable to a wide range of 2D materials. This approach is also scalable when combined with large area synthesis techniques such as chemical vapor deposition (CVD) and liquid exfoliation.^{45,}

CHAPTER 5: SYNTHESIS AND CHARACTERIZATION OF ULTRATHIN HfO₂ FROM CHEMICAL TRANSFORMATION OF 2D HFSE₂

5.1 Background and Motivation

Scaling of silicon dioxide dielectrics brought revolution in electronics industry by making it possible to increase the number of transistors per chip alongside performance enhancement, low power consumption and reduced cost⁸⁸. However, in this process, the effective oxide thickness of SiO₂ reached almost to the limit of the Physical thickness. As the thickness of SiO₂ gate insulators is reduced to few atomic layers, charge carriers can flow through the gate dielectric by a quantum tunnelling mechanism^{90,91}. This mechanism involves the tunnelling of charge carriers through a trapezoidal energy barrier⁹². It is seen that the tunnelling probability increases exponentially as the thickness of SiO₂ layer decreases^{90,92}. In addition to gate leakage current, the reduction in width of gate oxide also causes a reduction in the ON/OFF ratios⁸⁹. To continue the downscaling of MOSFET, without facing the issues of leakage currents, study of dielectrics having high- κ value is in prime focus. Recently, a lot of efforts have been focused to investigate high- κ gate dielectrics such as, zirconium dioxide (ZrO₂)¹⁰⁷, hafnium dioxide (HfO₂)^{108,109}, aluminium oxide (Al₂O₃)¹¹⁰, titanium dioxide (TiO₂)¹¹¹, tantalum pentoxide (Ta₂O₅)^{112,113} etc. These high- κ dielectrics should possess thermal stability, high recrystallization temperature, smooth interface, suitable band gap etc. HfO₂ is a most promising candidate among these high- κ dielectrics with band gap of 6V, theoretical K value around 25 and crystallization temperatures beyond 450°C¹⁴³. Having large band gap, HfO₂ is expected to decrease the leakage current in compare to the Ta₂O₅¹⁴⁴. Also, HfO₂ is thermally stable on direct contact with Si in compare to other high- κ dielectrics such as Ta₂O₅, TiO₂¹⁴⁵.

For the enhancement of the device, TMDC as channel, the growth of conformal, uniform high- κ dielectric is necessary. The high- κ dielectric integration study so far has been based on

different growth methods (CVD, ALD, PLD, MBE, etc.). With these complex growth methods, the interface has always been issue. ALD is supposed to be more reliable deposition in case of TMDCs. McDonnell et. al., (2013) did the Atomic layer deposition (ALD) of HfO_2 on the MoS_2 surface¹⁴⁶, and found that the ALD on MoS_2 was not uniform. They could not detect covalent bonding between the HfO_2 and MoS_2 . In another study, when 15-17 nm HfO_2 was deposited by ALD, island type growth was observed resulting in non-uniform films¹²⁰. In their study, Lembke et al., (2015) found that, due to the absence of out of plane covalent functional group in MoS_2 , surface functionalization is needed to fabricate scaled 2 dimensional layered devices using ALD⁸. The uniform ALD growth of ~ 10 nm Al_2O_3 has been reported¹⁴⁷, but in contrast, non-uniform ALD of Al_2O_3 at same temperature and precursors has also been reported¹⁴⁸. Thus, it seems like ALD depends upon different factors and cannot rely upon same method in different conditions. And the problem of high- κ dielectric integration of TMDC is still on.

To get rid of the problems of ALD growth of dielectrics, we proposed two-dimensional flat high- κ dielectric by phase engineering. We prepared two dimensional atomically flat high- κ dielectric through mechanical exfoliation followed by thermal oxidation. In this study, we obtained planar Hafnium di-selenide (HfSe_2) using mechanical cleavage method, and oxidized it in air to obtain Hafnium Oxide (HfO_2). As we obtained HfSe_2 from the exfoliation of single crystal, our sample has relatively good interface. We also verified the surface topography of oxidized dielectric by AFM characterization. We found the oxidized surface topography remains preserved as before oxidation.

5.2 Results and Discussion

All samples in this study were mechanically exfoliated using scotch tape technique. Initially, HfSe_2 samples were exfoliated directly on Si/SiO_2 substrate to observe the color contrast.

Later, for the device fabrication purpose, Graphite were first transferred on Si/SiO₂ substrate and HfSe₂ samples were transferred over Graphite. The schematic diagram of the fabrication process is shown in figure 5.1.

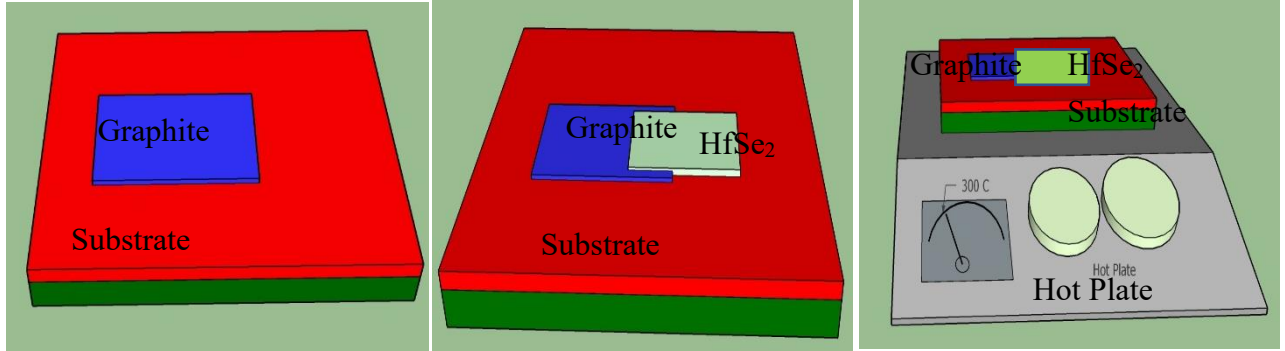


Figure 5. 1. Process for the device fabrication. a) few layer graphite transfer on Si/SiO₂ substrate, b) PDMS assisted HfSe₂ transfer on the top of Graphite c) heating substrate on a hotplate in ambient condition d) after electrode fabrication.

Oxidation of exfoliated samples was done in several stages to find the right combination of temperature and time of heating. HfSe₂ is highly reactive in air. HfSe₂ surface showed protrusions up to 60 nm on exposing in air for 1 day¹⁴⁹. In presence of air, the progressive oxidation of Hf happens due to the higher electronegativity of Oxygen in compare to the Selenium. The study showed that the Se-Hf ratio dropped from 2:1 to 1.4:1 in just 48 hours period.

The exfoliated samples were left in ambient condition for 24 hours. A slight change in color contrast was observed after 24 hours in air as shown in figure 2b. The change in color contrast clearly indicates phase transformation of HfSe₂ due to the replacement of Selenium atoms by oxide atoms¹⁵⁰. Then the samples were heated at different temperatures and observed further change in color contrast. Figure 5.2 shows the optical images of the HfSe₂ samples heated at different temperatures.

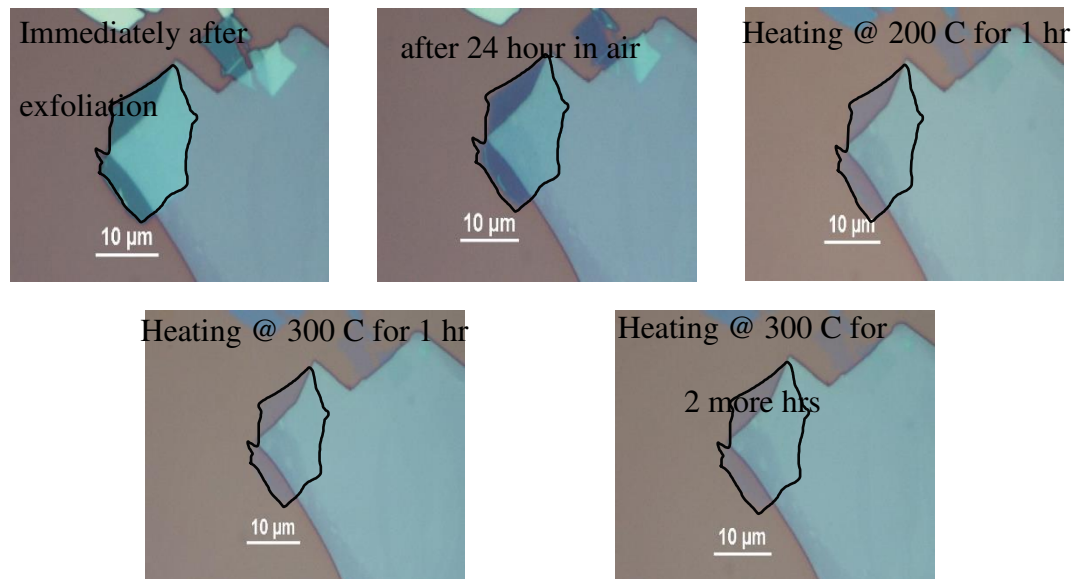


Figure 5. 2. Optical images of the HfSe_2 sample (inside solid area) on the top of Graphite a) immediately after the exfoliation, b) after exposing 24 hours in air, c) heating for 1 hour at 200°C in air, d) heating for 1 hour at 300°C and e) for 2 more hours at 300°C .

After exposing in air for 24 hours the color of the HfSe_2 samples changed slightly as shown in figure 1b. Then the samples were heated in hot plate subsequently at 200°C for 1 hour, 300°C for 1 hour and finally 300°C for 2 more hours to increase the uniformity and speed of oxidation process. The color contrast of the samples was changed with the increase in temperature (figures 1c – 1e). The surface roughness of the samples was decreasing with increase in temperature indicating more uniform oxidation (table 5.1). To further confirm the change, HfSe_2 samples at different stages of oxidation were characterized using non-contact AFM.

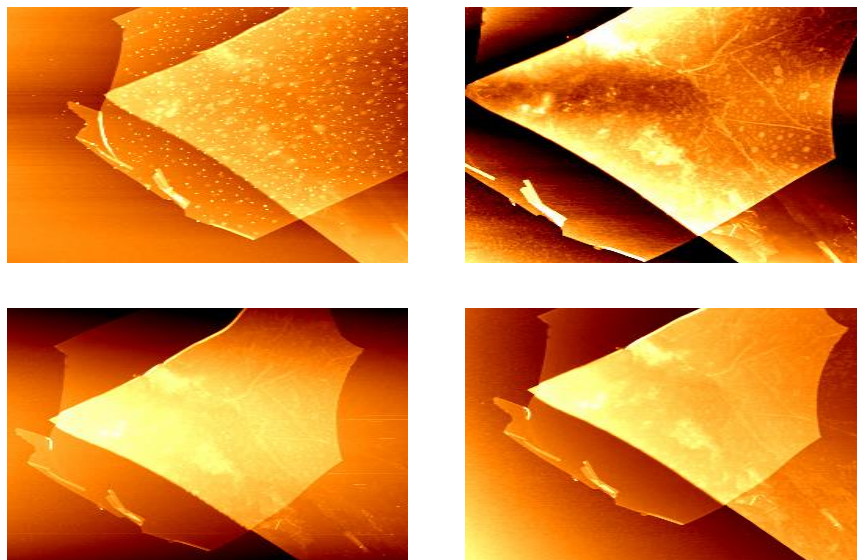


Figure 5. 3. AFM images of HfSe₂ sample a) after exposing in ambient condition for 24 hours, b) after heating 1 hour at 200° C, c) after heating for 1 more hour at 300°C and d) after heating 2 more hours at 300° C. Images were taken at the same area of the sample.

Thickness and roughness of the HfSe₂ surface were measured from AFM image of the samples at different stages of oxidation. Thickness and roughness, both were consistently decreasing with increase in oxidation temperature until it reached 300°C. At 300°C, the samples were heated twice, first for one hour and later for two hours. No significant change in thickness and roughness were observed for two hours heating. Figure 5.3 shows the AFM images of a sample (optical micrograph is shown in figure 2) at different stages of oxidation. The thickness and roughness measurement of two different samples are tabulated in table 1. Sample I was measured 14.34 nm thick after exposing in air for 24 hours. After heating the sample on the hot plate for 1 hour at 200°C, the thickness decreased to 12.48 nm. The sample was further heated for 1 hour on the hot plate at 300°C, thickness became 7.93 nm. We observed large change in thickness at this stage. The sample was further heated at the same temperature, 300°C, for 2 more hours, and the thickness was changed slightly to the 7.58nm. The roughness of the sample also decreased similarly. After 24 hours in air, roughness was 3.62 nm, which decreased to 1.14 nm after heating for 1 hour at

200°C and further decreased to 1.09 nm after heating at 300°C for 1 hour. On further heating at 300°C for 2 more hours, the roughness became 666 pm. Although there was not much change in thickness during the last 2 hours heating of the sample at 300°C, the roughness of the sample decreased significantly. For the measurements, same areas of the surface were chosen each time. A similar pattern of decreasing thickness and roughness is seen in the second sample as well. As seen in sample I, the thickness of the sample did not change significantly on heating for 2 hours at 300°C, but the roughness is decreased significantly. A similar pattern of change in thickness and roughness is observed in other samples as well.

		In air for 24 hours	Heating @ 200 C for 1 hour	Heating @ 300 C for 1 hour	Heating @ 300 C for 2 hours
Sample I	Thickness	14.34 nm	12.48 nm	7.93 nm	7.58 nm
	Roughness	3.62 nm	1.14 nm	1.09 nm	666 pm
Sample II	Thickness	12.84 nm	11.59 nm	6.62 nm	6.69 nm
	Roughness	4.81 nm	2.41 nm	1.31 nm	938 pm

Table 5. 1. Thickness and roughness measurement of HfSe₂ surface at different stages of the oxidation process. Same areas of the sample were chosen for each measurement.

After exposing the HfSe₂ sample in air for 24 hours, the sample surface was filled with bubbles (white dots on image). This is due to the accumulation of selenium atoms at the surface, which were replaced by the oxygen atoms to form an oxide. These bubbles (protrusions) appeared to fade out with an increase in temperature as seen from the subsequent AFM images. We compared the AFM image of the surface after exposing in air for 24 hours with the image after heating at 300°C for 3 hours to see whether the bubbles are gone completely or not. We choose an area of the HfSe₂ that is on Si substrate and studied the line profile. Figures 4c and 4d show the line profile of the surface along the line shown in figures 5.4a and 5.4b respectively. It is seen that the variation

is in multiple of tens of nanometer (~ 30 nm) in image 4a (after exposing 24 hours in air), while the variation in image 5.4b (after heating at 300°C for 3 hours) is seen less than 1nm indicating the removal of selenium accumulation from the surface and uniform oxidation of the sample.

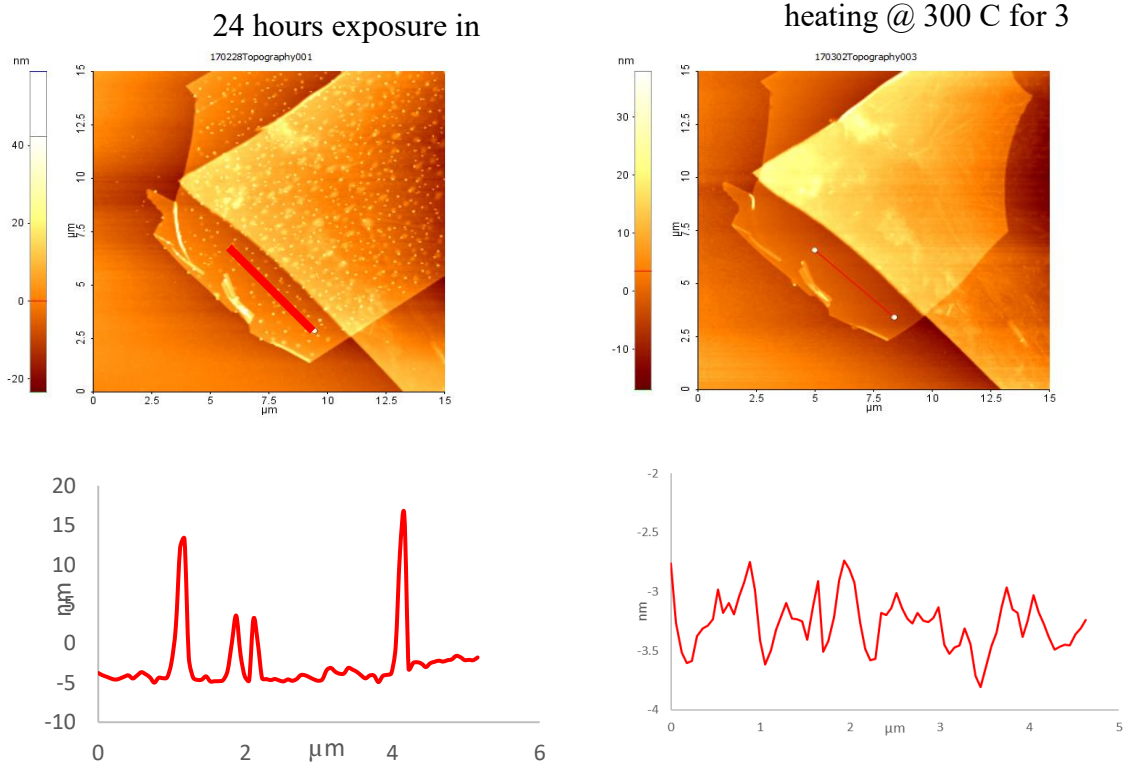


Figure 5. 4. a) AFM image of HfSe_2 sample after exposing in air for 24 hours. b) after heating at 300°C for 3 hours. c & d) line profile of the surface of the sample along the red line of the sample a & b.

During previous tests, the sample was oxidized in different stages (24 hours exposure in air, 1hour heating at 200°C , 1hour heating at 300°C and 2 hours heating at 300°C). The thickness and roughness of the sample were found to be changed significantly during the heating at 300°C . The change during previous stages were nominal. So, we skipped the previous oxidation stages and directly oxidized the sample by heating on the hot plate at 300°C for 3 hours. Figure 5.5 shows the images of the sample heated immediately after exfoliation and quick AFM characterization.

The HfSe₂ sample was transferred over the multi-layer Graphite using PDMS assisted dry transfer. After transfer, the sample was characterized using AFM and heated on the hotplate at 300°C for 3 hours in ambient environment. The devices were again imaged after oxidation.

Optical image shows the change in color without any change in shape of the sample. Change in color is quite significant on heating at 300°C for 3 hours (figures 5.5a and 5.5b). Figure 5c and 5d are the AFM images of figures 5.5a and 5.5b respectively. The topography of the sample was same but the thickness was changed from 20.8 nm, before oxidation, to 12.4 nm, after oxidation. The change in thickness was in close agreement with the thickness change during previous oxidation. Figure 5.5e and 5.5f are the 2µm x 2µm image taken from the same area of the device 5.5a and 5.5b before and after the oxidation. The big bubbles on figure 5.5e (before oxidation) completely disappeared in figure 5.5f (after oxidation) and the surface looked smoother indicating the removal of the selenide accumulation. The measurement of the roughness of the sample, mean square fluctuation, was decreased from 3.6 nm to 471 pm manifesting the uniformity of transformed oxide. The change in thickness and roughness of the samples were consistent with the previously studied several stages oxidation. After careful consideration of the results obtained from oxidation at different condition, we were convinced that similar to the cases of Ta₂O₅ and TiO₂^{151,152}, Hfse₂ as well oxidize and completely convert to HfO₂ upon heating at 300°C in ambient condition for 3 hours.

Before Oxidation

70

After Oxidation

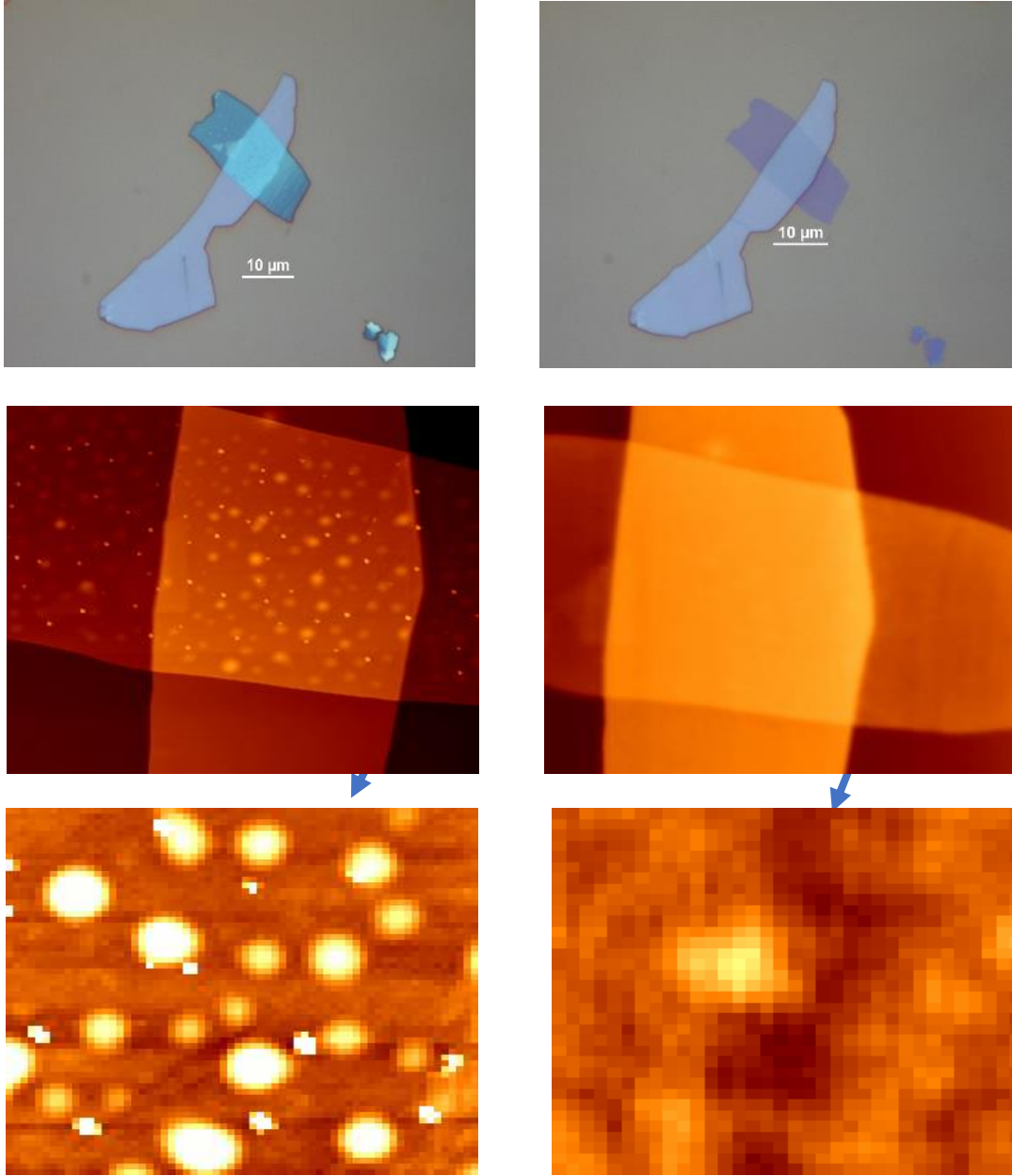


Figure 5. 5. Optical image of HfSe₂ on the top of multilayer Graphite a) immediately after transformation b) After performing oxidation by heating at 300°C in ambient condition for 3 hours. AFM image of the same device c) immediately after transformation d) After performing oxidation. 2x2 image of the same area of the device e) before and f) after oxidation.

We carried out the systematic investigation of the thickness of HfO₂ sample after oxidation, as a function of the thickness of HfSe₂ sample before oxidation. Figure 5.6 shows the thickness of HfO₂ as a function of the thickness of HfSe₂. Experimental data has been plotted using the data

obtained from the AFM image analysis (shown in table 5.2). For theoretical curve, mass density formula has been used. The molar mass of HfO_2 and HfSe_2 are found to be 210.49 gm/mole and 336.43 gm/mole from the literature. The density of HfO_2 and HfSe_2 are given as 9.68 gm/cm³ and 7.50 gm/cm³. Using, $\text{Volume} = \text{Mass} / \text{Density}$, we found the volume per mole for HfO_2 and HfSe_2 as 21.75 cm³ and 44.86 cm³. As the topography of the sample has not been observed changing (as seen from AFM images), change in volume is solely due to the change in thickness of the sample. Using these two volumes, we found the conversion factor for transformation from HfSe_2 to HfO_2 as 0.48. The detail calculation of the conversion factor is given in table 5.3. The theoretical curve is plotted with the conversion factor as a slope and passing through (0,0). The experimental data points seem to be slightly higher in comparison to the theoretical values, indicating the density of HfO_2 after oxidation is slightly lower than that of crystalline HfO_2 , suggesting the amorphous nature of the transformed oxide.

Thickness before oxidation (nm)	Thickness after oxidation (nm)
7.70	5.50
7.80	6.70
12.50	8.44
12.80	6.69
14.30	7.58
19.20	9.04
20.80	12.40
23.70	13.80

Table 5. 2. Thickness of Hafnium samples immediately after exfoliation (HfSe₂) and after heating in air for 3 hours at 300° C.

	HfSe ₂		HfO ₂
molar mass (g/mol)	336.43		210.49
density (g/cm ³)	7.50		9.68
Volume per mole	44.86		21.75
Conversion ratio		0.48	

Table 5. 3. Calculation of conversion factor on the basis of mass density relation.

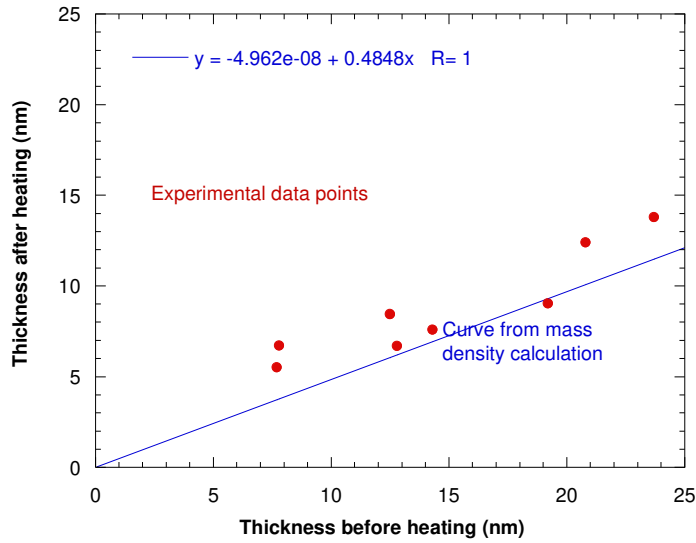


Figure 5. 6. Thickness profile of conversion of HfSe_2 into HfO_2 . Red dots are the actual data points obtained from the experiment. Blue curve has been obtained using 0.4848 as the slope origin as the starting point.

To measure the capacitance of thermally converted HfO_2 , we fabricated the MIM junction diodes. For MIM junction diodes, we used Graphite or Ti/Pt as the bottom electrode. We stacked the mechanically exfoliated HfSe_2 onto the bottom electrode using PDMS assisted dry transfer method. The substrate was then heated at 300°C for 3 hours in air. Then electrodes were fabricated and Ti/Au were deposited to make the electric connection as shown in figure 5.7. Figure 5.7a shows the schematics of MIM junction diode with HfO_2 as a dielectric layer between Ti/Pt or few-layer Graphite and Ti/Au electrodes. HP 4284A precision LCR meter is used to measure the capacitance of the dielectric. It has a frequency range from 20 Hz to 1 MHz with different mode of measurements. Capacitance is measured by sweeping the bias voltage at different frequencies level by applying low AC system voltage (50 mV to 100 mV). The capacitance is measured in Cp:D

configuration to minimize the parasitic capacitance effects. To measure the capacitance more precisely, the recorded measure value was set at least average of 8 consecutive measurements.

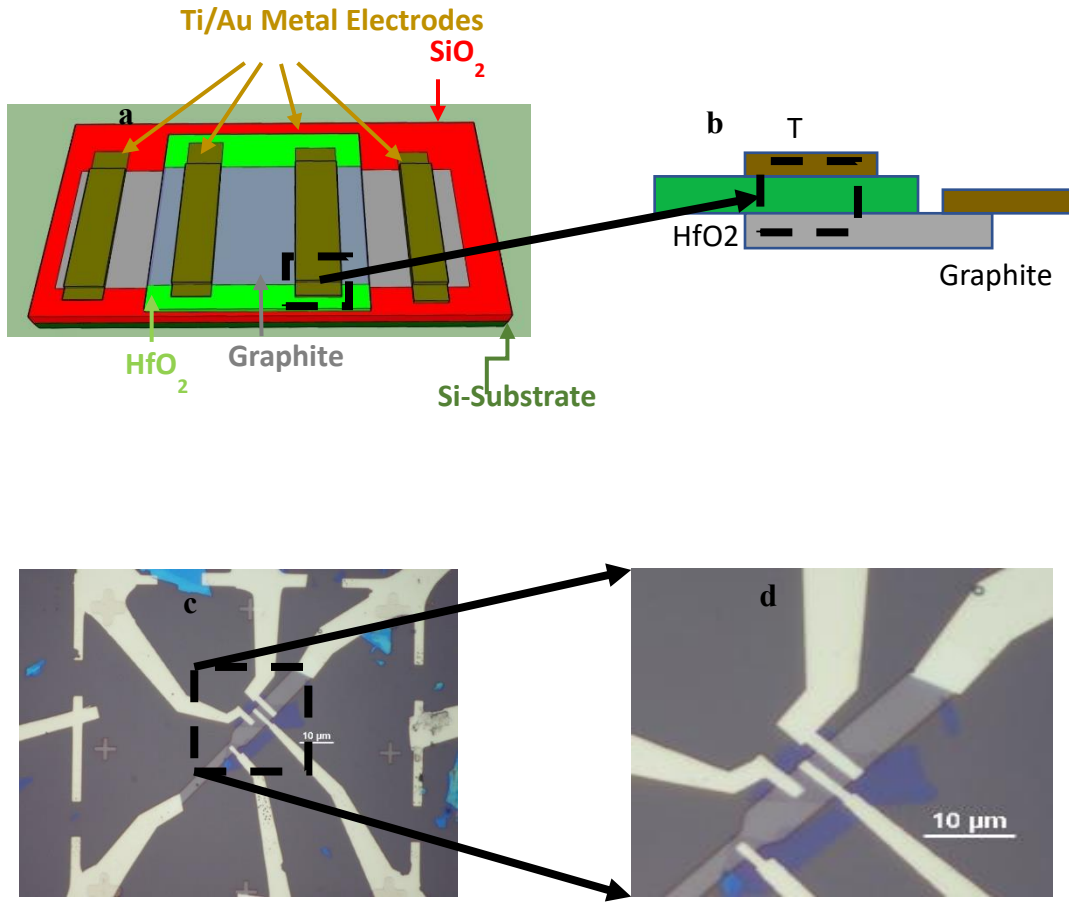


Figure 5. 7. a) Schematic diagram of MIM junction, b) cross-sectional view of MIM junction, which forms a parallel plate capacitor, c) MIM junction with Ti/Pt as a bottom electrode and HfO₂ as a dielectric (insulator) and Ti/Au as a top electrode, d) Magnified part of image c.

MIM junction forms a parallel plate capacitor with the bottom and top electrodes work like two plates of a capacitor (figure 5.8). The capacitance of the parallel plate capacitor is given as,

$$C = \kappa \epsilon_0 \frac{A}{t_{ox}}$$

Where A is the area of the capacitor plate, t_{ox} is the distance between two plates, κ is the dielectric constant and ϵ_0 is the permittivity of free space and has the value 8.85×10^{-12} F/m. In our case, A is the area of electrode and t_{ox} is the thickness of the dielectric layer. For a given dielectric, κ is a constant, t_{ox} is constant and ϵ_0 is always constant. That means the capacitance of a given dielectric varies linearly with the area of the electrode, and the slope of the C versus A curve gives the dielectric constant of the material.

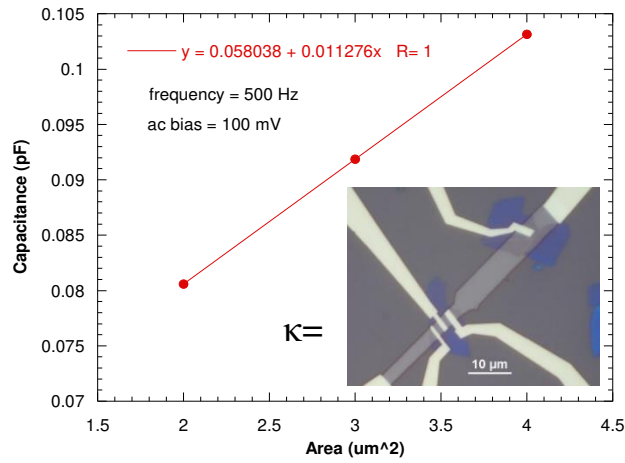


Figure 5. 8. Capacitance versus Area plot of MIM junction diode with thermally converted HfO_2 as a dielectric layer sandwiched between Ti/Pt and Ti/Au electrodes. Inset shows the optical micrograph of the device.

The capacitance vs area plot for a MIM junction device is shown in figure 5.8. The bottom electrode was composed of 5 nm Ti and 15 nm Pt while top electrode was composed of 5 nm Ti followed by 45 nm of Au. The C-V measurement was done for the dielectric of thickness 10 nm at frequency 500 Hz with an AC excitation voltage 100 mV. Capacitance was measured sweeping DC voltage from -1V to 1V and vice versa with the step size of 0.05V. Capacitance value was independent of voltage and average of all values was taken to calculate the capacitance. Area of the electrode defined the area of a plate of the capacitor. Using capacitance relation, from the slope

of the linear fit, the dielectric constant of HfO_2 was found ~ 11.5 , which is almost 3 times the value for SiO_2 ¹⁵³ and h-BN¹⁵⁴.

To further understand the thermally oxidized HfO_2 , we performed I-V measurement to investigate the leakage current as a function of the applied field. We used Keithley 4200 Semiconductor parameter analyzer to measure the electric properties of the device. The devices with Ti/Au electrodes are kept in Lakeshore cryogenic probe station chamber and pumps it overnight to reach the pressure down to $\sim 1 \times 10^{-6}$ Torr. The Keithley 4200 parameter analyzer is used to characterize its electrical properties. The current is measured by applying voltage once from 0 to positive voltage and next in another direction from 0 to negative voltage. The voltage value was increased until sudden jump in current was observed. The optical micrograph, AFM image and I-V plots are shown in figure 5.9. Figure 5.9a shows the MIM junction device used for the I-V measurement. AFM image of the device after oxidation shows the smooth surface of the dielectric on the top of Ti/Pt bottom electrode. For this device, the thickness of the dielectric was 10 nm. The area of the electrodes was $2 \mu\text{m}^2$, $4 \mu\text{m}^2$, $6 \mu\text{m}^2$, $8 \mu\text{m}^2$ respectively. Figure 5.9c1 represents the plot when a positive potential is applied across electrode L1 and the bottom electrode. The measurement was stopped when drain current suddenly starts to increase. We found the leakage current suddenly start to increase at voltage 6.8 V. Figure 5.9c2 represents the plot when negative voltage sweep was performed between the bottom electrode and the top electrode L1. Leakage current started to build up at 5.8 V. As seen from the plots on figure 5.9, the current through the HfO_2 dielectric layer is very small (of the order of 10^{-10} A) for a large range of applied voltage up to 6V. This clearly indicates the device with HfO_2 dielectric layer exhibits low leakage current and is favorable for large back gate voltage range.

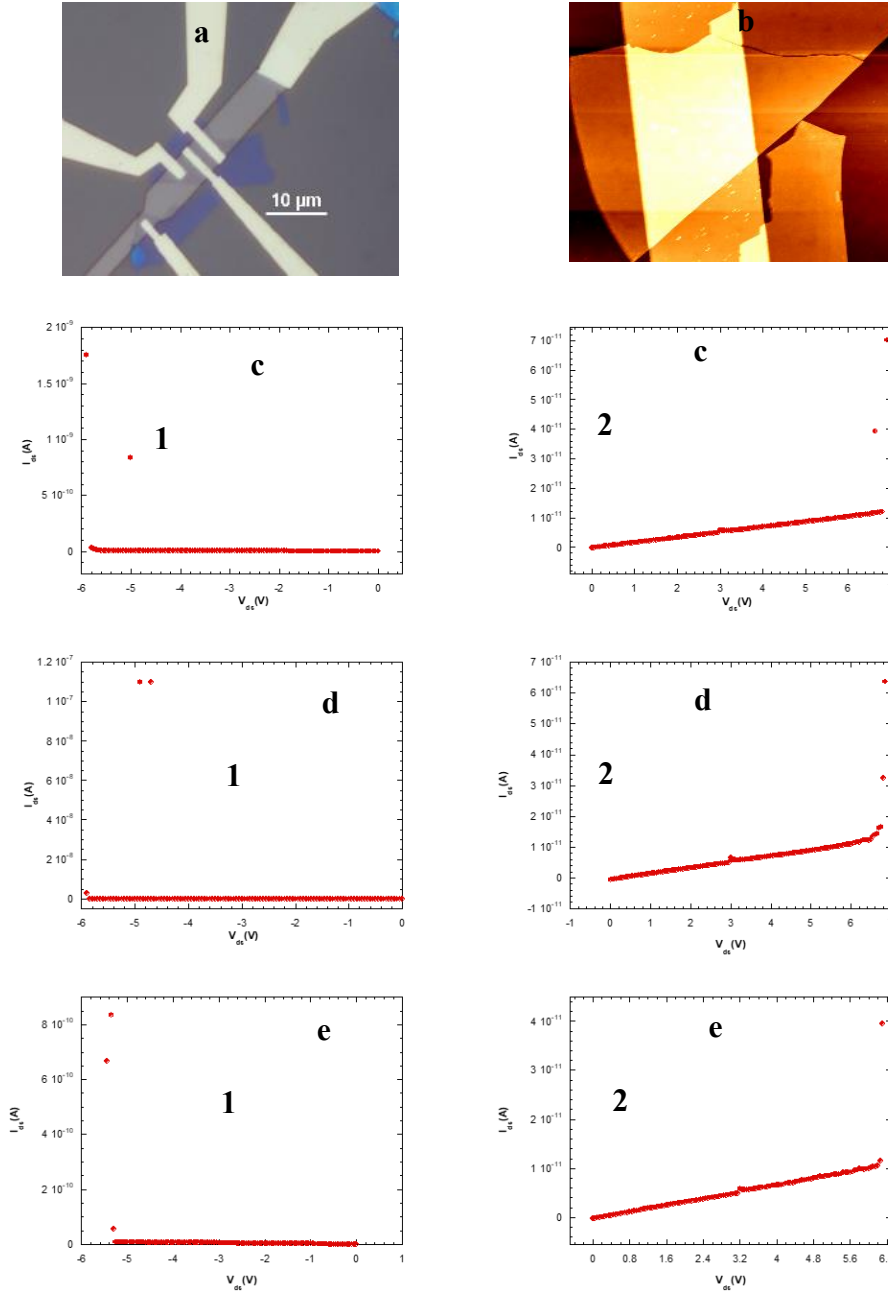


Figure 5.9. a) Optical micrograph of MIM junction diode, b) AFM image of the diode, c1) positive voltage sweep (0V - 1V) on electrode L1, c2) negative voltage sweep (0V - -1V), d1, d2) sweep on electrode B, e1, e2) sweep on electrode T.

The value of applied voltages until leakage current starts to build up for different voltage sweep in different electrodes obtained from figure 5.9 is tabulated in table 5.4.

Electrode	B	L1	T
Area(μm^2)	2	4	8
Applied Voltage (positive voltage sweep)	6.8	6.8	6.3
Applied Voltage (negative voltage sweep)	5.8	5.9	5.3

Table 5. 4. Value of applied voltages for the study of leakage current for the device shown in figure 9.

From the table 5.4, the average applied voltage for the thermally oxidized HfO_2 before leakage current suddenly start to build up is found ~ 6.15 V. From the measurement it is observed that the thermally converted HfO_2 have small leakage current of the order of 10^{-10} A up to the applied field of ~ 6 MV/cm making it suitable to use in FETs as a gate dielectric.

5.3 Summary

In summary, we successfully transformed two dimensional HfSe_2 into HfO_2 using thermal oxidation method. The transformation was confirmed optically by monitoring the color contrast of the sample and from the AFM characterization. The thickness of the phase transitioned HfO_2 is consistent with the expected thickness obtained from the mass-density relation. The surface of the oxide was clean and smooth. We fabricated several devices using HfO_2 as a dielectric layer and performed C-V, I-V characterizations. The dielectric constant of the oxide is found 11.5 and can withstand the higher electric field up to 6 MV/cm. The lower leakage currents at field value up to 6 MV/cm ensures the phase transitioned HfO_2 can be useful to decrease the leakage current and increase the gate voltage range for the 2D electronic devices.

FUTURE WORK

During this dissertation work, we systematically studied the thermal oxidation of Metallic TMDCs like TaS₂, HfSe₂, TiS₂. These metallic TMDCs unlike the semi-conducting TMDCs (MoS₂, MoSe₂, WSe₂ etc.) are air sensitive and oxidize easily. We successfully converted metallic TMDCs into their oxides by heating the samples in air. Further, we characterized the thermally oxidized dielectric and found the dielectrics are atomically flat, spatially uniform, and forms a nearly charge-trap free interface with the channel material. This new approach enables us to assemble high-quality dielectric on top of pristine TMDCs channels to form top-gated FETs while circumventing the constraints of ALD methods.

C-V characterization of chemically converted Ta₂O₅ dielectric showed the dielectric constant ~ 15.5 . MoS₂ FETs fabricated using thermally oxidized thin Ta₂O₅ as gate dielectric show nearly hysteresis-free transfer characteristics, suggesting high interface quality. MoS₂ FETs with the thermally oxidized Ta₂O₅ top-gate dielectric demonstrate a current on/off ratio of $\sim 10^6$, a high field-effect mobility $> 60 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, and a near ideal subthreshold swing (SS) of $\sim 61 \text{ mV/dec}$ at room temperature, along with pronounced drain-current saturation in their output characteristics. Thermally converted Ta₂O₅ showed impressive role to enhance the performance of MoS₂ channel. But as Ta₂O₅ has a low band gap ($\sim 4.5 \text{ eV}$), we could measure the transfer characteristics for an only small range of back gate voltage (up to 3 V) without increasing leakage current.

HfO₂ has a large band gap ($\sim 5.7 \text{ eV}$) in comparison to the Ta₂O₅, which gives us the freedom to increase the range of the voltage without increasing the leakage current. The dielectric constant of the HfO₂ is slightly lesser than the Ta₂O₅ but having large band gap is useful to decrease the leakage current for large back gate voltages. Similar to the Ta₂O₅, we successfully converted HfSe₂

into two dimensional HfO_2 by using thermal oxidation and characterized them. The dielectric constant of the thermally oxidized HfO_2 is found to be 11.5, as expected slightly lesser than that of Ta_2O_5 (~15.5). Ta_2O_5 , having a large band gap, decreased the leakage current as we applied higher voltages. We could apply the voltage up to 6 V without significantly increasing the leakage current. The breakdown field of the HfO_2 is found 6.15 Mv/cm, which is almost 3 times the breakdown field of SiO_2 .

As HfO_2 can operate successfully for large voltages, without appreciably increasing the leakage current, it will be useful to fabricate FETs with thermally converted HfO_2 as a dielectric. These FETs with HfO_2 will work for a large range of gate voltages. Since, the thermal oxidation method produces ultraclean, spatially flat two-dimensional dielectrics, we can fabricate both top and bottom gated FET using PC pickup and dry transfer methods circumventing the problems with other forms of dielectric integration (ALD, CVD etc.).

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ABSTRACT

DOPED AND CHEMICALLY TRANSFORMED TRANSITION METAL DICHALCOGENIDES (TMDCS) FOR TWO-DIMENSIONAL (2D) ELECTRONICS

by

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August 2018

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Transition metal dichalcogenides (TMDCs) as the semiconductor counterparts of graphene have emerged as promising channel materials for flexible electronic and optoelectronic devices. The 2D layer structure of TMDCs enables the ultimate scaling of TMDC-based devices down to atomic thickness. Furthermore, the absence of dangling bonds in these materials helps to form high quality heterostructures with ultra-clean interfaces. The main objective of this work is to develop novel approaches to fabricating TMDC-based 2D electronic devices such as diodes and transistors. In the first part, we have fabricated 2D p - n junction diodes through van der Waals assembly of heavily p -doped MoS_2 (WSe_2) and lightly n -doped MoS_2 to form vertical homo-(hetero-) junctions, which allows to continuously tune the electron concentration on the n -side for a wide range. In sharp contrast to conventional p - n junction diodes, we have observed nearly exponential dependence of the reverse-current on gate-voltage in our 2D p - n junction devices, which can be attributed to band-to-band tunneling through a gate-tunable tunneling barrier. In the second part, we developed a new strategy to engineer high- κ dielectrics by converting atomically thin metallic 2D TMDCs into high- κ dielectrics because it remains a significant challenge to deposit

uniform high- κ dielectric thin films on TMDCs with ALD due to the lack of dangling bonds on the surfaces of TMDCs. In our study, we converted mechanically exfoliated atomically thin layers of a 2D metal, TaS₂ (HfSe₂) into a high- κ dielectric, Ta₂O₅ (HfO₂) by thermal oxidation. X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), energy dispersive spectroscopy (EDS), and atomic force microscopy (AFM) were used to understand the phase conversion process. Capacitance-voltage (C-V) measurements were carried out to determine the dielectric constant of thermally oxidized dielectrics. We fabricated MoS₂ field-effect transistors (FETs) with thermally oxidized ultra-thin and ultra-smooth Ta₂O₅ as top-gate and bottom-gate high- κ dielectric layers. We observed promising device performance, including a nearly ideal sub-threshold swing of ~ 61 mV/dec at room temperature, negligible hysteresis, drain-current saturation in the output characteristics, a high on/off ratio $\sim 10^6$, and a room temperature field-effect mobility exceeding $60 \text{ cm}^2/\text{Vs}$. To further reduce the leak current and improve the device performance, we have also investigated the chemical transformation of HfSe₂ to HfO₂ high- κ dielectric, which has significantly larger band gap than Ta₂O₅.

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2D Mater. **4**, 31002 (2017).