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Fabrication of p-type Double gate and Single gate Junctionless silicon nanowire transistor by Atomic Force Microscopy Nanolithography

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Abstract. In this work, we have investigated the fabrication of Double gate and Single gate Junctionless silicon nanowire transistor using silicon nanowire patterned on lightly doped (10^5 cm^{-3}) p-type Silicon on insulator wafer fabricated by Atomic force microscopy nanolithography technique. Local anodic oxidation followed by two wet etching steps, Potassium hydroxide etching for Silicon removal and Hydrofluoric acid etching for oxide removal, were implemented to reach the structures. Writing speed and applied tip voltage were held in 0.6 μm/s and 8 volt respectively for Cr/Pt tip. Scan speed was held in 1.0 μm/s. The etching processes were elaborately performed and optimized

by 30%wt. Potassium hydroxide + 10%vol. Isopropyl alcohol in appropriate time, temperature and humidity. The structure is a gated resistor turned off based on a pinch-off effect principle, when essential positive gate voltage is applied. Negative gate voltage was unable to make significant effect on drain current to drive the device into accumulation mode.

Introduction

Scaling of the transistors has become a crucial area in nanotechnology, which provided several obstacles in the course of shrinking the size of the devices. Scaling down the size of the transistors and the gate length of metal–oxide–semiconductor field-effect transistors (MOSFETs) raised several issues such as short channel effect (SCE), leakage current or low current. Several methods suggested to conquer these problems, such as high κ dielectrics [1], metal gate electrodes [2], and new transistor architectures based on silicon-on-insulator (SOI), such as FinFETs [3] or gate-all-around FETs [4]. Junction less transistors (JLTs) appeared to be the new and promising alternative for the new generation of transistors [5-6]. The JLTs have a constant and high doping concentration through the source, the channel and the drain[6]. The principle of AFM nanolithography, using Local anodic oxidation (LAO) on SOI, has been described for the first time by Snow and Campbell et al. [7-8]. Ionica et al. [9] have remarkably reported the electrical characteristics of the devices made by AFM nanolithography. Also some recent works were performed to improve this method [10-11].

The widely used wet etching is still an applicable method, since it is more adaptable to the current CMOS technology. Tetramethyl-amino-hydroxide (TMAH) and potassium hydroxide (KOH) saturated in isopropyl alcohol (IPA) are two well-known etchant which used for etching of nanostructures fabricated by LAO technique [12]. TMAH is used since it ensures a very high selectivity ratio between Si/SiO_2 (etch rate 2000:1) [9] and KOH+IPA is used because of the better controllability and providing smooth structure after etching process [10, 13]. The fabrication of SGJLSNWT already has been reported briefly. We investigated the charge transmission [14-15] and

hysteresis effect [16] of the p-type side gate JLT device with simple structure, low doping concentration and no gate oxide layer. The conventional MOSFETs functions are strongly dependent on the oxide layer and the capacitance of the gate oxide layer, but for JLSNWTs, capacitance dependence does not have a strong effect [17]. Therefore, in our JLTs devices, lacking of the gate oxide layer could be acceptable. Moreover, it can eliminate the difficulty of the gate oxide layer stacking for very small size.

In this work we have modified the experimental method and elaborately investigated the effect of the experimental procedure on the device fabrication. This can be used as a guide for future experimental works in AFM nanolithography, including to the previous ones. In this matter, the preparation method, the impact of LAO parameters, Relative humidity (RH) and etching processes will be expressed. At the end, pinch-off effect for positive gate voltage and the effect of negative gate voltage on the channel will be investigated as well.

Methodology

The process of fabrication of Double gate (DG) and Single gate (SG) JLSNWT by means of AFM-LAO nanolithography on SOI substrate will be elaborately expressed. The fabrication process is divided into three separate and major steps which are shown in one flowchart in Fig. 1. After sample preparation and cleaning, the LAO process has been followed by two wet etching steps, KOH etching for Si removal and Hydrofluoric acid (HF) etching for oxide removal. The writing speed, scanning speed and applied tip voltage were optimized. The etching processes were also elaborately examined and optimized by 30%wt. KOH + 10%vol. IPA in appropriate time, temperature and humidity. The brief report of experimental process can be found in [14].

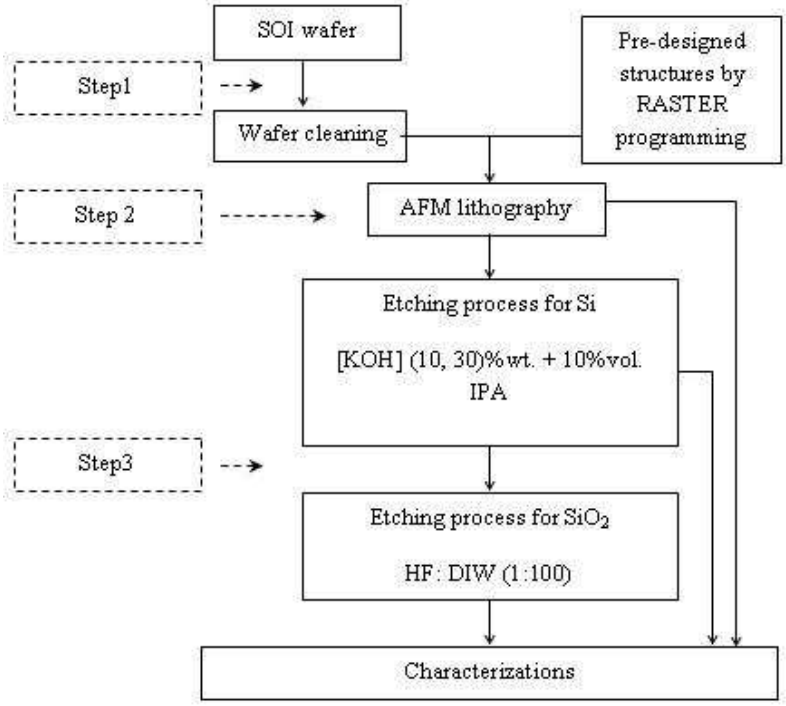

Fig. 1. Flow chart of methodology and steps of fabrication the device by AFM- LAO nanolithography.

Cleaning and preparation. The first step of fabrication is the cleaning process, which was applied by modifying the standard RCA technique [18]. Low doped (10^{15} cm−3) p-type (100)SOI wafer prepared using Unibond™ (Unibond International Ltd., Uxbridge, Middlesex, UK) process with a 145-nm buried oxide (BOX) thickness. The top Si layer has a thickness of 90 nm and a resistivity (ρ) of 13.5-22.5 Ω cm. During optimization of the cleaning process, the ratio of chemical concentration, temperature and time are the major parameters. The standard method and other researchers have suggested that the chemical ratio of 1:50 for HF: DIW for RCA method. However, in our case this ratio caused some roughness on the surface of the samples. The best ratio we found for our condition was 1:100 for HF: DIW. The temperature is also important. Any change more than 3 °C in temperature interval, exceeding the temperature of 80 °C or lowering below 77 °C during the cleaning process would give rise to inequality or even twisting of the sample surface. SOI with a thin Si layer found to be very sensitive to the heat treatment. The use of ultrasonic cleaning before applying the RCA method was very useful. Using the acetone/methanol washing before the RCA

cleaning also produces good results. The timing of immersing or even rinsing is also an important factor. For examples after each step the sample was immediately put into the beaker containing DIW to prevent it from long time air exposure which might cause the native oxide appearing on the surface of the sample. In addition, type and brand name of SOI wafer can be important in each step of the cleaning. Fig.2 shows the AFM images of the SOI sample before and after the cleaning process.

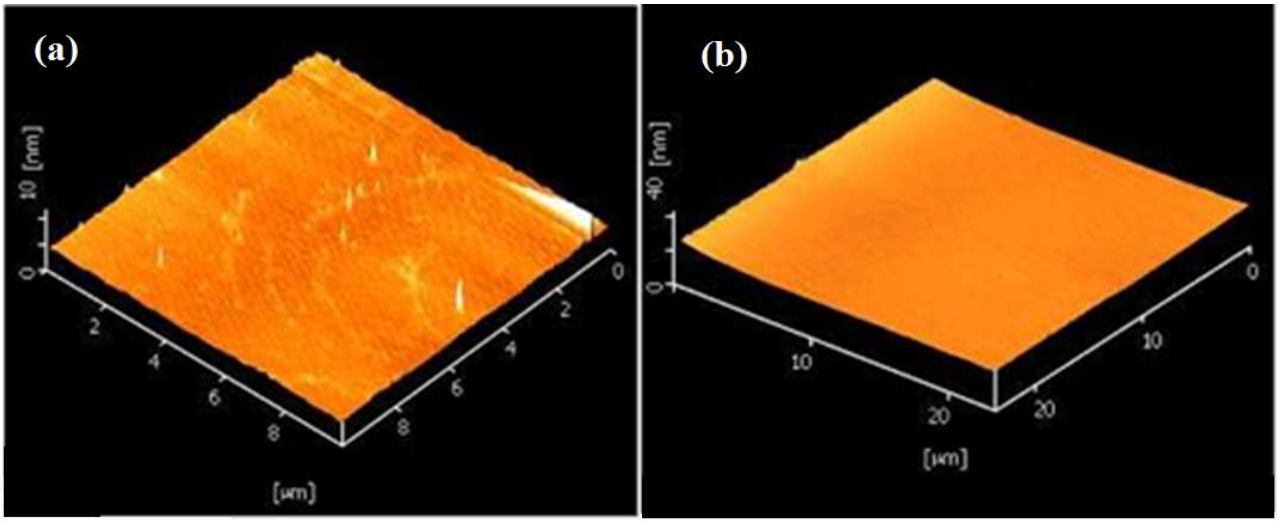

Fig. 2. AFM image of the SOI substrate (a) before and b) after optimized RCA cleaning process, native oxide and other contamination removal is recognizable after cleaning.

LAO parameters. The oxide growth mechanism can be described as the following [19]. After cleaning process Si-H bonds will be formed on the surface since the native oxides were removed. When the surface was de-passivated, the first layer of Si-Si bonds became polarized due to the high electron negativity of the OH^-. Then, the Si-Si bonds reacted to the polar H_2O molecules from humidity to form a monolayer of silicon oxide, SiO_2. It happens when the electric field is created between the first silicon oxide layer and the substrate by applying a voltage on AFM tip. Not only the electrical fields enhanced the OH^- formation, but also provide the correct direction to cause the OH^- diffusion through the oxide film. Writing speed and AFM tip voltage are two parameters to

optimize the LAO process. Fig. 3 shows the effect of applied voltage on the AFM tip (Au-coated) at a constant writing speed of 0.4μm/s (a,b),and for different writing speeds with the same applied voltage of 8V (c). High voltage (Fig. 3a,b) provides thicker oxide layer with more uniformity on the substrate surface. The best result was derived from the applied voltage of 8 V. On the other hand, low writing speeds can make wider oxidation effect on the substrate, whereas faster writing speed did not provide any oxidation effect on the substrate in 8V (Fig. 3c). For writing speeds of 1.0 and 1.5μm/s the oxidation tracks were not recognizable. In the case of gold (Au) coated AFM tip, the speed of 0.6μm/s and the voltage of 8 V were the optimized parameters. The scan speed was held in 1.0μm/s.

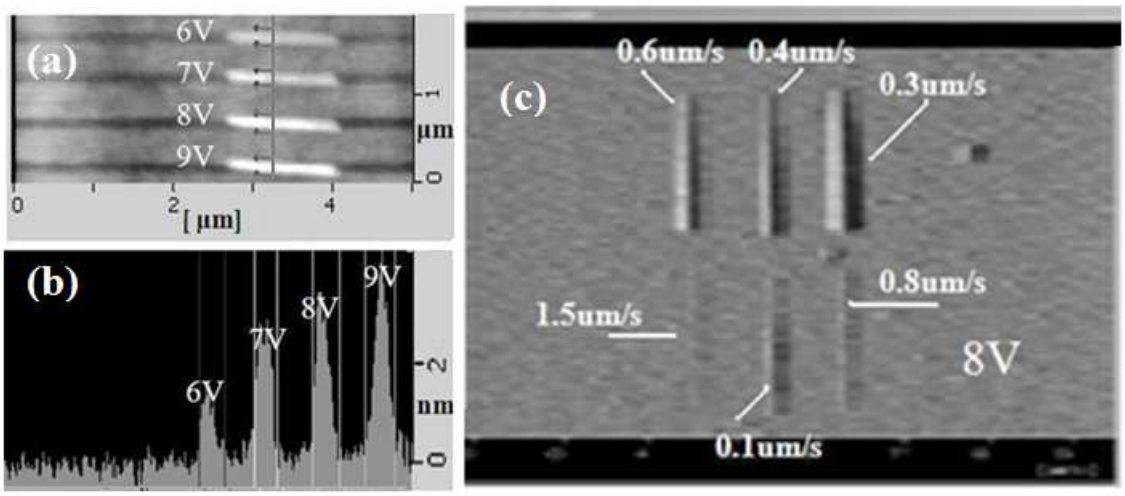

Fig. 3. Effective parameters during LAO process, a) and b) effect of different applied voltage on AFM tip and c) effect of different writing speed.

Relative humidity (RH). Another parameter that plays an important role in LAO is the RH, when RH% increased, the thickness of oxide increased simultaneously. The oxidation rate is very sensitive to the field strength at high RH%. The oxide thickness extremely depends on the humidity and the AFM tip voltage. In Fig. 4 for Au coated AFM tip, the relation between oxide thickness and RH% at room temperature with constant applied voltage of 8V is shown. Humidity and temperature are

affecting the device structure during patterning. In this experment, best patterning were found at the temperature range of 22 - 26 °C and between 65 - 68% for RH%. When RH% was increases beyond 70%, the rate of increasing oxide thickness was also incresed and a shadow effect was observed.

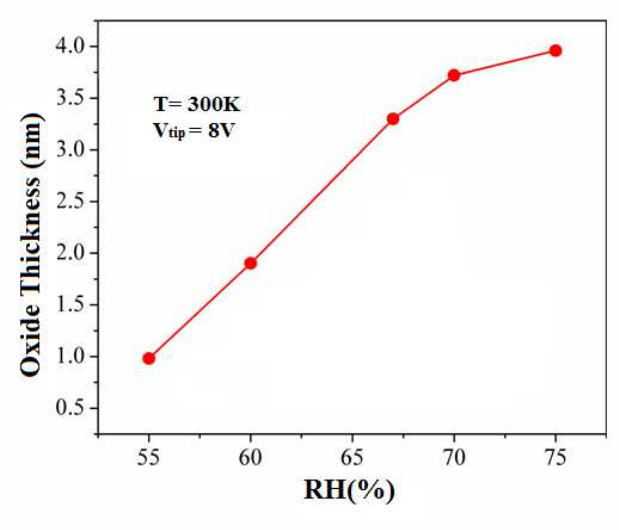

Fig. 4. Relation between oxide thickness and RH %, at room temperature (8V applied voltage).

These results support the previous findings on AFM nanooxidation about the influence of humidity on the growth of oxide over Si surface, when the other parameters were constant [19-21]. Fig. 5a and b, shows the AFM topography images of the pads prepared by LAO technique before and after the etching process. The presence of the shadow around the pad can be seen, which deformed the shape as well. This phenomenon had also been reported by researchers [22].

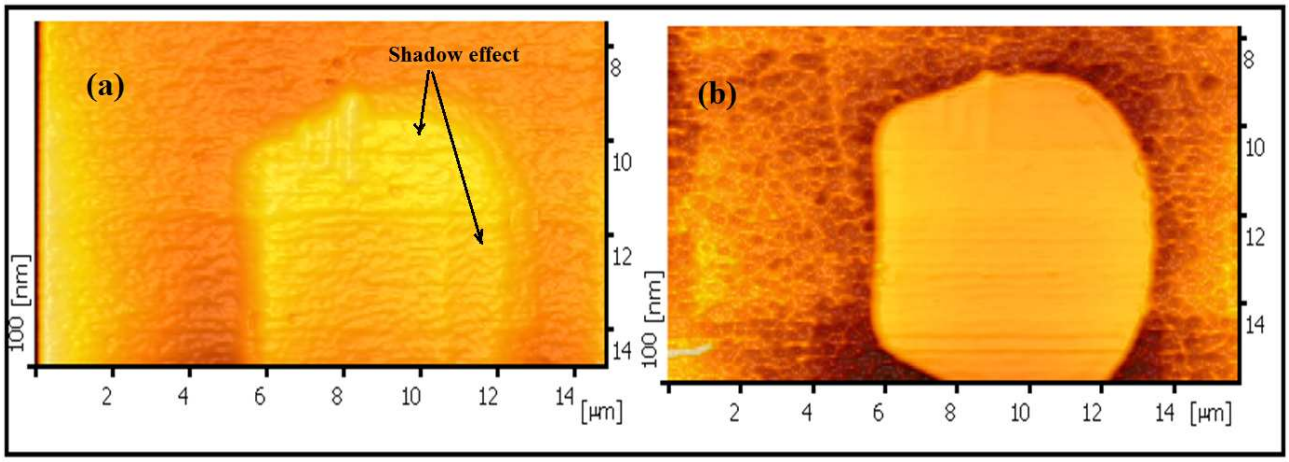

Fig. 5. AFM topography images of the pad with the shadow effect due to LAO in high RH %(a) after LAO and (b) after etching.

Effect of KOH etching on device fabrication. KOH wet etching is a very significant part in the fabrication of JLSNWT. In fact, having contamination, ill-etched or over etching structure was hardly avoidable in wet etching; accordingly, the accuracy and precaution are important. To remove the undesired Si area, KOH was used as the etchant. Referring to the previous reports in KOH wet etching [23-24], it can be seen that the surface roughness improved as the concentration of KOH increased. Fig. 6 (a-c) demonstrates AFM micrograph images of the etched substrates (SOI) under the different KOH percentage in solution (%wt). It can be seen that surface roughness changes as the %wt of KOH increases up to 40%. Lower %wt of KOH can cause the rougher surface compare to higher. IPA was used in this work as initiator. IPA reduces the etch rate by improving the surface roughness. It also can increase the controllability of the etching process[13] with higher uniformity of the surface roughness [23, 25]. Based on this work and the literatures for optimization, the best percentage of IPA added to the solution was taken as10% vol. in the KOH etchant. Apart from the concentration of the etchant, the immersing time and temperature are also playing important roles in obtaining the most optimum result for nanostructure formation. The etching effect of KOH (different concentration, 20% to 40% wt) on nanostructured SOI surface are shown in Fig. 6. The heating temperature was 63-65 °C and stirred at 600 rpm for 20-22 seconds. The surface roughness of the sample etched by 20%wt. KOH + 10%vol IPA (Fig. 6d) is more than the ones etched with 30%wt or 40%wt. KOH + 10%vol. IPA (Fig. 6 d,f). The structure etched by 30%wt KOH + 10%vol. IPA shows acceptable quality and sharpness taken as the optimized etching parameters. In fact, it would have anisotropic etching to the structure etched with KOH + IPA [26-27]. In anisotropic etching for (100) Si, the rectangular hole will form a pyramid shaped etch pit and the wall will be flat and angled.

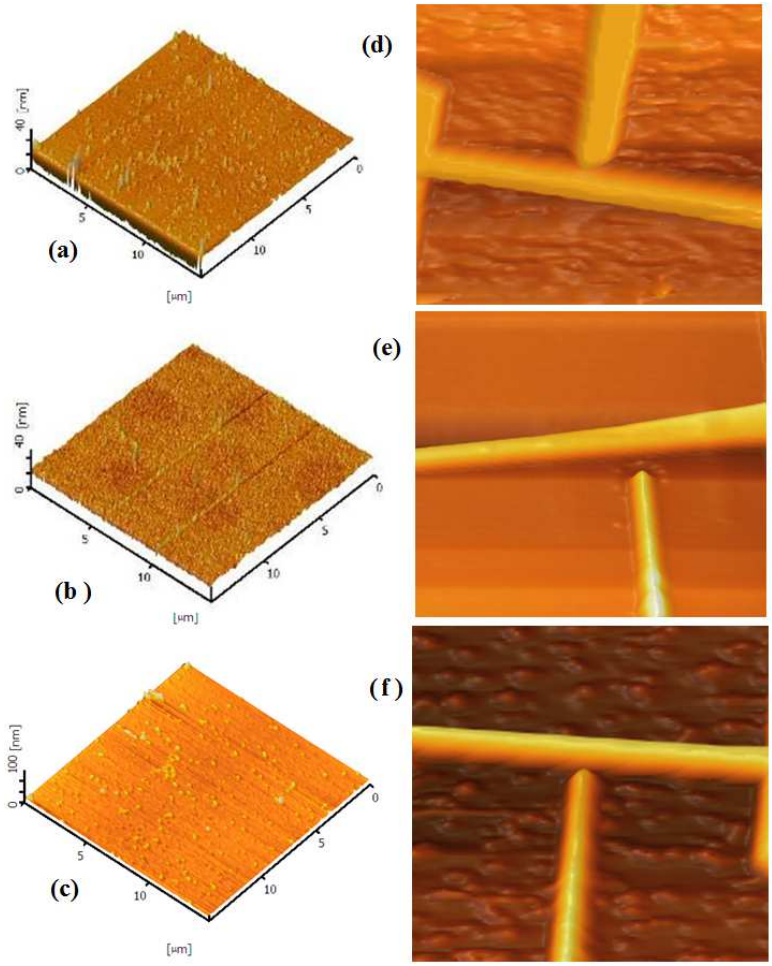

Fig. 6. AFM images of SOI surface etched with KOH: 20%wt (a), 30%wt (b) 40%wt (c), and AFM images of nanostructure etched with 20%wt. KOH + 10%vol. IPA (d), 30%wt. KOH + 10%vol. IPA (e) and 40%wt. KOH + 10%vol. IPA (f).

Fig. 7 shows the SEM images of two complete structures after etching by different concentration of KOH. Where, Fig. 7a shows the complete SG structure after optimized etching procedures. The over etching effect (Fig. 7b) on the structure for 40%wt. KOH + 10% IPA at 65 °C, after 30 seconds immersing time can be seen compare to the one etched by 30%wt KOH + 10% IPA (Fig. 7a). Some parts of the structure are gone due to re-etching with high concentration of KOH. So, it it can be predicated that, at higher concentration the over etching would be more damaging than the higher immersing time or temperature.

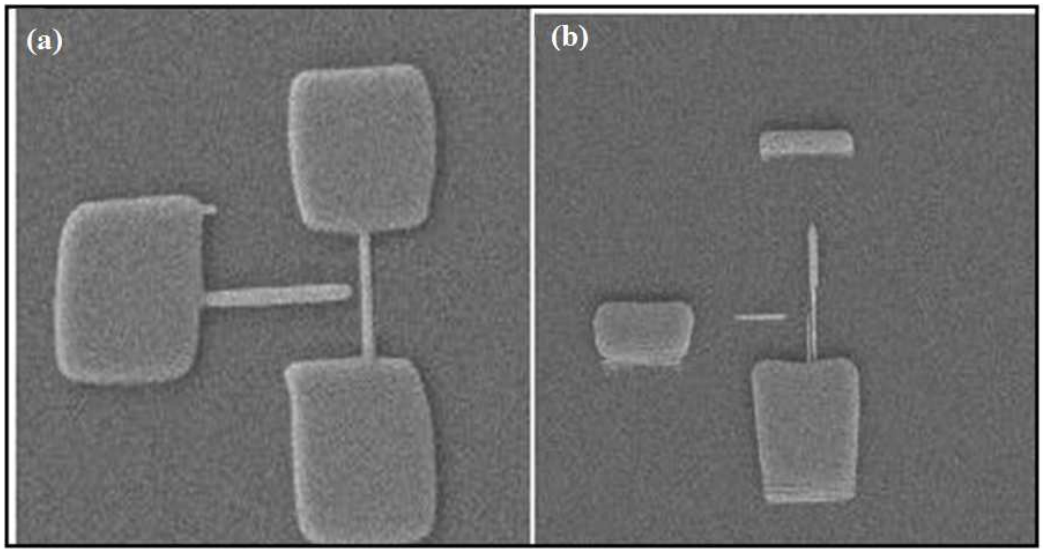

Fig. 7. SEM images of the complete structure after etching process a) etched by the solution of 30%wt KOH + 10% IPA at 63 °C, b) etched by the solution of 40%wt KOH + 10% IPA at 63 °C.

Optimum condition for etching. In this study, previous works for reaching to the optimum condition for KOH etching are considered and adopted [28-32]. The best condition according to the fabrication environment and other parameters is the solution of 30%wt KOH with 10%vol. IPA for wet etching at 63 °C, and 20 seconds for immersing time stirred at 600 rpm. Stirring the solution is to ensure the uniformity of the etching process.

Effect of oxide removal on device fabrication. The oxide removal was the last step for this fabrication method. After etching by KOH admixture with IPA solution, the oxide mask should be removed. For this purpose diluted solution of HF was used and the etching process was carried out at room temperature for 12-14 seconds and stirred at 600 rpm. During this process the oxide layer including the native oxide and the mask were removed.

Other parameter issues. In the fabrication process, in addition of major factors like preparation process, RH% or applying voltage and exposure time, there are some minor factors which are also able to make a significant effect. Like, the type of the AFM tip is very important. The tip must be specified for contact mode (tapping mode and non-contact mode tips are nonfunctional). For this experiment three types of contact mode tips which were Au coated, Cr/Pt coated conductive probe [14] and Al reflex coating were tested. The coating layer also enhances the laser reflectivity of the cantilever. In fact, Cr/Pt and Au coated probe showed the acceptable result [33-34], but the Al reflex coating did not provide any acceptable results. Another issue is the order of oxidation. By experiment, it was learned that we cannot make the whole pattern structure in one time unless, proper humidity in ambient air already been provided. Fig. 8 shows that the second pad (right side) is ill-shaped due to the lack of proper humidity in ambient air to make the perfect LAO.

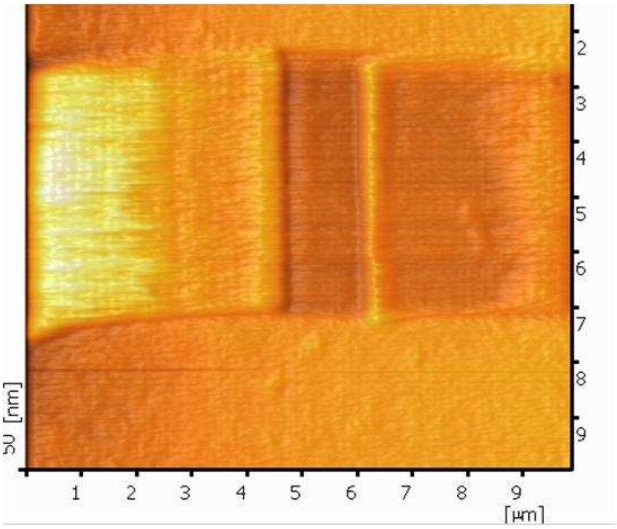

Fig. 8. AFM image of successive LAO, the right pad is ill-shaped due to the lack of proper humidity in ambient.

We also should considered about the unwanted native oxide layer on the top of the sample a while after the fabrication. The native oxide could be probably the important reason for hysteresis effect

we already reported [16]. In Fig. 9, SEM images for the over etching effect of the samples etched by 30%wt. KOH + 10% IPA for long immersing time (35-40 seconds) are shown. It can be recognized that some parts of the structure were removed due to longer immersing time.

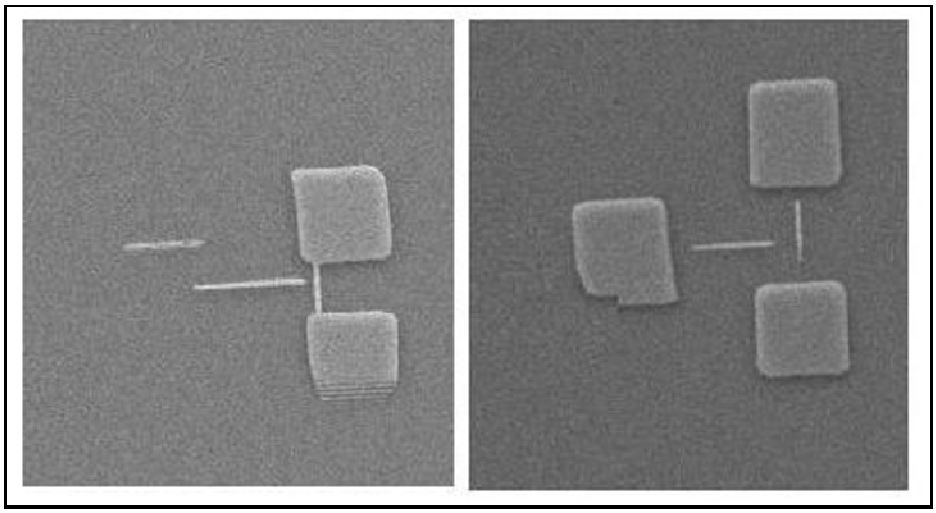

Fig. 9. SEM images of over etched sample after KOH/ HF etching due to longer immersing time.

Results and Discussions

Fig. 10, shows the AFM images of DG and SG JLSNWT after LAO. The whole structure of the source, channel and the drain are uniformly doped and made of p-type SOI with same thickness of 90 nm of the Si layer. Both devices have 100 nm for the channel width, the gate gap of 100 nm, 200 nm for the channel length and 4 μm for the distance between the source and drain. For the characterization of the device we used Agilent HP4156C SPA device or semiconductor parametric analyzer to monitor current-voltage relationship in different configurations. This analyzer has four medium power source monitor units (SMU), each of which can supply up to 50 V with maximum current of 100 mA and the current resolution of 1 pA. If proper cares are taken, such as the cable are kept in a dark and vacuumed environment (the SPA equipped with the vacuum facility), it is possible to measure down to 10 fA of current. For the side(s) gated measurement, first the side gate (V_G) was swept from -3 V to +3 V while the drain to source voltage (V_{DS}) has kept constant and negative because the channel is p-type.

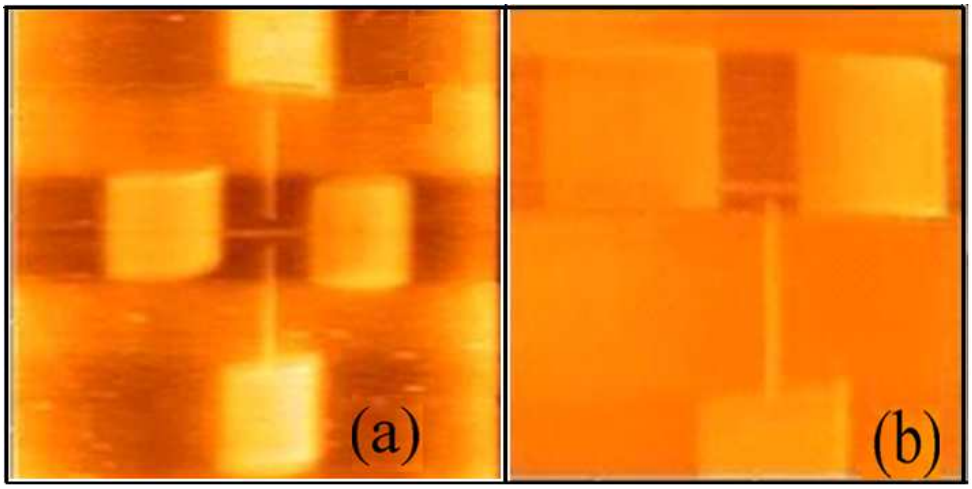

Fig. 10. AFM images of DG a) and SG b) JLSNWT.

I_D-V_G graphs for SG and DGJLSNWT at V_{DS}= -1, are shown in Fig. 11a. It illustrates the pinch-off effect [35] due to a positive lateral gate applying on the channel. It shows that the devices are in *on* state for zero gate voltage, and by increasing the positive gate voltage, the current will be dropped. The output characteristics (I_D-V_D) of the SGJLSNWT are shown in Fig 11b for different gate voltages. We can also observe the field effect under the lateral positive gate voltage. When the device is in *on* state and a positive gate voltage is applied to the lateral gate(s), the current value will be dropped and the channel starts to deplete at a sufficient positive gate voltage and the device reaches to the pinch off state [14, 36].The output characteristic shows that the drain current (I_D) does not significantly increase with the negative increase of the gate voltage. Also, high and positive threshold voltage indicates that the transistor is in *on* state with zero gate voltage.

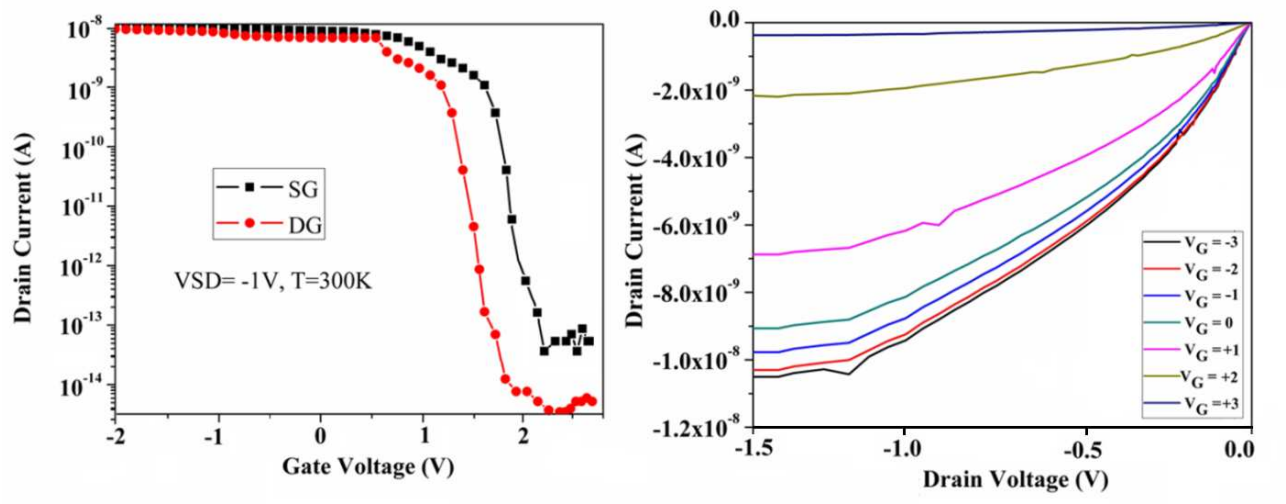

Fig. 11. (a) Transfer characteristic comparison for DG and SG structures, (b) output characteristics for SGJLSNWT at T= 300K.

In JLTs, the gate voltage controls the channel resistivity. Unlike the conventional MOSFETs where it is necessity of reverse bias for *off* state condition, in JLTs the channel is depleted by the gate electrostatic potential, producing high resistivity in the channel. The *on/off* ratio for DG and SGJLSNWT were 10^6 and 10^5 respectively (Fig. 11a). The Subthreshold swing (SS) for DG and SG structure were100 mV/decade and 167mV/decade respectively. High SS for the SG structure can be explained by asymmetry of the gate regarding to the channel [14] which as we expected for DG structure, the SS was decreased compare to SG structure. The pinch off effect occurred in +1.5 V and +2.5 V in DG and SG structure respectively. Low current is due to the low doping concentration profile (10^{15} cm $^{-3}$) though the channel, which is lower than reported current value of the high doping concentration profile ($5x10^{19}$ cm^{-3}) JLTs [6]. The MOSFETs or JLTs with high doping concentration mostly suffered with a high scattering effect or threshold voltage variation. Low channel doping can improve field-effect mobility. It can also be helpful to provide low *off* current or decrease the scattering effect and threshold-voltage variations [37]. Providing low *off* current can be more important for our device, since it is working on depletion mood and reaching to *off* state under the influence of lateral gate(s) voltage is very essential. Electrical characteristics of the devices have the

same trend compared to the reported cases fabricated by AFM nanolithography with nearly similar structure [7,9,38]. But, as we mentioned before, in none of the reported cases, the devices were used as the pinch off device.

Conclusions

The fabrication process of simple structures, as the DG and SG side gate junctionless Si nanowire transistors, on low doped SOI by improved AFM nanolithography was elaborately investigated. Sample preparation and cleaning process were modified from RCA method. The AFM-LAO parameters were optimized to achieve the best shape and structures. Two wet etching process implemented to extract the structure after LAO process. First, the KOH etching to remove the uncovered Si and then, the HF etching for Si oxide removal were used. The output and transfer characteristic of the device investigated showing the device is in *on* state for zero gate voltage. The pinch off effect observed for positive gate voltage and no significant current increasing for negative gate voltage.

Acknowledgements

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