Solar Energy Materials & Solar Cells 95 (2011) S2–S7

Contents lists available at ScienceDirect

Solar Energy Materials & Solar Cells

journal homepage: www.elsevier.com/locate/solmat

Three novel ways of making thin-film crystalline-silicon layers on glass for solar cell applications

I. Gordon *, F. Dross, V. Depauw, A. Masolin, Y. Qiu, J. Vaes, D. Van Gestel, J. Poortmans

imec, Kapeldreef 75, B-3001 Leuven, Belgium

ARTICLE INFO

Available online 30 December 2010

Keywords:
Thin film
Solar cell
Crystalline silicon
Porous silicon
Seed layer
Wafering

ABSTRACT

Monolithic solar modules made from thin-film crystalline-silicon layers of high quality on glass substrates could lower the price of photovoltaic electricity substantially. This paper describes three different approaches that we are currently investigating to address the challenge to form high-quality crystalline-silicon layers on glass substrates. The SLiM-Cut approach is a wafering technique that results in 50-micron thick layers with a minimum of material loss. We show that crack initiation can be used as a means to better control the lift-off process. The epifree approach involves the lift-off of ultra-thin monocrystalline films formed by reorganization of cylindrical macropore arrays in silicon upon annealing. So far, films with a thickness of around 1 μm and very simple cells with an efficiency of up to 4.1% have been achieved. Finally, a seed layer approach is presented based on the epitaxial thickening by thermal CVD of monocrystalline silicon layers bonded on glass-ceramic substrates. Very promising cell efficiencies of 11% and Voc values of up to 610 mV have been achieved using a very simple and non-optimized cell structure.

1. Introduction

Monolithic solar modules made from thin-film crystalline-silicon layers of high quality on glass substrates could lower the price of photovoltaic electricity substantially. Around one third of the price of wafer-based silicon solar modules is currently due to the cost of the silicon wafers themselves. Using thin crystalline-silicon films on inexpensive substrates as the active material instead of silicon wafers provides several advantages: First, the silicon consumption can be reduced drastically which should lead to a substantial cost reduction. Second, the use of very thin silicon layers allows achieving high cell efficiencies with silicon material of relatively lower crystalline quality compared to that used in wafer-based cells [1], on the condition that excellent light trapping can be achieved. Although imposing more severe demands on the quality of surface passivation to achieve the ultimate efficiency, reducing the thickness of silicon solar cells relaxes constraints on bulk quality and thus increases the efficiency limit. Along the years, the different limiting intrinsic phenomena were described in detail and the recent papers on the subject derive an efficiency limit fundamentally peaking for a thickness in the range of 40–60 μm [2]. Finally, if the crystalline silicon films can be formed directly on large-area glass, monolithic modules can be made like in other thin-film technologies, but with the demonstrated stable performance over time and irradiation of crystalline silicon. On top of these advantages, the knowledge about silicon wafer physics can easily be transferred and applied to crystalline silicon thin films. The main challenges of achieving highly efficient thin-film silicon modules are to develop a cost-effective process that enables to form a silicon layer of sufficient crystalline quality on a large-area glass substrate and to have an outstanding light trapping scheme in place.

This paper deals with the challenge to form a thin layer of high-quality crystalline-silicon on a glass substrate. Three different techniques to do so, currently being investigated at imec, are presented, namely a wafering technique called "SLiM-Cut", a lift-off approach based on reorganization of porous silicon that does not require epitaxial growth called "Epifree", and a seed layer approach based on the formation of a thin monocrystalline silicon layer that is epitaxially thickened.

2. SLiM-cut

The 'Stress induced LIft-off Method' (SLiM-Cut) is a kerf-free method for thin silicon fabrication, being developed at imec for photovoltaic applications [3]. This method makes particularly efficient use of bulk material by reducing kerf losses and producing wafers with a thickness of around 50 μm, thus cutting down the silicon cost.

The envisaged SLiM-Cut wafering method relies on a thermo-mechanical treatment: a high stress field is applied to a silicon substrate (preferably an ingot but so far only demonstrated on wafers) so that a crack propagates in the silicon substrate parallel to the

* Corresponding author. Tel.: +32 0 16 28 82 49; fax: +32 0 1628 15 01.
E-mail address: gordoni@imec.be (I. Gordon).

0927-0248/$ - see front matter © 2010 Elsevier B.V. All rights reserved.
doi:10.1016/j.solmat.2010.11.031

surface at a given depth. The top silicon layer is separated from the parent substrate and processed into a solar cell [3]. The parent substrate can be re-used. So far, we have routinely made SLiM-Cut samples with a size of 50 cm^2 in the laboratory and one can envisage making such samples with a size as large as a typical Si ingot. This method comprises a number of consecutive steps (Fig. 1):

- A material with a thermal expansion coefficient different from the one of silicon (e.g. metal) is deposited and bonded at high temperature on a bare silicon substrate.
- The structure is then cooled down. Upon cooling, the overlying layer induces a very high stress in the silicon. When stress intensity exceeds the fracture resistance of silicon, a crack propagates in the substrate. When the right conditions of applied metal paste with respect to composition and thickness, peak temperature (ranging between 700 °C and 850 °C) , and cooling rate (typically air quenching to room temperature) are met, the crack propagates in the direction parallel to the surface of the substrate and will spall off the top layer from the substrate.
- A cleaning treatment is carried out to dissolve most of the stress inducing layer: the resulting structure is thus flat and ready to be further processed.
- The parent wafer is conditioned to be re-used in the first step.

Some years ago, we demonstrated proof-of-concept cells made from SLiM-Cut wafers with a thickness of around 50 μm [4]. Applying a very simple process with no front side texturing and no rear-surface passivation (which are nonetheless crucial for such ultra-thin wafers), a 1 cm^2 solar cell was fabricated, exhibiting an energy-conversion efficiency of around 10%. Since then, our research has mainly focused on improving the material quality and the reproducibility of the process. In this paper we report on crack initiation as a means to better control the process.

During a typical SLiM-Cut wafering process, there are several crack-fronts nucleating on each sample. If a reproducible foil thickness is required, the plane of the crack needs to be tightly controlled. By inducing an artificial singularity in the silicon ingot before the stress application, one can eliminate random crack nucleation and reduce the required stress for crack propagation. In general, different shapes of stress concentrators can be used to force the onset of the crack propagation during lift off. This thus brings two advantages to the SLiM-Cut process

(1) It eliminates the stochastic nucleation of cracks at different depths.
(2) It reduces the required stress for the crack to grow, and thus diminishes the need for higher temperatures, improving the foil quality in terms of dislocation density and contamination.

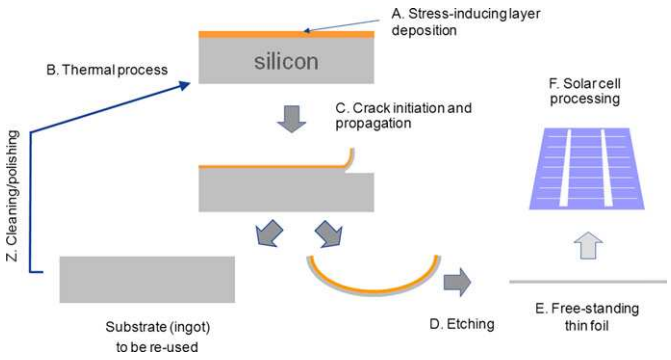

Fig. 1. Schematic of the SLiM-cut process.

Two types of cracks can be envisaged, one perpendicular to the final propagation direction, the other in the propagation plane.

Fig. 2 shows the results of three calculations obtained by the finite element method (FEM) of how the stress is affected by the sample and paste geometry at the edge of the sample. Since with the FEM the calculated stresses are averaged over the element, this calculation gives a relative estimate for a fixed element size, only allowing a relative comparison for the three geometries. The actual increase of the local stress is eventually determined by the crack shape: a low radius of curvature gives a high stress concentration and thus higher local stress values at the crack tip. The FEM simulation also shows how the direction and magnitude of the principal stress is dependent on the presence of the crack. For our case, a pure mode I (crack opening) stress maximization, the side notch is preferred.

The crack can be made in different ways but is preferably shallow and not rounded at the end. A straightforward method for achieving higher stress intensity is notching the substrate from the top with a narrow diamond blade of 20 μm. The experimental effect of doing so is qualitatively shown in the left-hand side of Fig. 3: the lift off has started on the side of the sample where the notch was given. Using this simple notching technique enables a much better reproducibility of the process. However, the mechanical top notch is ill defined (right-hand side of Fig. 3), causing more defects / stress concentrators on a microscopic scale than originally expected. Furthermore, these defects are expected to be of the same order of magnitude as the uncontrolled defects that are induced during the sample preparation of the SLiM-Cut samples. Moreover, it has been shown that edge finishes coming from grinding or sawing during sample preparation can have a large impact on the final strength of the samples [5].

Currently, we are carrying out a feasibility study of laser ablation to create the notch. The laser process has the potential to yield a better defined crack with lower radius of curvature and less unintentional defects (see Fig. 4). Ideally, this type of crack is induced from the side of the ingot, in the plane of the crack propagation, to have a maximal reduction of thermal stress needed for crack propagation.

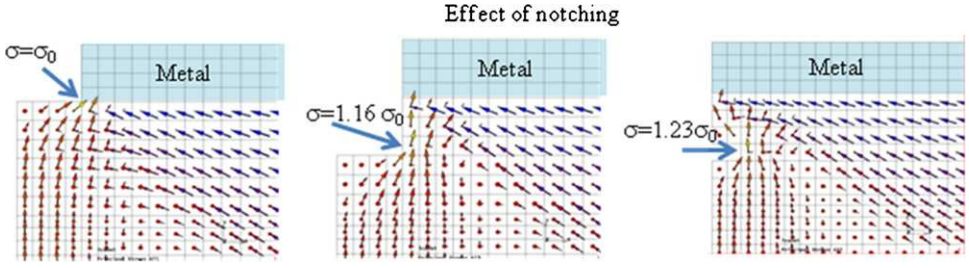

Fig. 2. FEM approximation of the increase in magnitude and change of direction of the principal stress for different geometries: (left) no notch, (middle) top notch and (right) sub-planar notch parallel to the surface.

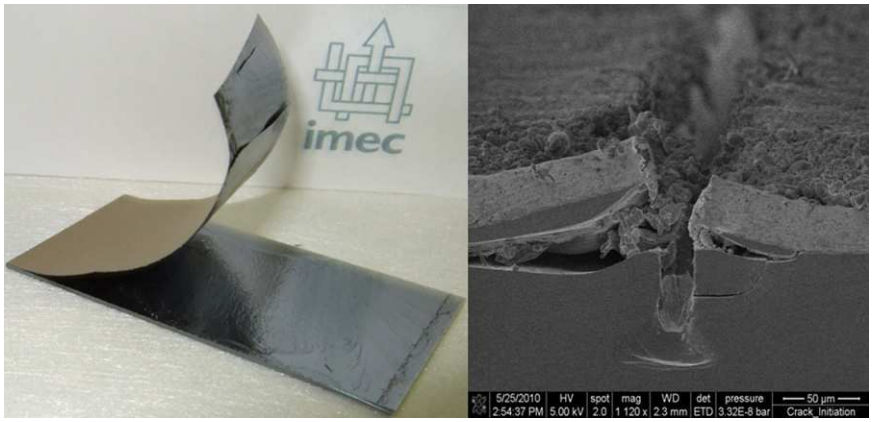

Fig. 3. The picture on the left shows a SLiM-Cut sample partially lifted off with a crack starting at the side where a notch was sawn from the top. The SEM-micrograph on the right shows the morphology of the notch.

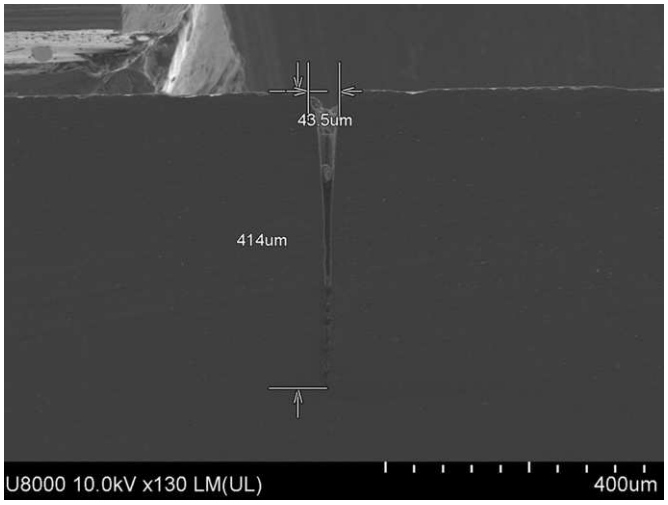

Fig. 4. Cross-section SEM picture of a notch made by laser ablation.

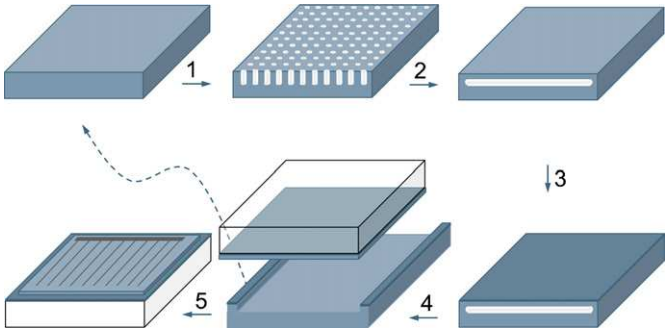

Fig. 5. Epifree solar-cell process consisting of five steps of (1) pore formation, (2) annealing, (3) processing of the first cell side, (4) bonding to a low-cost substrate, (5) and processing of the second side of the cell with re-use of the parent.

3. Epifree

The "Epifree" process takes advantage of the properties of macroporous silicon to enable the lift-off of a perfect ultra-thin layer of mono-crystalline silicon without resorting to epitaxial deposition. Arrays of pores of appropriate dimensions can indeed merge at high temperature and transform into a wide plate-like void under a detachable micron-thin film. This phenomenon called "empty-space-in-silicon" (ESS) was pioneered by Toshiba [6]. Using the over-layer as the active layer of a solar cell requires to upscale this technique to centimeter-wide areas and to develop a specific solar cell process for this ultra-thin material. This Epifree process is divided into five steps, namely (1) formation of regular macropores, (2) annealing of these pores, (3) solar-cell processing of the first side of the film, (4) bonding to a glass substrate and detachment from the parent wafer and (5) processing of the second side, while the parent wafer can be re-used (Fig. 5). A proof of concept with 1-μm-thin working cells of 2.6% energy-conversion efficiency was presented in [7] and the next developments are focused on achieving high-efficiency cells. In this section we briefly present how the material is prepared and the latest cell results that we obtained.

The preparation of a uniform and detachable film requires etching of a perfectly uniform array of pores with specific dimensions (step 1 of Fig. 5) and its annealing at a temperature over 1000 °C in non-oxidizing atmospheres (step 2 of Fig. 5).

The technique that we currently use to form perfectly uniform pore arrays is a combination of deep-UV lithography (DUV) with reactive ion etching (RIE). The perfect control on the array and the uniformity offered by this process make it attractive in the frame of a proof of concept. However, because of its complexity and its equipment cost, it is not compatible with a low-cost approach and we are hence replacing DUV and RIE by two low-cost techniques, nanoimprint lithography (NIL) and anodization in hydrofluoric acid. The second process step, annealing at high temperature, has to provide a sufficient mobility to silicon atoms to enable pore transformation, and this, for a sufficient time to enable complete pore merging. The mobility is favored by higher temperatures, lower pressures and requires a non-oxidizing ambient (e.g. H_2 or Ar), in order to ensure the presence of dangling bonds at the pore surface. Moreover, to avoid formation of defects (surface roughening, pitting, holes or pillars), the density of particles and the concentration of oxidizing impurities should be as low as possible [8]. Currently, we anneal the wafers after pore formation at 1150 °C in hydrogen at 10 Torr in a chemical vapor deposition (CVD) reactor (Epsilon 2000 from ASM). Ambient pressure is restored after cooling down to 550 °C. The annealing time was shown to be dependent not only on pore size and temperature, but also on wafer area, for pore merging is not synchronous but starts from the edges of the wafer and propagates slowly towards the center [8]. In practice, our experiments demonstrate that 200-mm wafers covered by 550-nm pores become fully covered by a 1-μm-thin film after a varying time of 45–60 minutes of annealing in hydrogen (Fig. 6), and that this floating film is sufficiently stable to be further processed into a cell. Since the thermal budget will be of utmost importance for the material cost, we hope in the future to be able to reduce the annealing time.

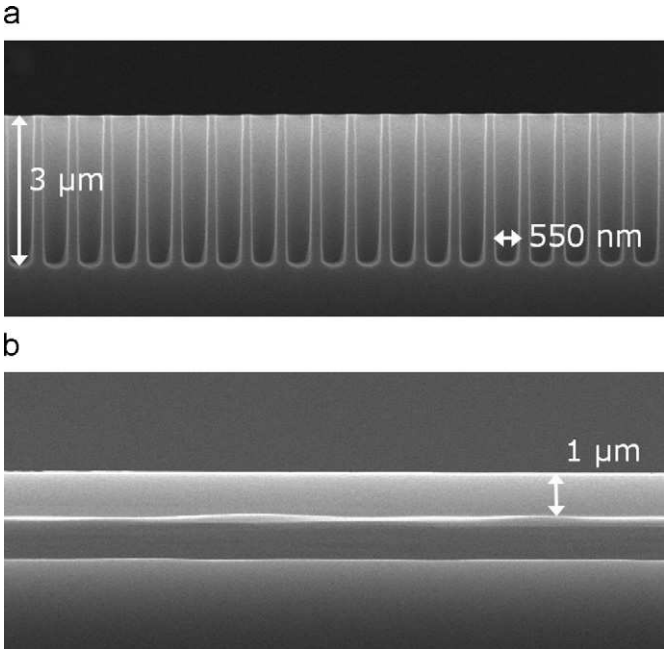

Fig. 6. (a) Regular pores with a diameter of 550 nm and a pitch of 800 nm obtained by DUV lithography and RIE and (b) transformation of these pores into a single void with an overlaying film of 1 μm thickness after annealing for 60 min at 1150 °C in hydrogen.

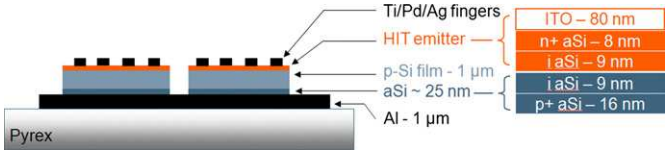

Fig. 7. Schematic cross section of the Epifree cells.

The solar cells that were fabricated so far aimed at providing a proof of concept and therefore had a very simple structure. Besides, the use of a low-cost glass substrate limits the process temperature below 400 °C. The cells were thus simple amorphous Si (a-Si)/crystalline Si (c-Si) hetero-junction diodes, p-type based, without any light-trapping or passivation schemes [7] and reached 2.6% of energy-conversion efficiency. Their short-circuit current (Jsc) of 14 mA/cm^2 was promising for a 1-μm-thin material without light trapping, but their open-circuit voltage (Voc) of only 340 mV was very low, despite the low doping of the substrate (~10 ohm cm). Inclusion of a rear-side passivation was therefore the first necessary step towards high-efficiency cells. A stack of intrinsic and p+ a-Si layers was chosen as passivation for its simplicity. In fact, it did not require any other process modification than depositing a-Si on the top side of the film after annealing. First, a thin layer of intrinsic a-Si was deposited to ensure the passivation and then a thicker layer of p+ was added to serve as a back-surface field (BSF) and improve the contact with the aluminum (Fig. 7). However, this deposition highlighted the challenge of processing the top side of the film, which is at that stage very weakly bonded to its parent silicon substrate and therefore prone to lift-off. A temporary bonding technique would be preferable to avoid any risk of lift-off, but the floating film can however be processed under certain well controlled conditions that avoid any thermal or pressure shock [9]. In particular, the a-Si deposition could successfully be realized by decreasing the pumping rate of the system and loading the sample at room temperature instead of directly at 170 °C. With this additional a-Si stack, the efficiency of the best cells increased to 4.1% (Table 1). All cell performance indicators improved, but the increase in Voc to 430 mV was still limited and always bound to a decrease in Jsc. This drop in Jsc is probably caused by the strong absorption coefficient of a-Si for wavelengths below ~700 nm [9] and the reasons for the limited Voc are being investigated. Possible factors that could decrease the passivating properties of the a-Si stack are its direct contact with aluminum, which is known to induce crystallization of a-Si at temperatures as low as 170 °C, anodic bonding, which subjects the cell to 250 °C and 1000 V for 10 min, damage caused by the direct plasma needed for the deposition of a-Si, or also the low substrate doping combined with the thinness of the material, which is about as thick as the depletion region of the cell. For these reasons, an alternative passivating stack has to be developed for the next cells to prove that high Voc values can be reached with the Epifree material.

Table 1
Improvement of the energy-conversion efficiency of Epifree solar cells after passivation of the rear side of the cell by a thin stack of a-Si layers.

Cell	Jsc (mA/cm^2)	Voc (mV)	FF (%)	Efficiency (%)
Reference	13.7	338	53	2.5
Passivated rear	12.8	426	75	4.1

A significant improvement of efficiency will require not only an efficient rear-surface passivation but also a thicker material. In fact, with the low absorption coefficient of silicon, an increase from 1 to 2 μm would strongly improve the Jsc of the current cells. The film thickness is directly and only related to the pore dimensions and interdistance [10], and limited by the annealing time [11]. Optimizing the film thickness therefore means finding the pore array morphology with the largest pores and interdistance that can be annealed in a few hours only. For this purpose we designed a new DUV lithography mask that will let us test different arrays and determine the most suitable to achieve films thicker than 2 μm. In theory, thicknesses from 3 to 5 μm may be obtained, which open the way to advanced cell processes and high device efficiencies.

4. Seed layer approach

The "seed layer approach" is a two-step process in which a thin crystalline-silicon seed layer is first created, followed by epitaxial thickening of this seed layer (Fig. 8). At imec, we perform the epitaxial thickening by thermal chemical vapor deposition (CVD). Although high-temperature CVD restricts the type of substrates that can be used, it provides two main advantages compared to other techniques: it achieves the growth of high quality epitaxial layers leading to enhanced electronic properties of the silicon absorber layers and, at the same time, it provides a deposition rate above 1 micron per minute, which is an important parameter in view of achieving a high throughput.

In the past, we made promising thin-film polycrystalline-silicon (pc-Si) solar cells at imec by using aluminum-induced crystallization (AIC) of amorphous silicon to obtain the seed layers. Maximum pc-Si cell efficiencies of 8.0% and 6.4% were reached on opaque alumina and transparent glass-ceramic substrates respectively [12,13]. Although the AIC process enables the fabrication of pc-Si layers with large grains [14,15], the limited structural and electronic quality of our present AIC seed layers was found to be one of the main cell-efficiency-limiting factors [16]. Seed layers of better quality are therefore needed to improve the cell efficiencies. We are currently working on improving the AIC seed layer quality, but are also looking for alternatives. We recently published the first results on monocrystalline-silicon cells made by an

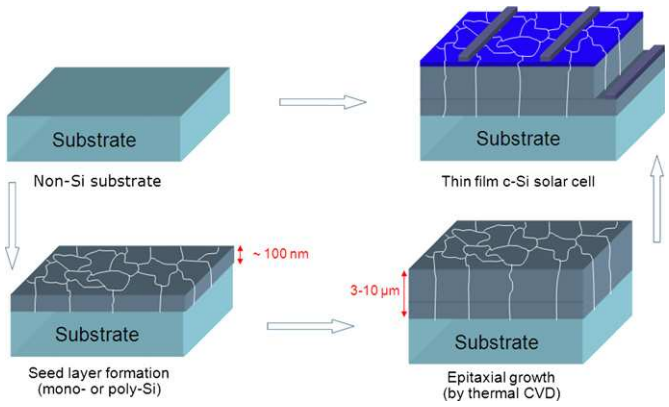

Fig. 8. Schematic representation of the seed layer approach.

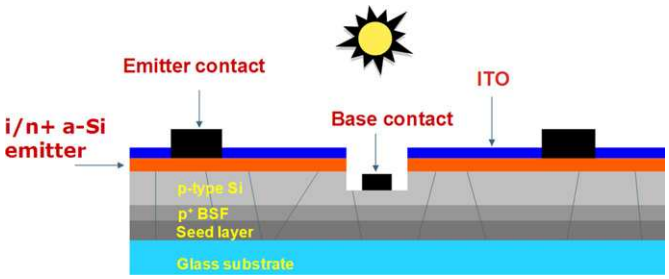

Fig. 9. Schematic cross section of the seed-layer based cells (not in scale).

alternative seed layer approach [17] and in this paper we report on recent improvements.

Monocrystalline-silicon seed layers were created at Corning Inc. by transferring 300 nm-thin (0 0 1)-oriented monocrystalline-silicon layers onto glass-ceramic substrates using Corning's proprietary technology that is based on anodic bonding and implant-induced separation [18]. The size of the seed layers that can be transferred like that is only limited by the size of the Si substrate that is used to start from. For this work we have used 4 inch substrates. Corning's spinel glass-ceramic (code 9664) substrates were used since these substrates can withstand the high temperatures needed for the thermal CVD and they have a coefficient of thermal expansion (CTE) that matches the CTE of silicon [19]. The transferred seed layers were then epitaxially thickened into monocrystalline-silicon absorber layers at imec by thermal CVD. Layers with a p+/p structure were grown consisting of 2 micrometer p+ ($\sim 5 \times 10^{19}\,cm^{-3}$) and 2–8 micrometer p ($10^{16}\,cm^{-3}$). The p+ layers act as back surface field (BSF) and the p-type layers as absorber layers in the resulting solar cells. The resulting epitaxial layers had various thicknesses and a typical defect density in the order of $10^5\,cm^{-2}$ [17], well below the $10^9\,cm^{-2}$ observed for our AIC layers [16].

Simple solar cell structures (Fig. 9) were made from the epitaxial mono-silicon layers grown on the glass-ceramic substrates, showing efficiencies of up to 11%. The main difference between the structure of these cells and the cells reported in [17] lies in the contacts: interdigitated finger patterns were used this time for emitter and base contacts instead of having the base contacts at the periphery of the cells as in [17]. The use of such interdigitated contacts compared to base contacts at the periphery of the cells will slightly lower the current density of the cells due to enhanced shadowing losses but will boost the fill factor from below 50% to above 70% due to a lowered series resistance. All reported cells had

Table 2
Averaged cell results for mono-Si samples with a different p-layer thickness made by the seed layer approach.

Original p-layer thickness microns	Jsc (mA cm^{-2})	Voc (mV)	FF (%)	Efficiency (%)
8	24.3	598	74	10.8
6	23.1	600	71	9.9
4	19.9	613	73	8.9
2	16.3	576	61	5.7

an area of 1 cm^2. We investigated the influence of the p-layer thickness on the cell results and applied the same plasma texturing process that removed around 1.5 microns of the original p-layer on all samples. This plasma texturing reduces the front surface reflection and enhances the current densities of the cells [20]. Table 2 summarizes the solar cell results of the investigated layers. The best single cell efficiency was 11%. The Voc values above 600 mV illustrate the good material quality of these thin monocrystalline-Si layers on glass-ceramic substrates. Since these Voc values are a lot higher (600 mV versus 530 mV) than the ones reported in [17], the material quality of the cells reported here must be substantially better than that of the cells reported in [17] since a difference in contact structure alone cannot account for such a difference in voltage. The reason for this different material quality is yet unknown. The Jsc values are still relatively low due to the absence of advanced light trapping structures in these cells and the fact that the cells are in substrate configuration on transparent substrates and do not have a back reflector incorporated. The much lower fill factor of the thinnest cells is probably an artifact due to the processing and hence not inherently related to a layer thickness of 2 microns.

5. Conclusions and outlook

We presented three different approaches that are currently under investigation at imec to form a thin layer of crystalline-silicon for solar module purposes. The SLiM-Cut approach is a wafering technique that results in 50-micron thick layers with a minimum of material loss. We showed that crack initiation can be used as a means to better control the lift-off process. The epifree approach involves the lift-off of ultra-thin monocrystalline films formed by the reorganization upon annealing of cylindrical macropore arrays in silicon. So far, films with a thickness of around 1 µm and very simple cells with an efficiency of up to 4.1% have been achieved and future development will focus on fabricating thicker films. Finally, a seed layer approach was presented based on the epitaxial thickening by thermal CVD of monocrystalline Si layers bonded on glass-ceramic substrates. Very promising cell efficiencies of 11% and Voc values of up to 610 mV were achieved using a very simple and non-optimized cell structure.

Besides improving the quality of the Si material obtained by these three approaches, we will focus in the near future also on using more advanced cell structures to obtain higher cell efficiencies. Advanced light trapping features such as plasmonic particles and nanostructured layers will be the key to obtain high current densities in these thin Si solar cells.

Acknowledgements

The authors are very grateful to Kris Van Nieuwenhuysen for her help with the epitaxial depositions, to Rufi Kurstjens for some of the SEM pictures and to Mario Gonzales for the FEM modeling and discussion with respect to thermally induced stresses. The authors

would also like to thank Alexandre Mayolet, Donnell Walton and Ta-Ko Chuang of Corning for supplying the seed layers on glass-ceramics. Furthermore, the financial support of the Flemish government (SBO project nr. 090047 - 'Silasol - New Silicon Materials for Solar Applications'), is greatly acknowledged. The cells were measured against a reference cell which is calibrated (traceable) to the World Radiometric Reference by the European Solar Test Installation (ESTI) of the European Commission Joint Research Center, an ISO 17025 accredited calibration laboratory.

References

[1] K. Alberi, I.T. Martin, M. Shub, C.W. Teplin, M.J. Romero, R.C. Reedy, E. Iwaniczko, A. Duda, P. Stradins, H.M. Branz, D.L. Young, Material quality requirements for efficient epitaxial film silicon solar cells, Applied Physics Letters 96 (2010) 073502.

[2] M.J. Kerr, P. Campbell and A. Cuevas, Lifetime and efficiency limits of crystalline silicon solar cells, roc. Proceedings of the 29th IEEE Photovoltiac Specialists Conference, 438, New Orleans, USA, 2002.

[3] F. Dross, A. Milhe, J. Robbelein, I. Gordon, P.O. Bouchard, G. Beaucarne and J. Poortmans, Stress induced lift-off method for kerf-loss-free wafering of ultra-thin crystalline Si wafers, in: Proceedings of the 33rd IEEE Photovoltiac Specialists Conference, doi:10.1109/PVSC.2008.4922741, May 2008, San Diego, USA, 2008.

[4] F. Dross, J. Robbelein, B. Vandevelde, E. Van Kerschaver, I. Gordon, G. Beaucarne, J. Poortmans, Stress-induced large-area lift-off of crystalline Si films, Applied Physics A 89 (2007) 149.

[5] Y. Yang, R.C. Teixeira, P. Roussel, B. Swinnen, B. Verlinden, I. De Wolf, Statistical Analysis of the Influence of Thinning Processes on the Strength of Si, Mater. Res. Soc. Symp. Proc 1112 (2009) E03-09.

[6] I. Mizushima, T. Sato, S. Taniguchi, Y. Tsunashima, Empty-space-in-silicon technique for fabricating a silicon-on-nothing structure, Applied Physics Letters 77 (2000) 3290.

[7] V. Depauw, I. Gordon, G. Beaucarne, J. Poortmans, R. Mertens, J.P. Celis, Proof of concept of an epitaxy-free layer-transfer process for silicon solar cells based on the reorganisation of macropores upon annealing, Materials Science and Engineering B 159 (2009) 286.

[8] V. Depauw, I. Gordon, G. Beaucarne, J. Poortmans, R. Mertens, J.P. Celis, Large-area monocrystalline silicon thin films by annealing of macroporous arrays: Understanding and tackling defects in the material, Journal of Applied Physics 106 (2009) 033516.

[9] V. Depauw, Y. Qiu, K. Van Nieuwenhuysen, I. Gordon, and J. Poortmans, Epitaxy-free monocrystalline silicon thin film: First steps beyond proof-of-concept solar cells, Paper accepted for publication in Progress in Photovoltaics: Research and Applications.

[10] T. Sato, I. Mizushima, S. Taniguchi, K. Takenaka, S. Shimonishi, H. Hayashi, M. Hatano, K. Sugihara, K, and Y. Tsunashima, Fabrication of Silicon-on-nothing structure by substrate engineering using the empty-space-in-silicon formation technique, Japanese Journal of Applied Physics 43 (2004) 12.

[11] T. Müller, D. Dantz, W. von Ammon, J. Virbulis, U. Bethers, Modelling of morphological changes by surface diffusion in silicon trenches, ECS Transactions 2 (2006) 363.

[12] I. Gordon, L. Carnel, D. Van Gestel, G. Beaucarne, J. Poortmans, 8% efficient thin-film polycrystalline-silicon solar cells based on aluminium-induced crystallization and thermal CVD, Progress in Photovoltaics: Research and Applications 15 (2007) 575.

[13] I. Gordon, L. Carnel, D. Van Gestel, G. Beaucarne, J. Poortmans, L. Pinckney, and A. Mayolet, Thin-film polycrystalline-silicon solar cells on glass-ceramics, Proceedings of the 22nd European Photovoltaic Solar Energy Conference, 3-7 September 2007, Milano, Italy, 1993.

[14] O. Nast, S. Wenham, Elucidation of the layer exchange mechanism in the formation of polycrystalline silicon by aluminum-induced crystallization, Journal of Applied Physics 88 (2000) 124.

[15] D. Van Gestel, I. Gordon, L. Carnel, K. Van Nieuwenhuysen, J. D'Haen, J. Irigoyen, G. Beaucarne, J. Poortmans, Influence of seed layer morphology on the epitaxial growth of polycrystalline-silicon solar cells, Thin Solid Films 511-512 (2006) 35.

[16] D. Van Gestel, M.J. Romero, I. Gordon, L. Carnel, J. D'Haen, G. Beaucarne, M. Al-Jassim, J. Poortmans, Electrical activity of intragrain defects in polycrystalline silicon layers obtained by aluminium-induced crystallization and epitaxy, Applied Physics Letters 90 (2007) 092103.

[17] I. Gordon, S. Vallon, A. Mayolet, G. Beaucarne, J. Poortmans, Thin-film monocrystalline-silicon solar cells made by a seed layer approach on glass-ceramic substrates, Solar Energy Materials and Solar Cells 94 (2010) 381.

[18] D. Dawson-Elli, C. Kosik Williams, J. Couillard, J. Cites, R. Manley, G. Fenger, K. Hirschman, Demonstration of high performance TFTs on silicon-on-glass (SiOG) substrate, ECS Transactions 8 (1) (2007) 223.

[19] L.R. Pinckney, Transparent, high strain point spinel glass-ceramics, Journal of Non-Crystalline Solids 255 (1999) 171.

[20] H.F.W. Dekkers, G. Agostinelli, D. Dehertoghe, and G. Beaucarne, Improved performances of mc-Si solar cells by isotropic plasma texturing, Proceedings of the 19th European Photovoltaic Solar Energy Conference 2004, 412.