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A simple and cost-effective approach for fabricating pyramids on crystalline silicon wafers

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ABSTRACT

A simple and cost-effective approach for texturing crystalline silicon wafers is proposed. The advantage over conventional texturization processes is the fact that no surfactant is added in alkaline etchants. Hydrogen bubbles, regarded as residuals in conventional texturization processes, are utilized in this approach as etch masks on a silicon surface. This is accomplished by placing a metal grid with suitable openings on silicon wafers to confine the hydrogen bubbles created during etching. Pyramids with a size ranging from 6 to 9 μm are uniformly fabricated using this method. Without antireflection coating, an average weighted reflectance of 15.1% is achieved.

1. Introduction

Surface texturization of (1 0 0)-oriented crystalline silicon wafers is a frequently used technique in modern solar cell processing to reduce optical reflections. Many successful approaches based on texturing silicon surface utilizing alkaline solutions [1,2] have been reported. Alkaline etchants such as sodium hydroxide (NaOH) [3] or potassium hydroxide (KOH) [4] at low concentration in water expose Si {1 1 1} faces resulting in square-based pyramids randomly distributed over the cell surface. This texture will enhance light trapping capability by increasing both coupling of lights into the cell and reflectivity [5,6] of lights trying to escape from the cell [7,8]. In general, isopropyl alcohol (IPA) is added to the alkaline etchants to improve the uniformity of the random pyramid texture. Though IPA is expensive, it is essential for the process because it removes hydrogen bubbles sticking on the silicon wafer by improving the wettability of the wafer surface. In a typical texturing condition, high concentration of IPA is required [9] to obtain uniform pyramid textures. However, the etching rate of silicon decreases drastically with IPA concentration [10]. In addition, IPA is volatile in a heated etching bath. To maintain a sufficient wettability of the silicon surface, IPA must be constantly added to the solution to compensate the amount lost due to evaporation. In current commercial texturing technique based on alkaline anisotropic etching, the cost of IPA can be the key factor of overall texturization cost reduction approach.

Recent research on low-cost silicon texturization centers on investigating alternative solutions [11,12] for surface texturing and reducing amount of IPA in the solutions [13]. Several novel processing techniques were reported using different chemicals, such as tetramethyl ammonium hydroxide (TMAH) and sodium phosphate (Na_3PO_4). Moreover, Nishimoto and Namba [14] successfully textured the silicon surface with sodium carbonate (Na_2CO_3) solution and claimed that no IPA was needed for the process. In this paper, we propose a different approach based on KOH texturization without adding any surface-active additive in the solution. In a conventional alkaline etching process, KOH reacts with silicon in water producing hydrogen bubbles. These hydrogen bubbles with 2–3 mm diameter can stick on the silicon surface and suppress chemical reaction between the silicon surface and the KOH solution. This will lead to insufficient pyramid nucleation and result in poor texture uniformity and reproducibility. However, these bubbles can also be used as a "pseudo-mask" [15] as long as they can be constantly trapped on the silicon surface during the etching process. This is accomplished by placing a metal grid with periodic opening at close proximity to the silicon wafers. The hydrogen bubbles created due to KOH-Si reaction can be confined by the openings of the metal grid because of surface tension of the bubbles. Thus the hydrogen bubbles, which are regarded as residuals in the conventional texturization processes, are utilized in this approach as the etch-mask on the silicon surface. Pyramids with a size ranging from 6 to 9 μm are uniformly fabricated using this method.

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2. Pyramid fabrication

The etching experiments were carried out using 3″, *p*-type, ⟨100⟩; oriented, crystalline silicon wafers with resistivity 1–3 Ωcm. Before texturization, the wafers were etched in 10% hydrofluoric acid (HF) to remove native oxide and rinsed in deionized water. The wafers were then etched in KOH (1 wt%) solutions at different temperatures for 10, 15, and 20 min. The etching solution was heated with a temperature-controlled hot plate. No surfactant was added in the etchants during the processes. The hydrogen bubbles produced during etching were trapped on the wafer surfaces utilizing the stainless steel metal grids with different square openings. To optimize the size and uniformity of the pyramid, we tested four metal grids with 1, 1.5, 2, and 3 mm square opening for texturing at 1 and 2 mm wafer-to-grid separations. After the etching process, the surface morphology of the silicon wafers was examined by a surface scanning electron microscope (SEM). To characterize the optical performance, hemispherical surface reflectance of the textured surfaces was measured. An integrating sphere/spectroradiometer was used with light in the wavelength range from 400 to 1100 nm at near-normal incidence. Finally, the weighted reflectance was calculated by normalizing the reflectance using AM1.5 solar spectrum.

3. Results and discussion

The pyramids fabricated using the proposed approach are dependent not only on the conditions of the KOH etchants but also on the structures of the metal grids to the silicon wafers. Both must be considered to obtain pyramid structures with satisfactory optical performance. The etching was performed by placing the metal grid on top of the silicon wafer and submerged them into the KOH solution. At the beginning of the etching process, hydrogen bubbles were observed to emerge from the wafer surface and captured by the openings of the metal grid. Shortly after the etching started, hydrogen bubbles were found to fill most of the grid openings if suitable size of the openings was used. As the etching process continued, the bubbles in the openings grew in size until a pressure balance on the bubbles was reached. The hydrogen bubbles released from the wafer surface in the subsequent etching could be pushed away from the openings and were observed to escape from the edges of the grid. However, the bubbles within the openings were found to stay within the openings throughout the etching process. They can now function as the pseudo-mask for pyramids fabrication. It is generally believed that the formation of pyramids on monocrystalline silicon wafers makes use of anisotropic etching with alkaline solutions. So there is no basic difference in the etching mechanism between the proposed method and other texturization techniques.

Fig. 1 shows the SEM photos of the surface morphology of the silicon wafers textured in 1 wt% KOH solution at 70 °C for 10, 15, and 20 min without ultra-sonic agitation. The size of the opening of the metal grid is 2 mm × 2 mm, and the separation between the grid and the wafers is 1 mm. Fig. 1a depicts the pyramids formed with the metal grid during the initial stages of texturization. Random upright pyramids were observed but were distributed sparsely on the wafer surface. Poor surface coverage was obtained. Fig. 1b shows that the pyramid structures had grown in size after an etching time of 15 min. The size of the pyramids increased with increase in etching time, which indicated that the nucleation and growth of the pyramids took place simultaneously. In addition, the surface coverage of the sample improved substantially. The average pyramid base size was between 3 and 6 μm. As shown in Fig. 1c, however, some of the pyramid structures were found to collapse. For a 20 min duration of texturization, some pyramids can grow at the expense of others, resulting in a decrease of uniformity in size. Nevertheless, the surface coverage of the

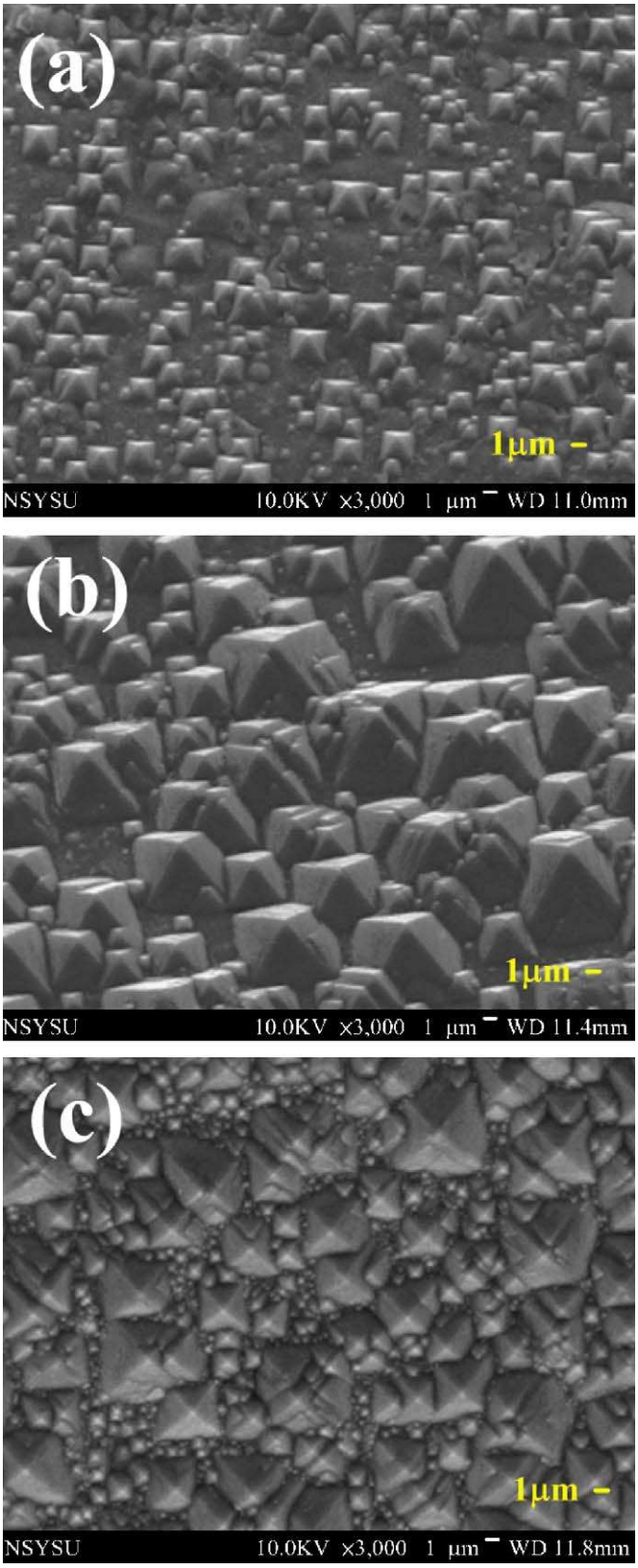

Fig. 1. The SEM photos of the surface morphology of the silicon wafers textured in 1 wt% KOH solution at 70 °C for (a) 10, (b) 15, and (c) 20 min.

pyramid structures improved with increase in etching time. The overall coverage of the pyramid structures exceeded 90% after 20 min of texturization as shown in Fig. 1c.

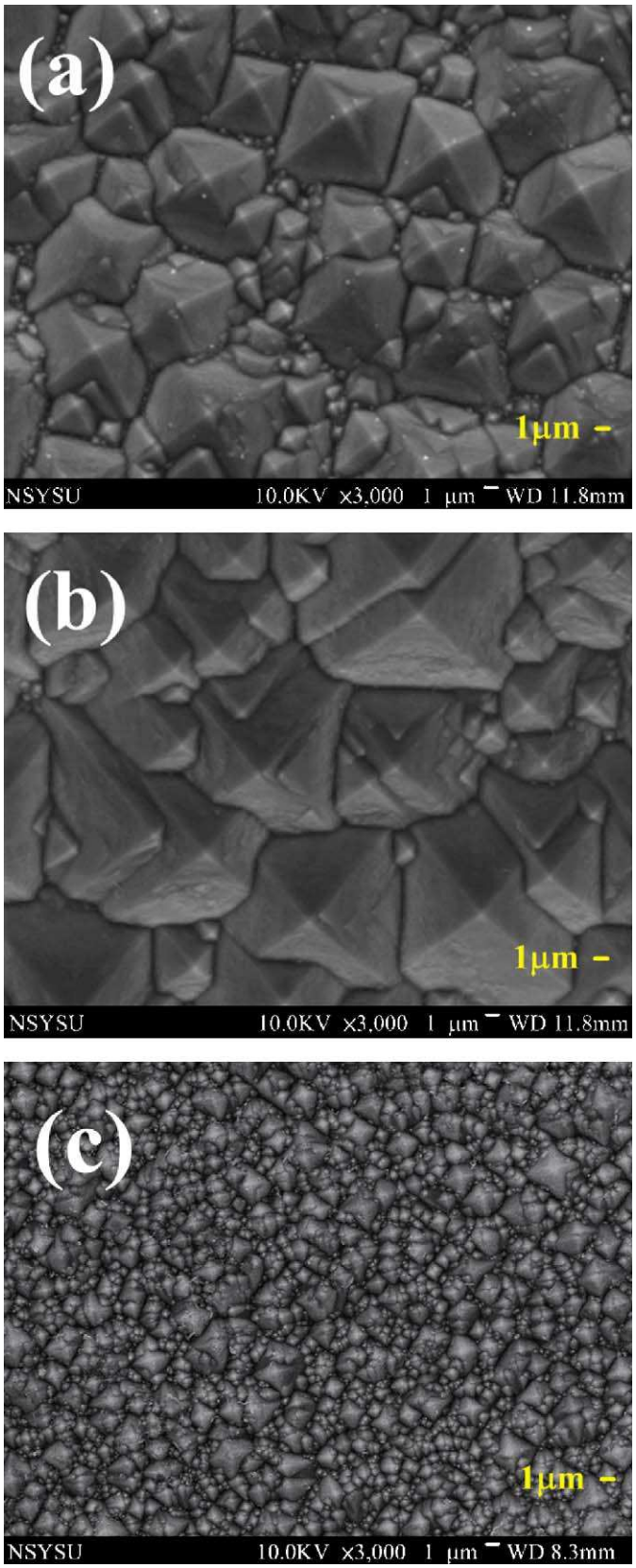

Fig. 2. The SEM images of the wafers etched in (a) 80 °C, (b) 90 °C, and (c) 90 °C without using the metal grid, in KOH (1 wt%) solutions for 20 min.

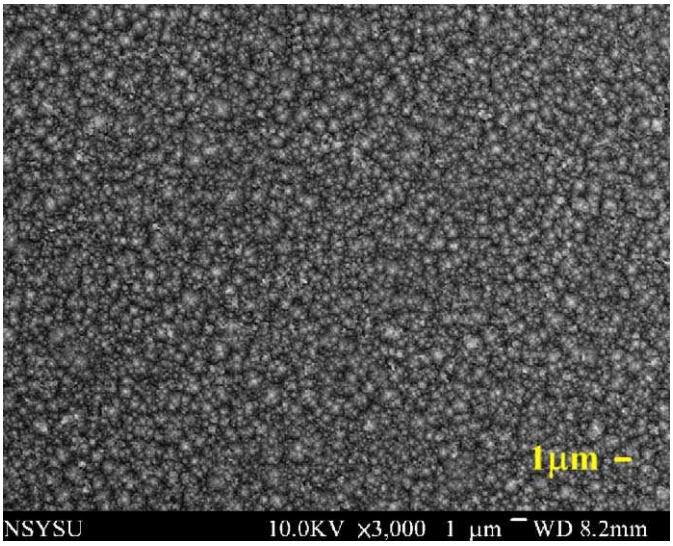

Fig. 3. The SEM image of the wafers etched in 90 °C, 1 wt% KOH solution for 20 min. The separation between the wafer and the grid is 2 mm.

To improve the uniformity of the size of the pyramids, we increased the etching temperature of the wafers to 80 and 90 °C in 1 wt% KOH solutions while keeping the 20 min etching time. The size of the opening of the metal grid was kept at 2 mm × 2 mm. The SEM photos of the etched wafers are shown in Fig. 2a and b. In addition, Fig. 2c shows the wafer textured at 90 °C without using the metal grid for comparison. As shown in Fig. 2a and b, both the size and surface coverage of pyramid structures improve significantly. This is because the etching rate of (100) and (110) crystallographic planes increases faster than the rate of the (111) crystallographic plane. As the temperature increases, the differences in etching rates can lead to the formation of large pyramids. For samples textured in 90 °C KOH solution (Fig. 2b), we found that the sizes of the pyramids varied from 6 to 9 μm and the surface overall coverage of the pyramid structures was better than 95%. Uniform texturization throughout the silicon surface was achieved without any addition of IPA. However, the pyramid structure of the wafer displayed in Fig. 2c was found to reduce in size and the sizes of the structure differentiated greatly (1–4 μm) without using the metal grid. The effectiveness of using the metal grid for texturing was demonstrated.

Fig. 3 shows the SEM photo of the wafer textured with 2 mm separation between the wafer and the metal grid in 90 °C, 1 wt% KOH solutions for 20 min. The opening of the metal grid is 2 mm square. As shown in the figure, the pyramidal structure collapsed when the separation was increased from 1 to 2 mm. We believe that the 2 mm separation was too large to keep the bottoms of the bubbles in close contact with the wafer surface since the typical diameter of the bubbles was around 2–3 mm. Therefore, the bubbles could not function as the etch mask effectively during the etching. The bubble trapping capability of the grid decreased if the wafer and the grid were further separated.

Fig. 4 shows the SEM photos of the surface morphology of the silicon wafers textured in the KOH solution at 90 °C for 20 min using the metal grids with different sizes of openings. The separation between the wafers and the grids was kept at 1 mm. As can be observed from the figure, uniform texturization throughout the silicon surfaces of the samples a–c was obtained. The overall coverage of the pyramid structures ranged from 90% to 95%. In addition, the size of the pyramid was found to increase with the dimensions of the grid openings. The sizes of the pyramid varied from 2–5 to 6–9 μm when the size of the opening changed from 1 to 2 mm^2, as shown in Fig. 4a–c. We could,

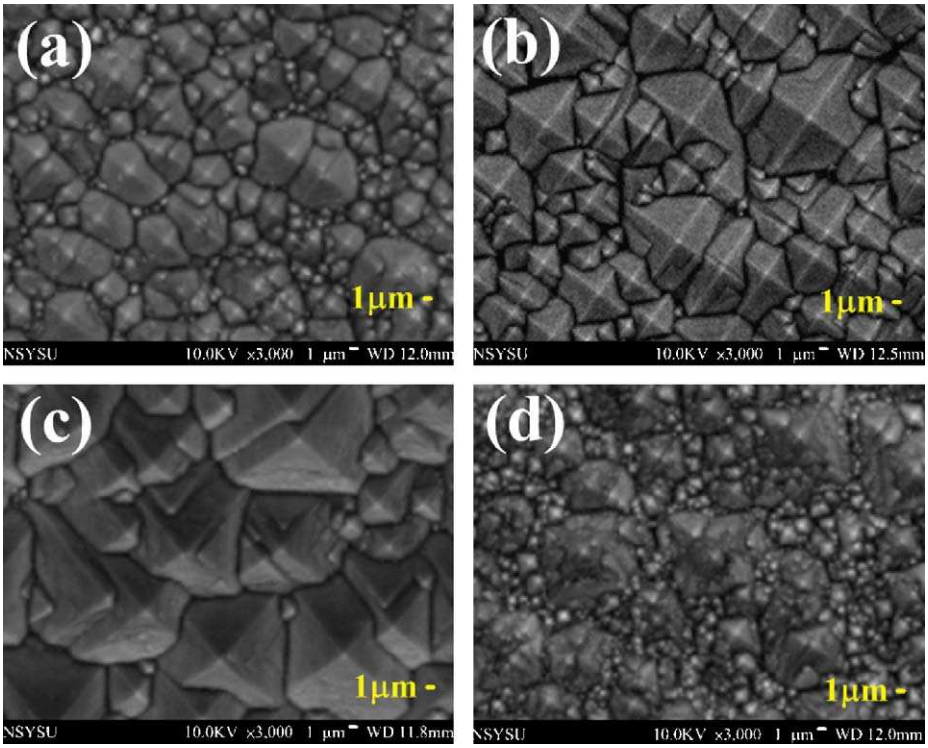

Fig. 4. The SEM photos of the surface morphology of the silicon wafers textured in 1 wt% KOH solution at 90 °C for 20 min using metal grids with (a) 1, (b) 1.5, (c) 2, and (d) 3 mm^2 openings.

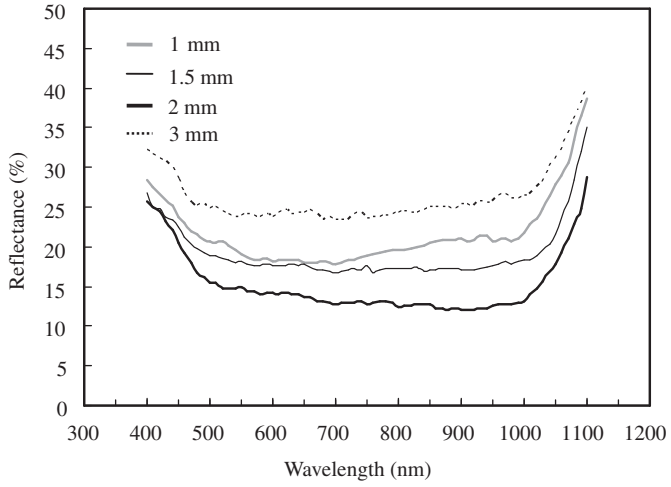

Fig. 5. The influence of the size of the opening to the reflectance of the silicon surfaces.

therefore, make the assumption that texturing with wide opening grids allows masking the silicon surfaces with larger bubbles and results in the formation of larger pyramids. However, the pyramid structures shown in Fig. 4c were not as sharp as the pyramids fabricated using conventional KOH/IPA processes [1]. Therefore less light trapping capability is expected. In Fig. 4d, the pyramid structures collapsed for texturing with a 3 mm square opening. In this case, many grid openings were found to be without the hydrogen bubbles. Hydrogen bubbles were observed to escape from either the edges or the surface of the grid during the etching process. This implied that the dimension of the openings was too large to effectively confine the bubbles released from the wafer surface. The bubble trapping capability of the grid was reduced.

The dependence between the sizes of the grid openings and the reflectance of the silicon surfaces with respect to optical wavelength is shown in Fig. 5. The measured reflectance decreased with the size of the opening up to 2 mm due to the formation of larger pyramids. Without any antireflection coating, an average weighted reflectance of 15.1% is achieved. Beyond this size, the surface reflectivity increased significantly due to the collapses of the pyramid structures, as shown in Fig. 4d. The pyramid size, surface coverage, and weighted reflectance of the attempts at 1 mm separation together with the wafer textured without using the metal grid are summarized in Table 1.

In addition to the fact that IPA was no longer needed in the etching process, the proposed approach was applicable to batch process by stacking the wafers vertically for texturing. This will make it commercially attractive because of the possibility of mass production at low cost. Fig. 6 shows the cost comparison between the proposed approach and the conventional KOH/IPA texturing process [16] based on texturing 3″ Si wafers in a 4-wafer stacked etch system. From the figure, we found that the cost of the raw materials used throughout the entire texturization (buffered-HF pre-treatment, KOH-only texturing and HCl/buffered-HF/DI-water post-treatment) of the proposed approach is 0.105 USD/wafer, a considerable reduction if compared with the cost of 0.154 USD/wafer in the conventional texturing process.

4. Conclusion

In conclusion, we have shown a simple and cost-effective approach to texture crystalline silicon wafer surfaces. This texture was realized by trapping the hydrogen bubbles as pseudo-mask on the wafer surfaces utilizing the metal grids with periodic openings. Using the metal grid with 2 mm^2 opening and 1 mm separation between the grid and the wafers, our optimized process lasted for 20 min at 90 °C, 1% KOH solution without

Table 1
The pyramid size, surface coverage, and weighted reflectance of the wafers prepared with different texturing conditions.

Wafer #	Temp. (°C)	Etch time (min)	Grid opening (mm^2)	Coverage (%)	Pyramid size (μm)	Reflectance (%)
1	70	10	2×2	70	1–3	29.4
2	70	15	2×2	90	3–6	22.7
3	70	20	2×2	91	2–6	21.7
4	80	20	2×2	90	5–8	21.5
5	90	20	2×2	95	6–9	15.1
6	90	20	—	86	1–4	21.9
7	90	20	1×1	92	2–5	20.9
8	90	20	1.5×1.5	95	2–8	18.9
9	90	20	3×3	77	1–5	25.7

Metal grid to wafer separation is 1 mm.

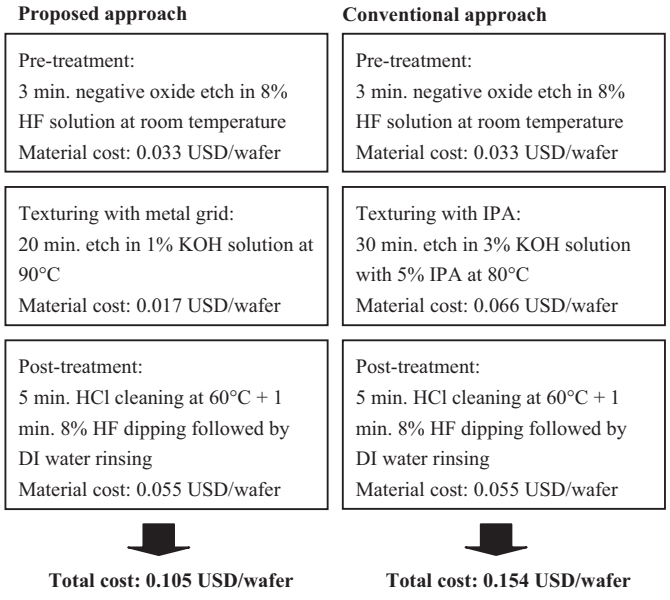

Fig. 6. The cost comparison between the proposed approach and the conventional KOH/IPA texturing process based on texturing 3″ Si wafers in a 4-wafer stacked etch system.

adding any IPA. After texturing, we obtained reliable and uniform pyramid structures with an average weighted reflectance of 15.1%. The proposed technique offers a unique alternative for fabricating texture surfaces for silicon solar cell and may well lead to novel photovoltaic applications.

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