Improving the Quality of Epitaxial Foils Produced Using a Porous Silicon-based Layer Transfer Process for High-Efficiency Thin-Film Crystalline Silicon Solar Cells

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***Abstract*—A porous silicon-based layer transfer process to produce thin (30–50 μm) kerfless epitaxial foils (epifoils) is a promising approach toward high-efficiency solar cells. For high efficiencies, the epifoil must have high minority carrier lifetimes. The epifoil quality depends on the properties of the porous layer since it is the template for epitaxy. It is shown that by reducing the thickness of this layer and/or its porosity in the near-surface region, the near-surface void size is reduced to $<$65 nm and in certain cases achieve a 100 nm-thick void-free zone below the surface. Together with better void alignment, this allows for a smoother growth surface with a roughness of $<$35 Å and reduced stress in the porous silicon. These improvements translate into significantly diminished epifoil crystal defect densities as low as $\sim$420 defects/cm^2. Although epifoils on very thin porous silicon were not detachable, a significant improvement in the lifetime (diffusion length) of safely detachable n-type epifoils from $\sim$85 ($\sim$300 μm) to $\sim$195 μs ($\sim$470 μm) at the injection level of 10^{15}/cm^3 is achieved by tuning the porous silicon template. Lifetimes exceeding $\sim$350 μs have been achieved in the reference lithography-based epifoils, showing the potential for improvement in porous silicon-based epifoils.**

***Index Terms*—Crystal defects, epitaxy, layer transfer, minority carrier lifetime, porous silicon, stress, surface roughness.**

I. Introduction

THE continuous scaling-down of the silicon solar cell wafer thickness to reduce the consumption of silicon (and hence the cost) has fueled research groups to look into kerf-less production of very thin ($<$50 μm) silicon and innovative handling techniques. One such promising route is the electrochemically etched porous silicon-based layer transfer approach that was first proposed by Tayanaka *et al.* [1]. An extensive review of this approach in its various embodiments (sintered porous silicon (SPS) by Sony [1] and the University of Stuttgart [2], [3]; porous silicon process (PSI) by ZAE Bayern [4], [5]); and other associated methods is given by Brendel [6]. Other groups that have also been developing the layer transfer of thin silicon during the early years include Institut National des Sciences Appliquées de Lyon (INSA Lyon) [7] and IMEC [8], [9]. Presently, several institutes and companies are active in this field such as the Institute for Solar Energy Research (ISFH) [10], [11], Solexel [12], Crystal Solar [13], Episun [14], AmberWave [15], and IMEC [16].

In this approach, monocrystalline epitaxial silicon layers of $\sim$30–50 μm thickness, which are grown on sintered porous silicon with a double layer stack of two different porosities, are detached from the silicon parent substrates using a mechanically weak high-porosity porous silicon layer. However, the handling of thin silicon films (epifoils) after detachment from the parent substrate in a free-standing configuration will lead to increased yield loss due to breakages. In order to overcome this issue, the epitaxial film can first be front-side (sunny side) processed while attached to the parent substrate and then bonded to a superstrate glass before further processing into solar cells, such that the thin foils are never handled free-standing, as shown in Fig. 1. Several groups including IMEC follow this route [14], [17]. Alternatively, the epitaxial film can be rear-side (dark side) processed, while it is still attached to the parent substrate and then layer-transferred to a conductive substrate before the front-side is processed while bonded to the foreign substrate. This is the approach followed by AmberWave, where the epitaxial film is transferred to a steel substrate [15].

Although cell processing after the silicon foil is bonded to quartz has its constraints and complications (since compatibility with quartz and silicone is essential), conversion efficiencies of $\sim$18% have been achieved on solar cells processed with FZ silicon bonded to quartz prior to rear-side processing [17]. More impressively, Solexel has announced its world record conversion efficiency of $>$20% on 156 mm by 156 mm full-square solar cells using a 43 μm-thick epitaxial silicon in a back-contact/back-junction configuration [12]. At IMEC, the

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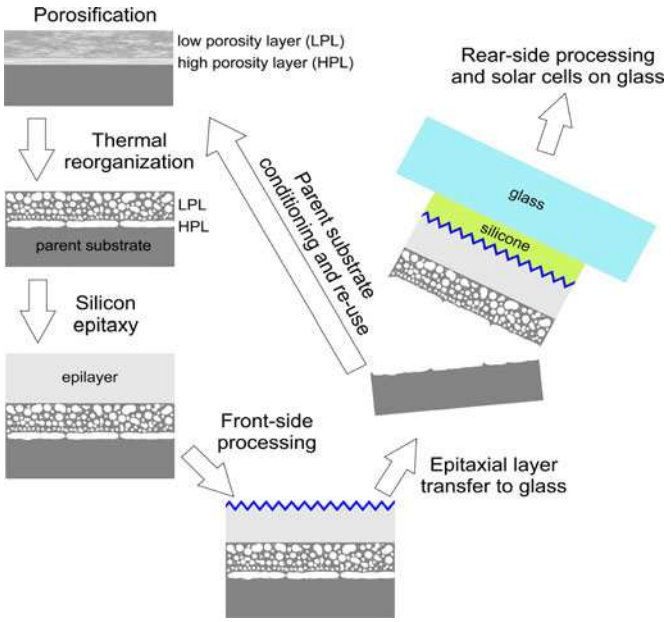

Fig. 1. Process flow for solar cells based on epifoils depicting the main steps of the porous silicon-based layer transfer sequence.

first attempt at processing quartz-bonded epifoils into solar cells have been made recently. Although there were contacting issues, high open-circuit voltages of ∼650 mV were already achieved, highlighting the potential of this concept. In both cases, one of the key determinants toward the excellent cell performance characteristics is the high minority carrier lifetime, the improvement of which is the subject of this paper.

II. Porous Silicon as a Template for Epitaxy

Integral to the layer transfer process is the double layer stack of porous silicon (a low porosity layer (LPL) of ∼1–2 μm on top of a high porosity layer (HPL) of ∼300 nm) that is electrochemically etched on a highly doped silicon substrate. After etching, the porous silicon is sintered at a high temperature and the as-etched, fine columnar pores reorganize such that the HPL becomes a large extended void interrupted by tiny pillars, while the LPL transforms into smaller spheroidal voids embedded in a monocrystalline silicon matrix such that the surface is ideally free of open voids [18], [19], suitable for high-quality epitaxial growth, as depicted in Fig. 1. Thus, the HPL acts as the plane of detachment and the annealed LPL surface acts as the template for epitaxial growth of the epifoil. The efficiency potential of solar cells that is based on epifoils is mainly determined by the minority carrier lifetime achievable in these epifoils, which in turn depends on the quality of the epifoils that are grown on the porous silicon template. Therefore, it is expected that the properties of the porous silicon will strongly influence the crystal quality and hence the minority carrier lifetime of the epifoils.

The porous silicon layer can influence the epifoil quality in several ways. First, prior to epitaxy, since the epitaxial growth starts on the LPL surface, the morphological and topographical nature of the LPL surface will significantly influence the epitaxial growth process. Second, during epitaxy and subsequently, the evolution of the intrinsically present stress distribution in the porous silicon layer as a whole can cause strain during epitaxial growth or even during the cool down and this is also expected to have an impact on the quality of the epifoil. Finally, in the postepitaxy stage, the morphological nature of the HPL determines the ease of detachment of the epifoil and thereby the amount of mechanical stresses that are induced in the foil during detachment. The easier the detachment, the better will be the epifoil quality.

In this study, the influence of the porous silicon layer on the epitaxial layer quality is studied, particularly focusing on the properties of the LPL, to understand how the epifoil quality can be improved by creating a better porous silicon template.

III. Experimental Method

All the sets of samples that are used in the series of experiments described in this paper were prepared using mirror-polished monocrystalline Czochralski (Cz) silicon wafers with a high boron doping concentration of 10^{19} cm^{-3}. On each of these wafers, a layer of porous silicon, typically with a double-layer structure that consists of an LPL (∼30% porosity) on top of an HPL (∼60% porosity), was electrochemically etched using an HF/ethanol mixture (22% HF by volume) as the electrolyte. This double layer structure is achieved by applying different current densities for the different layers: 1.4 mA/cm^2 for the LPL and ∼73.5 mA/cm^2 for the HPL. The void size and void alignment in the LPL can be varied by altering its thickness and porosity. The thickness of the LPL was varied by varying the etching time between 40 s and 13 min, resulting in LPLs of thicknesses between 160 and 2100 nm. In two of the samples, a third layer of porous silicon of a slightly different porosity was added on top of a typical double-layer structure. This was done by using an applied current density of ∼0.36 mA/cm^2 (denoted triple layer A) and ∼6.9 mA/cm^2 (denoted triple layer B) for the third layer, respectively. The etching time for the two layers were 150 and 15 s, respectively, such that the thickness of the top layer is ∼100 nm.

Following this, the samples were thermally treated at 1130 °C in hydrogen ambient at atmospheric pressure for 10 min. In one set of samples, no epitaxial layer was grown. In the other set, 40-μm-thick, n-type silicon epitaxial layers with an arsenic doping concentration of 10^{16} cm^{-3} were grown using atmospheric pressure chemical vapor deposition (APCVD) with trichlorosilane as the precursor.

Both types of samples were inspected using the Nova NanoSEM scanning electron microscope (SEM) to image the morphology of the different annealed porous silicon layers. From this, the median pore size at the LPL surface can be evaluated.

On the samples without an epilayer, stylus-based high-resolution profilometry measurements were performed on the LPL surface using HRP-200 (distributed by KLA Tencor), in order to analyze the local surface roughness of the growth surface after sintering. A typical scan length of ∼20 μm was used and more than 20 profiles were measured in each sample. In addition, some of these samples were also used for noncontact

optical profilometry measurements using NT9300 (distributed by Wyko), in order to measure the curvature of the substrate, from which the nature of the stress in porous silicon can be understood.

Some of the samples with an epilayer were defect-etched using the Wright etch solution [20] in order to calculate the crystal defect densities of the epilayers grown on different porous silicon templates. The defect-etched samples were inspected using an optical microscope with a differential interference contrast (DIC) setup in order to visualize and count the defects.

Two of the epilayer samples were also analyzed in cross section using a LabRam micro-Raman spectrometer with a laser of 514.5-nm wavelength to measure the stress distribution in the two porous silicon layers in cross section.

The remaining epilayer samples were passivated on the front side with 20 nm of intrinsic amorphous silicon and 10 nm of n^+ amorphous silicon (i/n^+ a-Si) using plasma-enhanced chemical vapor deposition (PECVD) at 200 °C. The detachment area was then defined by laser grooving using the TruMark Station 7000 distributed by Trumpf. The sample was then bonded to quartz using a 2-component silicone adhesive ("PV6100 Cell encapsulant," provided by Dow Corning), with the adhesive area smaller than the foil to be detached, such that the silicone is shielded during subsequent plasma processes, in order to minimize plasma-silicone interaction that will degrade the surface passivation quality and hence effective minority carrier lifetime [21]. After curing in a vacuum at 200 °C for more than 1 h, the samples were ultrasonicated for a few minutes in order to detach the epifoils from the parent substrates. The detached surface is then etched using an alkaline etchant to remove the residual porous silicon and the rear side is then passivated with PECVD i/n^+ a-Si as before. Minority carrier lifetime measurements are then performed on these passivated samples using the commercially available PL imaging tool (LIS-R1) from BT Imaging in which both quasi-steady-state photoconductance measurements (QSSPC) [22] as well as photoluminescence (PL) measurements can be performed. The samples were illuminated from the side of the quartz.

As a reference for lifetime measurements on porous silicon-based epifoils, lithography-based epifoils were also fabricated whereby the electrochemical etching of mesoporous porous silicon is replaced by dry etching of macropores patterned by deep-ultraviolet (DUV) lithography. This is based on the empty-space-in-silicon technique introduced by Mizushima *et al*. [23] and extended for solar cell applications by Depauw *et al*. [24]. This results in a epitaxial growth template that is close to ideal, as will be explained in Section IV-D. The rest of the process steps are the same as those for the porous silicon-based layer transfer process.

IV. Results and Discussion

The effect of varying the LPL thickness and porosity on the morphology and microstructure of the porous silicon, the stress distribution inside the porous silicon, the crystal defect density of the epilayer, and the lifetime of the epifoils is analyzed and explained in the coming sections.

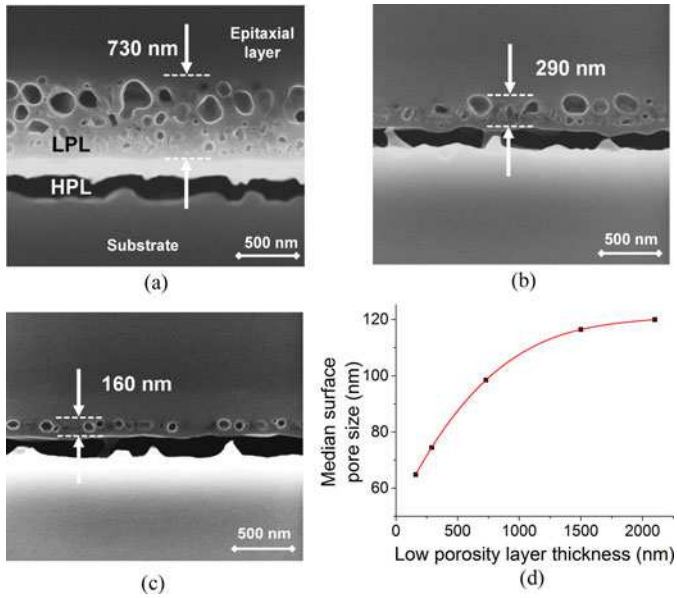

Fig. 2. Cross-sectional SEM images showing an epitaxial layer grown on top of a stack of porous silicon of two different porosities with a (a) 730 nm, (b) 290 nm, and (c) 160 nm thick LPL. (d) A plot depicting the correlation between the LPL thickness and the average surface pore or void size.

A. Annealed Porous Silicon Microstructure

The cross-sectional SEMimages of three epifoil samples fabricated as explained previously with three different LPL thicknesses (160, 290 and 730 nm) are shown in Fig. 2(a)–(c). Note that the two samples with thicker LPLs show a distribution of decreasing void sizes in depth, with the voids closer to the HPL being much smaller than those close to the epitaxial layer. This is in contrast with what was observed in [19] (who observed a uniform distribution of void sizes in the separation layer) and in [18] (who observed the opposite trend of increasing void sizes in depth).

This can be explained using the classical sintering theory. Porous silicon reorganization occurs through vacancy diffusion processes driven by a vacancy concentration gradient between the pore (or void) and its surrounding lattice. Voids grow or shrink in size depending on the direction of this vacancy gradient. The vacancy gradient depends on the vacancy concentration at the rim of the pore relative to the lattice vacancy concentration. The vacancy concentration C_v, at the rim of a pore of radius, r, is given by [18]

$$C_v = C_0 \left(\frac{2\alpha}{r} \frac{V_0}{kT} + 1 \right) \tag{1}$$

where C_0 is the equilibrium lattice vacancy concentration in silicon at temperature T (in kelvins), α is the surface tension coefficient, V_0 is the intrinsic vacancy volume in silicon, and k is the Boltzmann constant. From this relation, it is clear that the vacancy concentration surrounding a larger void is smaller. Due to this, there exists a critical void radius r_c beyond which voids grow in size and below which voids shrink and disappear depending on the direction of the vacancy gradient. This critical radius is inversely proportional to the lattice vacancy

supersaturation, which is defined as the excess lattice vacancy concentration above the equilibrium value at temperature T [19]. The lower the supersaturation, the higher the critical radius. As a result, as thermal reorganization proceeds and the overall vacancy supersaturation in the porous silicon reduces, the average void size increases throughout the porous silicon.

The surface of the porous silicon layer is a vacancy sink with the vacancy concentration close to the thermodynamic equilibrium (C_0). This results in a steep vacancy gradient that sharply reduces the vacancy supersaturation close to the porous silicon layer surface. This in turn increases the critical void radius near the porous silicon surface, resulting in an overall increase in the sizes of the voids there. As the near-surface vacancy supersaturation reduces, there will be a vacancy gradient from deeper in the porous silicon toward the surface, resulting in a continued growth of voids near the surface, and then subsequently deeper and deeper in the porous silicon. This eventually results in a distribution of smaller and smaller void sizes deeper into the porous silicon layer. A similar vacancy gradient also exists between the LPL and the HPL which drains vacancies from the LPL at the interface region, resulting in the further accentuation of this void size distribution in depth.

This void size enlargement at the porous silicon surface becomes more prominent for the case of the thicker LPLs, since there are greater number of shrinking voids deeper in the LPL contributing to this void growth. A similar consequence for the HPL exists for the samples with very thin LPL, the smaller volume of the LPL contributing to the enhancement of the porosity of the HPL results in a lower porosity in the HPL after annealing compared with a stack with thicker LPL. This results in a greater density of thicker interruptions or pillars, making detachment of epifoil samples on very thin LPL more difficult or impossible. In the case of the thinnest LPL (i.e., 160 nm), the entire LPL interacts with the HPL and the surface, both of which act as vacancy sinks resulting in the shrinking of all LPL voids.

Important morphological differences can be identified among the samples with different LPL thicknesses. First, the median size of the voids closest to the epitaxial growth surface increases with increasing LPL thickness, from ∼65 to ∼120 nm in the investigated samples. This trend continues to be true up to an LPL thickness of ∼2 μm, at which point it appears to saturate, as shown in Fig. 2(d). Second, the LPL voids have only reached their equilibrium shape in the thinnest LPL sample [see Fig. 2(c)], characterized by clearly discernible faceting. In contrast, the majority of the voids in the thicker LPL samples are in constant flux (shrinking or growing), thus having random shapes. Finally, while the voids in the thicker LPL samples are randomly stacked, the voids of the thinnest LPL are well aligned in a single lateral array. These differences are expected to manifest in the quality of the LPL growth surface.

The LPL surface, before epitaxy but after thermal reorganization, was analyzed using high-resolution profilometry. More than 20 profile scans were done and the root-mean-squared (RMS) values of all profiles were calculated, which is indicative of the roughness of the growth surface. Fig. 3 shows the distribution of the RMS values for four different LPL thicknesses. Clearly, the surface roughness of the growth surface

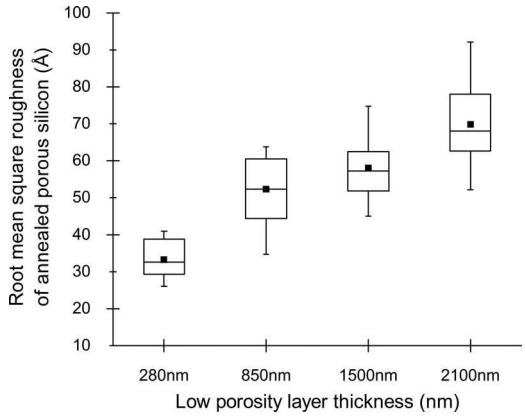

Fig. 3. Distribution of root-mean squared (RMS) values of the surface ordinates of the annealed LPL surface, calculated from more than 20 high resolution profilometry scans for four different LPL thicknesses, namely 280, 850, 1500, and 2100 nm. The three lines of the box plot refer to the 25th, 50th (median), and 75th percentiles and the lines/whiskers above and below the box extend to the 5th and 95th percentiles. The square symbol in the middle of the box plot refers to the mean value.

increases with the thickness of the LPL, because the pores are larger and more misaligned in the thicker LPLs, resulting in a rougher surface. A similar trend in the peak-to-peak roughness values was also observed, with the median peak-to-peak roughness that increases from ∼18 nm for the thinnest LPL to ∼35 nm for the thickest LPL investigated.

During epitaxy, the reactants are first adsorbed on the wafer surface where they react to form silicon atoms on the surface. This is followed by surface diffusion of the silicon atoms to the lowest energy sites on the surface, typically the edge of a step, leading to step flow growth. One of the factors that determine the quality of the epitaxy is the surface diffusion rate relative the arrival rate of the reactants. For high-quality epitaxy, the surface diffusion rate should be much greater than the arrival rate of the reactants. In a rougher surface, the surface diffusion rate is reduced and this will lead to more defects in the epitaxial layer. Thus, it can be expected that thinner LPL templates should result in a better growth surface for epitaxy.

B. Residual Stress in Porous Silicon

There have been reports on the presence of a residual tensile stress in electrochemically etched porous silicon, shown experimentally using X-ray diffraction [25] and micro-Raman spectroscopy [26] and explained theoretically by considering vacancy relaxation strain at the pore surfaces and thermal strain due to the difference in thermal expansion coefficients of silicon and porous silicon [27]. The residual stress is said to increase with pore size and has been reported to be in the range of a few hundred mega pascasl up to 1–3 GPa [26], [28]. The ultimate tensile strength of silicon is ∼7 GPa.

Cross-sectional micro-Raman spectroscopy measurements were performed on the epifoil samples of two different LPL thicknesses, 850 and 1500 nm. In the absence of stress, the Raman peak for unstrained silicon occurs at a wavenumber of $\nu_0 = 520.75\ \text{cm}^{-1}$. A shift in this wave number is a result of stress or change in crystallinity. Since the porous silicon layer is

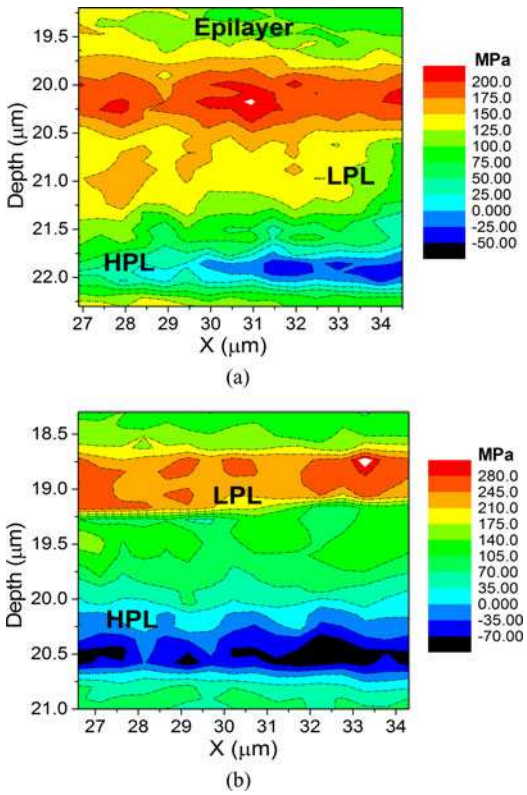

Fig. 4. Stress distribution maps obtained from cross-sectional micro-Raman spectroscopy for an epifoil sample with an LPL thickness of (a) 850 nm and (b) 1500 nm.

a quasi-monocrystal filled with voids, any peak shift is expected to be associated with a residual stress in porous silicon. The shift in the measured wavenumber ν relative to the unstrained silicon peak is then translated into stress values, σ (in Pa) according to [29]

$$\Delta\nu = \nu - \nu_0 = -2 \times 10^{-9}\sigma. \quad (2)$$

The cross-sectional stress distribution maps of the epifoil samples are shown in Fig. 4. Note that for the sample with an LPL thickness of ~850 nm, the entire porous silicon layer has been mapped [see Fig. 4(a)], while for the sample with an LPL thickness of ~1500 nm, only part of the LPL is shown in Fig. 4(b). Several observations can be made from these maps. First, a band of compressive stress (negative values) corresponding to the region around the HPL can be observed. Due to the relatively large spot size of ~1 μm compared with the 200 nm-thick HPL, it is not possible to conclude if this observed compressive stress is from the HPL or from the silicon surrounding this layer.

Second, the region above this band can be expected to correspond to the LPL which is predominantly in tensile stress (positive values) with values in the range of 100–300 MPa. As mentioned previously, this agrees well with investigations reported earlier. In addition, optical profilometry measurements to evaluate the curvature of samples with different LPL thicknesses without epilayer also indicate the presence of a tensile stress in porous silicon.

Third, a band of high tensile stress occurs in the region where the LPL transits into the epilayer. This feature [not shown in Fig. 4(b)] was observed in both samples. It should be noted that while the measured stress distribution gives an averaged value over a relatively large area of porous silicon, the stresses in the porous silicon could be much higher locally and more widely distributed. Although the stress distribution is rather nonuniform, the epifoil sample with a thicker LPL shows a higher average tensile stress compared with that with a thinner LPL.

This has important implications for the quality of the epifoil. First, a higher stress in the porous silicon implies a larger strain (even if we assume negligible difference in the Young's modulus between the two LPLs) and hence a larger lattice mismatch between the porous silicon and the growing epitaxial silicon. Although the silicon epilayer will grow pseudomorphically at the beginning despite the slight lattice mismatch, the strain will eventually be relaxed via dislocations and stacking faults after the film has reached a critical thickness. Second, it has been reported that strain fields are intensified near sharp features [30]. Thus, a rougher porous silicon template with a similar intrinsic stress is likely to have local concentrations of higher stress at the growth surface. Third, a thinner LPL with smaller pore size distribution (and possibly lower porosity [see Fig. 2(c)] is likely to be stiffer than a thicker LPL [31], [32]. A stiffer material with the same intrinsic stress will induce a lower amount of strain in the growing silicon epilayer. All of these support the fact that the intrinsic stress in porous silicon is likely to be more detrimental for epilayers grown on thicker LPL templates.

C. Crystal Defect Density Analysis

To verify the impact of the porous silicon properties on the quality of the epilayers, the defect densities of epifoils grown on different porous silicon templates were evaluated. Three epifoil samples with LPL thicknesses of 250, 1500, and 2100 nm, and two epifoil samples with triple layers (triple layer A and B) of porous silicon as explained in Section III, were defect-etched using Wright etch solution for ~70 s to reveal crystallographic defects present in the epilayer. A DIC optical microscope image of a defect-etched sample is shown in Fig. 5(a). The main defects observed in the epifoils after defect etching are dislocations, stacking faults, multiple stacking faults, and hillocks. Slip lines and orange peel defects were also observed among other defects. The square-shaped features in Fig. 5(a) correspond to etch pits, where stacking faults occur in the epifoil. The oval-shaped etch pits which appear as dots in the image are dislocations.

By sampling more than 50 locations in a defect-etched area of 3 cm × 3 cm, the areal density of the various crystal defects were calculated and the results are shown in Fig. 5(c). There is a clearly observable reduction in all the crystal defects as the LPL thickness is reduced. The total defect density reduces from ~1230 defects/cm^2 in the sample with a 2100 nm-thick LPL to ~420 defects/cm^2 in the sample with a 250 nm-thick LPL. This confirms our hypothesis that thinner LPL has a smoother surface and lower intrinsic stress, allowing a higher quality epilayer to be grown.

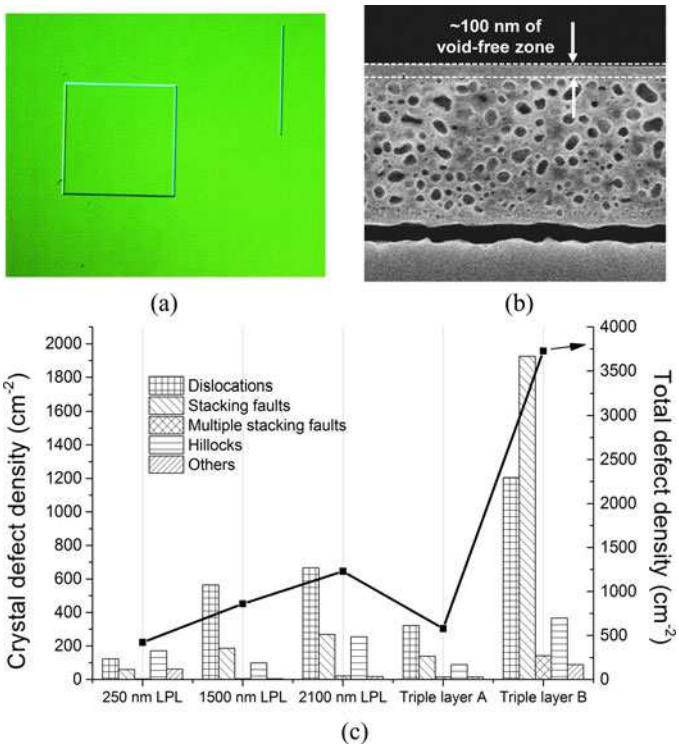

Fig. 5. (a) Optical microscope image in differential interference contrast (DIC) mode of an epitaxial layer surface after defect-etching using the Wright etch solution showing stacking faults and dislocations. (b) Cross-sectional SEM image showing the porous silicon template for the trilayer layer A sample with a third layer of lower porosity than that of the LPL, showing ~100 nm of void-free zone near the surface. (c) Areal density of various crystal defects for epifoil samples with different porous silicon templates. The total defect density is depicted as line and should be read off on the vertical axis on the right side.

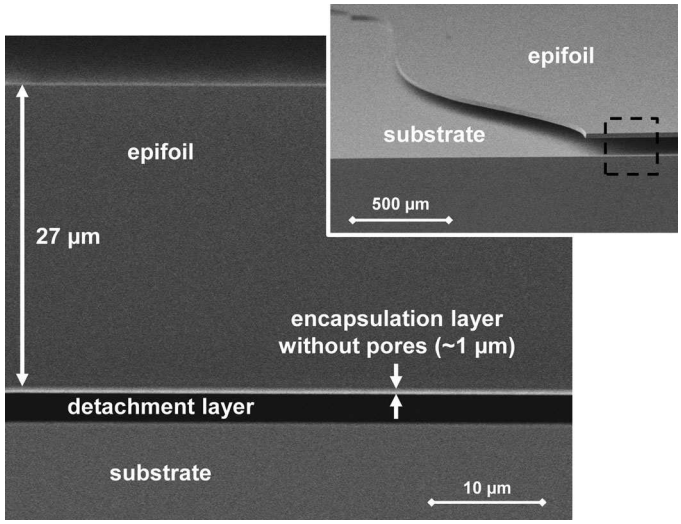

Fig. 6. Cross-sectional SEM image of the DUV lithography-based epifoil, showing pillar-free detachment layer and a pore-less encapsulation layer. (inset) Tilted view of the same sample at lower magnification.

For the triple layer sample A, it was observed that the overall defect density is significantly diminished to ~580 defects/cm^2 compared with a porous silicon template without this 100 nm layer (~860 defects/cm^2). By inspecting this porous silicon template (without an epilayer) using SEM [see Fig. 5(b)], it was observed that the top 100-nm region was almost void-free and the original lower porosity top layer acted as a sacrificial layer to create a zone free of voids. In contrast, the sample with an additional 100 nm of higher porosity top layer (triple layer B), the defect density is significantly increased to ~3730 defects/cm^2. This suggests that it is indeed the surface roughness and the stress distribution of the near surface region of the LPL that are critical in determining the crystal quality of the epifoil. In typical double layer stacks, a 10-nm-thick void-free zone near the surface has been reported [19] but besides being much thinner than the triple layer approach, it is not uncommon to find sporadic defects such as open voids breaching this zone.

D. Minority Carrier Lifetime Measurements

The ultimate figure of merit to benchmark the quality of the epifoil is minority carrier lifetime. Lifetime measurements were performed on two sets of glass-bonded n-type arsenic-doped (10^{16}/cm^3) epifoils. The first set was obtained using the porous silicon-based layer transfer approach, while the second set was fabricated using lithography-based layer transfer process, which creates a pillar-free detachment layer, encapsulated by a pore-free monocrystalline silicon seed layer [24], as depicted in Fig. 6. Since the encapsulating layer is pore free, epifoils produced from this approach can act as a reference for the lifetime measurements on porous silicon-based epifoils. For the porous silicon-based epifoils, three different LPL templates of the following thicknesses were used: 2100, 1400, and 720 nm. These samples were safely detachable with high yield. Much thinner LPL samples ($\leq$250 nm) that were investigated did not detach well, since they had higher densities of thicker pillars in the HPL making detachment impossible. Dedicated optimization is needed to achieve good detachment in samples with very thin LPL.

Lifetime measurements on both sets of epifoils were performed using quasi-steady-state photoconductance (QSSPC), and the best lifetime results are plotted in Fig. 7. Among the porous silicon-based epifoils, a clear trend in the effective lifetime is observed whereby the highest lifetime was measured in the epifoils grown on the thinnest LPL and reaches an excellent lifetime of ~195 μs at an injection level of 10^{15} cm^{-3}, whereas the epifoil with the thickest LPL only yielded ~85 μs at the same injection level. A comparison of the reference lithography-based epifoils with the porous silicon-based epifoils show a drastic difference in the best lifetimes obtained thus far, with the lithography-based epifoils exceeding 350 μs at the injection level of 10^{15} cm^{-3}. Since both sets of epifoils are identical except for the template layer for epitaxial growth, it is clear that by reducing the LPL thickness and/or porosity such that the voids in the LPL vanish (at least close to the interface with the epilayer), a drastic improvement in the lifetimes of porous silicon-based epifoils can be achieved. This is why porous silicon stacks like the one of triple layer A have potential in further improving the lifetime of porous silicon-based epifoils.

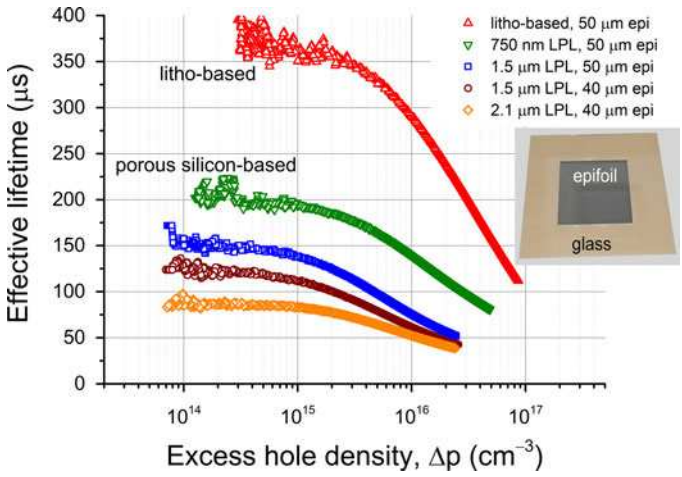

Fig. 7. Effective lifetimes as a function of injection level measured using QSSPC for porous silicon-based epifoils grown on three different porous silicon templates as well as lithography-based epifoils, confirming that higher quality epitaxial growth is obtained on thinner low-porosity layers. (inset) A photograph of a layer-transferred epifoil.

V. Conclusion

The quality of the epifoils produced using a porous silicon-based layer transfer process can be improved by controlling the properties of the LPL, which acts as the template for epitaxy. By reducing the thickness of this layer or the near-surface porosity of the porous silicon, the average near-surface pore size is reduced and better void alignment is achieved. This results in a less-defected and smoother surface with a lower residual stress distribution in porous silicon leading to a lower epilayer defect density of $<$420 defects/cm^2.

However, epifoils grown on very thin ($\leq$250 nm) LPL templates have detachment issues due to the reduced porosity and increased pillar density and size in the HPL. Thus, for the range of samples investigated, the thinnest LPL that still allows reliable detachment is $\sim$720 nm thick. Therefore, lifetime measurements could only be performed on epifoils grown on templates with an LPL thickness of $\geq$720 nm, which has higher defect densities than the best reported in this paper. Nevertheless, an enhancement in minority carrier lifetime in n-type epifoils of $>$100 μs has been achieved by reducing the LPL thickness up to $\sim$720 nm, with the effective diffusion length improving from $\sim$300 to $\sim$470 μm. Thus, the best porous silicon stack for achieving high lifetimes while maintaining reliable detachment is the one where the LPL thickness is $\sim$720 nm. This is much less than the standard thickness of $\sim$1–2 μm that is currently used [16], [33]. However, it should be noted that optimization of the porous silicon stack for reliable detachment was not done as part of this study, which leaves scope for improvement of the detachment yield of porous silicon stacks with thinner LPL (which could result in higher lifetimes).

Another alternative that is proposed in this study is to engineer a porous silicon template in such a way that the voids of the LPL are kept as far away from the growth surface as possible after sintering. To this end, a triple layer approach is introduced in this study, whereby a third very low porosity layer is added on top of the LPL to create a 100 nm-thick zone free of voids. This reduces the defect density of the standard detachable stack by more than 1.5 times. However, lifetime measurements on epifoils from such a stack must be performed to prove the actual benefit of this, while still allowing reliable detachment. An ideal reference system is the lithography-based epifoil, which has a seed layer free of enclosed voids. Lifetimes on such epifoils exceeded 350 μs (i.e., 600 μm diffusion length), indicating that it is possible to further improve the lifetime of porous silicon-based epifoils if the presence of voids in the LPL can be completely eliminated. To the best of our knowledge, these lifetime values are the best reported so far in thin silicon.

It must be noted that these results were obtained starting from mirror-polished substrates. It is expected that the nature of the starting surface will also influence the quality of the epitaxial film that is eventually grown on it. One of the corner stones of the layer transfer approach is the reuse of the parent substrate. It can be expected that the starting surface roughness of parent substrates is likely to be higher after the first layer transfer has been performed. Thus, it is worthwhile performing a similar study on reused substrates. Nevertheless, the results reported in this study are expected to largely hold for parent substrates that will be reused after surface conditioning (as indicated in Fig. 1). This is because, first, for an optimized layer transfer process, the surface of the parent substrate after detachment remains highly polished with nanoscale roughness that results from broken pillars during detachment. Second, it is not only the surface roughness that influences the epifoil quality but also the stress in porous silicon as was suggested in this study. Third, the substrate has to be chemically (or electrochemically) polished before reuse to remove the surface layer containing broken pillars which returns the surface close to that of a mirror-polished surface before the next cycle of layer transfer. Polishing removes $<$5 μm of silicon and this is still an order of magnitude less than the current state-of-the-art kerf loss for wafers [34].

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