Practical High-Resolution Programmable Josephson Voltage Standards Using Double- and Triple-Stacked $MoSi_2$-Barrier Junctions

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***Abstract*—We have developed vertically stacked superconductor- normal-metal-superconductor Josephson junction technology for the next-generation quantum voltage standards. Stacked junctions provide a practical way of increasing the output voltage and operating margins. In this paper, we present fully functioning programmable voltage standard chips with double- and triple- stacked $MoSi_2$ barrier Josephson junctions with over 100 000 junctions operating simultaneously on a 1 cm $\times$ 1 cm chip. The maximum output voltages of the double- and triple-stacked chips were 2.6 V and 3.9 V, with respective operating current margins of 2 mA and 1 mA. A new trinary-logic design is used to achieve higher voltage resolution. Thermal transport in these high-density chips will be briefly discussed.**

***Index Terms*—Josephson arrays, programmable voltage standard, superconducting integrated circuits, superconductor-normal-superconductor devices.**

I. Introduction

SUPERCONDUCTOR-NORMAL-METAL-SUPERCONDUCTOR (SNS) Josephson junctions have been successfully used in programmable Josephson voltage standards (PJVS) [1]–[3] and Josephson arbitrary waveform synthesizer (JAWS) [4]. For PJVS, PdAu-barrier junction-based 1-V programmable systems are now used in metrology labs [5]–[7]. For JAWS, a quarter-volt output of single-tone ac voltage waveform was recently demonstrated with harmonic distortion below -93 dBc and excellent operation margins [6], [7]. These systems consist of series arrays of junctions, whose performance (e.g., the maximum output voltage, operating margins, and frequency response) can be enhanced by increasing the linear junction density. The most promising method seems to be stacking junctions vertically [8]–[10]. We have found that $MoSi_2$ provides a stable, reproducible, and dry-etchable barrier for stacked SNS junctions. We also found that stacked junctions can be made with small 20 nm superconducting intermediate electrode thicknesses [11]. We have demonstrated uniform arrays with up to 10 junctions per stack that show flat constant voltage steps with a microwave bias [12]. We have also recently generated precision ac waveforms using double- and triple-junction stacks [13], [14].

In this paper, we report fully functional programmable voltage standard circuits with double- and triple-junction stacked arrays that are sufficiently uniform that precision dc voltages can be produced with practical operating margins.

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TABLE I

Cell Number	Number of Stacks	Double-stack current margins (mA)	Triple-stack current margins (mA)
1	4400	2.28	1.26
2	4400	2.01	1.15
3	4399	1.96	1.35
4	4400	2.03	1.36
5	4398	2.05	1.18
6	4400	2.21	1.23
7	4396	2.06	1.10
8	1944	2.17	1.25
9	648	2.07	1.48
10	8	2.82	2.10
11	24	2.44	2.01
12	72	2.76	2.31
13	216	2.55	2.06

Array cell characteristics for double- and triple-stacked chips operated at 18.5 GHz. Number of stacks in the cells should be multiplied by the number of junctions in a stack (2 for double, and 3 for triple) to get the total number of junctions in each cell. The current margins are defined as the range of bias current over which the quantized $n = 1$ voltage step is flat within a 1 μV threshold. $n = 0$ steps are larger than 7 mA in all cells at the optimum microwave power.

II. Design and Fabrication

The chip design we have used is basically the same as that for the NIST 1 V programmable Josephson voltage standard circuit with PdAu-barrier SNS junctions. Our previous circuit used a binary-logic design in which a series-connected junction array was divided into smaller array cells in a binary sequence [1]. Binary logic uses two states of the junction, one at a fixed voltage on the Shapiro step and the other at zero volts. However, since we have both $n = \pm 1$ constant-voltage steps available in addition to the zeroth step, we are able to use three different voltage states for our PJVS. Hence we redesigned the array cells in a trinary-logic sequence, in order to utilize all three voltage levels and increase the voltage resolution [15]. The number of junctions in each cell, as well as the operating range, is summarized in Table I. The zero step ranges are larger than 7 mA, which is sufficient for easy operation. This new design allows us to access a single stack as the least significant bit (LSB or the smallest

voltage increment), by combining two large cells with opposite (one positive and one negative) polarities, while keeping the same number of array cells and bias leads as the previous design [1], [15]. At 18.5 GHz, the voltage resolution corresponds to 38 μV for a single junction, and 115 μV for a triple-junction stack. This is a significant improvement upon our conventional binary-logic circuit, which has 128 junctions (or stacks) in the smallest cell and thus a resolution of 4 mV at 16 GHz operating frequency [1]. Our new high-resolution PJVS design contains 33 705 stacks divided into 13 cells on a 1 cm $\times$ 1 cm chip; hence the total number of on-chip junctions is 67 410 for the double-stacked chip and 101 115 for the triple-stacked chip. As a direct consequence of the increase in the junction number, the maximum programmable voltage is doubled or tripled by using the stacked junctions.

The fabrication process begins with a multilayer deposition of Nb electrodes and 22 nm thick $MoSi_2$ barrier layers on an oxidized 3-inch Si wafer. Rectangular-shaped $4\ \mu\mathrm{m} \times 8\ \mu\mathrm{m}$ junctions are defined by use of an inductively-coupled-plasma (ICP) deep reactive-ion etching (DRIE) with a mixture of etch (SF_6) and passivation (C_4H_8) gases [12]. The Nb base electrode is defined with a SF_6 RIE, followed by deposition of an insulating SiO_2 layer by means of a plasma-enhanced chemical-vapor- deposition (PECVD) system with backside He gas cooling. Vias in the SiO_2 oxide and Nb wiring are respectively RIE patterned with CHF_3 and SF_6 gases. Subsequently, a PdAu film is patterned by lift-off for on-chip resistors and contact pads. Finally, a layer of insulating SiO_2 is deposited for passivation, followed by via etch and lift-off of additional PdAu for robust pads.

Because of the excellent controllability of $MoSi_2$-barrier junctions, the characteristic voltage $V_c = I_c R_n$ can be tuned to better than $\sim$ three microvolts. For the PJVS chips reported in this paper, the characteristic voltage of the junction is chosen to be 48 μV, and the corresponding junction critical current I_c is 11.5 mA.

III. Results

The chip is tested on a commercially available NIST 1-V PJVS cryoprobe with a flip-chip fingerboard that is immersed in liquid helium during the measurement [16]. Fig. 1 shows the current-voltage $(I-V)$ characteristics of one of the largest array cells on a triple-stacked chip at 22 GHz microwave bias. Although the other individual array cells operate well over a wide range of frequencies up to $\sim$23 GHz, the frequency response of the entire chip strongly depends on the operating frequency [15]. Therefore, we fixed the operation frequency at 18.5 GHz, which appears to be optimal for this circuit. The operating current ranges of the individual cells in double- and triple-stacked circuits are summarized in Table I. These current ranges reflect the bias range over which the step is at the correct voltage within a 1 μV voltage threshold on the digital nanovoltmeter's 1 V scale. The microwave power is adjusted to generate an optimum current range. Functionality of the entire chip is determined with a high-resolution voltage measurement near zero volts, where half of the junctions are biased on the positive step and the other half on the negative step [15]. The current range of the voltage step in this precision measurement determines

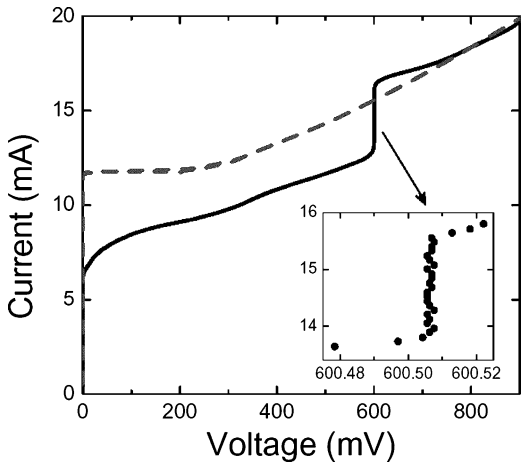

Fig. 1. Current-voltage $(I-V)$ characteristics of the largest array cell of 4400 stacks with three Josephson junctions per stack (13 200 series junctions). With 22 GHz microwave drive (solid line and the inset), the cell shows a flat voltage step at 600 mV with current range greater than 1 mA. Dashed line is the $I-V$ characteristic without the microwave bias.

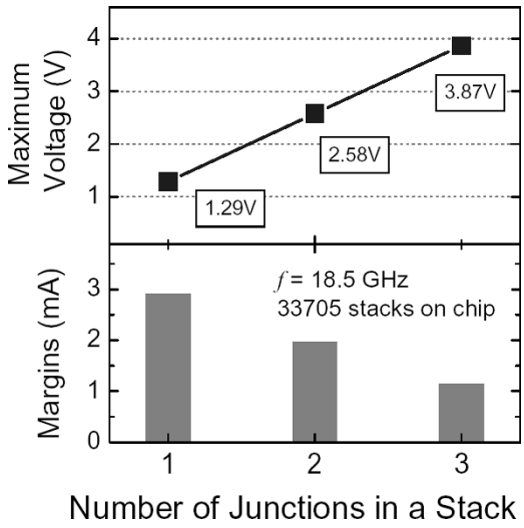

Fig. 2. Maximum programmable voltages and operating current margins measured at 18.5 GHz in single-, double-, and triple-stacked junction circuits. Each 1 cm $\times$ 1 cm chip contains 33 705 stacks divided into 13 array cells, with a trinary-logic design for high voltage resolution. The margins apply to full chip operation, namely the current range over which all junctions on the chip are simultaneously biased on a non-zero quantized voltage step.

the operating margin for the entire circuit, and was found to give nearly a 2 mA margin for the double-stacked circuit and a 1 mA margin for the triple-stacked circuit. The maximum programmable voltages were respectively 2.58 V and 3.87 V for double- and triple-stacked circuits.

Fig. 2 summarizes the maximum programmable voltage and the current margins of single-, double-, and triple-stacked circuits at 18.5 GHz. The reduction in the operating margins is most likely due to microwave attenuation along the increasingly longer arrays as the stacks get taller and each array cell has more junctions. The frequency dependence of the circuits [15] is likely due to the nonuniformity in the distribution of the microwave power across the chip, and can be improved by our new soldered flexible cryopackaging [17]. Since the circuit was originally designed to be operated at 16 GHz, which is determined

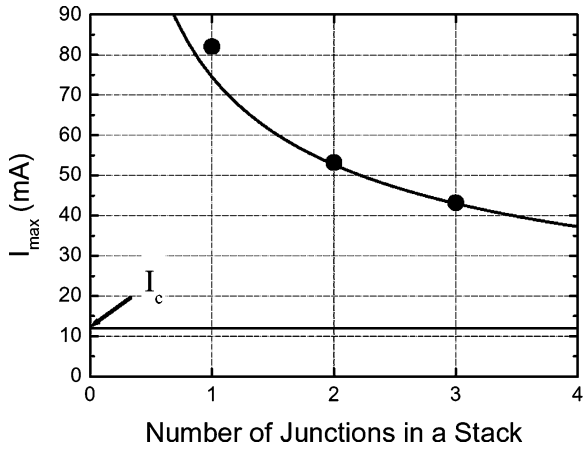

Fig. 3. Maximum current (I_{max}) of the junction array before the Nb wiring goes normal. The line is a fit to the thermal transport model with I_{max} proportional to $N^{-1/2}$, where N is the number of junctions in a stack. The thin middle Nb electrode is the superconducting layer that goes normal first for the stacked arrays. The single, non-stacked junctions have I_{max} above the model curve since it has no middle electrode, so that a thicker top or bottom electrode turns normal at an I_{max} slightly higher than the curve which is fit to the stacked array data.

by the center frequency of the on-chip quarter-wave filters and impedance transformers [1], the microwave design needs to be further optimized if we wish to operate the circuit at frequencies other than 16 GHz. However, the operating margins of these chips are already sufficient to be used in practical metrology applications that require programmable, quantum- based, precision dc voltages [5].

IV. Thermal Design

Fig. 3 shows the maximum current (I_{max}) of the junction array circuit at which some superconducting element in the junction circuit goes normal (without microwave) due to excessive heat from the resistive junctions. We have previously studied this maximum current and used it to investigate and optimize the thermal properties of the stacked junction circuits [18]. According to the model, I_{max} will follow the scaling

$$I_{\max} \propto W_J^{\frac{3}{2}} N^{-\frac{1}{2}}, \tag{1}$$

where W_J is the lateral junction dimension and N is the number of junctions in a stack, assuming the base electrode size is larger than the thermal healing length [18]. We observe a reduction of I_{max} as we increase the number of junctions in a stack, as shown in Fig. 3. For practical use, the value of I_{max} should be much larger ($\sim$3 times) than I_c or the typical operating current; otherwise the junctions easily trap magnetic flux producing a lower junction critical current due to flux-flow, which in turn reduces the operating margins of the constant voltage steps. This is also an indication that self-heating of the junctions or stacks becomes more significant as the junctions are more densely packed. Therefore, an improved thermal design is required for taller-stack arrays.

Note that when our PJVS chip is fully biased, the triple-stack chip is dissipating $\sim$200 mW of combined dc plus microwave power. As a result, the circuit itself generates a large amount of heat during operation. Although the chip is fully immersed in liquid helium, we begin to see signs of heating, such as a slight reduction of I_{max}, when junctions in other cells are biased in the voltage state, compared to that of biasing a single cell alone. It also implies that cooling of the chip is already an important issue, and such high power dissipation will eventually affect the chip performance in any cryocooled dense circuits. When circuits are designed for even higher voltage or higher junction densities, thermal considerations must be foremost in the design.

V. Conclusion

We have successfully demonstrated programmable voltage standard circuits with a 3.87 V maximum programmable voltage and having practical operating current margins greater than 1 mA. Double- and triple-stacked Josephson junction arrays with $MoSi_2$ barriers showed sufficient uniformity, yield and reproducibility to allow fabrication of those circuits with more than 100 000 junctions. This is a significant step forward toward the development of a robust 10-volt programmable voltage standard system with large operating current range.

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