PAPER

A Single-chip 1 GHz Band-Pass LNA for RF ICs

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Summary
A fully integrated tuned band-pass low noise amplifier at 1 GHz using the Boot-Strapped Inductor approach is described. The main performance of the circuit are: a bandwidth of 30 MHz, a Noise Figure of 2.33 dB, a transducer power gain of 28.5 dB, an Input-referred third-order Intercect Point of –17.2 dBm and a power consumption of 19.5 mW. The total area occupancy on silicon die is 0.92 mm^2.

Key words:
Low noise amplifier, fully integrated, active inductor, wireless, radio frequency.

1. Introduction

A key issue for the design of integrated resonant LC filters suitable for modern wireless systems is represented by inductors. Though the design of integrated inductors has been widely explored [1], at the moment it is not possible to obtain high-quality inductors in standard silicon technologies without extra-process steps. In [2] the idea of using an integrated transformer and a current amplifier, to obtain high quality factor *(Q)* equivalent inductors, has been proposed. This solution, has been called Boot-Strapped Inductor (BSI) in order to distinguish this topology from those based on the utilization of active devices and capacitors [3][4], and from those based on the implementation of negative resistance bipoles [5]. The BSI circuit has been demonstrated to be capable to get Q > 40 [2] and it can be efficiently used to design fully-integrated, band-pass, Low Noise Amplifiers (LNAs) [6].
Such an approach has allowed to design single-chip RF heterodyne receiver front-end with high signal image rejection [7].
In this paper, the basic concepts about the BSI are summarized in the Section 2. The selective LNA based on BSI approach is presented in the Section 3 and the simulation results are reported in the Section 4. The experimental results of the LNA prototype are highlighted in the Section 5. Finally, in the Section 6, the conclusions are drawn.

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2. The Boot-Strapped Inductor circuit

The BSI circuit exploits the magnetic coupling between two spiral inductors (L_1 and L_2 in Fig.1) to increase the value of the equivalent inductance seen between two input terminals (1- 1').

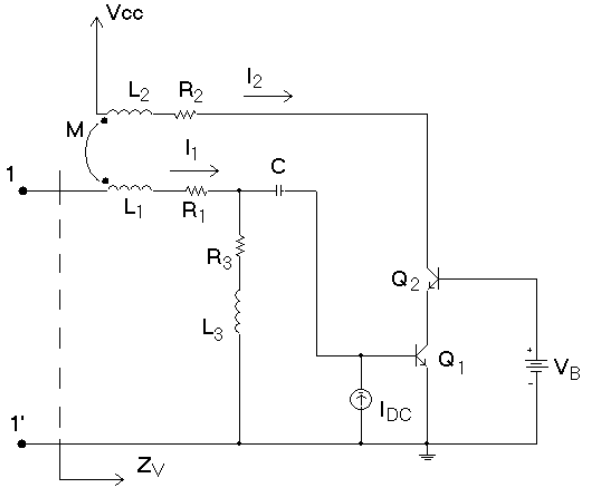


Figure 1. Simplified scheme of the Boot-Strapped Inductor circuit.

The input impedance Z_V of the BSI circuit in Fig.1 is [1]:

$$Z_V = [R_1 - \omega \cdot M \cdot h_{fe} \cdot \sin\varphi] + j\omega \cdot [L_1 + M \cdot h_{fe} \cdot \cos\varphi] \qquad (1)$$

where, R_1 is the parasitic series resistance of L_1 and M is the mutual inductance between L_1 and L_2. h_{fe} is the magnitude of the current gain for small signal (I_2/I_1) and φ its phase. L_3 allows to compensate the effect of the input capacitance (Cin) of the cascode amplifier. In this way, φ can be kept very close to 0° and an increase of the imaginary part and, at the same time, a reduction of the real part of Z_V can be achieved. The current gain h_{fe} can be controlled by varying I_{DC} ,whereas the value of φ can be controlled by varying the voltage V_B. Infact, chosing the operating point of Q_1 and Q_2 around the knee of the Cin curve (see Fig.2, Cin vs. V_B), a large range of variation for the equivalent inductance value offered by the BSI (at the terminals 1-1') can be achieved. This effect can be used in order to compensate the spreading of the parameters due

to process tolerances for thermal variations. The robustness of this approach has been demonstrated in [8][9].

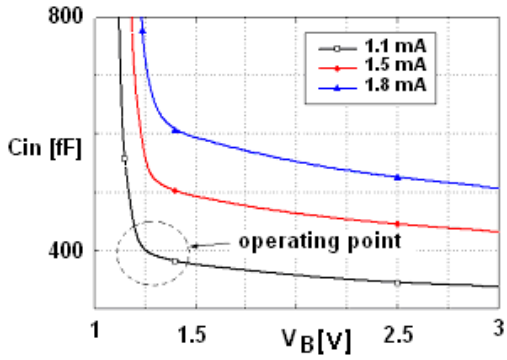


Figure 2. The input capacitance (Cin) of the cascode amplifier vs. $V_{B,}$ for different values of the bias current I_{DC}.

3. The LNA based on the BSI approach

To validate the effectiveness of the BSI approach, a selective LNA, based on the circuit depicted in Fig.3, for 1 GHz operations, has been designed.

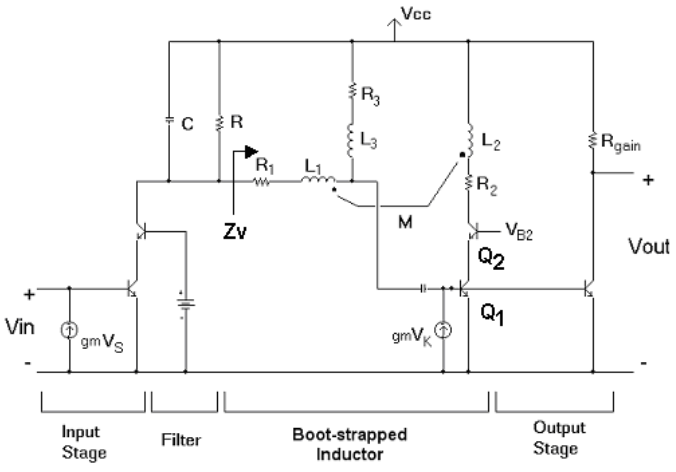


Figure 3. Simplified schematic of the selective LNA.

The input stage is a cascode amplifier which sets the overall Noise Figure (NF). It drives a RLC filter where L is the equivalent inductance realized by means of the BSI circuit in which V_K and V_{B2} are two control external voltages. R allows to fix the maximum gain and the output stage drives the load. V_K and V_S are the bias voltages of the input and output current mirrors respectively (to simplify the scheme shown in Fig.3, only the equivalent transconductance gm is shown).

The amplifier has been designed in STM's HSB2 (high speed bipolar) process with 25 GHz of cut-off frequency and three levels of metal. The layout is shown in Fig. 4: the overall chip size is 0.96 mm^2.

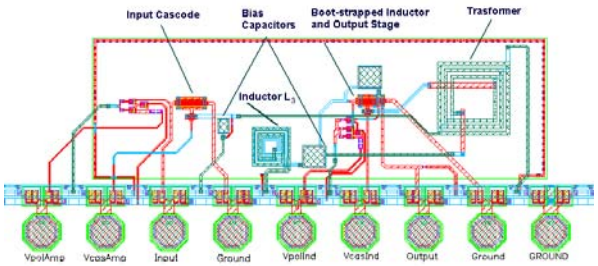


Figure 4. Layout of the LNA.

4. Post-layout simulation results

As far as the integrated transformer and inductor is concerned, the results of the electromagnetic simulations described in [8] have been confirmed by means of Asitic simulator as well. At 1 GHz, the values are: L_1= L_2= L_3=2.5 nH, R_1=5Ω, R_2=16Ω, M=2.2 nH and R_3=6. An accurate modelization of the package [10], of the bonding wires and of the evaluation board has been done to obtain reliable results. The complete circuit (post-layout and parasitic effects) have been simulated by means of Advanced Design System™ (by Agilent Technologies). The transducer power gain G_T (defined as the ratio between the power supplied to the load (50 Ω) P_L and the available power at the input P_{ain}) vs. frequency is depicted in Fig. 5.

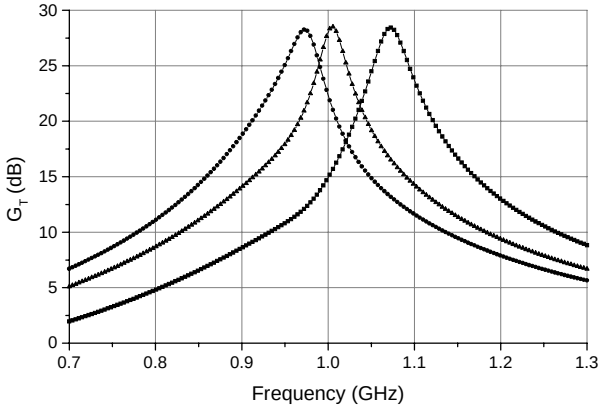


Figure 5. Trasducer power gain G_T vs. frequency.

The intermediate curve reaches a peak value of 28.5 dB at 1 GHz for a band-width of 30 MHz, which results in a quality factor Q (defined as f_0/B, where, f_0 is the central

frequency of the filter and *B* is the Bandwidth) of 33. The central frequency of the amplifier can be tuned by means of the control voltages V_K and V_{B2} also to compensate for thermal excursions and/or variations of the process parameters. Figure 5 shows that f_0 can be varied from 0.97 GHz to 1.07 GHz with a Q always greiter than 25.
The Noise Figure, with a source impedance of 50 Ω, is 2.33 dB. The Input (Output) 1 dB Compression Point, ICP_{1dB} (OCP_{1dB}), is – 34 dBm (-6.5 dBm) as shown in Fig.6.

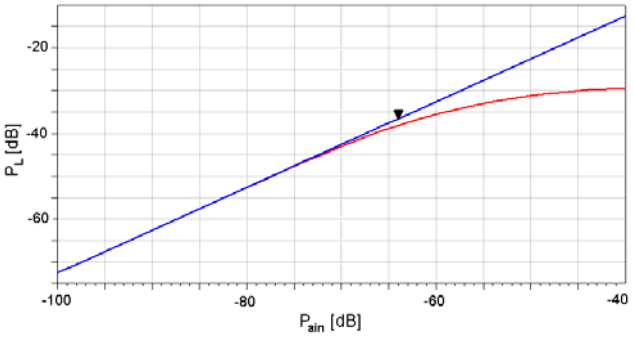


Figure 6. The 1 dB Compression Point. P_L is the power supplied to the load (50 Ω) and P_{ain} is the available power at the input.

The Input-referred third-order Intercept Point (IIP3) has been evalueted considering two foundamental tones at f_1 =1.001 GHz and f_2 =1.011 GHz. The IIP3 is -17,2 dBm as shown in Fig. 7.

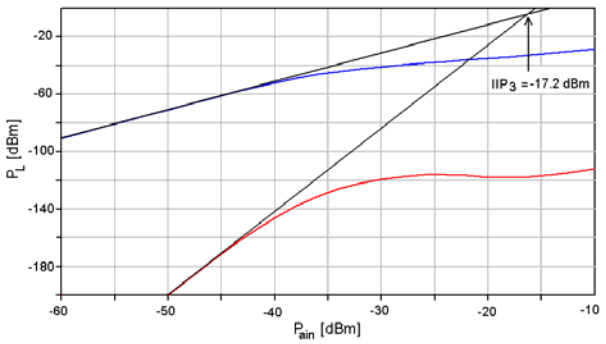
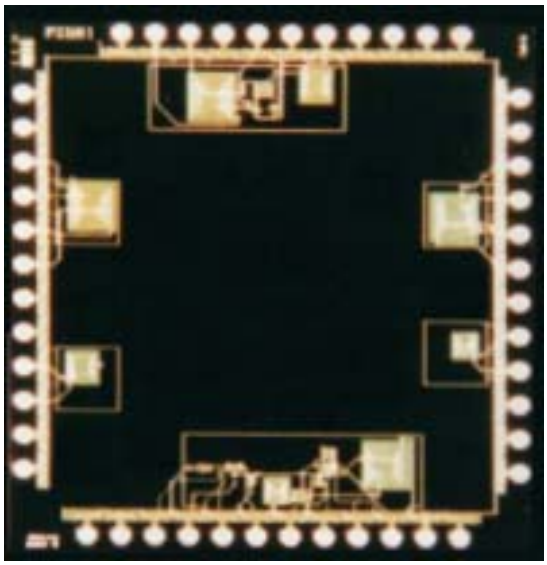


Figure 7. The 3-rd order Intercept Point: the two fundamental tones are at f_1 =1.001 and f_2 =1.011 GHz.

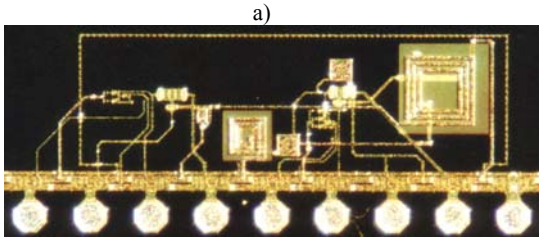
5. Experimental results

A picture of the chip prototype, manufactured by ST (Catania site, Italy) is shown in Fig. 8. The die has been packaged in a TQFP48.

The typical measured frequency response of the LNA in terms of transducer power gain (G_T) is depicted in Fig. 9. The curves have been obtained by using the same sample with three different couples of values for the control voltages V_{B2} and V_K. The amplifier is tunable between a central frequency of 0.957 (curve 1) and 1.027 GHz (curve 3); in all cases, G_T is always greater than 27 dB and the



a)



b)

Figure 8. a) Picture of the entire chip: the BSI circuit is on upper side of the die; the LNA is below; two different couples of passive inductors and transformers are on left and right side. b) The LNA circuit as detail of the previous picture.

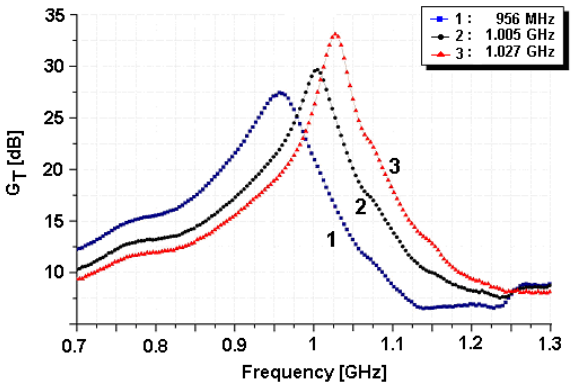


Figure 9. Trasducer power gain G_T vs. frequency.

quality factor is greater than 20. The value of Q is maximum at the highest value of the explored frequency range (i.e., f_0 = 1.027 GHz for this sample). Figure 10 shows the good matching between simulation and measurement results.

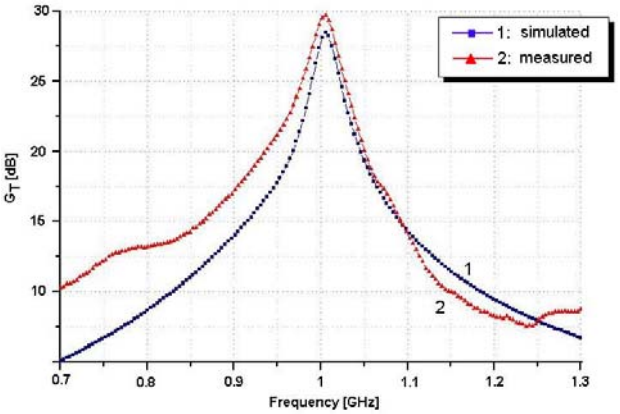


Figure 10. G_T vs. frequency : a comparison between simulation (curve 1) and measurement results (curve 2).

The measurements have been performed on a set of 10 packaged samples. They have been characterized in order to give an indication of the repeatability of the results and of the possibility to compensate the process parameter tolerances by means of the external control voltages. The results of the test chip campaign are as follows: i) one sample failed, ii) seven devices were tuned to the same nominal resonance frequency (that is f_0 =1.016 GHz) with an attenuation greater than 20 dB at 1.216 GHz (that is 200 MHz above f_0); iii) two samples showed a slightly higher resonance frequency (about 1.09 GHz) which could be tuned to the nominal value f_0 (even using the control voltages) only at the expenses of a degradation in the selectivity (i.e. accepting an attenuation greater than 20 dB). The results are summarized in Figure 11.

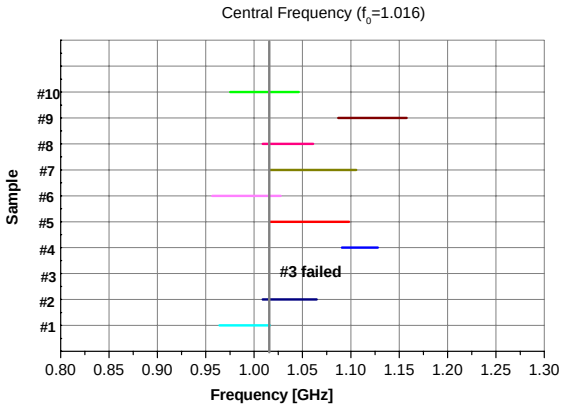


Figure 11. Results of the prototype samples characterization.

In Figure 11, for each sample, the solid line determs the frequency range within f_0 can be varied and the attenuation at 200 MHz (from f_0) is greater then 20 dB.
This means that, by using a supereterodyne architecture with 100 MHz of intermediate frequency, and by considering the aforementioned performance in terms of f_0 and attenuation as a "pass/reject" criterion, the yield of the process would be equal to 70%.

6. Conclusions

The results this characterization of the manifactured chip demonstrate the potentiality of the Boot-Strapped Inductor technique in terms of selectivity, power consumption, robustness of the design, controllability of the resonance frequency f_0 and yield.
A comparison with actual state of the art for band-pass LNAs [11] is reported in Table I.

	Q (f_0/B)	***f_0*** [MHz]	***NF*** [dB]	***IIP3*** [dBm]	P_D [mW]
Wu	30*	869-893*	6*	-14*	78*
Chan	34	881	6	-12.4	52.5
Than.	30-56	900-1000	4.3	-27	50*
Abou	20	1900	5.3	-	-
Leung	32	947.5	5.2	-32.5	45
Chan	32	1800	3.56	-15.26	35.7
Our	33 *	957-1027*	2.33	-17.2	19.5*

Table I: Comparison with the state of the art. The results marked with ' * ' are referred to measurements.

It can be observed that our solution is the only one capable to contemporaneously acheive high selectivity, low Noise Figure and low power consumption. The linearity, in terms of IIP3, is quite good as well. Moreover, it should be noted that only the circuit given by Wu, presents the

results of the experimental characterization of a prototype, whereas the other data in the table refer to simulations. Finally, only in our case a preliminary characterization has been carried out, in terms of repeatibility of the results and yield.

Acknowledgments

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