Tuned LNA for RFICs using *boot-strapped* inductor

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Abstract — **In this paper, the principle of operation of a new type of active inductor and its application to a tuned LNA are described. The design is optimized at *1.8* GHz. An integrated transformer in connection with a current amplifier realizes a "boot-strapped" inductor with a L x Q factor never obtained before at this frequency. This way a selective LNA with a *60* MHz bandwidth, corresponding to a Q of *30*, was designed. The circuit exhibits a matched noise figure of *1.8* dB with *25.5* dB transducer power gain while dissipating *20.7* mW from a *3* V power supply.**

I. INTRODUCTION

The realization of high quality factor (Q) integrated inductors is one of the most intriguing problems in the design of RF front-ends for integrated transceivers. In a previous work [1] the results which can be obtained in terms of inductance (L) and Q values by using a novel circuit topology have been described. This solution, whose basic principles will be briefly summarized in Section II, allows to obtain very high value of the Q x L factor. Other solutions, based on the utilization of active devices, have been proposed in the past to improve the Q factor with respect to that of passive spiral inductors [2-3]. However, none of these solutions is capable to increase the effective L value which, in silicon integrated devices, is normally limited to a few nanoHenry at frequencies of about *2* GHz. The approach proposed in this paper allows to improve both the effective values of L and Q, almost up to a factor of *10*, while keeping practically constant the occupied silicon area. As it will be shown in Sections III an IV this solution can be advantageously used to design tuned Low Noise Amplifiers (LNA) capable, for instance, of attenuate the image frequency by *25* dB @ *200* MHz of intermediate frequency.

II. BOOT-STRAPPED INDUCTOR

In order to increase the Q-factor of integrated inductors (defined as the ratio between the imaginary part and the real part of its impedance) many techniques have been presented [4, 5]. Nevertheless it is not simple to obtain Q-factors greater than *8* for inductors of few nH. Indeed, achievable Q values decrease as the inductor value rises. An improvement of Q can be obtained by using active circuits to compensate for the losses of the integrated inductor [6]. This method, anyway, does not provide any increase of the inductance value and it may lead to instability. Moreover, the robustness versus the process parameter tolerances, and, consequently, their practical implementation, has not been demonstrated yet.

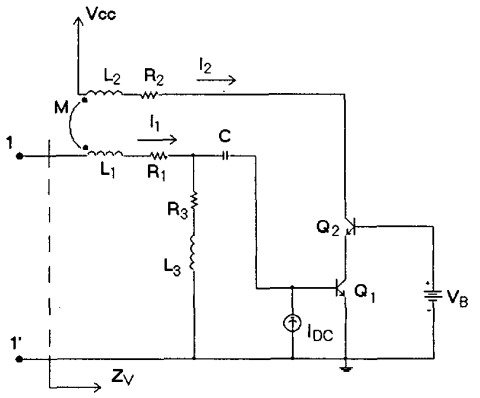

Fig. 1: Boot-strapped inductor

Here, we propose a solution based on the circuit depicted in Fig 1. This circuit exploits the magnetic coupling between two spiral inductors (L_1 and L_2 in Fig. 1) to increase the inductance value seen at the input terminals 1-1'. The inductor L_3, its parasitic series resistance R_3 and the base-emitter capacitance of Q_1 realize an LRC filter. If the value of L_3 is chosen in such a way to resonate with the input capacitance of Q_1, then the current through L_1 is in phase with the base-to-emitter voltage of Q_1. In this case, the currents I_1 and I_2 are in phase, provided that the equivalent transconductance g_m^* of the cascode stage is a real value. Because of the magnetic coupling, the voltage drop on L_1 is increased by the factor $\omega M g_m^* r_\pi I_1$, where ω is the operating frequency, M is the mutual inductance between L_1 and L_2 and r_π is the base-to-emitter differential resistance of Q_1. In this case the value of the equivalent inductance seen at the terminals 1-1' would be increased

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by a factor $Mg_m^* r_\pi$. More in general the input impedance seen at terminals 1-1' (Z_V) is expressed by the following formula:

$$Z_V = [R_1 + r_\pi - \omega \cdot M \cdot g_m^* \cdot r_\pi \cdot \sin\varphi] + j\omega \cdot [L_1 + M \cdot g_m^* \cdot r_\pi \cdot \cos\varphi] \quad (1)$$

where R_1 is the parasitic series resistance of L_1 and φ is the angle between I_1 and I_2. This way the equivalent inductance value is increased by a factor $Mg_m^* r_\pi \cos\varphi$, whereas the real part is decreased by $\omega M g_m^* r_\pi \sin\varphi - r_\pi$. By changing φ, which depends on the intrinsic capacitances of Q_1 and Q_2, different values of the effective inductance can be obtained. This task can be accomplished by changing the bias current of Q_1 and the base voltage of Q_2 [1].

In Fig. 2 the performances of actual integrated inductors in Si-Ge technology [7], in terms of Q and L, are compared with the typical performance which has been obtained by using the new circuit block depicted in Fig. 1, which has been called "boot-strapped" inductor.

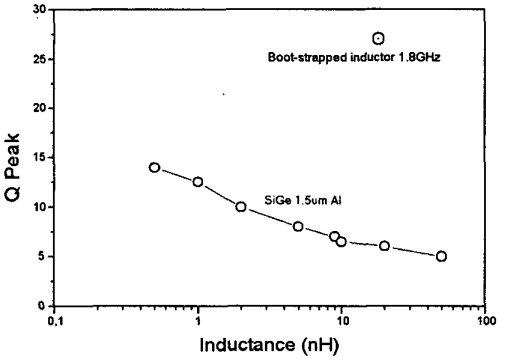

Fig. 2: Q versus L for SiGe spiral inductors [7]. Circle with dot represents a typical result obtained by using the boot-strapped inductor described in this paper.

III. TUNED LNA

The LNA is the most critical stage as far as the overall Noise Figure (NF) of the receiver is concerned. NF values as low as *2* dB are sometimes required in modern wireless terminals. In supereterodyne architecture, which is, at present, the most widely adopted for this type of application, the LNA should perform also another task: it should introduce a sufficiently large attenuation of the image frequency. Indeed, presently realizable image rejection mixer are unable to obtain an image frequency rejection larger than *40* dB, whereas some applications, for instance GSM standard, require overall attenuation as high as *70* dB. To this end tuned amplifiers using high Q monolithic external filters (ceramic or surface acoustic wave types) are required. The drawback of this solution consists of the need of supplemental pins and external components which are more costly and introduce noise and attenuation also in the pass band. The realization of entirely integrated tuned amplifiers, in the GHz range, represents a very stimulating target for RF IC designers. Several solutions have been proposed in literature using active inductors, realized by means of a gyrator [8, 9] or by shunting passive spiral inductors with an active bipole presenting a negative resistance [10]. In all of these cases, the operating frequency is lower or equal to *1* GHz and the dissipated power and/or the noise figure are quite high. Moreover the possibility of compensating for the effect of the silicon process tolerances and of the temperature variations has not been demonstrated. A comparison between their performances and those obtained by using boot-strapped inductors is presented at the end of Section IV.

The circuit scheme of a tuned LNA using this new type of active inductor is depicted in Fig. 3. It is based on a transconductance stage to drive the current into a shunt LRC resonant filter, where R and ωL are the real and the imaginary part of Z_V respectively, which is realized following the boot-strapped inductor approach described in Section II.

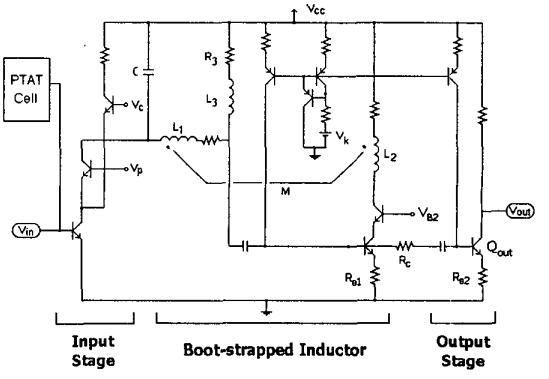

Fig. 3: Schematic of the selective LNA.

The input stage sets the noise figure of the amplifier, while the effective inductance value and the quality factor Q of the boot-strapped inductor, can be controlled by means of V_K and V_{B2}. The variable component of the current through L_1 has a maximum at the frequency f_0 at which the LRC filter resonates. The output stage is a

current mirror which transfers this current, multiplied by the current gain of Q_{OUT}, to the external load. A PTAT (Proportional To Absolute Temperature) cell to bias the input stage is used in order to counteract temperature variations effects on LNA voltage gain (A_v). As it will be detailed in Section IV, the voltage Vc, driven by a signal proportional to the LNA output power level could be used to expand the LNA input dynamic range.

The amplifier is designed on ST's HSB2 bipolar process (a *0.4* μm emitter width trench oxide isolated bipolar process with three layers of metal and *20* GHz bjt's cut off frequency). The integrated transformer is made up by two identical coupled inductors, the first one in metal 3, the second one in metal 2: square shaped, *225* μm per side, three turns each, metal track *10* μm wide, *10* μm spacing between adjacent metal tracks. The inductor L_3 is also square shaped, *120* μm per side, *2* turns in metal 3 (*10* μm wide with *8* μm spacing) in series with *3* turns in metal 2 (*8* μm wide with *8* μm spacing). A thick grid of trenches underneath the inductors has been used to reduce the induced currents in the substrate, so allowing a higher value of the Q-factor. The layout of the complete LNA is shown in Fig. 4 (where trenches underneath inductors were removed for a sake of clarity): the overall chip size is *0.52* mm^2 and it is mainly due to the distance (nearly *400* μm) between the transformer and the passive inductor, needed to achieve a sufficient magnetic de-coupling between the two structures [11].

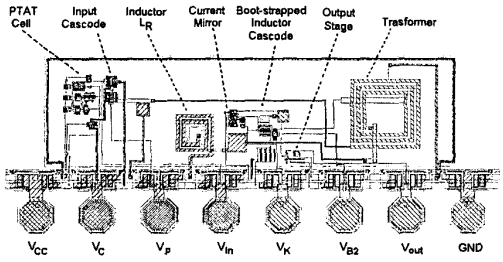

Fig. 4: Layout of the LNA.

IV. Simulation and Results

The design of the amplifier has been preceded by an accurate electromagnetic simulation of the transformer and the passive inductor, as described in [12]. Then the extracted Z parameters of the equivalent circuit of the transformer were input to the Mentor Graphics ELDO™ simulator to obtain the frequency response of the overall circuit. The transducer power gain (G_T), defined as the ratio between the power supplied to the load and the available power at the input, is depicted in Fig. 5 versus frequency. These data are based on post-layout simulations for the case of minimum NF matching. It reaches a peak value of *25.5* dB at *1.8* GHz for a band-width of *60* MHz, which results in a quality factor of *30*. This corresponds to an image-reject filtering of *18.8* dB and *25* dB for a *100* MHz and *200* MHz intermediate frequency respectively.

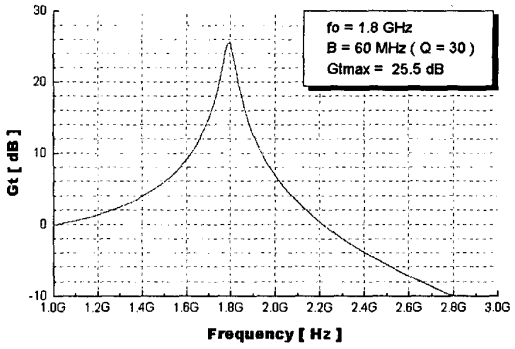

Fig. 5: LNA transducer gain based on post-layout simulations.

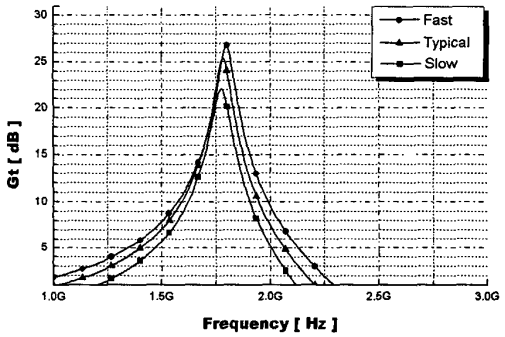

Fig. 6: LNA transducer gain variation due to silicon process tolerances based on post-layout simulations (slow, typical and fast process models).

One of the limiting factor in the utilization of highly selective integrated circuit is the reproducibility of the results which is affected mainly by the spreading of the parameters of the active devices. To this end the effect of the process tolerances have been simulated by using typical, as well as slow and fast models for bipolar transistors. In Fig. 6 it is shown as this effect can be quite completely compensated by using the two control voltages V_{B2} and V_K. Particularly, the variation of the resonance frequency and of the bandwidth can be kept below *0.3*% and *5*% respectively, by acting on V_{B2} and V_K and below below *0.8*% and *5*% by using only V_K.

By using the PTAT cell of Fig. 3, which determines a negligible silicon area increase, the LNA voltage gain due to temperature variations in the range [0°C-80°C] is kept below *6.5%*.

The amplifier results unconditionally stable at least up to *5* GHz (the upper limit used for circuit analysis). The minimum NF of the LNA, obtained through proper impedance matching with the input signal source, is *1.8* dB and it is mainly due to the input stage according to the Friis formula.

Another very critical characteristic for wireless applications is the dynamic range, namely the *1* dB compression point (CP_{1dB}). The proposed circuit is characterized by a CP_{1dB} of *–50* dBm. By varying the control voltage V_C, in the range [*2.6* V – *2.9* V], it is possible to increase the input dynamic range up to *-20* dBm without any modification of the resonance frequency and of the bandwidth but at the expenses of a voltage gain reduction.

Finally in Table 1 a comparison among the main characteristics of silicon integrated tuned LNA presented in literature and the solution described in this paper is shown. To be noted that none of these circuits have been optimized for an operating frequency higher than *1* GHz. The ones with similar and/or higher selectivity than ours exhibit a NF from *2.5* to *4.2* dB higher and a power consumption greater than almost *3* to *4* times. Moreover, the proposed amplifier outperforms the others in terms of voltage gain.

TABLE I
PROPOSED LNAS COMPARISON

	Technol.	A_V [dB]	NF [dB]	f_0 [GHz]	P_d [mW]	Q
[8]	CMOS	17	6	0.9	78	30
[9]	BiCMOS	18	4.3	1	57	56
[10]	CMOS	20	3.6	1	14	5
OUR	BJT	22.5	1.8	1.8	20.7	30

V. CONCLUSION

The design and post layout simulation results of a tuned LNA have been presented. By using a new type of active inductor a Q value of *30* at *1.8* GHz has been obtained, while keeping the NF very close to its minimum value compatible with the used technology. The robustness of the design versus temperature variations and silicon process tolerances have been demonstrated. The integration of such an LNA with a novel image rejection mixer [13] is currently pursued targeting to an integrated RF front-end capable of attenuating by *70* dB the image frequency without external components.

ACKNOWLEDGEMENT

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