1 V and 10 V SNS Programmable Voltage Standards for 70 GHz

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***Abstract*—Programmable Josephson voltage standards (PJVSs) in combination with fast switchable DC current sources have opened up new applications in the field of low-frequency AC metrology. The growing interest in output voltages of up to ± 10 V initiated efforts by several National Metrological Institutes to realize 10 V PJVSs. Presently, only 10 V PJVSs from PTB based on SINIS junctions have been successfully incorporated into existing setups for AC metrology. However, the fabrication of 10 V SINIS arrays that are driven at 70 GHz suffers from very low yield. The recent technological progress made at NIST enabled the drop-in replacement of the low-yield SINIS arrays by more robust SNS arrays. The N-material is an amorphous $\mathrm{Nb_xSi_{1-x}}$ alloy near the metal-insulator transition and is deposited by co-sputtering. For the first time, fully operational 1 V and 10 V PJVSs with SNS junctions that are suitable for a 70 GHz drive have been fabricated and tested. This work was done in close cooperation between NIST and PTB.**

***Index Terms*—AC Josephson voltage standard, Josephson arrays, programmable Josephson voltage standard, SINIS junction, SNS junction.**

I. Introduction

THE STATE of the art in AC voltage metrology is based on two fundamental achievements of recent Josephson technology: the Programmable Josephson Voltage Standard (PJVS) [1] operated by sinusoidal microwaves and the Josephson Arbitrary Waveform Synthesizer (JAWS) [2], which is driven by ultra-short current pulses. According to the fundamental equation for Josephson voltage metrology,

$$U(t) = nM(t)f/K_{\mathrm{J-90}}, \tag{1}$$

the PJVS systems exploit this equation by rapidly programming the voltage $U(t)$ by changing the junction number M by biasing different sub-arrays with different numbers of junctions. $K_{\mathrm{J-90}}$ is the Josephson constant ($K_{\mathrm{J-90}} = 483\,597.9\ \mathrm{GHz/V}$), n denotes the order of Shapiro steps (typically using the three voltage states $n = 0$, and ± 1) and f the microwave frequency. Despite the use of fast switchable DC bias sources, the unavoidable transients during the change of voltage states restrict the possible applications of the PJVS to DC and low frequencies, less than 1 kHz. However, in contrast to pulse-driven arrays (JAWS), which allow synthesis of fundamentally accurate AC voltages, only the PJVS can be operated at higher voltages of up to 10 V with an acceptable technological effort. Such 10 V PJVS systems enable new applications in the field of low-frequency AC metrology, especially when the time-varying Josephson voltage is used as a reference to measure a waveform differentially [3]. In this paper, we focus on the use of a junction-barrier material near the metal-insulator transition that could help to overcome fabrication yield limitations for PJVS circuits fabricated by the SINIS junction technology at PTB ($\mathrm{S} = \mathrm{superconductor}$, $\mathrm{I} = \mathrm{insulator}$, $\mathrm{N} = \mathrm{normal\ metal}$). We describe how two National Metrology Institutes, NIST in the U.S.A. and PTB in Germany, cooperate to realize the first 1 V and 10 V PJVS with a $\mathrm{Nb_xSi_{1-x}}$ barrier that can be driven at 70 GHz.

II. Requirements on Josephson Junctions Suitable for PJVS Arrays

In order to generate stable and rapidly programmable DC voltages, Hamilton *et al.* proposed and developed the first PJVS [1]: an array subdivided into smaller array segments following a binary (or later ternary) sequence for the number of junctions. This array sequence allows, in combination with individual and fast switchable DC bias sources, the rapid generation of quantized voltages. The combined total step number nM for the whole array can thus be set to any integer value between $-M$ and $+M$. Fast changes in the output voltage are possible only if there are single-valued Shapiro steps in the current-voltage characteristic (IVC) under microwave irradiation. This condition requires the use of overdamped Josephson junctions that display an IVC with negligible hysteresis.

For their first approach, Hamilton and co-workers used externally shunted SIS junctions based on the reliable Nb-Al technology at NIST. However, due to the external shunt resistance and its large parasitic inductance (which creates microwave-design problems and additional fabrication difficulties), the implementation of SIS junctions in a PJVS was abandoned shortly afterwards. Some years later, Seppä *et al.* from VTT, Finland, took up the original idea and developed a 1 V PJVS with externally shunted SIS junctions driven with microwaves at around 75 GHz [4]. The small current margins obtained ($\approx 150\ \mu\mathrm{A}$), made AC applications difficult. All of these disadvantages can be avoided by the use of internally shunted Josephson junctions such as SINIS or SNS.

When NIST first implemented SNS junctions [5], the low resistivity of the junction barrier required a "low" frequency drive

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around 15 GHz. At that time, the commonly used and technologically available barrier materials for SNS junctions such as AuPd, TiHf or later on TiN_x resulted in I_cR_n products (I_c: critical current, R_n: normal resistance) of typically 10 μV to 40 μV when deposited to reasonable thicknesses to make micrometer-sized junctions with practical current densities. NIST and AIST succeeded in the fabrication of such programmable circuits [6], [7], but the large number of junctions operating at 16 GHz required to reach 10 V remains a challenge for this junction technology. In spite of all the technological problems, the junction uniformity demonstrated by the planar SNS fabrication process was the motivation to start the present collaboration on SNS junctions and circuits designed to operate at 70 GHz that would require considerably fewer junctions.

PTB followed an alternative route and explored SINIS junctions for PJVSs [8]. These junctions use the same 70 GHz microwave drive that is the typical bias frequency for conventional SIS Josephson voltage standards (JVSs), which are commonly used by the voltage-metrology community. This is possible because the I_cR_n product of this junction type with double insulating barriers can easily be tuned over a large frequency range. Therefore the necessary number of junctions is 4 to 5 times fewer than in a PJVS driven at 15 GHz, and the entire microwave distribution network can be fabricated on-chip. Moreover, except for some minor modifications, the array fabrication is based on the reliable Nb-Al standard technology for conventional JVSs [9].

Today, SINIS 1 V PJVSs displaying current margins larger than 1 mA, a value that provides enough noise immunity for AC applications, are fabricated routinely at PTB with an acceptable yield of about 30%. Programmable 10 V SINIS junction arrays with 69 632 Josephson junctions divided into 22 segments (16 bits) and current margins larger than 600 μA have also been produced in small numbers [10] and their suitability for numerous metrological AC applications has been proven [11]–[13]. Unfortunately, the fabrication yield of these 10 V PJVSs is quite low (about 5%). However, the demand for such systems is continuously increasing. For that reason, PTB is seeking new materials and evaluating their suitability for a programmable SNS version that would enable higher fabrication yield and that can be used as a drop-in replacement for existing 70 GHz SIS or SINIS systems.

III. Comparison of SINIS and SNS Arrays and Their Impact on Technology and Design

A. Fundamental Junction Properties

Both SNS and SINIS Josephson junctions belong to a class of weak links that are dominated by the proximity effect [14]. The main difference is that SINIS junctions have well-defined (engineered) interfaces between the superconducting electrodes and the sandwiched normal metal N. These well-defined interfaces are extremely thin (1 nm to 2 nm thick) AlO_x barriers. Fortunately, the necessary increase of the transparency of these barriers, up to a level dominated by pinholes, does not lead to a large spread of electrical parameters due to the averaging of the pinhole contributions from the two interfaces [14]. Nevertheless, achieving practical run-to-run reproducibility is a challenging task because the required oxygen exposure, product of pressure and oxidation time, is extremely low (less than 25 $\mathrm{Pa \cdot s}$). The main problem in the fabrication of SINIS arrays at PTB seems to be plasma-induced damage during wafer processing. We believe that locally enhanced voltages during the plasma processes create large pinholes (larger than the coherence length!) that result in additional current contributions. Similar effects have also been found for SIS junctions with high current densities [15]. This kind of damage is visible by singular increased critical currents, observed for about 0.01% of the junctions in an array. Depending on their exact I_c, the effected junctions remain either superconductive; i.e., they provide no contribution to the step voltage ("missing junctions") or they contribute in a way that the step is no longer usable (too small or sloped). Among all possible failure sources in the very complex SINIS fabrication process, the excessive critical currents are the main reason for the low yield of 10 V PJVSs.

The technology for classical SNS junctions is much simpler and more robust, because only the thickness of a given N-layer determines both I_cR_n and the current density j_c under the condition of clean interfaces and negligible interdiffusion. Until recently, most applications had to take into consideration a low I_cR_n (10 μV to 40 μV) and at the same time a large j_c (80 $\mathrm{kA/cm^2}$ to 200 $\mathrm{kA/cm^2}$) [5], [6]. Recent progress made in junction technology based on N-materials near the metal-insulator (M-I) transition paved the way to "high"-frequency applications above 70 GHz [16], [17]. Today, NIST is able to fabricate Nb junctions with amorphous Nb_xSi_{1-x}-barriers that can be tuned by changing the Nb content of the barrier from nearly SIS (small x) to SNS behavior ($x > 0.12$) [18]. For the first time, programmable voltage standards able to operate either at "low" or "high" frequencies and fabricated by practically the same technology but with differently tuned barriers are a realistic goal.

B. Junction and Circuit Design for 70 GHz

Our first approach assumes nearly identical microwave designs for SNS and SINIS circuits, except for the junction area ($l \cdot w$) and the stripline impedance Z_0. Details have been described elsewhere and are summarized in Table I [10]. Similarly, the design of a single SNS junction ($N = Nb_xSi_{1-x}$) embedded in a stripline follows the principles valid for SINIS junctions. That means, in terms of the RSJ model, according to Kautz [19]:

- Negligible hysteresis, i.e., $\beta_c = I_c/I_R \approx 1$ (McCumber parameter, $I_R = \mathrm{switching - back\ current\ of\ the\ IVC}$).
- A normalized frequency $\Omega = f/f_c \approx 1$, with $f_c = hf/(2eI_cR_n)$, delivering an optimum $I_cR_n = 145\ \mu$V.
- A critical current $I_c \leq 3$ mA to limit the RF power per stripline: $P_{rf} = Z_0I_{rf}^2/2$, to ≈0.3 mW ($I_{rf} \approx 2I_c$: RF current amplitude and $Z_0 = 16\ \Omega$). Under similar conditions, both 1 V (64 parallel microwave stripline branches) and 10 V (128 branches) SINIS circuits ($Z_0 = 12\ \Omega$ can be driven by Gunn diodes with a maximum output power of 100 mW.
- Preliminary investigations at NIST on junctions with high-resistivity Nb_xSi_{1-x}-barriers delivered a current density of $j_c \approx 2000\ \mathrm{A/cm^2}$ for the targeted $I_cR_n = 150\ \mu$V. With this value, the dimensions of a single junctions were fixed to $l = 6\ \mu$m (length) and $w = 20\ \mu$m (width). Both are less

TABLE I
DESIGN PARAMETERS FOR BINARY DIVIDED SINIS AND SNS CIRCUITS

Parameter	Circuit	SINIS	SNS (N=Nb_xSi_{1-x})
Number of junctions	1 V	8 192	8 192
	10 V	69 632	69 632
Striplines connected in parallel	1 V	64	64
	10 V	128	128
Number of junctions per stripline	1 V	128	128
	10 V	136--562	136—582*
Stripline impedance [Ω]		12	16
Junction length [μm]		12	6
Junction width [μm]		30	20
Current density [A/cm^2]		750	2500
Critical current [mA]		3.5	3
Normal resistance [mΩ]		41	48

*in contrast to SINIS, the number of junctions in some striplines is slightly different.

than 4 times the Josephson penetration depth $\lambda_J = 8.2\,\mu m$, so that we can assume a nearly homogeneous current distribution, i.e., $I_c = j_c l w$ [20].

The maximum number of SNS junctions (Table I) that can be embedded into one of the parallel-driven striplines, in order to maintain an approximately constant microwave current, is one of the most important design parameters for the microwave circuit. This number is determined by the microwave attenuation of the stripline and is due mainly to losses from the embedded junctions. The damping per junction α_J can be estimated for a passive stripline ($I_{dc} = 0$), according to Kautz [21], as

$$\alpha_J = 10 \log_{10} \left[1 - 3/(4\pi^2 f^2 R_n Z_0 C^2)\right]. \qquad (2)$$

With the above design parameters and an effective junction capacitance $C = 47$ pF deduced from $\beta_c = 1$, this formula delivers $\alpha_J = 0.04$ dB per junction. This value is comparable to the measured microwave damping of SINIS arrays and would never allow the integration of a large number of junctions in a single stripline [22]. However from our earlier investigations with SINIS arrays, it is known that in active striplines ($I_{dc} > I_c$) self-oscillation coupling effects between the junctions partly compensate the increased attenuation [22]. This effect is well described by a virtual model for our SINIS circuits by Kim *et al.* [23].

Nevertheless, for our PJVS designs, we had to take into consideration that all unbiased array segments can present a non-negligible microwave attenuation. For that reason, the first stripline (on one side of the circuit) has all the smallest array sections (bits: 0–6) and is the most critical in regard to microwave attenuation. Thus, the segments with 64 junctions for the 1 V circuit (or with 68 junctions for the 10 V circuit) combined with the "largest" array striplines (128 or 582 JJs), which are always biased collectively, determine the attainable current margins of the microwave-induced steps. The number of striplines connected in parallel, 64 for the 1 V design (8 192 total JJs) and 128 for the 10 V design (69 632 total JJs) is a compromise between tolerable damping (including self-excitation) and available microwave power (less than 50 mW at antenna) at 70 GHz. The distribution of all junctions over the striplines is determined by an exact (1 V) or an approximated (10 V) binary sequence for the number of junctions in the array segments.

Besides the primary design goal of maintaining nearly the same microwave power for all junctions, the circuit area containing all junctions should be concentrated as much as possible, to minimize the parameter spread. For that reason, DC connections to the array segments have been restricted to the ends of the striplines and to one of the two outermost striplines. All these practical considerations and a number of experimental investigations on test arrays resulted in a "homogenous" 1 V design with 128 junctions in each stripline and an "inhomogenous" 10 V design. The 69 632 junctions are subdivided into 22 segments with different numbers of junctions per stripline: 4 striplines with 136 JJs, 2 striplines with 272 JJs, and 122 striplines with junction numbers between 544 and 582. All striplines are extended beyond the array length with superconducting wires in order to reach the microwave termination and to match all the lengths.

IV. FABRICATION PROCESS

A. Trilayer Deposition at NIST

Trilayer films are grown on SEMI standard 76.2 mm Si wafers with 150 nm of dry thermal oxide to passivate the bare wafer. The wafer is loaded into a load-locked vacuum chamber where an initial rf plasma is used to clean the surface of contamination. An initial layer of 245 nm of Nb is grown as a base electrode, followed by an additional rf plasma to enhance the planarity of the base electrode. After waiting 3 min for the wafer and guns to reach thermal equilibrium, the Nb-Si is co-sputtered from the Nb sputter gun (under the same conditions as the electrode Nb) and a p-doped Si sputter target. Finally, the Nb top-electrode of 200 nm thickness is deposited.

Because the exact Nb content in a film is not measured, the best characterization of the Nb content is the power from the Nb sputter gun, assuming a fixed power on the Si sputter gun. For the trilayers in this study, a power of 17 W was used on the Nb gun and 200 W on the Si gun giving a Nb content of ~8%. As the sputter targets age, this composition slightly changes. The same process may be used to fabricate stacks of junctions by inserting a middle Nb electrode and additional Nb_xSi_{1-x} layer before the top-electrode growth.

B. Trilayer Patterning at PTB

In contrast to SINIS arrays [9], SNS circuits were fabricated with a conventional self-aligning process that is very similar to the fundamental SNEP process first developed by Gurvich *et al.* [24]. The main difference is the amorphous Nb_xSi_{1-x} barrier instead of AlO_x. With the exception of the groundplane and the load resistor, all metallic and insulating layers were patterned using e-beam lithography.

The trilayer patterning starts with the junction definition (Fig. 1). This is done by ICP (Inductive Coupled Plasma) etching of the Nb top electrode (200 nm thick) and the NbSi barrier (10 nm) with a mixture of SF_6 and C_4F_8. As there is no natural etch-stop, a laser endpoint-detection system indicates

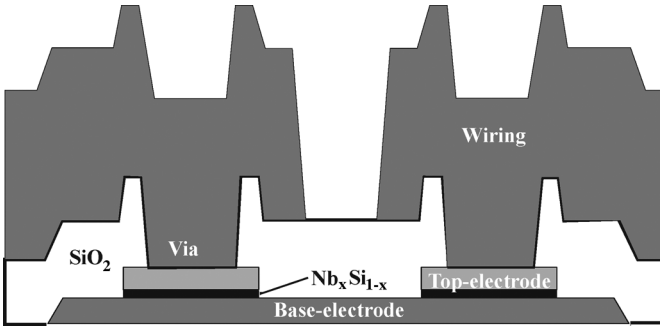

Fig. 1. Cross-section of all layers of the DC circuit.

when the interfaces between the NbSi-barrier and the Nb of the top and bottom electrode are successively cleared. In a second fabrication step, the base electrodes ($\sim$ bottom Nb, 245 nm thick) are reactively ion-etched (RIE-parallel plate reactor) with CF_4 and O_2. To insulate the base electrodes from the wiring, SiO_2 is deposited to a thickness of 350 nm using a PECVD (Plasma Enhanced Chemical Vapor Deposition) system with an ICP-source. Rectangular shaped vias (3 μm by 17 μm) to the top electrodes are etched through the oxide by ICP-etching with CHF_3 and O_2. Prior to the deposition of the 500 nm thick Nb wiring, an in-situ cleaning process by rf etching enables superconducting contact ($I_{max} > 70$ mA) between the top electrode and the wiring. The patterning process of the wiring level by RIE etching in $CF_4 + O_2$ completes the DC circuit. Fig. 1 shows a cross-sectional view of all layers in the DC circuit. The microwave circuit is completed with a 1.5 μm thick PECVD SiO_2 insulating layer, a superconducting ground-plane (250 nm Nb) and a load-resistance built by a normal metal plane from AuPd (200 nm thick). The microwave layers on top of the DC circuit are patterned by optical-contact lithography. In the final fabrication step, the thick SiO_2 covering the DC pads, is removed by wet etching.

V. Experimental Results and Discussion

During a first stage of the PTB—NIST collaboration, the focus was on the development of a reliable fabrication process and on relevant electrical properties, such as the parameter-spread of the SNS junction arrays with NbSi-barriers tuned for 70 GHz. In the initial search for the right deposition recipe, 5 trilayer wafers with slightly varied barriers were deposited as described above and patterned into 1 V circuits. Only one of these (trilayer #1 in Table II) was close to the targeted electrical parameters. The other processed wafers had values for I_c and I_cR_n that were too large and showed various chaotic behaviors under microwave irradiation. Most of the 21 circuits were evaluated from the wafer with trilayer #1. From these measurements we could deduce a spread for I_c and I_cR_n across the wafer of $\pm 25\%$ and $\pm 12\%$, respectively. The evaluation of the other wafers has not been completed.

Fig. 2 presents a typical IVC of a 1 V circuit from trilayer #1 without (a) and with (b) microwave bias. The first Shapiro step extends, as demonstrated by the inset picture, over a current range of approximately 1.4 mA, and the hysteresis does not influence the low-current edge of the step. It seems that the

TABLE II
Electrical Parameters of Trilayers Used for 1 V and 10 V PJVSs

trilayer #	I_c^{av} (mA)	$I_cR_n^{av}$ (μV)
#1 (only 1V)	2.3	170
#2	0.75	200
#3	3	150
#4	2.5	125

I_c^{av}, $I_cR_n^{av}$: averaged values, R_n determined at $2I_c$. All trilayer barriers were nominally 11 nm thick. Trilayer #2 was grown with an aged Nb target, thus the Nb content is likely to be less than the nominal 8%.

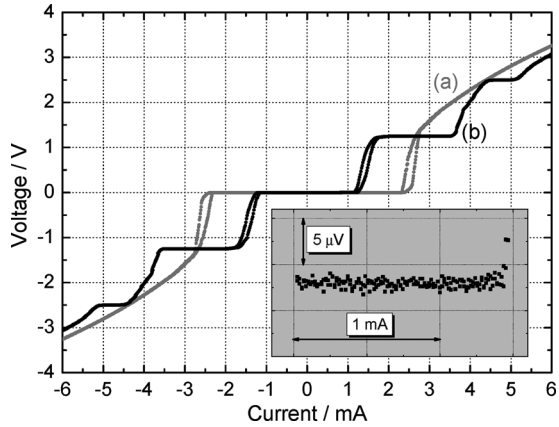

Fig. 2. IVC of a 1 V-PJVS with 8 192 SNS junctions, (a) without microwaves, (b) with microwaves at 73.668 GHz and 20 mW at antenna. The inset picture shows the first Shapiro step with high resolution. Junction parameters: $I_c = 2.35$ mA, $I_cR_n = 160\ \mu$V (at $2I_c$).

I_cR_n product of 160 μV, measured at $2I_c$ of the bending IVC, presents approximately a limit for non-hysteretic higher-order steps. Measurements on circuits from the same wafer demonstrated that a further increase of I_cR_n beyond this limit renders the constant-voltage steps increasingly hysteretic. The undesirable hysteretic parts at one or both ends of a step can be removed by applying a sufficiently large microwave power. However, in such cases the optimum operating condition for PJVSs of "equal step widths" [19] for the steps $n = 0$ and $n = \pm 1$ is no longer fulfilled. In order to demonstrate that the 1 V PJVS is fully operational, the IVCs under microwave irradiation of all array segments have been recorded. Fig. 3 shows that all current margins are approximately 1.4 mA. This value gives sufficient noise immunity for most AC applications. The equal step-width condition serves as a figure of merit for the microwave design and the junction uniformity. For the fabricated 1 V PJVSs with SNS junctions, we have measured a value of approximately 0.6 I_c. Equally good results have been obtained with SINIS circuits [10].

Encouraged by the good performance of the 1 V PJVSs, five more trilayers were grown and patterned into 10 V circuits using the design described previously. Due to a necessary optimization of some critical fabrication steps, including e-beam lithography, only the trilayers #2, #3 and #4 delivered 10 V circuits that could be evaluated. Despite the parameter spread evaluated previously for trilayer #1, and considering the "large" area covered by the junctions in the 10 V design (7.5 mm by 9

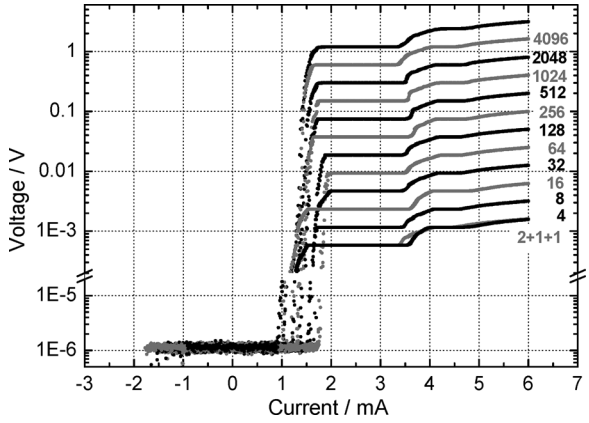

Fig. 3. IVC of a complete 1 V array and of all segments under microwave irradiation at 70.5 GHz and 15 mW at antenna. The number of junctions in each segment is indicated to the right of the corresponding curve and increases from bottom to top in a binary sequence.

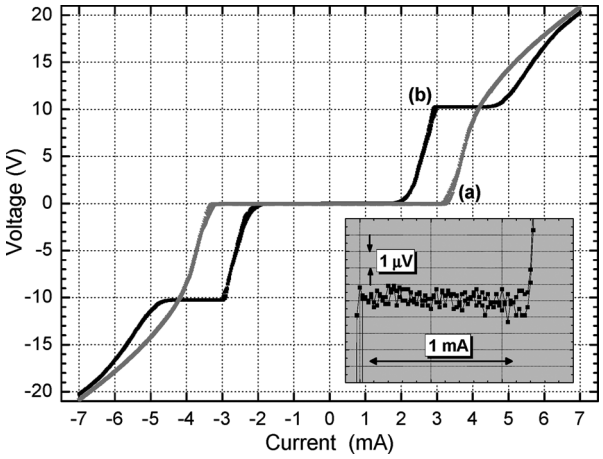

Fig. 4. IVC of a 10 V PJVS with 69 632 SNS junctions, (a) without microwaves, (b) with microwaves at 71.28 GHz and 50 mW at antenna. The inset shows the 10 V step with high resolution. Junction parameters: $I_c = 3.05\ \mathrm{mA}$, $I_c R_n = 150\ \mu\mathrm{V}$ (at $2I_c$).

mm), the measurements on 10 V arrays delivered surprisingly good results. In particular, the circuits patterned from trilayer #3, with values for I_c and $I_c R_n$ nearly equal to the design values, demonstrated excellent performance. The IVC with microwaves (shown in Fig. 4(b)) demonstrates current margins for the 10 V step of approximately 1.2 mA. Steps as large as 1.4 mA were obtained by optimizing the microwave signal. These current margins are nearly two times larger than those obtained for 10 V PJVSs with SINIS junctions. Moreover, a precision measurement of the step voltage (see inset of Fig. 4) reveals that all of the 69 632 junctions are phase-locked to the external microwave at 71.28 GHz. All 10 V SINIS arrays fabricated to date have had at least one "missing junction".

One of the fabricated 10 V SNS arrays (from trilayer #2) was used to perform a comparison with the 10 V SIS JVS of the PTB. This comparison showed good agreement at the 10 V level with a difference of $\Delta U_{\mathrm{SIS-SNS}} = 0.04\ \mathrm{nV} \pm 0.41\ \mathrm{nV}$ (type A uncertainty).

Other remarkable features of the IVC are the nonhysteretic IVC without microwaves (Fig. 4(a)) and the smooth (smeared)

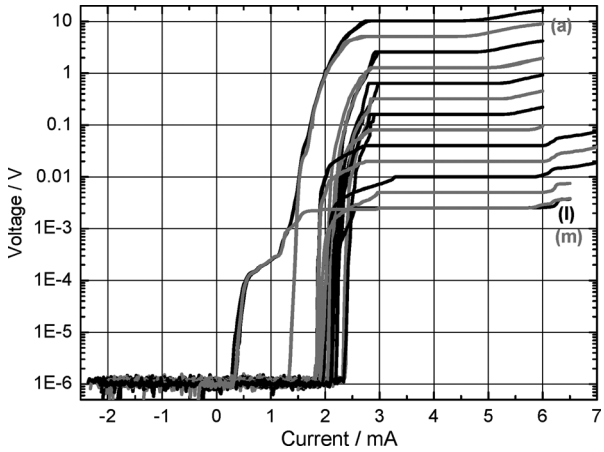

Fig. 5. IVC of a complete 10 V array and of different array segments under microwave irradiation at 71.28 GHz and 50 mW at antenna. For clarity, the smaller segments were grouped for curve (m) The number of Josephson junctions in each segment decreases alphabetically from top to bottom: (a) 34 816, (b) 17 408, (c) 8 704, (d) 4 352, (e) 2 176, (f) 1 088, (g) 544, (h) 272, (i) 136, (j) 68, (k) 34, (l) 17, and (m) $1+1+1+2+4+8=17$. The IVC for the complete array is dominated by (m) at low currents, then (a). The width of the step is limited by the overlap between (a) and (j).

transition at the ends of the microwave-induced $\mathrm{n} = 0$ step. The reason for the latter phenomenon is visible in Fig. 5, which shows the IVCs of the whole 10 V PJVS and of nearly all array segments of the 10 V PJVS under microwave irradiation. Clearly, the first 17 junctions, which are the sum of the smallest bits $(3 \times \mathrm{bit}\ 0 + \mathrm{bit}\ 1 + \mathrm{bit}\ 2 + \mathrm{bit}\ 3)$, display a step width for $n = 0$ of only 500 μA, whereas the "large" bits are close to the target-value of "equal step widths". We believe that the reason for this behavior, which was not observed on any SINIS circuits, is the special design situation of the outer stripline of the 10 V array with many narrowly spaced DC connections to the first array segments. These connections (without filters) can act as antennae for parasitic microwaves, so that the first junctions are overdriven and, due to the special Bessel-function behavior of the Shapiro steps [16], [17], rapidly reduces the step width for $\mathrm{n} = 0$. Nevertheless, the obtained step width of at least 0.4 I_c for the first Shapiro step in all segments is an excellent figure of merit for our 10 V design.

VI. Conclusion

The fabricated arrays with co-sputtered $\mathrm{Nb_xSi_{1-x}}$ barriers can be used as drop-in replacements for SINIS arrays in existing 1 V and 10 V PJVS systems operated at 70 GHz. 10 V SNS arrays show an improved performance as compared to 10 V SINIS arrays, having better yield and larger current widths of the steps. The SNS junction technology has better yield, most likely because plasma process-induced damage of the barrier is eliminated. Further improvements of the 10 V design should focus on the first stripline with the smallest bits in order to achieve nearly equal stepwidths for all array segments.

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