

## Josephson voltage standards

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## REVIEW ARTICLE

### Josephson voltage standards

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This paper reviews the development and use of Josephson voltage standards over the last 30 years, including classical dc standards, programmable standards based on binary weighted arrays, pulse-driven delta-sigma standards for ac wave-form synthesis, and single-flux-quantum voltage multipliers. [S0034-6748(00)00810-8]

#### I. INTRODUCTION

In 1962, Brian Josephson, a graduate student at Cambridge University, derived equations for the current and voltage across a junction consisting of a thin insulating barrier separating two superconductors.<sup>1</sup> His equations predicted that if a junction is driven at frequency  $f$ , then its current-voltage ( $I-V$ ) curve will develop regions of constant voltage at the values  $nhf/2e$ , where  $n$  is an integer and  $e/h$  is the ratio of the elementary charge  $e$  to the Planck constant  $h$ . This prediction was verified experimentally by Shapiro<sup>2</sup> in 1963 and has become known as the ac Josephson effect. It found immediate application in metrology because it relates the volt to the second through a proportionality involving only fundamental constants. Initially, this led to an improved value of the ratio  $h/e$ . Today, it is the basis for voltage standards around the world.

Before proceeding with a review of Josephson standards, it is useful to review the International System of units (abbreviated SI) and the definitions of electrical quantities in that system.<sup>3,4</sup> The SI was established by the 11th General Conference on Weights and Measures (CGPM) in 1960. A formal diplomatic organization, the CGPM is one of the international bodies created by the Treaty of the Meter in 1875. The SI meets the need for a world-wide set of units that is uniform and coherent. Of the seven base units in the SI, only the ampere relates to electrical measurements. The ampere is defined as

“that constant current which, if maintained in two parallel straight conductors of infinite length, of negligible circular cross section, and placed 1 meter apart in vacuum, would produce between these conductors a force equal to  $2 \times 10^{-7}$  newtons per meter of length.”

Coherency of electrical power (current times voltage) and mechanical power (force times distance divided by time) leads to the following definition for the volt:

“The volt is that electromotive force between two points on a conductor carrying a constant current of 1 ampere when the

power dissipated between the two points is 1 watt.”

The realization of the SI volt, therefore, depends on experiments that relate the ampere and the volt to mechanical units of length, force, and power. These experiments are extremely difficult and time consuming.<sup>5-8</sup> Note that the definition of the SI volt has nothing to do with the Josephson effect.

Modern instrumentation requires voltage measurements with a reproducibility that exceeds the uncertainty of the realization of the SI volt. To meet this need, metrologists have developed artifacts and experiments that generate voltages that are stable and reproducible to a level approaching 0.001 parts in  $10^6$  (ppm). These standards are said to *represent* the SI volt and serve as a kind of flywheel to remember the result of the SI volt realization. Before 1972, representations of the volt were made by assigning values to carefully stabilized banks of Weston cells.<sup>9</sup> Drift and transportability problems with Weston cells limited the uniformity of voltage standards around the world to about 1 ppm. This uniformity was greatly improved by the standards resulting from Josephson's discovery.

Josephson's equation for the supercurrent through a superconductive tunnel junction is given by

$$I = I_c \sin \left[ (4\pi e/h) \int V dt \right], \quad (1)$$

where  $I$  is the junction current,  $I_c$  is the critical current, and  $V$  is the junction voltage.  $I_c$  is a function of the junction geometry, the temperature, and any residual magnetic field inside the magnetic shields that are used with voltage standard devices. When a dc voltage is applied across the junction, Eq. (1) shows that the current will oscillate at a frequency  $f_J = 2eV/h$ , where  $2e/h \approx 484$  GHz/mV. The very high frequency and low level of this oscillation make it difficult to observe directly. However, if an ac current at frequency  $f$  is applied to the junction, the junction oscillation tends to phase lock to the applied frequency. Under this phase lock, the average voltage across the junction equals  $hf/2e$ . This effect, known as the ac Josephson effect, is observed as a constant voltage step at  $V = hf/2e$  in the voltage-current ( $I-V$ ) curve of the junction. It is also possible for the

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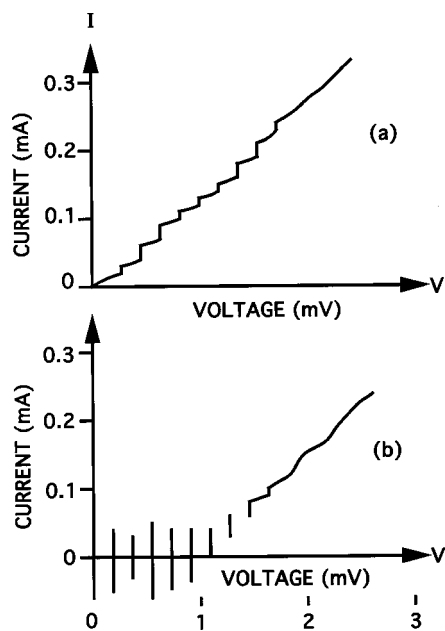


FIG. 1. Constant voltage steps in the  $I$ - $V$  curve of a junction driven with microwave radiation for (a) a low-capacitance junction and (b) a high-capacitance junction.

junction to phase lock to harmonics of  $f$ . This results in a series of steps at voltages  $V = nhf/2e$ , where  $n$  is an integer, as shown in Fig. 1(a).

The Josephson effect was initially used to improve the measurement of the constant  $2e/h$  based on voltage values derived from the SI volt realization as maintained by Weston cells. The uncertainty of these measurements was limited by the uncertainty of the SI volt realization and the stability of the Weston cells.<sup>10,11</sup> The stability of the Josephson volt depends only on the stability of  $f$  (which can easily be a part in  $10^{12}$ ), and is much better than the stability of Weston cells. Thus, in the early 1970s, many national standards laboratories adopted a value for the Josephson constant  $K_J = 2e/h$  and began using the ac Josephson effect as the practical standard of voltage.<sup>12,13</sup> Owing to small differences in existing national standards, different values of  $K_J$  were adopted by various countries. This inconsistency was corrected in 1990 when, by international agreement, the constant  $K_{J-90}$  was assigned the value 483 597.9 GHz/V and adopted by all standards laboratories.<sup>8</sup> The assigned value is based on a weighted average of volt realization measurements made prior to 1990 at many national measurement institutions. The uncertainty in  $K_{J-90}$  is 0.4 ppm. Standards such as the Josephson volt that depend on fundamental constants rather than physical artifacts are known as intrinsic standards. Although the Josephson voltage standard (JVS) does not realize the SI definition of the volt, it provides a very stable reference voltage that can be reproduced anywhere without the need to transfer artifacts such as Weston cells.

The accuracy of the Josephson voltage-frequency relation  $V = nf/K_J$ , and its independence from experimental conditions, such as bias current, temperature, and junction materials, have been subjected to many tests.<sup>11,14-22</sup> No significant deviation from this relation has ever been found. In the most precise of these experiments, two Josephson de-

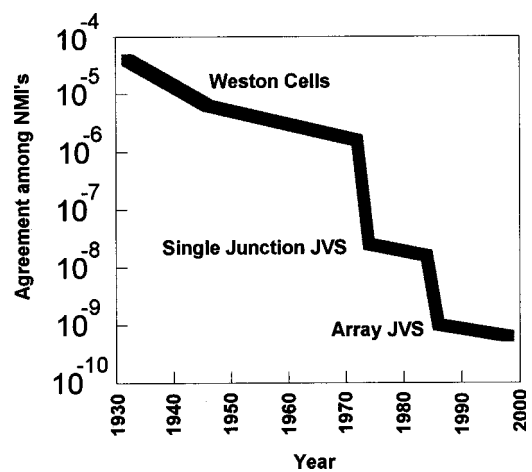


FIG. 2. Approximate level of agreement in dc voltage measurements among standards laboratories through the years 1930–2000.

vices are driven by the same frequency source, biased on the same step, and connected in series opposition across a small inductor. Since the loop is entirely superconductive, any voltage difference leads to a changing magnetic field in the inductor. This field is detected with a superconducting quantum interference device (SQUID) magnetometer and its constancy has set an upper limit on the voltage difference of less than 3 parts in  $10^{19}$ .<sup>23,24</sup>

Figure 2 is a semilog plot that illustrates how typical differences in dc voltage measurements among National Measurement Institutes (NMIs) have decreased over the last 70 years.<sup>25-31</sup> The two major improvements coincide with the introduction of single-junction Josephson standards in the early 1970s and the introduction of series-array Josephson standards beginning in 1984.

Although the ac Josephson effect provides a much more stable voltage reference than Weston cells, the first single-junction Josephson standards<sup>25,26,32-38</sup> were difficult to use because they generated very small voltages (1–10 mV). Several attempts were made to raise the voltage by connecting two or more junctions in series. The most ambitious of these<sup>39</sup> used 20 junctions in series to realize a voltage of 100 mV with an uncertainty of a few parts in  $10^9$ . Ensuring that every junction was on a constant voltage step required 20 individually adjustable bias currents. The difficulty of this procedure makes arrays of more than 20 junctions impractical.

In 1977, Levinson *et al.*<sup>40</sup> made a suggestion that would ultimately lead to a solution to the multiple-bias problem. Levinson pointed out the importance of the parameter  $\beta_c = 4\pi e I_c R^2 C/h$  in determining the characteristics of rf-induced Josephson steps.  $\beta_c$  is a measure of the damping of Josephson oscillations by the junction shunting resistance  $R$ . In particular, he showed that junctions with a large capacitance  $C$  and a large  $R$  ( $\beta_c > 100$ ) could generate a  $I$ - $V$  curve with hysteretic constant-voltage steps like those shown in Fig. 1(b). These steps have become known as zero-crossing steps because they cross the zero-current axis of the  $I$ - $V$  curve. The lack of stable regions between the first few steps means that for small dc-bias currents, the junction voltage must be quantized. With a common bias current at or near

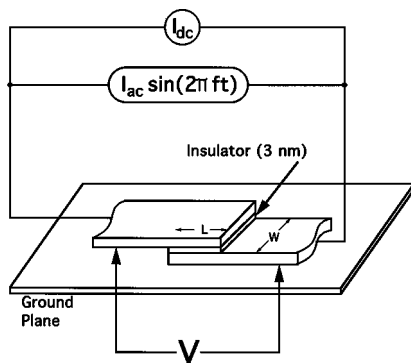


FIG. 3. Structure of a superconductor–insulator–superconductor Josephson junction typically used in dc voltage standards.

zero, the voltage across a large array of these junctions must also be quantized. The possibility of obtaining constant-voltage steps at zero current over a wide range of junction and operating parameters suggested the possibility of building a voltage standard using large arrays of junctions.

After several preliminary experiments,<sup>41–43</sup> a joint effort in 1984 between the National Bureau of Standards in the U.S. and the Physikalisch–Technische Bundes-Anstalt in Germany resolved the problems of junction stability and microwave distribution and created the first large Josephson array based on Levinson’s idea.<sup>44</sup> Further design improvements and system development produced the first practical 1 V Josephson standards in 1985.<sup>45,46</sup> Advances in superconductive integrated-circuit technology, largely driven by the quest for a Josephson junction computer,<sup>47</sup> soon made possible much larger arrays. In 1987, the design was extended to a chip with 14 484 junctions that generated about 150 000 quantized voltages spanning the range from ISO rule in this case is to have a unit for both numbers  $-10$  V to  $+10$  V.<sup>48</sup> Numerous further refinements were made as 10 V Josephson standards were implemented in many national standards laboratories.<sup>49–61</sup> By 1989, all of the hardware and software for a complete voltage metrology system were commercially available. Today, there are Josephson array voltage standards in more than 50 national, industrial, and military standards laboratories around the world. A program of international comparisons carried out by the Bureau International des Poids et Mesures (BIPM) has measured differences between a traveling Josephson standard and those of the NMI that are typically less than 1 part in  $10^9$ .<sup>27–30</sup>

While zero-crossing steps have been the enabling technology for present day Josephson voltage standards, they have important disadvantages because of the difficulty of selecting the value of the step number  $n$  and its susceptibility to spontaneous noise-induced transitions. In the following sections, we shall see that overcoming these disadvantages has been a major occupation of metrologists over the last 15 years. We focus on practical aspects of Josephson standards (see also Ref. 62) and new ideas for generating arbitrary wave forms with Josephson accuracy. For a more physics-oriented view of electrical metrology and Josephson standards, see reviews by Niemeyer<sup>31</sup> and Kautz.<sup>63</sup>

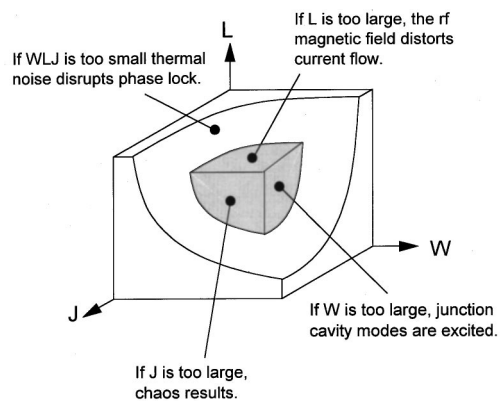


FIG. 4. Three-dimensional visualization of the region of stable voltage operation as a function of junction length  $L$ , width  $W$ , and critical-current density  $J$ .

## II. JOSEPHSON ARRAY VOLTAGE STANDARD TECHNOLOGY

### A. Junction design constraints

Figure 3 illustrates the basic structure of one junction in a large series array. The junction is an overlap between two superconductive thin films that are separated by a thin oxide barrier. The junction sits above a ground plane and is separated from it by a few micrometers of insulation. A dc current  $I_{dc}$  and a microwave current  $I_{ac}$  are driven through the junction. The design parameters for the junction are its length  $L$ , width  $W$ , critical current density  $J$  (critical current per unit area), and the microwave drive frequency  $f$ . The practical realization of an array voltage standard requires a thorough understanding of how these parameters affect the stability of the quantized voltage levels shown in Fig. 1(b). Stable operation requires that four conditions be satisfied: (1)  $L$  must be small enough that the flux induced through the junction area by the microwave magnetic field is much less than the flux quantum  $h/2e$ ; (2) both  $W$  and  $L$  must be small enough that the lowest resonant cavity mode of the junction is greater than  $f$ ; (3) to avoid chaotic behavior, the junction plasma frequency  $f_p$ , which is proportional to  $J^{0.5}$ , must be less than about one third  $f$ ; and (4) the junction’s critical current  $I_c = WLJ$  should be as large as possible to prevent noise-induced quantum step transitions. If any of these conditions is violated, the junction voltage is likely to switch randomly among several steps, making measurements impossible. A rigorous derivation of these conditions is the subject of several papers by Kautz.<sup>63–67</sup> Figure 4 illustrates the region of stable behavior in the three-dimensional space of  $L$ ,  $J$ , and  $W$ . The margin of stable operation, represented by the

TABLE I. Junction design parameters.

|                              |                                       |
|------------------------------|---------------------------------------|
| Junction materials           | Nb/Al <sub>2</sub> O <sub>3</sub> /Nb |
| Critical current density $J$ | 20 A/cm <sup>2</sup>                  |
| Junction length $L$          | 18 μm                                 |
| Junction width $W$           | 30 μm                                 |
| Critical current $I_0$       | 110 μA                                |
| Plasma frequency $f_p$       | 20 GHz                                |
| Lowest resonant cavity mode  | 175 GHz                               |
| Rf drive frequency $f$       | 75 GHz                                |

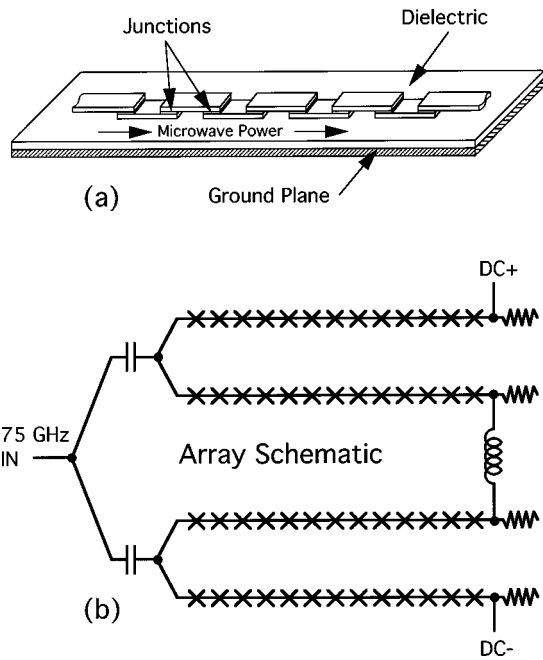


FIG. 5. (a) Series of Josephson junctions arranged to form a stripline and (b) the circuit of a typical Josephson voltage standard.

shaded volume in Fig. 4, increases with  $f$  and is ultimately set by a trade-off between stability and the economics of providing a very-high-frequency microwave source. While stable arrays have been demonstrated at frequencies as low as 24 GHz,<sup>68,69</sup> most practical standards operate in the range 70–96 GHz. Table I lists a typical set of junction parameters for a commonly used design.

**B. Array design**

The  $I-V$  curve shown in Fig. 1(b) shows steps covering the range from about  $-1$  to  $+1$  mV and is for a junction driven by a nearly optimum level of microwave current. At lower microwave current the steps cover a smaller range of voltage, and at higher microwave current the steps become smaller and begin to move off the zero-current axis. In a large array, every junction must generate a large zero-crossing step, and thus the microwave power must be adjusted to a value low enough to accommodate the one junction receiving the largest microwave drive. Thus, in order to

obtain the largest voltage from the smallest number of junctions, an array standard requires a circuit design that can deliver nearly uniform microwave power to many thousands of junctions, all of which are connected in series. The solution to this problem is a simple extension of Fig. 3 to a series of junctions in a line over a ground plane, as shown in Fig. 5(a). This results in a microwave stripline that can propagate microwave power with relatively low loss.<sup>44</sup> The capacitive impedance of the junctions is so small (approximately  $1\text{ m}\Omega$ ) relative to the stripline impedance (approximately  $3\ \Omega$ ) that each junction has a very minor effect on the propagation of microwave power in the stripline. Typically, each junction will absorb about 0.02%–0.04% of the power propagating through it. It is thus possible to connect several thousand junctions in series and still achieve a power uniformity of about  $\pm 1.5$  dB. With careful design, striplines with as many as 4800 junctions have been used.<sup>57</sup>

Because 10 V Josephson standards require about 20 000 junctions, it is necessary to adopt a series/parallel circuit similar to that shown in Fig. 5(b).<sup>46</sup> Here, a network of low- and high-pass filters allow the microwave power to be split into four parallel paths while maintaining a dc path in which all junctions are connected in series.

A typical integrated-circuit layout for an array of 20 208 junctions is shown in Fig. 6. The microwave-drive power is collected from a waveguide by a finline antenna, split 16 ways, and injected into 16 junction striplines of 1263 junctions each. The junction striplines are separated from a superconductive ground plane by about  $2\ \mu\text{m}$  of  $\text{SiO}_2$  dielectric. Symmetry in the splitting network ensures that the same power is delivered to each subarray. Several precautions are required to avoid reflections that would lead to standing waves and the consequent nonuniform power distribution within the subarrays: (1) Each stripline is terminated by a matched load that consists of several wavelengths of resistive stripline. The use of a resistive stripline rather than a discrete resistor guarantees a near-perfect match over a wide range of fabrication parameters.<sup>44</sup> (2) The dimensions of capacitors in the low- and high-pass filters are chosen to avoid resonances near the drive frequency. (3) The microwave bend radius has a minimum value of three times the stripline width.<sup>48</sup> Sharper bends result in unacceptable reflections. In order to meet the bend requirement while still packing the array strips close together, “curly” bends that turn  $215^\circ$  and

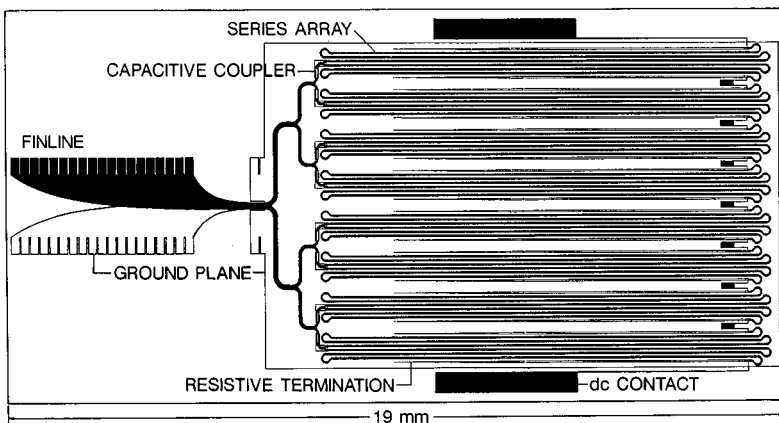


FIG. 6. Layout of a 20 208 junction, 10 V Josephson array voltage standard chip.

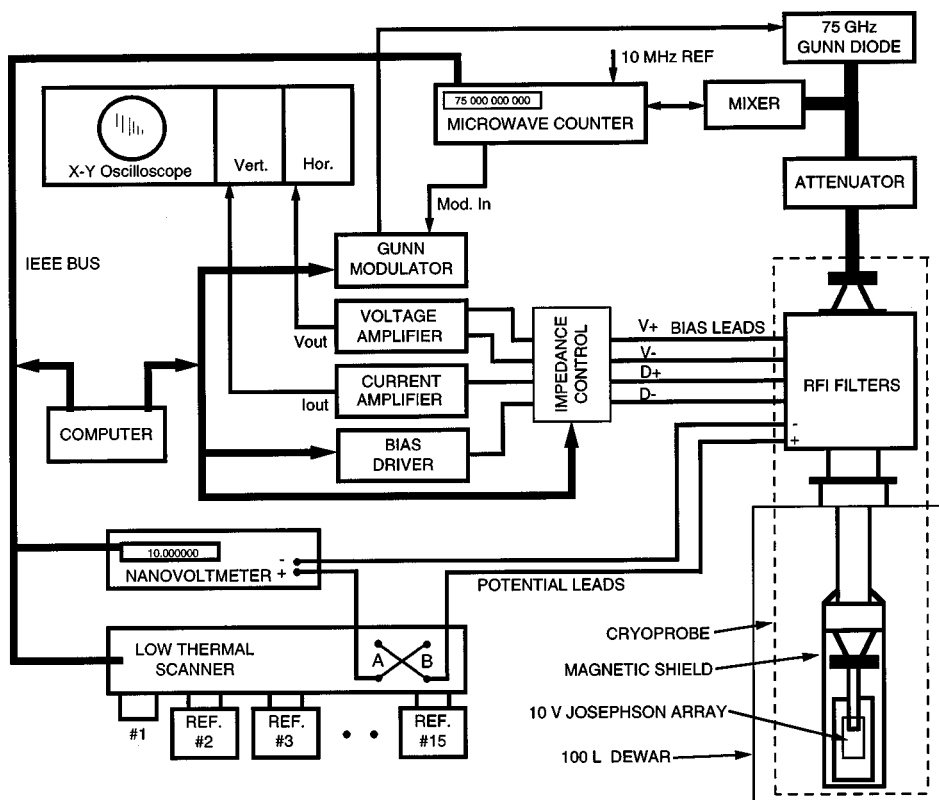


FIG. 7. Block diagram of a modern voltage standard system.

then back  $45^\circ$  are used. (4) The junction spacing along the line must be close enough to avoid a resonance between adjacent junctions.<sup>63</sup>

Microwave power is applied by inserting the finline end of the chip into a slot parallel to the  $E$  field in a WR-12 waveguide. A recent design uses a split finline that eliminates the need for one of the stripline splits.<sup>58</sup> The dc output appears across superconducting pads at the edge of the chip.

### C. Fabrication

Voltage standard chips are typically fabricated on silicon or glass substrates. The integrated circuit has eight levels: (1) a 300-nm-thick Nb ground plane, (2) a  $2\ \mu\text{m}$  layer of  $\text{SiO}_2$  that forms the microstripline dielectric, (3) a 200 nm Nb film that forms the lower electrode of the Josephson junctions, (4) a 3 nm metal oxide layer that forms the Josephson tunneling barrier, (5) a 100 nm Nb junction counterelectrode, (6) a 300 nm  $\text{SiO}_2$  film with windows for contacts to the counterelectrode, (7) a 400 nm film of Nb that connects the junction counterelectrodes, and (8) a 100 nm resistive film that forms the stripline terminations.

## III. MEASUREMENT SYSTEMS

A block diagram of a modern Josephson voltage standard system is shown in Fig. 7. The Josephson array chip is mounted inside a high-permeability magnetic shield at the end of a cryoprobe that makes the transition between a liquid-helium Dewar and the room-temperature environment. Three pairs of thermocouple-grade copper wires are connected to the array. One pair supplies bias current, a second monitors the array voltage with an oscilloscope, and the third pair delivers the array voltage to the calibration system. All

of the wires pass through multiple levels of radio frequency interference (RFI) filtering in a milled aluminum box at the top of the Dewar. The box, the filters, and the Dewar itself form a shield that protects the Josephson array from electromagnetic interference that could cause step transitions. Microwave power is delivered through a waveguide consisting of a 12-mm-diam tube with WR-12 launching horns on each end. Tubes of solid German silver<sup>70</sup> or stainless steel plated internally with silver<sup>60</sup> are commonly used. This waveguide simultaneously achieves low thermal loss ( $<0.5$  L liquid-He per day) and low microwave loss (as low as 0.7 dB at 75 GHz). A battery-operated liquid-helium-level sensor and readout may be built into the cryoprobe.

A phase-locked oscillator (PLO) operating at a frequency near 75 GHz provides the microwave power to the chip. The primary requirements for the source are: (1) its reference frequency must be known with high accuracy and (2) it should produce a stable output power of at least 50 mW. It is useful, although not essential, to be able to tune the source over a range of frequencies. The PLO may be constructed using a commercial microwave counter with feedback capability or it may be a custom-built phase-locked loop.<sup>59,71</sup> Figure 8(a) shows the block diagram of one example of a custom-built microwave system that is small enough to fit into the top of the cryoprobe.<sup>59</sup> The reference frequency for the PLO is typically obtained from a cesium clock or a global positioning system receiver. Its spectrum is narrowed with a crystal filter and then passed through two doublers to obtain a 40 MHz reference that is used to phase lock a dielectric resonant local oscillator (DRO) at 7.68 GHz. The tenth harmonic of the DRO is mixed with the output of a Gunn diode oscillating near 76.76 GHz to generate an in-

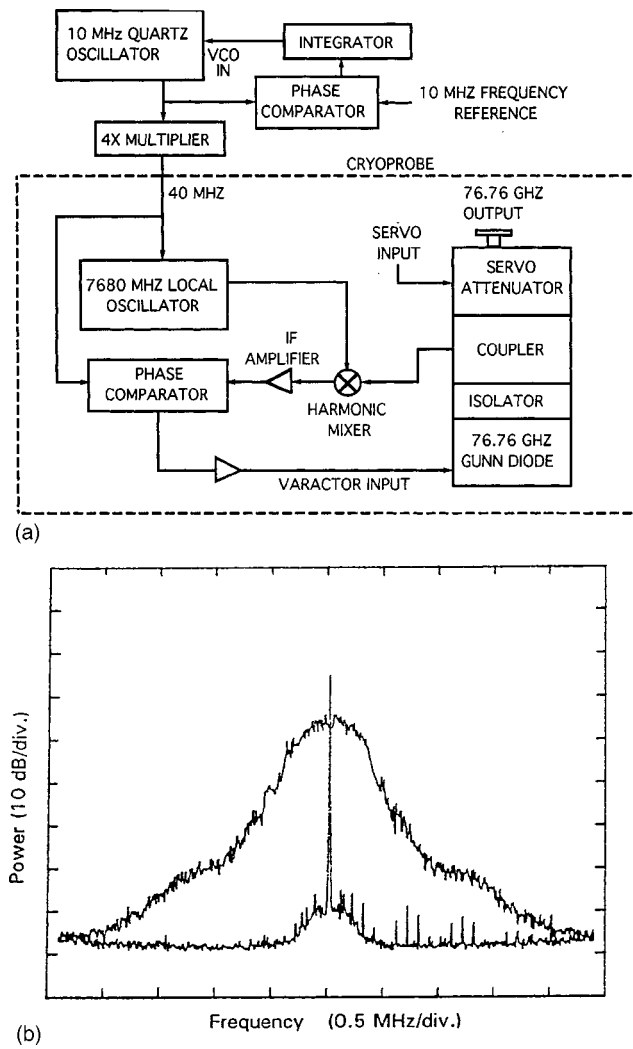


FIG. 8. (a) Block diagram of a 76 GHz phase-locked oscillator (PLO) for a Josephson voltage standard and (b) a comparison of the frequency spectrum of the PLO with a commercial frequency counter/stabilizer.

intermediate frequency (IF) beat signal near 40 MHz. The phase difference between the IF and the 40 MHz reference is used as an error signal to tune a varactor in the Gunn diode cavity and establish the phase lock. The wide bandwidth of the phase-locked loop in this system results in a phase noise of  $-55$  dBc (decibels below the carrier) at a 2 kHz offset from the center frequency. This is three orders of magnitude improvement over the phase noise achieved in typical systems that use microwave counters to stabilize the frequency. Figure 8(b) compares the spectral linewidth of a counterstabilized oscillator and a custom-built phase-locked loop. More importantly, the counterstabilized sources are not truly phase locked and typically have a small offset on the order of 10 Hz or about 0.000 13 ppm relative to the reference frequency.

As discussed previously, the zero-crossing steps of Fig. 1(b) allow a single-bias current while insuring that every junction in a large array is on a constant-voltage step. However, this leads to significant complication in setting the array to a particular desired step. Figure 9(a) illustrates a simplified diagram of the bias circuit. In this circuit, a computer sets the bias voltage  $V_s$  with one digital-to-analog converter

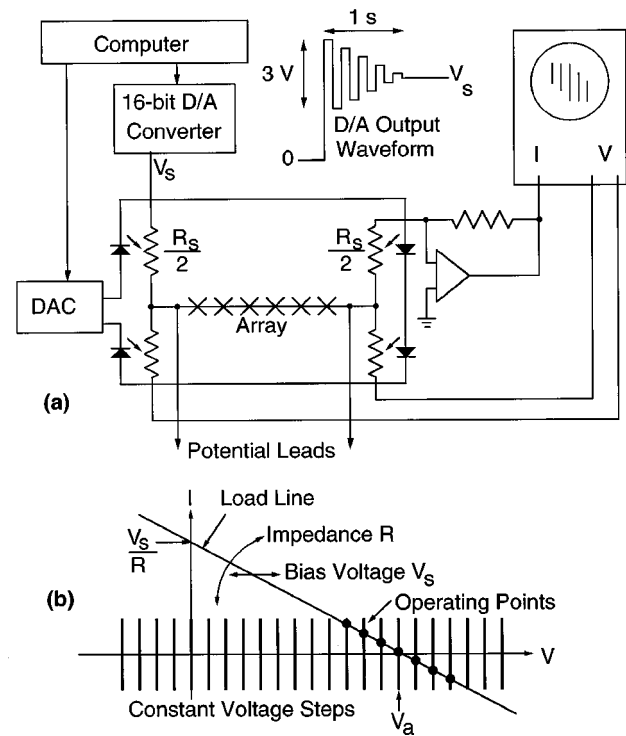


FIG. 9. (a) Bias circuit for a JVS and (b) a graphical solution of the operating points for the Josephson array.

(DAC) and uses a second DAC to control the bias impedance  $R_s$  via optically modulated resistors. Figure 9(b) shows a graphical solution for the stable operating points of the array and illustrates how control of both the bias voltage and the bias impedance is used to select a particular quantum voltage step.<sup>49</sup> The load line plots the range of voltage and current that are defined by the bias supply. The intersections of this load line with the  $I$ - $V$  curve of the array (vertical lines) are possible stable bias points. Changes to  $V_s$  shift the load line left and right, whereas changes to  $R_s$  change its slope. To select a step at a given voltage  $V_a$ , the source voltage is set to  $V_a$  and the source impedance is set to about  $f/K_J I_s \approx 10 \Omega$ , where  $I_s$  is the step height. This makes the load line steep enough to intersect only one or two steps and forces the array to a step at or very near  $V_a$ . Applying a damped oscillation to  $V_a$  helps move the array to the step closest to  $V_a$ . After a step is selected, the source impedance is smoothly increased on all four bias connections (load line becomes horizontal) until the array current goes to zero and the array is effectively disconnected from the bias source. This open-bias condition is the most stable state for the array and eliminates the possibility of any errors resulting from a small series resistance in the array—a common array defect. Computer control of this three-step process enables the system to find and stabilize the array voltage on a particular step within a few seconds. High-quality Josephson arrays will remain on a selected step for many hours.

Numerous algorithms have been developed to compare a Josephson standard with a secondary standard or another Josephson standard.<sup>29,51,59</sup> These algorithms differ in the amount of averaging used, the type and placement of reversing switches, and the statistical methods used to reduce the

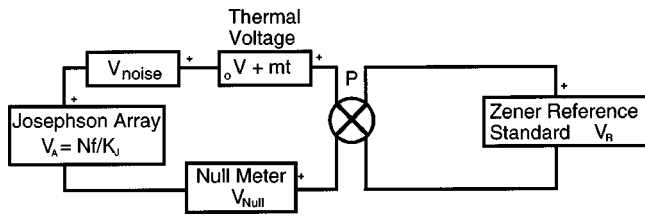


FIG. 10. Measurement loop used to determine the voltage of an unknown device relative to the Josephson standard.

data and compute uncertainty. The selection of an algorithm depends on the type of comparison, the desired level of uncertainty, and the time available. One commonly used algorithm that is appropriate for comparisons of Zener reference standards is described here.

**A. Example measurement algorithm**

The voltage of an unknown reference  $V_R$  relative to the Josephson array voltage is determined using the circuit shown in Fig. 10 (a subset of Fig. 7), in which the unknown and the Josephson array are connected in series opposition across a null meter. A reversing switch is used to eliminate the effect of thermal and other offset voltages. The step number  $n$  and sometimes the frequency  $f$  are adjusted to make the null voltage as small as possible. The circuit equation can then be written

$$V_a - V_{null} = nf/K_J - V_{null} = PV_R - V_o - mt - V_{noise} \quad (2)$$

Here,  $V_a = nf/K_J$  is the Josephson array voltage,  $V_o$  is a combination of thermal offset voltages and any offset voltage in the nullmeter,  $mt$  represents a linear drift component of the offset voltage,  $P = \pm 1$  is the polarity of the reversing switch,  $V_{null}$  is the differential null voltage, and  $V_{noise}$  represents noise in the unknown, the null meter, and any other sources of random noise. Now define a parameter  $V_i = nf/K_J - V_{null}$ , where  $V_{null}$  is a measurement at time  $t_i$  and  $n$  is determined from  $V_{null}$  using

$$n = \text{round}\{(K_J/f)(V_e + V_{null})\}, \quad (3)$$

where  $V_e$  is an initial direct measurement of  $V_R$  by the system voltmeter and the ‘‘round’’ function means rounded to the nearest integer. The direct measurement of  $V_R$  is obtained by setting the array to the  $n=0$  step, which can be seen from Fig. 7 to connect the voltmeter directly to the Zener reference.

Based on measurements of  $V_e$  and  $V_{null}$ , a set of values  $V_i$  and  $t_i$  is acquired for  $P = +1$ . Three successive values of  $V_{null}$  are examined for consistency within  $2 \mu\text{V}$  before the data are accepted. This eliminates data that may be corrupted by the transient that occurs when there is a spontaneous transition between quantum voltage steps. Since  $V_a$  and  $V_{null}$  change by equal amounts during a step transition,  $V_i$  remains constant thus making the data collection process relatively immune to step transitions. Data are collected efficiently even for a Josephson array chip that may be making as many as five transitions per minute. The scatter in the data that results from noise in the unknown and in the null meter can generally be modeled by a Gaussian process with one stan-

TABLE II. Potential sources of error and uncertainty for a Josephson standard.

|   |
|---|
| 1. Reference frequency offset and noise.  |
| 2. Voltage drops in the measurement loop caused by leakage currents.                      |
| 3. Null meter gain error, bias current, offset, input impedance, nonlinearity, and noise. |
| 4. Uncorrected thermal voltages in the measurement loop.                                  |
| 5. Offset owing to rectification of the reference frequency current in array defects.     |
| 6. Any effect of electromagnetic interference.  |
| 7. Defective junctions or connections leading to a bias-dependent voltage.                |
| 8. The product of series resistance in the array and any residual bias current.           |

dard deviation on the order of 20–100 nV. There are, however, occasional noise spikes that do not fit this process and generate glitches in the  $V_i$  data that may lie 1–10  $\mu\text{V}$  away from the well-behaved data. An outlier test is used to detect and eliminate such data.

After the collection of the first data set, the polarity of the unknown is reversed ( $P = -1$ ), the bias is readjusted to select a step that minimizes  $V_{null}$ , and a second set of data is acquired. Two more reversals generate third and fourth data sets. Best estimates for  $V_R$ ,  $V_o$ , and  $m$  are obtained from a least-squares recursion analysis that minimizes the root-sum-square error of the set  $V_i - (P_i V_R - V_o - mt_i)$  for all  $i$  in the four data sets. In typical measurements of Zener standards, the noise of the standard often dominates the computed value of  $m$ . The type-A uncertainty for  $V_R$  is the standard deviation of the mean for the set of  $V_i$ . Typically, this entire calibration algorithm is controlled by a computer and is completed in a few minutes. Except in the case of data with nonuniform delays between the reversals, a simple average of the absolute values of the full set of  $V_i$  is an equally good estimate of  $V_z$ .

Systems like that shown in Fig. 7 are used to calibrate secondary standards, such as Weston cells, Zener references, and precise digital voltmeters. These calibrations are greatly simplified by the fact that the Josephson array voltage can be set to any value  $V = nf/K_J$ , where the integer  $n$  can have any value in the range of about  $-75\,000$  to  $+75\,000$ . The typical uncertainty in measurements of 10 V Zener standards is limited by noise in the Zener to about 0.01 ppm. The ability to set the Josephson array to a wide range of discrete voltages also makes it the most accurate tool for measuring the linearity of high-accuracy digital voltmeters.

**B. Uncertainty**

While the voltage appearing across the terminals of a Josephson device is, in principle, given exactly by  $V = nf/K_J$ , in any real measurement there are a variety of potential sources of error and uncertainty. A list of the well-known ones is in Table II. In the case of a known error, such as a reference frequency offset or a known leakage resistance, a correction can be made. It is then the metrologist’s task to assign realistic numbers to all uncertainties including the uncertainty in the corrections. One method of doing this notes that only items 1 and 2 in Table II depend on the magnitude of the voltage being measured. All of the other components are about the same regardless of the voltage.



Therefore, the combined effect of items 3–8 can be quantitatively evaluated by making a set of measurements of a short circuit using exactly the same algorithm that is used for any other measurement. The standard error resulting from items 3–8 is just the root-mean-square (rms) value of the set of short-circuit measurements.<sup>72</sup> Additional experiments must be performed to estimate frequency and leakage uncertainty. Internationally accepted procedures for combining uncertainty and establishing confidence intervals are the subject of the BIPM's *Guide to the Evaluation of Uncertainty in Measurement*.<sup>73</sup> Typically, the total uncertainty contribution of a Josephson system in a measurement averaging time of a few minutes is a few nanovolts. Since the most common use of these systems is the calibration of Zener standards with a noise level of 50–100 nV, the contribution of the Josephson system is negligible.

### C. Traceability and equivalence

A Congressional act in 1904 established the U.S. Legal Volt to be a quantity defined by the National Bureau of Standards, now the National Institute of Standards and Technology (NIST). With the 1990 international agreement on the Josephson representation of the volt, NIST defined the U.S. Legal Volt to be the same as the international volt representation. Since the success of the first Josephson array voltage standards in 1984, their use has proliferated to more than 50 laboratories around the world. In addition to the approximately 35 national measurement institutes, there are now about 15 military and commercial laboratories using Josephson voltage standards. This has resulted in some confusion about the traceability of non-NMI's that are in possession of a JVS that is, in principle, as good as the national standard. Some guidance on this question is provided in International Standards Organization documents that state the general principle that intrinsic standards like the JVS, that have participated in a comparison with a NMI, can claim traceability.<sup>74</sup>

Unfortunately, traceability does not have a quantitative and universally accepted definition. Wood and Douglas<sup>75</sup> have proposed a resolution of this problem based on an approach known as quantified demonstrated equivalence. They show how measurements of a traveling standard at two different laboratories can lead to an equivalence statement of the form: "On the basis of measurements of a travelling standard by Lab A and Lab B, the results of similar measurements made at Lab A and Lab B can be expected to agree within  $X$  nV with 95% confidence." The value of  $X$  is a mathematical function of the measured difference and the uncertainties of the two standards laboratories. The problem when the equivalence of two Josephson standards is documented by a traveling artifact standard is that the uncertainty is usually dominated by the uncertainty introduced by the traveling artifact. This uncertainty is usually substantially greater than that obtained from a comprehensive analysis of the Josephson standard as discussed above. So, can a secondary standards laboratory with a Josephson standard claim an uncertainty based on an analysis of its standard (typically, a few nV) or claim only the uncertainty that can be docu-

mented by a comparison with a NMI (typically, 10 times larger)? If it is consistent with a NMI comparison, several laboratories in the U.S. use the lower number, that is, an analysis of their system's uncertainties, to describe their uncertainty relative to the U.S. Legal Volt. This view is not universally accepted by the NMIs and continues to be the subject of heated debate regarding the use and status of intrinsic standards at non-NMI standards laboratories.

## IV. PROGRAMMABLE VOLTAGE STANDARDS

Josephson voltage standards based on the zero-crossing steps of series arrays of hysteretic junctions have two important disadvantages: (1) the step number  $n$  cannot be quickly set to a desired value, and (2) noise may cause spontaneous transitions between steps. The step transition problem requires that the bandwidth of all connections to the chip be severely restricted in order to filter out noise. In the case of classical dc measurements, these are minor inconveniences that can be easily dealt with in software. However, the step stability, step selection, and bandwidth problems preclude measurements such as the rapid automated analysis of analog-to-digital (A/D) and digital-to-analog (D/A) converters and the synthesis of ac wave forms with a computable rms value.

### A. Binary weighted programmable arrays

To make possible these broader applications, a new type of Josephson voltage standard has been developed in which the output voltage  $V = nf/K_J$  is defined by digitally programming the step number  $n$ .<sup>76–84</sup> The key to this new Josephson standard is the use of junctions that are designed to be non-hysteretic, that is, the junction voltage is a single-valued function of the junction current, as in Fig. 1(a). This is achieved by choosing  $\beta_c$  to have a value less than 1. This, of course, brings us back to the situation in 1980 when it was deemed that arrays of such junctions would require individual bias currents to ensure that each junction was biased on a constant voltage step. There are two reasons why this is now practical. (1) Junction fabrication technology has advanced to the point where arrays of many thousands of junctions have a spread of critical currents of only a few percent. (2) Better microwave design allows very uniform distribution of power to very large arrays. These technological improvements allow a design in which each junction is biased only to the  $n = -1$ ,  $n = 0$ , or  $n = +1$  steps and large voltages are obtained by using very large arrays. The result is a large increase in the operating margin, that is, the range of current over which every junction is biased on the same constant-voltage step.

The circuit for this new standard uses an array of non-hysteretic junctions that is divided into a binary sequence of array segments, as shown in Fig. 11(a). The microwave excitation for each junction is set to equalize the amplitude of the  $n=0$  and  $n=\pm 1$  steps, as shown in Fig. 11(b). Each segment of the array can be set to the  $n = -1$ ,  $0$ , or  $+1$  step by applying a bias current ( $-I_s, 0, +I_s$ ) at the appropriate nodes. The combined step number  $N$  for the whole array can thus be set to any integer value between  $-M$  and  $+M$ , where

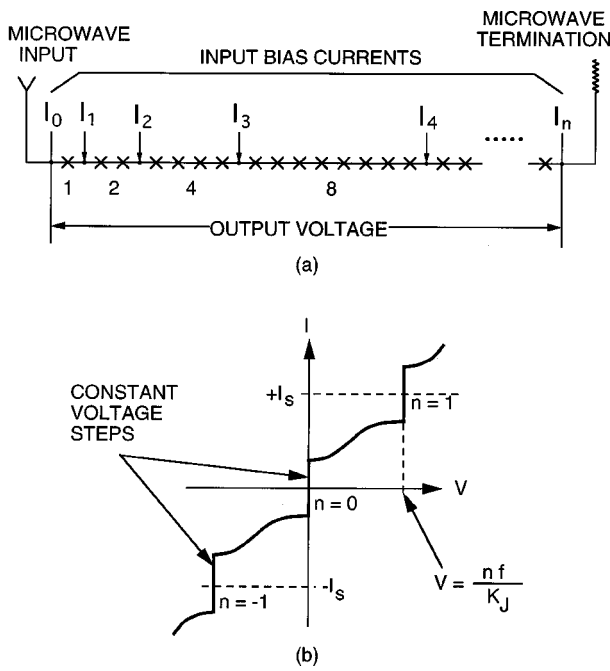


FIG. 11. (a) Schematic design of a programmable voltage standard based on a set of binary weighted arrays, and (b) the  $I$ - $V$  curve of a single junction with the microwave power set to equalize the amplitude of the  $n=0$  and  $n=\pm 1$  steps.

$M$  is the total number of junctions in the array. For example, to select step 5 we would set  $I_3 = I_1 = I_s$ ,  $I_2 = I_0 = -I_s$ . This would bias the single junction and the set of four junctions on the  $n=1$  step and leave all other junctions on the  $n=0$  step. Although all of the circuits of this type developed so far use the binary array sequence, we note that the array segments can have three possible voltages and thus a ternary-logic design would be more efficient. In this design, the array sequence would be 1, 3, 9, 27, ..., resulting in 25% fewer taps.

The rapid settling time and inherent step stability of the JVS in Fig. 11 make it potentially superior to a conventional JVS for dc measurements. (We define a dc measurement to be one in which the transient associated with changing  $N$  can be excluded from the measurement.) Such measurements include calibration of dc reference standards and digital voltmeters, and the characterization of A/D and D/A converters. The circuit of Fig. 11 can also generate a staircase approximation to a sine wave by selecting appropriate step numbers in rapid succession. In theory, the resulting wave form has a computable rms value and might be used to confirm the ac-dc difference of a thermal voltage converter and for other ac measurements. In the case of ac measurements, however, the transient wave form during step transitions is included in the rms value and may lead to an unacceptably large uncertainty.<sup>77</sup>

### B. SIS versus SNS junctions

Experimental realization of the programmable JVS has been pursued with a variety of junction technologies including resistively shunted superconductor-insulator-superconductor (SIS) (Refs. 76 and 84) junctions,

superconductor-normal-metal-superconductor (SNS) (Refs. 85 and 86) junctions, and superconductor-insulator-normal-metal-insulator-superconductor (SINIS) junctions.<sup>80,87-89</sup> In the case of SIS junctions, the required non-hysteretic  $I$ - $V$  curve is achieved by adding a shunt resistor in parallel with each junction. Theoretical analyses<sup>86,90-94</sup> have shown that the best combination of bias margin, stability, and microwave-drive power is achieved when the step voltage  $f/K_J$  is approximately equal to  $I_c R$ , where  $I_c$  is the junction critical current and  $R$  is the shunt resistor. In practice, the shunt resistor has an unavoidable parasitic inductance on the order of 1 pH. The resistor is effective only if its inductive reactance at the drive frequency  $f$  is small compared to its resistance. Thus, for practical frequencies,  $f < 100$  GHz, the maximum critical current is about  $300 \mu\text{A}$ . Practical measurements may require an output current of several mA, well beyond the ability of a SIS Josephson array to act as a current source. It has been proposed to solve this problem by adding a semiconductor D/A converter that supplies the predicted load current through a small resistor.<sup>95</sup> The array then acts as a fine trimmer by sinking or sourcing just enough current to bring the output voltage to the correct value. This addition to the bias circuit amplifies the available output current and minimizes transients at the step transitions.

Another approach to achieving large current output capability is to use SNS or SINIS junctions. For these junctions the shunt resistor is inherent to the metallic barrier, and its inductance is negligible. In this case,  $I_c$  is only limited by the available microwave power and/or heating effects, and step amplitudes of several milliamperes are easily achieved. Large critical currents are essential to achieve the noise immunity that high-speed operation demands. For this reason, the SNS or SINIS junction geometry is now the preferred design for programmable voltage standards.

A commonly used barrier material for SNS junctions is the palladium-gold barrier for which the  $I_c R_N$  product is, typically,  $5\text{--}20 \mu\text{V}$ .<sup>85,88</sup> The condition  $f \approx I_c R_N K_J$ , as described above, leads to an optimum drive frequency near 8 GHz. Pd-Au arrays work nearly as well at frequencies up to 15 GHz. Since the resolution of this type of Josephson standard is given by the step separation, the lower frequency relative to the SIS design results in higher resolution, but at the expense of requiring more junctions per volt of output range. (At 15 GHz, 32 240 junctions are required for 1 V.) Fortunately, the SNS junction fabrication process is able to generate large arrays of highly uniform junctions  $2.5 \mu\text{m}$  in diameter with critical currents near 5 mA.

Figure 12(a) shows one example of the physical layout of a SNS programmable voltage standard chip with 32 768 junctions. The lower frequency used in the SNS design makes the rf dividing network too large to fit on the chip, so the transition from semirigid coaxial transmission line to coplanar waveguide and a 1-4 divider network is etched onto the finger contact board to which the chip mounts. Each of the four coplanar feeds connects along the left edge of the chip to four impedance-matching transformers. An additional split at the end of each transformer results in a total of eight feeds to eight array segments of 4096 junctions each. The

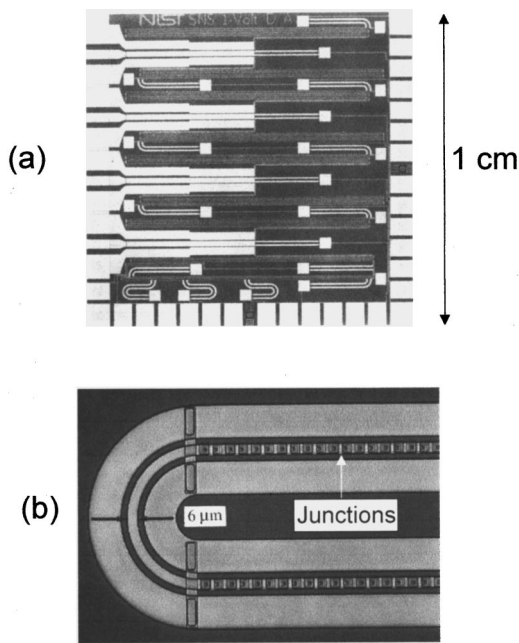


FIG. 12. (a) Physical layout of the  $1 \times 1$  cm, 32 768 junction, programmable-array chip and (b) a section of coplanar waveguide showing the distribution of junctions along the center conductor.

end of each array line is terminated with a  $50 \Omega$  resistor in series with  $10 \text{ pF}$  to ground. Power uniformity requires that the taps between array segments do not create reflections that would lead to standing waves. Each tap, therefore, includes a band-stop filter at the  $16 \text{ GHz}$  design frequency. The voltage range of this chip is  $\pm 1.1 \text{ V}$ .

Figure 12(b) shows in detail how the junctions are arranged in series along the center conductor of a  $50 \Omega$  coplanar waveguide. In contrast to the  $3 \Omega$  striplines used in the SIS design, the  $50 \Omega$  coplanar design eliminates two fabrication levels. Also, because of the larger ratio of line impedance to junction resistance, it is possible to maintain the required rf power uniformity through a larger number of junctions.

Programmable Josephson standards made with the SINIS junction process have a much larger  $I_c R_n$  product (approximately  $150 \mu\text{V}$ ), and thus can operate at much higher frequencies where fewer junctions are required and the entire microwave distribution network can be fabricated on chip. Studies of the microwave attenuation as a function of array length at this higher frequency have shown that the junctions themselves contribute a significant portion of the microwave power flowing down the line.<sup>80,90,91,96</sup> This makes it possible to use much larger arrays than would otherwise be possible, and opens up the possibility of a self-driven array in which all of the microwave power is self-generated with a small portion tapped off to phase lock the array to a frequency reference.

SNS and SINIS programmable arrays have been integrated into complete systems in which the bias currents that are applied to each tap are generated by a set of D/A converters that are controlled by a computer. The computer maps the optimum operating range of each array segment, tests for the flatness of the steps generated by each segment,

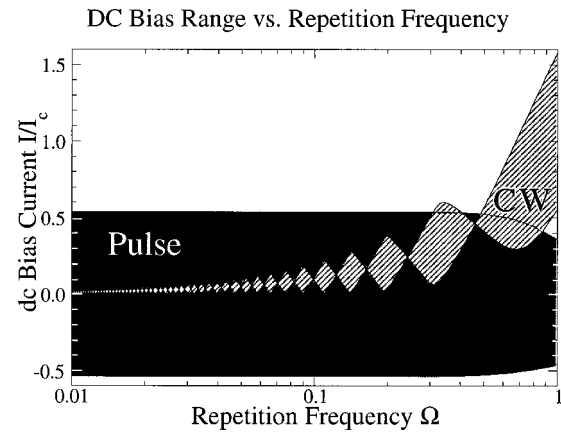


FIG. 13. Comparison of the normalized  $n=1$  step boundaries for a junction driven with a pulse train (black) and a continuous sine wave (shaded) as a function of normalized frequency  $\Omega = f/f_c$ .

and allows a user-defined program to synthesize a specified wave form. Direct dc voltage comparisons at  $1 \text{ V}$  between a programmable JVS (PJVS) and a classical JVS using zero-crossing steps have yielded a measured difference of less than  $0.5 \text{ nV}$  with a standard uncertainty of  $1 \text{ nV}$ .<sup>80,97</sup>

Programmable Josephson standards are being used in two different watt-balance experiments, which compare electrical and mechanical power with an uncertainty on the order of  $0.01 \text{ ppm}$ .<sup>98,99</sup> In these experiments they provide a precise and noise-tolerant voltage reference that can be rapidly switched between equal and opposite voltages. The programmable JVS has also been used to provide both the dc and ac inputs for the fast-reversed dc method of measuring the thermoelectric transfer difference of thermal voltage converters. The first use in this application yielded a type-A uncertainty of  $0.13 \times 10^{-6}$ .<sup>100</sup> The PJVS is also the planned voltage reference in a metrology triangle experiment in which the Josephson voltage is compared with the voltage across a quantum Hall resistor driven by an electron-counted current.<sup>101</sup>

### C. Pulse-driven Josephson arrays

Although quite useful in several new applications, binary programmable arrays have not been very successful in the synthesis of ac wave forms because the undefined voltage during transitions between steps adds an unacceptable level of uncertainty. Benz and Hamilton have developed another approach that biases the array with pulses and has the promise to solve this problem.<sup>102</sup> Thus far, we have discussed ways to program the voltage of a Josephson array by changing the step number  $n$  in the equation  $V = nf/K_J$ . It is clear that the same result might be achieved by changing  $f$ . Unfortunately, in the case of a sine-wave excitation, the step amplitudes collapse rapidly to zero as the frequency decreases. This means that it is practical to control the voltage via the frequency only over a range of frequency within about a factor of 2 of the optimum frequency  $f_c = I_c R K_J$ . However, simulations show that if the sine-wave excitation is replaced with a pulse excitation, then the step amplitude is independent of the pulse repetition frequency for all frequencies below  $f_c$ .<sup>102-105</sup> The optimum pulse width is  $\tau = 1/(2\pi f_c)$ . Figure 13 is a calculation of the  $n=1$  step boundaries for a

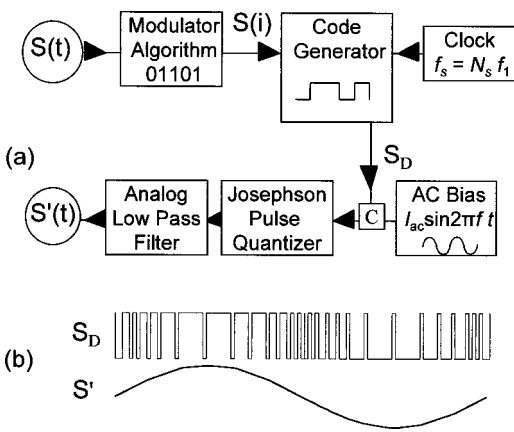


FIG. 14. (a) Josephson array pulse quantizer and (b) a block diagram of a delta-sigma digital-to-analog converter based on pulsed Josephson junctions.  $S(t)$  is the desired wave form and  $S'(t)$  is the output wave form.

junction driven with a sine wave (shaded area) and a pulse train (black area).<sup>102</sup> Note that for a pulse drive, the step amplitude is large, symmetric around zero, and independent of frequency all the way to zero frequency. In fact, if the pulse polarity is reversed, then the array can generate both positive and negative voltages.

A programmable voltage source based on this idea consists of a single large array of  $N$  junctions distributed along a wide bandwidth transmission line.<sup>102-106</sup> A pulse train at frequency  $f$  propagating down the line generates an average voltage  $Nf/K_J$  across the ends of the array. A complex output wave form can be generated by modulating the pulse train with a digital word generator. For example, using a clock frequency of  $f_c = I_c R K_J = 10$  GHz, the pulse sequence 11111000001111100000... creates an output square wave of amplitude of  $Nf_c/K_J$  and frequency of 1 GHz.

Figure 14 is a block diagram of the process that is used to generate an accurate sine wave of frequency  $f_1$  or any other periodic wave form from quantized Josephson pulses. The modulator algorithm block is a computer program that digitizes an input signal  $S(t)$  at a sampling frequency  $f_s$ . The algorithm is a second-order delta-sigma modulator that optimizes the signal-to-quantization-noise ratio over a desired frequency band.<sup>107</sup> For a repetitive wave form, the code generated by the modulator is calculated just once and stored in the circulating memory of a digital code generator. When the digital code generator is clocked at the sampling frequency, it recreates an approximation to the original signal as an output voltage in real time  $S_D(t)$ . It has been shown that combining  $S_D(t)$  with a sine-wave bias at  $(3/2)f_s$  to drive the Josephson array makes possible bipolar operation and results in a factor of 6 improvement in voltage range over that from driving the array with  $S_D(t)$  alone.<sup>108</sup> The function of the array is to perfectly quantize the input pulses, thus greatly reducing amplitude noise in  $S_D(t)$  within the signal band. It has been shown both theoretically and experimentally that a noise reduction on the order of 60 dB can be achieved with this method. When the ratio  $f_s/f$  is large (e.g.,  $>10^4$ ), the in-band component of the voltage across the array is an almost perfect reproduction of the input signal. An equally important feature of the quantized voltage pulses

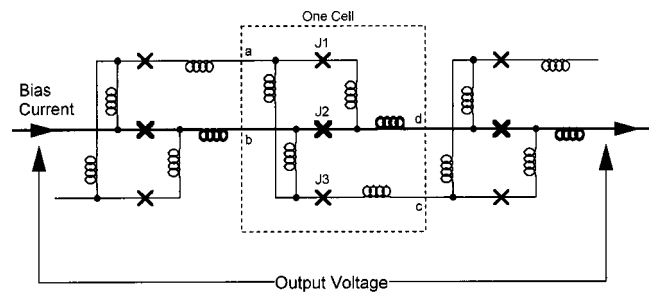


FIG. 15. Schematic diagram of three cells of a single-flux-quantum voltage multiplier.

generated by each junction is that their time integral is exactly equal to a single-flux-quantum  $h/2e = 1/K_J = 2.067\ 834$  mV ps. This means that a knowledge of the digital code, the sampling frequency, and the number of junctions in the array is sufficient to exactly compute the spectrum and the rms value of  $S'(t)$ .

The pulse-driven Josephson array has the potential to be both a dc voltage standard and an ac voltage standard with a bandwidth of 1 MHz or more. The realities are that: (1) this idea has been demonstrated to voltage amplitudes of only about 150 mV, and (2) a great deal of work is required to increase the voltage range and to prove that every pulse specified by the digital code is faithfully reproduced by every junction in the array. This can only happen if the transmission path to every junction is reasonably independent of frequency from dc to about 18 GHz, a very stringent requirement. Fortunately, there are a variety of simple tests for “lost pulses.” For example, the dc output of the circuit of Fig. 14 is proportional to  $n_1 - n_0$ , where  $n_1$  is the number of ones in the code and  $n_0$  is the number of zeros in the code. Exactly the same dc voltage should result from all codes that have the same  $n_1$  and  $n_0$  regardless of the distribution of ones and zeros within the code. When performed with nanovolt resolution, present circuits often fail this test. Another obvious test is to compare the computed rms voltage of a synthesized sine wave with the best available ac voltmeter. Not only should the agreement fall within the uncertainty of the voltmeter, but the measured voltage must have a “flat spot” when subjected to small variations in the amplitude of the digital code, the amplitude of the sine-wave drive, and their relative phase and offsets. Again, it is not uncommon for present circuits to fail this test. Efforts are under way to improve performance on these tests by improved design of the cryoprobe input transmission line, the launching network onto the chip, the array transmission line itself, and the taps that extract the synthesized signal.

#### D. Single-flux-quantum voltage multipliers

Another approach to the pulse-driven voltage standard is based on the unique ability of a Josephson junction to generate a voltage pulse whose time integral is perfectly quantized. These pulses are triggered when the junction is subjected to a current pulse with a width on the order of  $1/(K_J I_c R_n)$  and an amplitude on the order of  $I_c$ . Even though the time integral of the current pulse may vary over a substantial range, the time integral of the resulting voltage

pulse is exactly equal to the flux quantum  $h/2e = 1/K_J$ ,  $= 2.067\,834\text{ mV ps}$ . These single-flux-quantum (SFQ) pulses can be manipulated to make a perfect voltage multiplier.<sup>109–115</sup> Figure 15 illustrates a voltage multiplier consisting of an arbitrarily long string of cells.<sup>111</sup> Each of these cells consists of at least three junctions and several inductors. The center line of the circuit (in bold) can be seen to consist of a series array of junctions, one per cell. The circuit is powered by a dc-bias current flowing in series through each cell. When an input pulse is applied between terminals  $a$  and  $b$ , it triggers the three junctions of each cell to generate a SFQ pulse in the sequence J1, J2, J3. The delay between the pulse across J2 and J3 results in an output pulse at  $c$  and  $d$  that is sufficient to trigger the next cell. The pulse across J2 adds to the voltage output. When the first cell is triggered by a pulse, that pulse is regenerated in each cell and propagates through the entire array. The voltage pulse that develops across the ends of the array will have a time integral of  $N/K_J$  where  $N$  is the number of cells in the array. An array of these cells can be used in a delta-sigma converter exactly as described above but with two major improvements: (1) since the propagating pulse is regenerated in each cell, there is no cumulative distortion of the pulse drive and the number of cells is, in principal, unlimited; and (2) the pulse energy required to drive the first cell is only about  $10^{-18}\text{ J}$  and can be supplied by other SFQ circuits, such as a pulse multiplier. This makes it possible to manipulate the reference frequency on-chip with other SFQ circuits.<sup>111</sup> For example, the digital input could be a pulse train with a maximum frequency of 200 MHz, a very easily and cheaply generated signal. Each rising edge of the signal could generate a burst of 64 pulses at the output of an on-chip pulse multiplier and a  $64N/K_J$  time integral pulse across the array of voltage multiplier cells. With  $N=2500$  this circuit would have a voltage range of  $64Nf/K_J=1\text{ V}$ . The ability to manipulate the multiplier inputs on-chip also makes possible a design with a binary-coded input. In contrast to the binary-coded arrays described above, this design should eliminate any uncertainty in the number of SFQ pulses in the output.

These advantages have been gained at the expense of a much more complex circuit that is difficult to design and, as a result of the large number of elements per cell, even more difficult to fabricate. The development of these circuits has been actively pursued for more than ten years. The present state of the art is a  $5\text{ mm}\times 5\text{ mm}$  chip with a voltage range of 100 mV. Plans are under way to integrate ten of these chips into a system with 1 V capability. It will be necessary to subject these circuits to a variety of rigorous tests (particularly the “flat spot” test) to confirm that the generated voltage does indeed derive only from a perfectly controlled sequence of SFQ pulses.

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