# Josephson **DIA** Converter with Fundamental Accuracy

C. **A.** Hamilton, C. **J.** Burroughs, and R. L. Kautz

*Abstract-* **A binary sequence of series arrays of shunted Josephson junctions is used to make a 14-b D/A converter. With 13 bias lines, any step number in the range -8192 to**   $+8192 -1.2$  V to  $+1.2$  V can be selected in the time required **to stabilize the bias current (a few microseconds). The circuit is a fast accurate dc .reference, and it makes possible the digital synthesis of ac waveforms whose amplitudes derive directly from the internationally accepted definition of the volt.** 

## I. INTRODUCTION

TYPICAL Josephson array voltage standards uses 20 000 or more junctions driven at 75 GHz to generate about 200000 voltage steps that span the range from  $-14$  V to  $+14$ **V [l].** Although an array can be set to any step, the procedure to select a particular step is so slow that the standards are useful only for dc measurements. This paper describes a new Josephson circuit that allows the rapid selection of any step number. The new circuit has *N* digital inputs which define any one of  $2^N$  evenly spaced output voltages. The circuit is therefore a D/A converter whose output voltage has the full accuracy of the SI volt representation.

## II. CIRCUIT OPERATION

The junctions and microwave drive used in the new standard are designed to generate a current-voltage *(I-V)* curve similar to that shown in Fig. **1** (top). This curve has three stable voltages: 0,  $f/K_J$ , and  $-f/K_J$ , where f is the microwave drive frequency and  $K_J = 483$  597.9(1 $\pm$ 4×10<sup>-7</sup>) GHz/V is the Josephson constant. The three voltages are uniquely selected by the bias currents  $0, +I_s$ , and  $-I_s$ . The output voltage is accurate for any input current within about  $\pm 20\%$  of the nominal value. When  $M$  junctions similar to that described in Fig. 1 are connected in series, the steps occur at the voltages 0 and  $\pm Mf/K_J$ . Fig. 1 (bottom) is an experimental result using a reference frequency of 75 **GHz** and shows the *I-V*  curve of *2048* junctions in series. The steps occur at 0 and f2048~(75 **GHz)/(483** 597.9 *GHzN)=* **50.317** V..

As shown in Fig. 2, the Josephson D/A converter consists of a binary sequence  $(1, 2, 4, 8, \cdots)$  of independently biased arrays. **An** arbitrary output voltage is generated by applying bias currents to the appropriate set of arrays. The binary sequence of array lengths makes it possible to choose bias currents to generate a voltage  $\pm Mf/K_J$ , where *M* is any

Manuscript received July I, 1994: revised October 15, 1994. This work was supported in part by the U.S. Army, Redstone Arsenal, CCG Project 346. The authors are with the National Institute of Standards and Technology,

Boulder, CO 80303 USA. IEEE Log Number 9408700.



Fig. 1. (a) The *I-V* curve of a single shunted junction driven at 75 **GHz**  and (b) the  $I-V$  curve for an array of 2048 junctions.

integer from 0 to the total number of junctions in all arrays. The vertical steps in the junction's *1-V* curves ensure that the output voltage will be accurate over about a  $\pm 20\%$  variation in *Is* from its nominal value.

## **111.** JUNCTION DESIGN

The ideal *I-V* curve for the junctions used in the D/A converter has constant-voltage steps at  $V = 0$  and  $V =$  $f f/K_J$  that extend over the largest possible nonoverlapping ranges of dc bias. Large-amplitude steps are obtained, and chaotic behavior is avoided when the junction parameters meet either the condition

$$
2\pi f^2 C/K_J I_c \gg 1\tag{1}
$$

or the condition

$$
f/K_J I_c R \gg 1\tag{2}
$$

0018-9456/95\$04,00 *0* 1995 **IEEE** 



**Fig.** 2. A Josephson D/A converter based on a binary sequence of shunted junction **arrays.** 

where  $I_c$  is the junction critical current,  $R$  is the shunt resistance, and  $C$  is the shunt capacitance  $[2]$ . In either case, the dc bias range of the *n*th step at voltage  $V_n = nf/K_J$  is given by

$$
V_n/R - I_c|J_n(v_{rf})| < I < V_n/R + I_c|J_n(v_{rf})| \tag{3}
$$

where  $J_n$  is the *n*th order Bessel function and  $v_{rf} = V_{rf}/V_1$ is the amplitude of the applied microwave voltage  $V_{rf}$  normalized to the voltage  $V_1$  of the first step [2].

According to (3), the largest possible  $n = 0$  and  $n = 1$ steps are obtained in the same  $I-V$  characteristic when  $v_{rf}$  is chosen to simultaneously maximize  $|J_0(v_{rf})|$  and  $|J_1(v_{rf})|$ . The maximum occurs for  $v_{rf}^* = 1.435$ , for which argument  $J_0 = J_1 = 0.5476$ . Applying (3) to this case, we find that the  $n = 0$  and  $n = 1$  steps will overlap in dc bias unless

$$
f/K_J I_c R > 2|J_0(v_{rf}^*)| \ge 1.1.
$$
 (4)

However, we also require that the separation in dc bias between the  $n = 0$  and  $n = 1$  steps is relatively small. This condition helps insure that the  $n = 1$  step exists at a common bias for all junctions in the array. According to (3), the separation will be less than the step width when  $v_{rf} = v_{rf}^*$ provided that

$$
f/K_J I_c R < 4|J_0(v_{rt}^*)| \le 2.2. \tag{5}
$$

Thus, to obtain the optimum *I-V* curve, the normalized frequency  $f/K_JI_cR$  is limited to the range between roughly 1 and 2. At typical operating frequencies ( $\simeq$ 75 GHz), this condition requires a junction with an  $I_cR$  product of about 0.1 mV.

## IV. SHUNTED TUNNEL JUNCTIONS

Because chaos can be avoided by satisfying either (1) or *(2),*  two different strategies are possible in building the proposed D/A converter. We consider first the approach used in the present experiments, in which chaos is avoided according to (1) by making the junction's plasma frequency  $f_p =$  $\sqrt{K_J I_c/2\pi C}$  much less than the drive frequency f. Just as in zero-bias voltage standards, this condition requires a high-capacitance tunnel junction with a relatively low critical current density  $J_c$  [2]. However, because the subgap  $I_cR$ product of a tunnel junction is typically 20 mV, we must add a low-resistance external shunt to bring  $I_cR$  into the range specified by (4) and (5). Thus, the  $I-V$  curves shown in

Microwave Input Bias Currents<br>
In the bare tunnel junction and converts the *I*-*V* curve to the the bare tunnel junction and converts the  $I-V$  curve to the staircase pattern required for our D/A converter.

#### V. METALLIC-BARRIER JUNCTIONS

Although this paper focuses on **D/A** converters made with shunted tunnel junctions, we pause here to note that metallicbarrier junctions offer the possibility of significant performance improvements. The problem with shunted tunnel junctions stems from the fact that a low critical current density is required to meet the condition imposed by **(I).** Because the junction area is limited by phase bending effects, the useful critical current for a given operating frequency and junction material is bounded by a definite upper limit *121.* In the present instance, the maximum useful critical current is about 300  $\mu$ A. While 300  $\mu$ A is adequate for some applications, a larger critical current would provide greater immunity to noise and allow more current to be drawn from the D/A converter.

The possibility of larger critical currents is raised when chaos is avoided through the condition specified by (2). In this case,  $I_c$  can be made as large as desired, provided that  $R$ is selected to maintain  $f/K_JI_cR \sim 2$ . In principle, this strategy might be applied to a high- $J_c$  tunnel junction with an external shunt. The difficulty with this approach is that an external shunt always has an associated parasitic inductance. To be effective in eliminating chaos, the impedance of the parasitic inductance at the drive frequence must be less than the resistance of the shunt. Because practical fabrication methods do not allow the inductance to be reduced below about **1** pH, a shunt resistance less than about 0.5  $\Omega$  is ineffective at 75 GHz.  $I_c$  can therefore be no greater than about 150  $\mu$ A.

For metallic-barrier or **superconducting-normal-supercon**ducting **(SNS)** junctions, on the other hand, values of *I,R*  on the order of 0.1 mV are easily obtained without an external shunt. Because the internal resistance of an **SNS**  junction has no significant inductance, even low resistances are effective at high frequencies, and there is no known bound on the useful critical current that might be attained. The small capacitance of **an SNS** junction is also useful because it insures that chaos is avoided through the criterion  $\beta$  =  $2\pi K_I L_R^2 C \ll 1$ , regardless of whether (1) or (2) is satisfied. Thus, **SNS** junctions may be ideal for our **D/A** converter, providing extremely stable, large-amplitude steps that would allow significant current to be drawn by an external load.

# VI. MICROWAVE DISTRIBUTION

Even if all of the junctions in an array are nearly identical, their *I-V* curves will be similar only if each receives roughly the same microwave power. As in zero-bias arrays *121,* a uniform microwave distribution is obtained by designing the array to act as a low-loss transmission line terminated by a matched load. Because microwaves are not significantly attenuated between the beginning and end of the array, each junction receives nearly the same power.



Fig. 3. Synthesized triangle waves using the 4, 5, and 6 most significant bits of the Josephson D/A converter.

# VII. EXTERNAL LOADING

The circuit described so far has an important limitation because any current drawn at the output will shift the bias points of the junctions. Even small load currents of a few tens of microamperes may shift one or more junctions to a nonquantized voltage. However, if the load impedance is known. most of the load current can be supplied by a semiconductor D/A converter, which is programmed to deliver

# VIII. EXPERIMENTAL REALIZATION

We have fabricated and tested a 14-b version of the circuit shown in Fig. 2. Although fabrication defects and trapped magnetic flux prevented operation of some bits, the least significant nine bits are fully functional, leading to a maximum output voltage of  $\pm 77$  mV with 0.15 mV resolution. The accuracy of the output has been confirmed to  $\pm 1 \mu V$ . Fig. 3 (top) shows a synthesized  $\pm 77$  mV triangle wave using the most significant four bits of the Y-b converter. Fig. 3 (middle) and (bottom) shows the result with the five and six most significant bits in operation. Load compensation was not required for this data because the **D/A** output was connected only to the 1  $M\Omega$  oscilloscope input. The triangular wave frequency in the data of Fig. 3 is entirely limited by the automated test system used to drive the input bias currents. The Josephson D/A converter should be capable of input sampling rates greater than 1 MHz. This will make it a very fast, adjustable dc reference source with the possibility to synthesize ac waveforms with a calculable RMS value.

## **REFERENCES**

- [1] C. A. Hamilton, C. Burroughs, and K. Chieh, "Operation of NIST Josephson array voltage standards." *J. Res. Nat. Inst. Stand. Technol.*, vol. 95, pp. 219-235, May 1990
- 121 R. L. Kautz, "Design and operation of series-array Josephson voltage standards," in L. Crovini and T. J. Quinn, Eds., Metrology at the Fron*tiers of Physics and Technology.* Amsterdam: North-Holland. 1992, pp. 2.59-296.