CHAPTER 1: THE OP AMP

OP AMP SPECIFICATIONS (cont.)

CHAPTER 1: THE OP AMP

Introduction

In this chapter we will discuss the basic operation of the op amp, one of the most common linear design building blocks.

In section 1 the basic operation of the op amp will be discussed. We will concentrate on the op amp from the black box point of view. There are a good many texts that describe the internal workings of an op amp, so in this work a more macro view will be taken. There are a couple of times, however, that we will talk about the insides of the op amp. It is unavoidable.

In section 2 the basic specifications will be discussed. Some techniques to compensate for some of the op amps limitations will also be given.

Section 3 will discuss how to read a data sheet. The various sections of the data sheet and how to interpret what is written will be discussed.

Section 4 will discuss how to select an op amp for a given application.

SECTION 1: OP AMP OPERATION

Introduction

The op amp is one of the basic building blocks of linear design. In its classic form it consists of two input terminals, one of which inverts the phase of the signal, the other preserves the phase, and an output terminal. The standard symbol for the op amp is given in Figure 1.1. This ignores the power supply terminals, which are obviously required for operation.

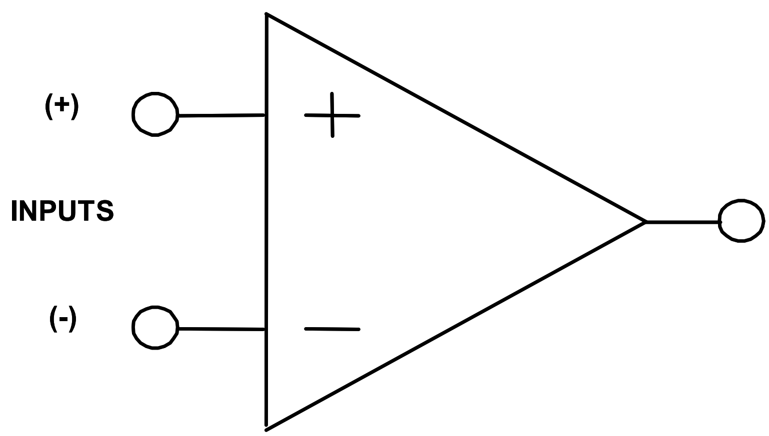


Figure 1.1: *Standard op amp symbol*

The name "op amp" is the standard abbreviation for operational amplifier. This name comes from the early days of amplifier design, when the op amp was used in analog computers. (Yes, the first computers were analog in nature, rather than digital). When the basic amplifier was used with a few external components, various mathematical "operations" could be performed. One of the primary uses of analog computers was during WWII, when they were used for plotting ordinance trajectories.

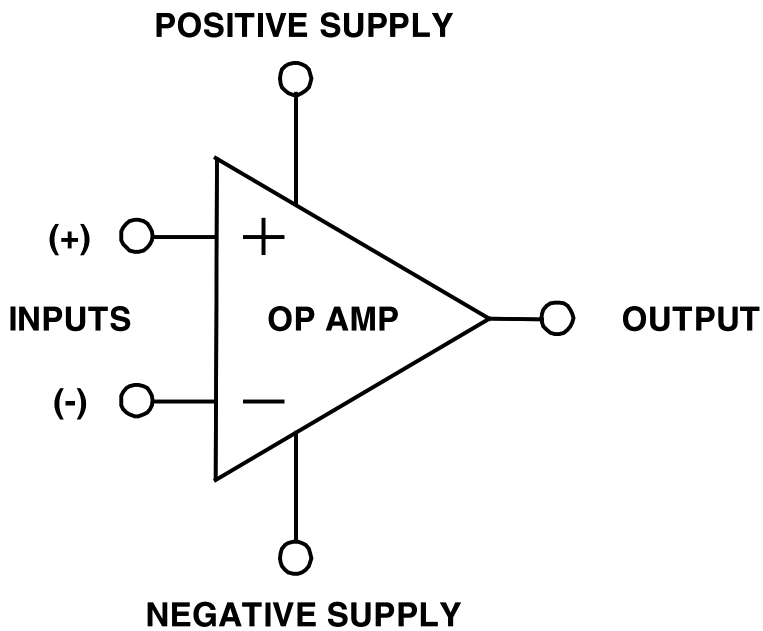
Voltage Feedback (VFB) Model

The classic model of the voltage feedback op amp incorporates the following characteristics:

1.) Infinite input impedance
2) Infinite bandwidth
3) Infinite gain
4) Zero output impedance
5) Zero power consumption

None of these can be actually realized, of course. How close we come to these ideals determines the quality of the op amp.

This is referred to as the voltage feedback model. This type of op amp comprises nearly all op amps below 10 MHz bandwidth and on the order of 90% of those with higher bandwidths.



- IDEAL OP AMP ATTRIBUTES
  - Infinite Differential Gain
  - Zero Common Mode Gain
  - Zero Offset Voltage
  - Zero Bias Current
  - Infinite Bandwidth
- OP AMP INPUT ATTRIBUTES
  - Infinite Impedance
  - Zero Bias Current
  - Respond to Differential Voltages
  - Do Not Respond to Common Mode Voltages
- OP AMP OUTPUT ATTRIBITES
  - Zero Impedance

Figure 1.2: *The Attributes of an Ideal Op Amp*

Basic Operation

The basic operation of the op amp can be easily summarized. First we assume that there is a portion of the output that is fed back to the inverting terminal to establish the fixed gain for the amplifier. This is negative feedback. Any differential voltage across the input terminals of the op amp is multiplied by the amplifier's open-loop gain. If the magnitude of this differential voltage is more positive on the inverting (-) terminal than on the noninverting (+) terminal, the output will go more negative. If the magnitude of the differential voltage is more positive on the noninverting (+) terminal than on the inverting (-) terminal, the output voltage will become more positive. The open-loop gain of the amplifier will attempt to force the differential voltage to zero. As long as the input and output stays in the operational range of the amplifier, it will keep the differential voltage at zero, and the output will be the input voltage multiplied by the gain set by the feedback. Note from this that the inputs respond to differential mode not common-mode input voltage.

Inverting and Noninverting Configurations

There are two basic ways to configure the voltage feedback op amp as an amplifier. These are shown in Figure 1.3 and Figure 1.4.
Figure 1.3 shows what is known as the inverting configuration. With this circuit, the output is out of phase with the input. The gain of this circuit is determined by the ratio of the resistors used and is given by:

$$A = -\frac{R_{fb}}{R_{in}} \quad \text{Eq. 1-1}$$

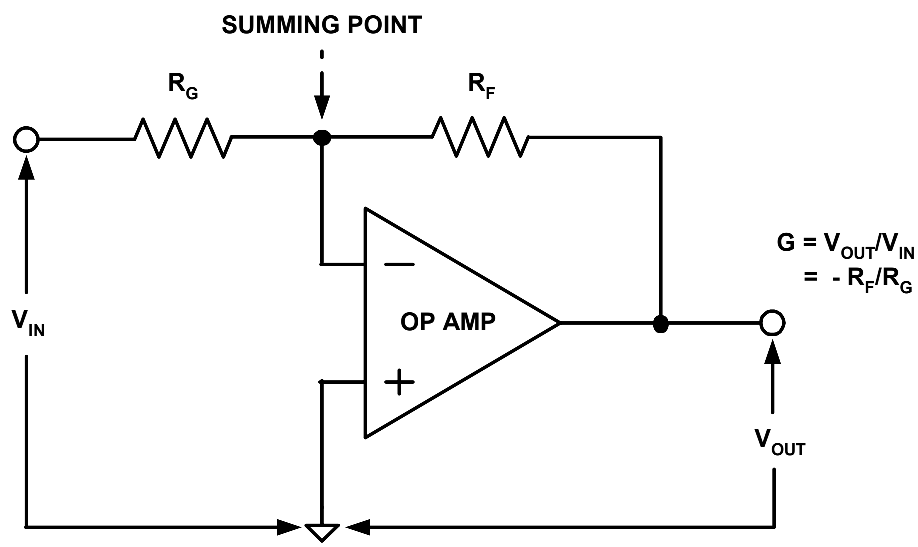


Figure 1.3: *Inverting Mode Op Amp Stage*

Figure 1.4 shows what is know as the noninverting configuration. With this circuit the output is in phase with the input. The gain of the circuit is also determined by the ratio of the resistors used and is given by:

$$A = 1 + \frac{R_{fb}}{R_{in}} \qquad \text{Eq. 1-2}$$

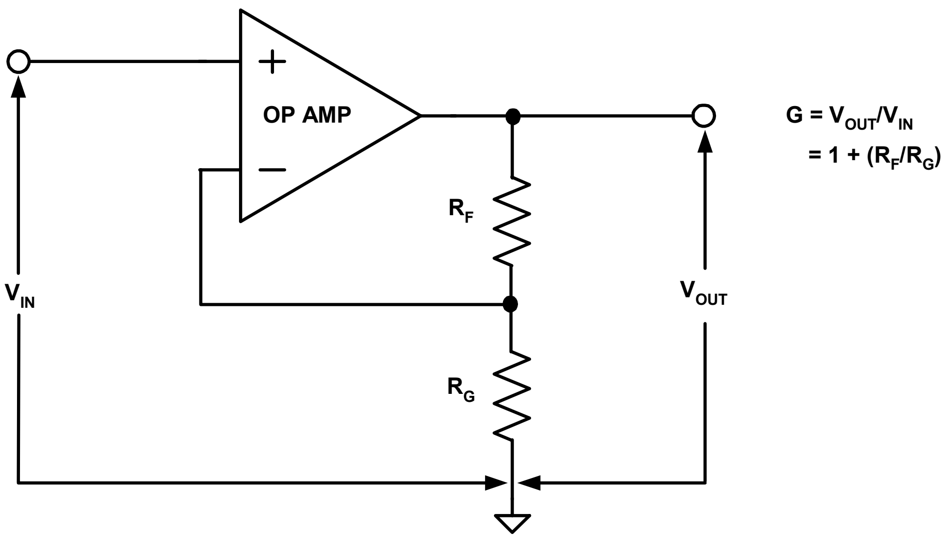


Figure 1.4: *Noninverting Mode Op Amp Stage*

Note that since the output drives a voltage divider (the gain setting network) the maximum voltage available at the inverting terminal is the full output voltage, which yields a minimum gain of 1.

Also note that in both cases the feedback is from the output to the inverting terminal. This is negative feedback and has many advantages for the designer. These will be discussed more in detail further in this chapter.

It should also be noted that the gain is based on the ratio of the resistors, not their actual values. This means that the designer can choose just about any value he wishes within practical limits.

If the values of the resistors are too low, a great deal of current would be required from the op amps output for operation. This causes excessive dissipation in the op amp itself, which has many disadvantages. The increased dissipation leads to self-heating of the chip, which could cause a change in the dc characteristics of the op amp itself. Also the heat generated by the dissipation could eventually cause the junction temperature to rise above the 150°C, the commonly accepted maximum limit for most semiconductors. The junction temperature is the temperature at the silicon chip itself. On the other end of the spectrum, if the resistor values are too high, there is an increase in noise and the susceptibility to parasitic capacitances, which could also limit bandwidth and possibly cause instability and oscillation.

From a practical sense, resistors below 10 Ω and above 1 MΩ become increasingly difficult to purchase especially if precision resistors are required.

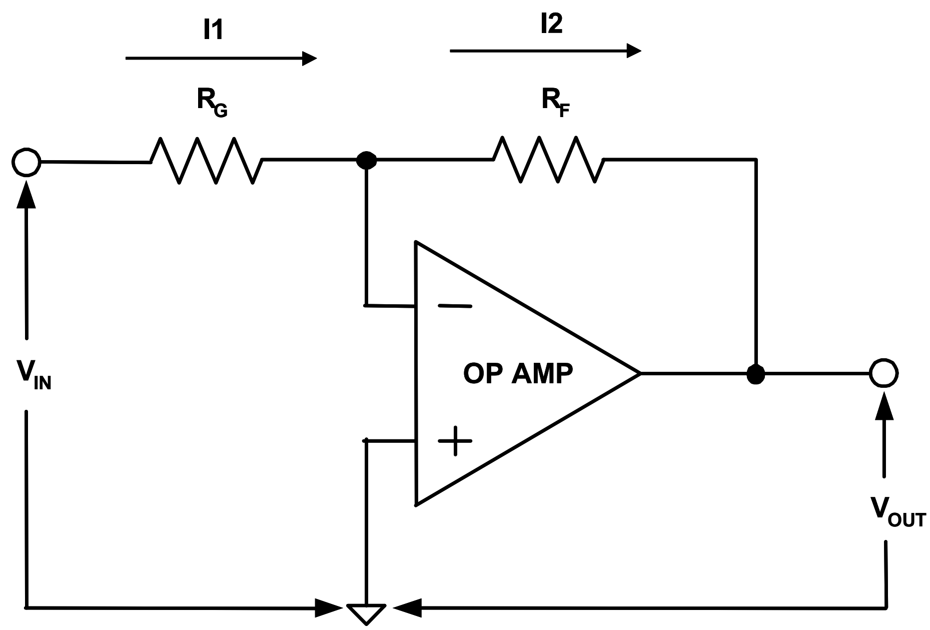


Figure 1.5: *Inverting Amplifier Gain*

Let us look at the case of an inverting amp in a little more detail. Referring to Figure 1.5, the noninverting terminal is connected to ground. (We are assuming a bipolar (+ and −) power supply). Since the op amp will force the differential voltage across the inputs to zero, the inverting input will also appear to be at ground. In fact, this node is often referred to as a "virtual ground."

If there is a voltage (V_{in}) applied to the input resistor, it will set up a current (I1) through the resistor (R_{in}) so that

$$I1 = \frac{V_{in}}{R_{in}} \qquad \text{Eq. 1.3}$$

Since the input impedance of the op amp is infinite, no current will flow into the inverting input. Therefore, this same current (I1) must flow through the feedback resistor (R_{fb}). Since the amplifier will force the inverting terminal to ground, the output will assume a voltage (V_{out}) such that:

$$V_{out} = I1 * R_{fb} \qquad \text{Eq. 1-4}$$

Doing a little simple arithmetic we then can come to the conclusion of eq. 1.1:

$$\frac{V_o}{V_{in}} = A = -\frac{R_{fb}}{R_{in}} \qquad \text{Eq. 1-5}$$

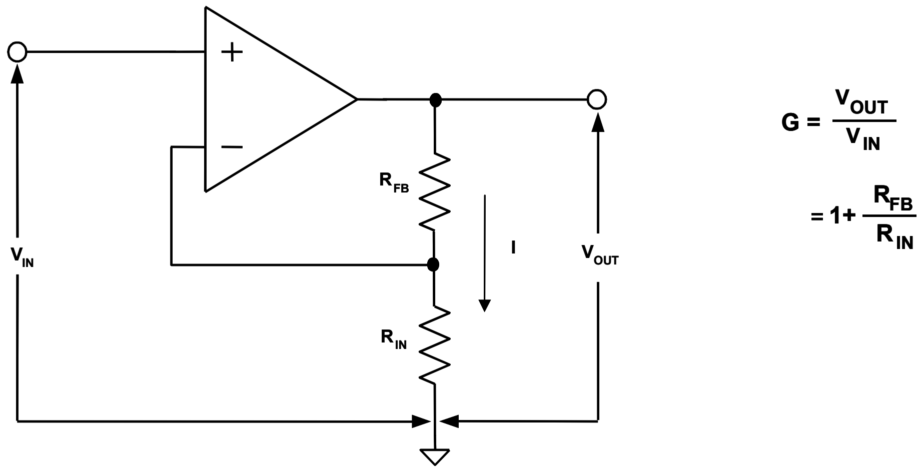


Figure 1.6: *Noninverting Amplifier gain*

Now we examine the noninverting case in more detail. Referring to Figure 1.6, the input voltage is applied to the noninverting terminal. The output voltage drives a voltage divider consisting of R_{fb} and R_{in}. The name "R_{in}," in this instance, is somewhat misleading since the resistor is not technically connected to the input, but we keep the same designation since it matches the inverting configuration, has become a de facto standard, anyway. The voltage at the inverting terminal (Va), which is at the junction of the two resistors, is

$$V_a = \frac{R_{in}}{R_{in} + R_{fb}} V_o \qquad \text{Eq. 1-6}$$

The negative feedback action of the op amp will force the differential voltage to 0 so:

$$V_a = V_{in} \qquad \text{Eq. 1-7}$$

Again applying a little simple arithmetic we end up with:

$$\frac{V_o}{V_{in}} = \frac{R_{fb}+R_{in}}{R_{in}} = 1 + \frac{R_{fb}}{R_{in}} \qquad \text{Eq. 1-8}$$

Which is what we specified in Eq. 1-2.

In all of the discussions above, we referred to the gain setting components as resistors. In fact, they are impedances, not just resistances. This allows us to build frequency dependent amplifiers. This will be covered in more detail in a later section.

Open-Loop Gain

The open-loop gain (usually referred to as A_{VOL}) is the gain of the amplifier without the feedback loop being closed, hence the name "open-loop." For a precision op amp this gain can be vary high, on the order of 160 dB or more. This is a gain of 100 million. This gain is flat from dc to what is referred to as the dominant pole. From there it falls off at 6 dB/octave or 20 dB/decade. (An octave is a doubling in frequency and a decade is X10 in frequency). This is referred to as a single-pole response. It will continue to fall at this rate until it hits another pole in the response. This 2nd pole will double the rate at which the open-loop gain falls, that is, to 12 dB/octave or 40 dB/decade. If the open-loop gain has dropped below 0 dB (unity gain) before it hits the 2nd pole, the op amp will be unconditional stable at any gain. This will be typically referred to as unity gain stable on the data sheet. If the 2nd pole is reached while the loop gain is greater than 1 (0 dB), then the amplifier may not be stable under some conditions.

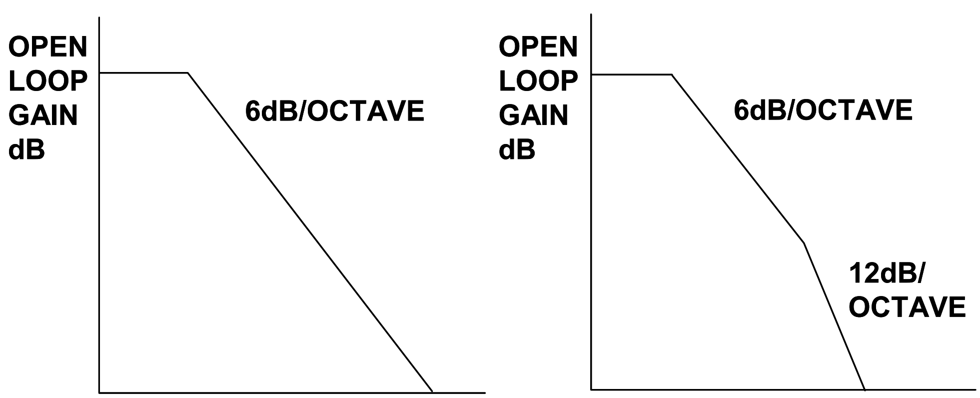


Figure 1.7: *Open-Loop Gain (Bode Plot)*

It is important to understand the differences between open-loop gain, closed-loop gain, loop gain, signal gain, and noise gain. They are similar in nature, interrelated, but different. We will discuss them all in detail.

The open-loop gain is not a precisely controlled spec. It can, and does, have a relatively large range and will be given in the specs as a typical number rather than a min/max number, in most cases. In some cases, typically high precision op amps, the spec will be a minimum.

In addition, the open-loop gain can change due to output voltage levels and loading. There is also some dependency on temperature. In general, these effects are of a very minor degree and can, in most cases, be ignored. In fact this nonlinearity is not always included in the data sheet for the part.

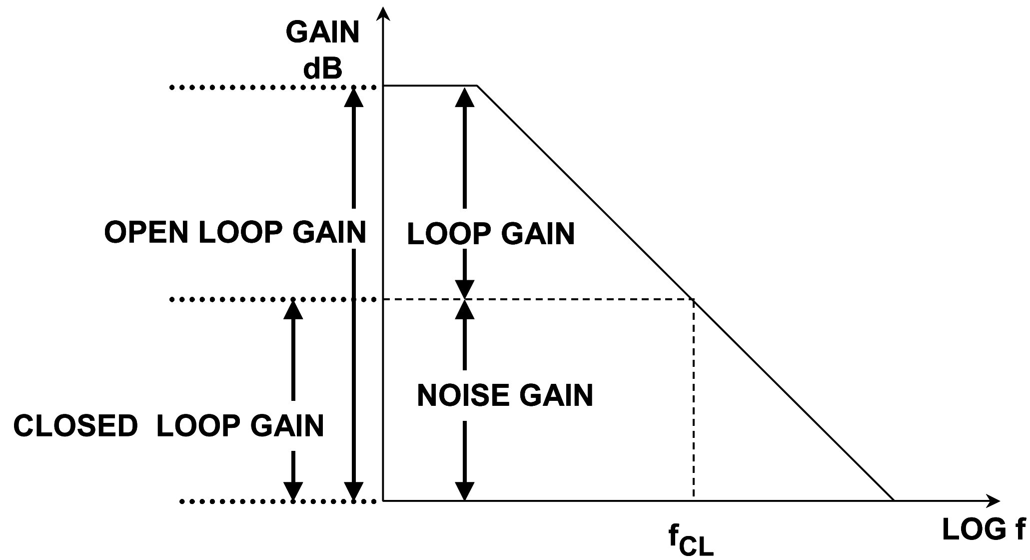
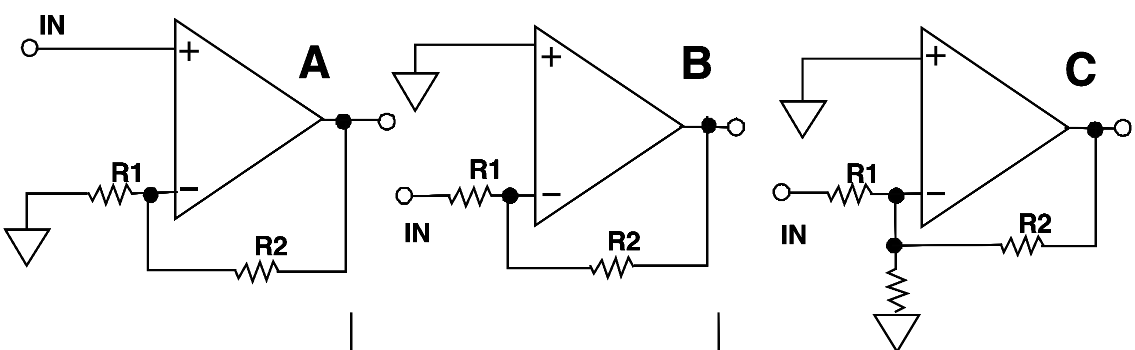


Figure 1.8: *Gain Definition*



A	B	C
Signal Gain = 1 + R2/R1	**Signal Gain =- R2/R1**	**Signal Gain =- R2/R1**
Noise Gain = 1 + R2/R1	**Noise Gain = 1 + R2/R1**	**Noise Gain = 1 +** $\frac{R2}{R1\|\|R3}$

- **Voltage Noise and Offset Voltage of the op amp are reflected to the output by the Noise Gain.**
- **Noise Gain, not Signal Gain, is relevant in assessing stability.**
- **Circuit C has unchanged Signal Gain, but higher Noise Gain, thus better stability, worse noise, and higher output offset voltage.**

Figure 1.9: *Noise Gain*

Gain-Bandwidth Product

The open-loop gain falls at 6 dB/octave. This means that if we double the frequency, the gain falls to half of what it was. Conversely, if the frequency is halved, the open-loop gain will double, as shown in Figure 1.8. This gives rise to what is known as the Gain-Bandwidth Product. If we multiply the open-loop gain by the frequency the product is always a constant. The caveat for this is that we have to be in the part of the curve that is falling at 6 dB/octave. This gives us a convenient figure of merit with which to determine if a particular op amp is useable in a particular application.

For example, if we have an application with which we require a gain of 10 and a bandwidth of 100 kHz, we require an op amp with, at least, a gain-bandwidth product of 1 MHz. This is a slight oversimplification. Because of the variability of the gain-bandwidth product, and the fact that at the location where the closed-loop gain intersects the open-loop gain the response is actually down 3 dB, a little margin should be included. In the application described above, an op amp with a gain-bandwidth product of 1 MHz would be marginal. A safety factor of at least 5 would be better insurance that the expected performance is achieved.

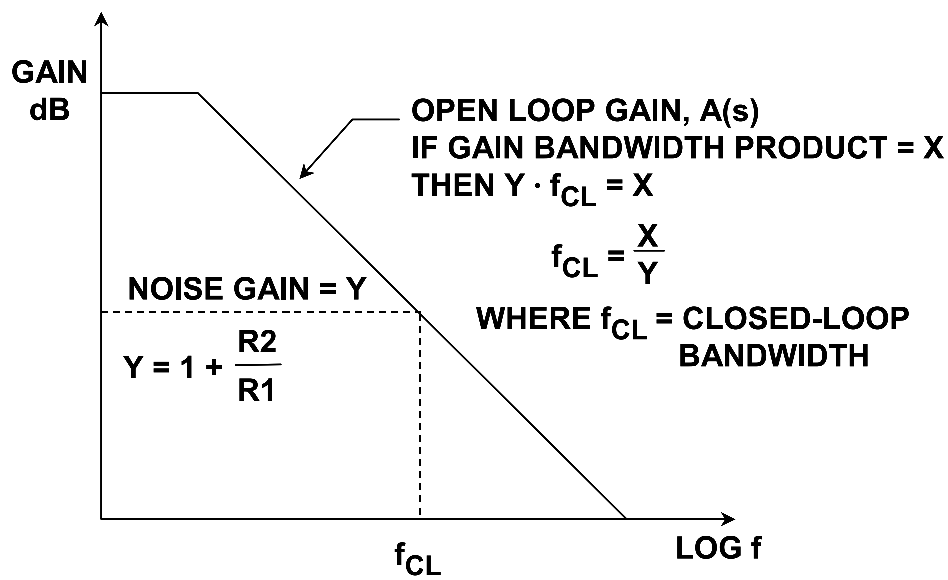


Figure 1.10: *Gain-Bandwidth Product*

Stability Criteria

Feedback theory states that the closed-loop gain must intersect the open-loop gain at a rate of 6 dB/octave (single-pole response) for the system to be stable. If the response is 12 dB/octave (2 pole response) the op amp will oscillate. The easiest way to think of this is that each pole adds 90° of phase shift. Two poles then means 180°, and 180° of phase shift turns negative feedback into positive feedback, which means oscillations.

The question could be then, why would you want an amplifier that is not unity gain stable? The answer is that for a given amplifier, the bandwidth can be increased if the amplifier is not unity gain stable. This is sometimes referred to as decompensated, But the gain criteria must be met. This criteria is that the closed-loop gain must intercept the open-loop gain at a slope of 6 dB/oct. (single-pole response). If not, the amplifier will oscillate.

As an example, compare the open-loop gain graphs in Figures 1.11, 1.12, 1.13. The three parts shown, the AD847, AD848, and AD849, are basically the same part. The AD847 is unity gain stable. The AD848 is stable for gains of 2 or more. The AD849 is stable for a gain of 10 or more. You can see from this that the AD849 is much wider bandwidth. So, if you are going to run at high gain, you get wider bandwidth.

There are a couple of tricks that you can use to help out in this regard in the circuit tricks section, which we will cover later.

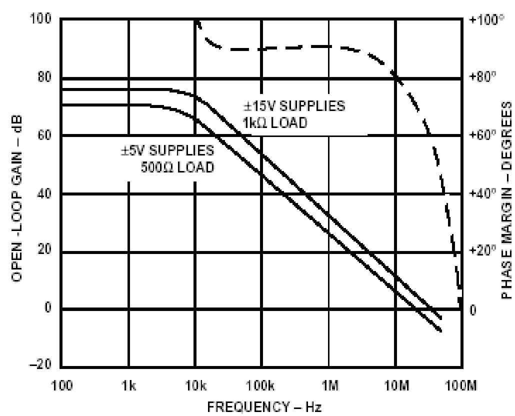


Figure 1.11: *AD847 Open Loop Gain*

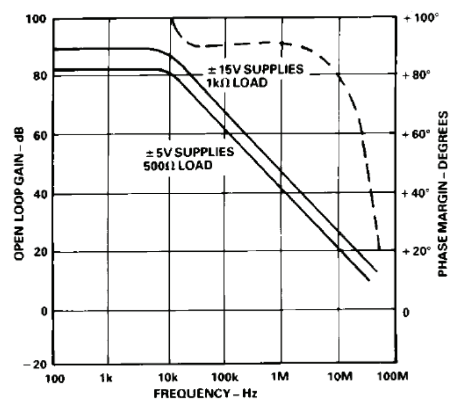


Figure 1.12: *AD848 Open Loop Gain*

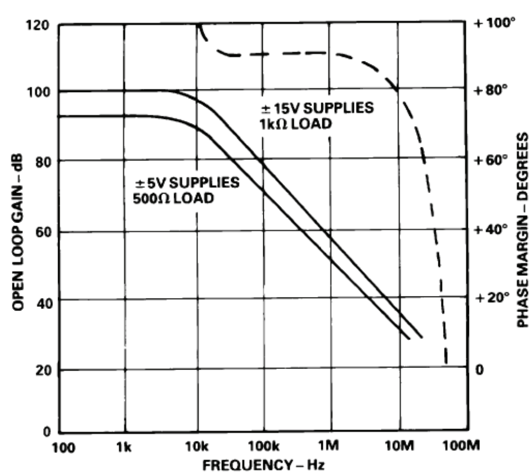


Figure 1.13: *AD849 Open-Loop Gain*

Phase Margin

One measure of stability is phase margin. Just as the amplitude response doesn't stay flat and then change instantaneously, the phase will also change gradually, starting as much as a decade back from the corner frequency. Phase margin is the amount of phase shift that is left until you hit 180° measured at the unity gain point.

The manifestation of low phase margin is an increase in the peaking of the output just before the close-loop gain intersects the open-loop gain. See Figure 1.14.

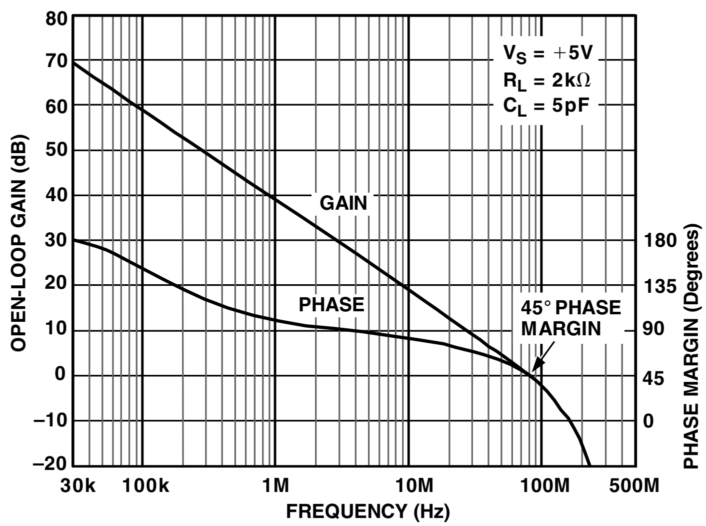


***Figure 1.14**: AD8051 Phase Margin*

Closed-Loop Gain

This, of course, is the gain of the amplifier with the feedback loop closed, as opposed the open-loop gain, which is the gain with the feedback loop opened. It has two forms, signal gain and noise gain. These are described and differentiated below.

The expression for the gain of a closed-loop amplifier involves the open-loop gain. If G is the actual gain, N_G is the noise gain (see below), and A_{VOL} is the open-loop gain of the amplifier, then:

$$G = N_G - \frac{N_G^2}{N_G + A_{VOL}} = \frac{N_G}{\frac{N_G}{A_{VOL}} + 1} \qquad \text{Eq. 1-9}$$

From this you can see that if the open-loop gain is very high, which it typically is, the closed-loop gain of the circuit is simply the noise gain.

Signal Gain

This is the gain applied to the input signal, with the feedback loop connected. In the basic operation section above, when we talked about the gain of the inverting and noninverting circuits, we were actually more correctly talking about the closed-loop signal gain. It can be inverting or noninverting. It can even be less than unity for the inverting case. Signal gain is the gain that we are primarily interested in when designing circuits.

The signal gain for an inverting amplifier stage is:

$$A = -\frac{R_{fb}}{R_{in}} \qquad \text{Eq. 1-10}$$

and for a noninverting amplifier it is:

$$A = 1 + \frac{R_{fb}}{R_{in}} \qquad \text{Eq. 1-11}$$

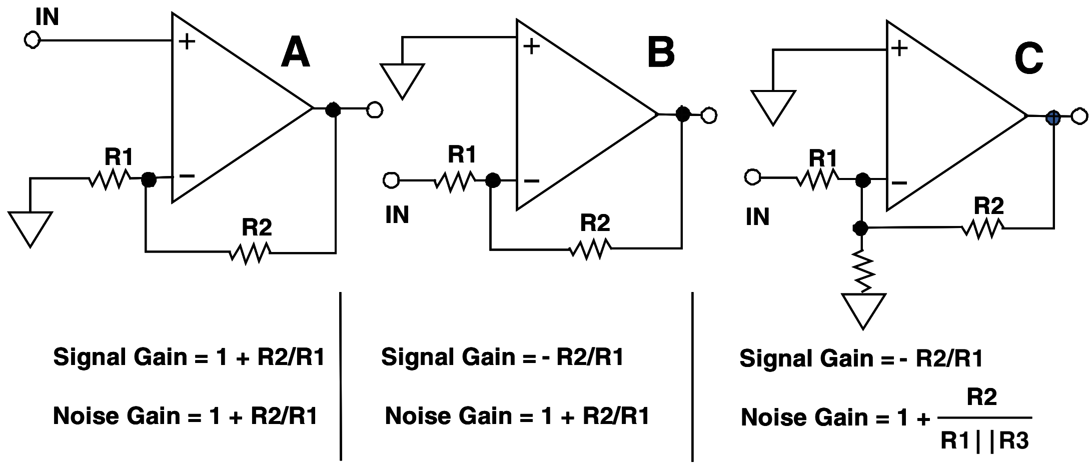
Noise Gain

Noise gain is the gain applied to a noise source in series with an op amp input. It is also the gain applied to an offset voltage. The noise gain is equal to:

$$A = 1 + \frac{R_{fb}}{R_{in}} \qquad \text{Eq. 1-12}$$

Noise gain is equal to the signal gain of a noninverting amp. It is the same for either an inverting or noninverting stage.

It is the noise gain that is used to determine stability. It is also the closed-loop gain that is used in Bode plots. Remember that even though we used resistances in the equation for noise gain, they are actually impedances.



- **Voltage Noise and Offset Voltage of the op amp are reflected tothe output by the Noise Gain.**
- **Noise Gain, not Signal Gain, is relevant in assessing stability.**
- **Circuit C has unchanged Signal Gain, but higher Noise Gain, thus better stability, worse noise, and higher output offset voltage.**

Figure 1.15: *Noise Gain*

Loop Gain

The difference between the open-loop gain and the closed-loop gain is known as the loop gain. This is useful information because it gives you the amount of negative feedback that can apply to the amplifier system.

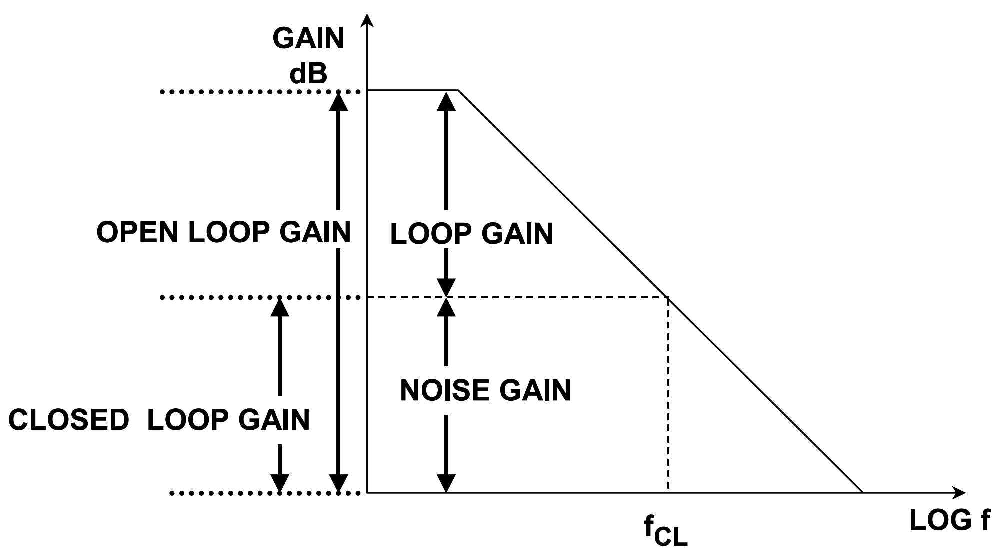


Figure 1.16: *Gain Definitions*

Bode Plot

The plotting of open-loop gain vs. frequency on a log-log scale gives is what is known as a Bode (pronounced *boh dee*) plot. It is one of the primary tools in evaluating whether a particular op amp is suitable for a particular application.

If you plot the open-loop gain and then the noise gain on a Bode plot, the point where they intersect will determine the maximum closed-loop bandwidth of the amplifier system. This is commonly referred to as the closed-loop frequency (F_{CL}). Remember that the true response at the intersection is actually 3 dB down. One octave above and one octave below F_{CL} the difference between the asymptotic response and the real response will be less than 1 dB.

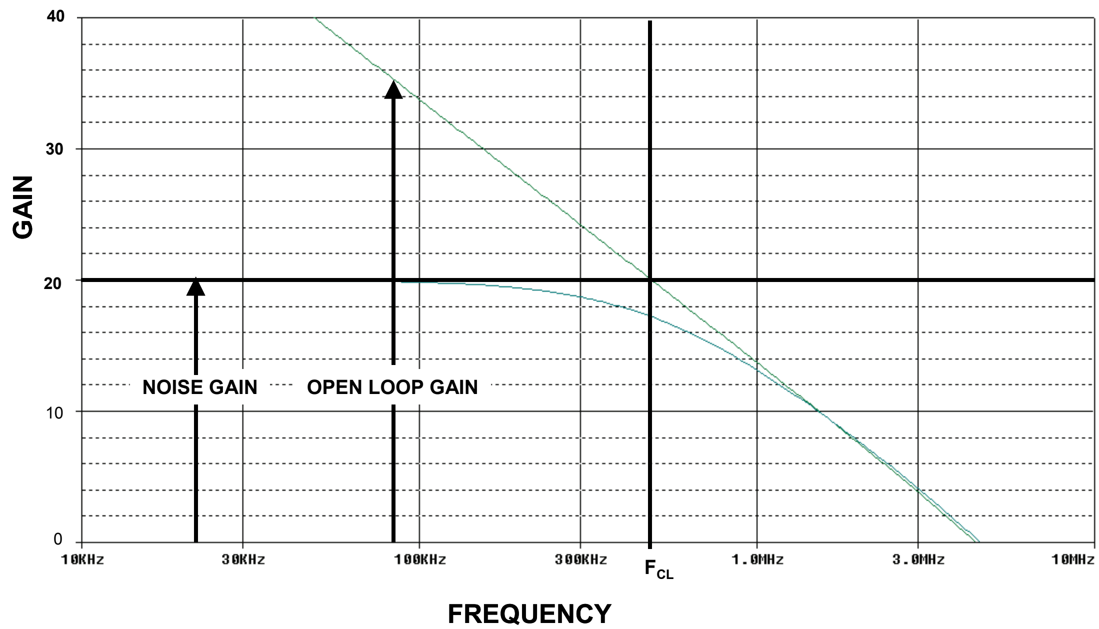


Figure 1.17: *Asymptotic Response*

The Bode plot is also useful in determining stability. As stated above, if the closed-loop gain (noise gain) intersects the open-loop gain at a slope of greater than 6 dB/octave (20 dB/decade) the amplifier may be unstable (depending on the phase margin).

Current Feedback (CFB) Model

There is a type of amplifier that have several advantages over the standard VFB amplifier at high frequencies. They are called current feedback (CFB) or sometimes transimpedance amps. There is a possible point of confusion since the current–to-voltage (I/V) converters commonly found in photodiode applications are also referred to as transimpedance amps. Schematically CFB op amps look similar to standard VFB amps, but there are several key differences.

The input structure of the CFB is different from the VFB. While we are trying not to get into the internal structures of the op amps, in this case, a simple diagram is in order. See Figure 1.18. The mechanism of feedback is also different, hence the names. But again, the exact mechanism is beyond what we want to cover here. In most cases if the differences are noted, and the attendant limitations observed, the basic operation of both types of amplifiers can be thought of as the same. The gain equations are the same as for a VFB amp, with an important limitation as noted in the next section.

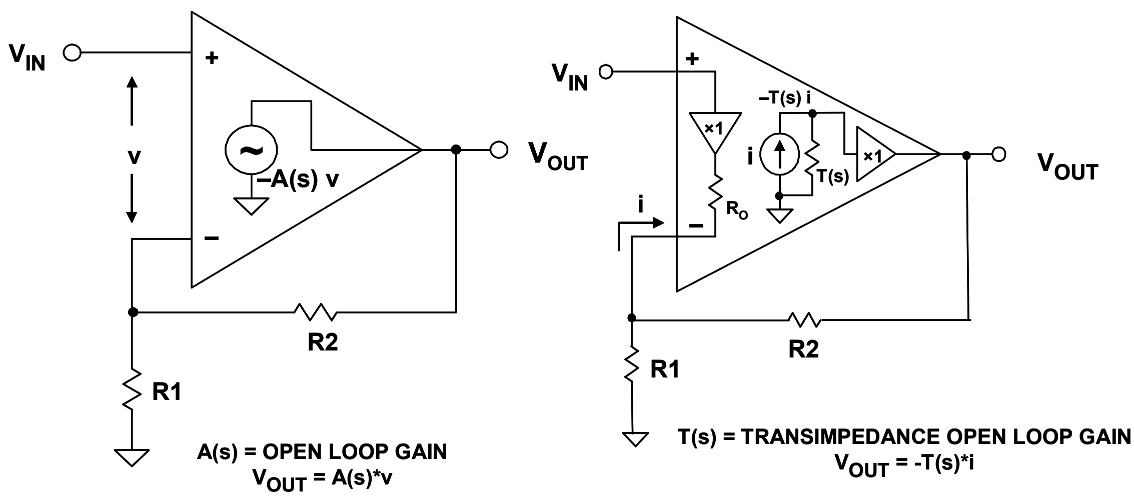
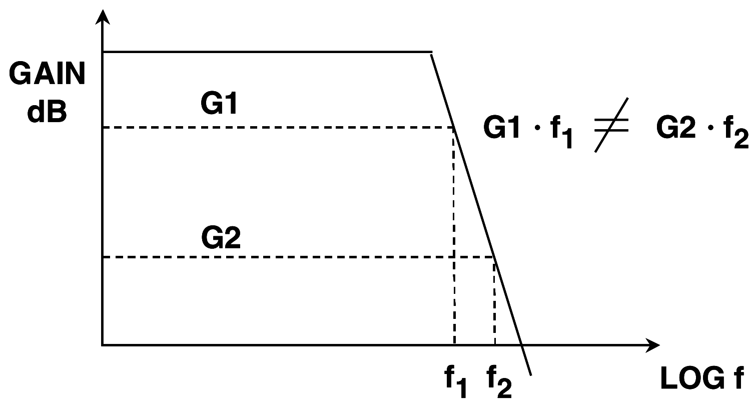


Figure 1.18: *VFB and CFB Amplifiers*

Difference from VFB

One primary difference between the CFB and VFB amps is that there is not a Gain-Bandwidth product. While there is a change in bandwidth with gain, it is not even close to the 6 dB/octave that we see with VFB. See Figure 1.19. Also, a major limitation that the value of the feedback resistor determines the bandwidth, working with the internal capacitance of the op amp. For every CFB op amp there is a recommended value of feedback resistor for maximum bandwidth. If you increase the value of the resistor, you reduce the bandwidth. If you use a lower value of resistor the phase margin is reduced and the amplifier could become unstable. This optimum value of resistor is different for different operational conditions. For instance, the value will change for different packages, for example, SOIC vs. DIP (see Figure 1.20).



- FEEDBACK RESISTOR FIXED FOR OPTIMUM PERFORMANCE. LARGER VALUES REDUCE BANDWIDTH, SMALLER VALUES MAY CAUSE INSTABILITY.
- FOR FIXED FEEDBACK RESISTOR, CHANGING GAIN HAS LITTLE EFFECT ON BANDWIDTH.
- CURRENT FEEDBACK OP AMPS DO NOT HAVE A FIXED GAIN-BANDWIDTH PRODUCT.

Figure 1.19: *Current Feedback Amplifier Frequency Response*

	AD8001AN (PDIP) Gain					AD8001AR (SOIC) Gain					AD8001ART (SOT-23-5) Gain				
Component	–1	+1	+2	+10	+100	–1	+1	+2	+10	+100	–1	+1	+2	+10	+100
R_F (Ω)	649	1050	750	470	1000	604	953	681	470	1000	845	1000	768	470	1000
R_G (Ω)	649		750	51	10	604		681	51	10	845		768	51	10
R_O (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_S (Ω)	0					0					0				
R_T (Nominal) (Ω)	54.9	49.9	49.9	49.9	49.9	54.9	49.9	49.9	49.9	49.9	54.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	340	880	460	260	20	370	710	440	260	20	240	795	380	260	20
0.1 db Flatness (MHz)	105	70	105			130	100	120			110	300	145		

Figure 1.20: *AD8001 Optimum Feedback Resistor vs. Package*

Also, a CFB amplifier should not have a capacitor in the feedback loop. If a capacitor is used in the feedback loop, it reduces the feedback impedance as frequency is increased, which will cause the op amp to oscillate. You need to be careful of stray capacitances around the inverting input of the op amp for the same reason.

A common error in using a current feedback op amp is to short the inverting input directly to the output in an attempt to build a unity gain voltage follower (buffer). This circuit will oscillate. Obviously, in this case, the feedback resistor value will be less the recommended value. The circuit is perfectly stable if the recommended feedback resistor of the correct value is used in place of the short.

Another difference between the VFB and CFB amplifiers is that the inverting input of the CFB amp is low impedance. By low we mean typically 50 Ω to 100 Ω. Therefore there isn't the inherent balance between the inputs that the VFB circuit shows.

Slew rate performance is also enhanced by the CFB topology. The current that is available to charge the internal compensation capacitor is dynamic. It is not limited to any fixed value as is often the case in VFB topologies. With a step input or overload condition, the current is increased (current-on-demand) until the overdriven condition is removed. The basic current feedback amplifier has no fundamental slew-rate limit. Limits only come about from parasitic internal capacitances and many strides have been made to reduce their effects.

The combination of higher bandwidths and slew rate allows CFB devices to have good distortion performance while doing so at a lower power.

The distortion of an amplifier is impacted by the open loop distortion of the amplifier and the loop gain of the closed-loop circuit. The amount of open-loop distortion contributed by a CFB amplifier is small due to the basic symmetry of the internal topology. Speed is the other main contributor to distortion. In most configurations, a CFB amplifier has a greater bandwidth than its VFB counterpart. So at a given signal frequency, the faster part has greater loop-gain and therefore lower distortion.

How to Choose Between CFB and VFB

The application advantages of current feedback and voltage feedback differ. In many applications, the differences between CFB and VFB are not readily apparent. Today's CFB and VFB amplifiers have comparable performance, but there are certain unique advantages associated with each topology. Voltage feedback allows freedom of choice of the feedback resistor (or impedance) at the expense of sacrificing bandwidth for gain. Current feedback maintains high bandwidth over a wide range of gains at the cost of limiting the choices in the feedback impedance.

In general, VFB amplifiers offer:

- Lower Noise
- Better DC Performance
- Feedback Component Freedom

while CFB amplifiers offer:

- Faster Slew Rates
- Lower Distortion
- Feedback Component Restrictions

Supply Voltages

Historically the supply voltage for op amps was typically ±15 V. The operational input and output range was on the order of ±10 V. But there was no hard requirement for these levels. Typically the maximum supply was ±18 V. The lower limit was set by the internal structures. You could typically go within 1.5 or 2 V of either supply rail, so you could reasonably go down to ±8 V supplies or so and still have a reasonable dynamic range.

Lately though, there has been a trend toward lower supply voltages. This has happened for a couple of reasons.

First, high speed circuits typically have a lower full scale range. The principal reason for this is the amplifiers ability to swing large voltages. All amplifiers have a slew rate limit, which is expressed as so many volts per microsecond. So if you want to go faster, your voltage range must be reduced, all other things being equal. A second reason is that to limit the effects of stray capacitance on the circuits, you need to reduce their impedance levels. Driving lower impedances increases the demands on the output stage, and on the power dissipation abilities of the amplifier package. Lower voltage swings require lower currents to be supplied, thereby lowering the dissipation of the package.

A second reason is that as the speed of the devices inside the amplifier increased, the geometries of these devices tend to become smaller. The smaller geometries typically mean reduced breakdown voltages for these parts. Since the breakdown voltages were getting lower, the supply voltages had to follow. Today high speed op amps typically have breakdown voltage of ±7 V, and so the supplies are typically ±5 V, or even lower.

In some cases, operation on batteries established a requirement for lower supply voltages. Lower supplies would then lessen the number of batteries, which, in turn, reduced the size, weight and cost of the end product.

At the same time there was a movement towards single supply systems. Instead of the typical plus and minus supplies, the op amps operate on a single positive supply and ground, the ground then becoming the negative supply.

Single Supply Considerations

There is nothing in the circuitry of the op amp that requires ground. In fact, instead of a bipolar (+ and −) supply of ±15 V you could just as easily use a single supply of +30 V (ground being the negative supply), as long as the rest of the circuit was biased correctly so that the signal was within the common mode range of op amp. Or, for that matter, the supply could just as easily be –30 V (ground being the most positive supply).

When you combine the single supply operation with reduced supply voltages you can run into problems. The standard topology for op amps uses a NPN differential pair (see Figure 1.21) for the input and emitter followers (see Figure 1.24) for the output stage. Neither of these circuits will let you run "rail-to-rail," that is from one supply to the other. Some circuit modifications are required.

The first of these modifications was the use of a PNP differential input See Figure 1.22. One of the first examples of this input configuration was the LM324. This configuration allowed the input to get close to the negative rail (ground). It could not, however, go to the positive rail. But in many systems, especially mixed signal systems that were predominately digital, this was enough. In terms of precision, the 324 is not a stellar performer.

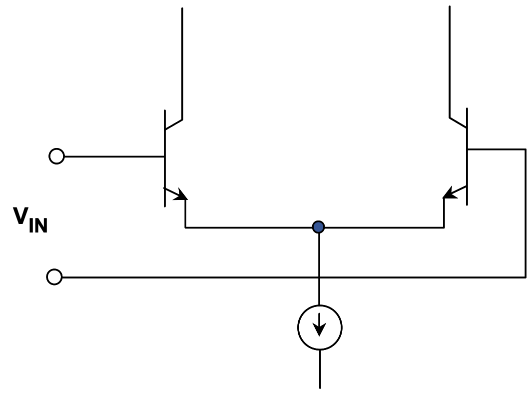


Figure 1.21: *Standard Input Stage (Differential Pair)*

The NPN input cannot swing to ground. The PNP input can not swing to the positive rail. The next modification was to use a dual input. Here a NPN differential pair is combined with a PNP differential pair. See Figure 1.23. Over most of the common-mode range of the input both pairs are active. As one rail or the other is approached, one of the inputs turns off. The NPN pair swings to the upper rail and the PNP pair swings to the lower rail.

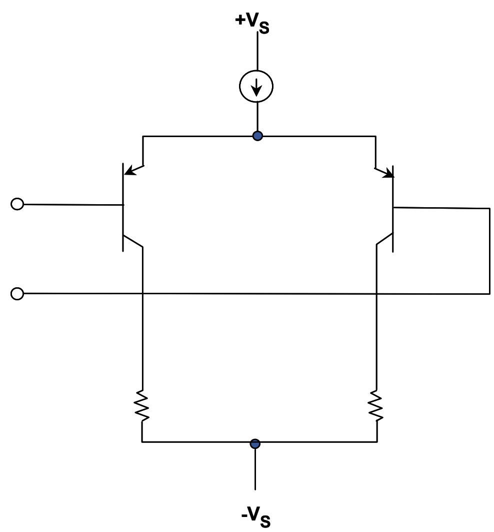


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Figure 1.22: *PNP Input Stage*

It should be noted here that the op amp parameters which primarily depend on the input structure (bias current, for instance) will vary with the common-mode voltage on the inputs. The bias currents will even change direction as the front end transitions from the NPN stage to the PNP stage.

Another difference is the output stage. The standard output stage, which is a complimentary emitter follower (common collector) configuration (Figure 1.24), is typically replaced by a common emitter circuit. This allows the output to swing close to the rails. The exact level is set by the V_{CEsat} of the output transistors, which is, in turn, dependent on the output current levels. The only real disadvantage to this arrangement is that the output impedance of the common emitter circuit is higher than the common collector circuit. Most of the time this is not really an issue, since negative feedback reduces the output impedance proportional to the amount of loop gain. Where it becomes an issue is that as the loop gain falls this higher output impedance is more susceptible to the effects of capacitate loading.

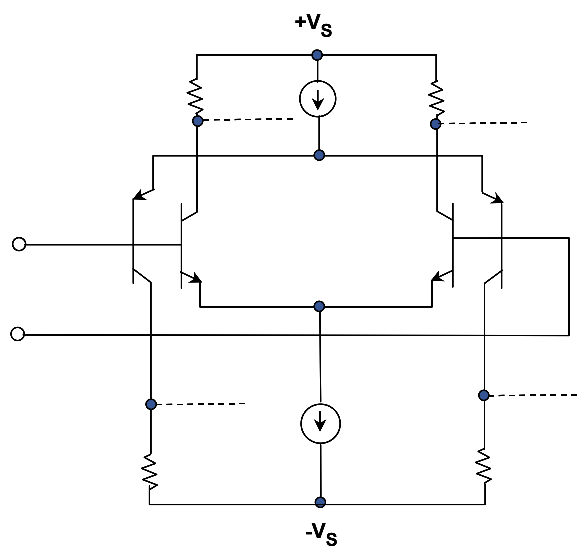


Figure 1.23: *Compound input Stage*

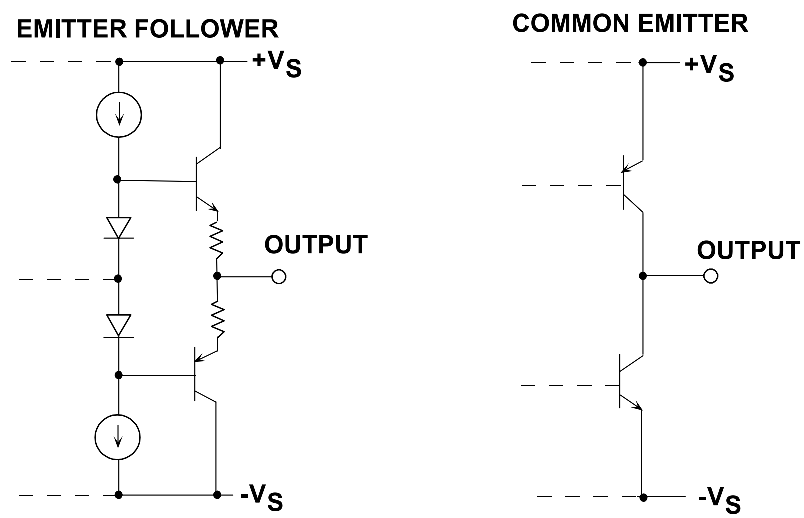


Figure 1.24: *Output Stages. Emitter Follower for Standard Configuration And Common Emitter for "Rail-to-Rail" Configuration*

Circuit Design Considerations for Single Supply Systems

Many waveforms are bipolar in nature. This means that the signal naturally swings around the reference level, which is typically ground. This obviously won't work in a single-supply environment. What is required is to ac couple the signals.

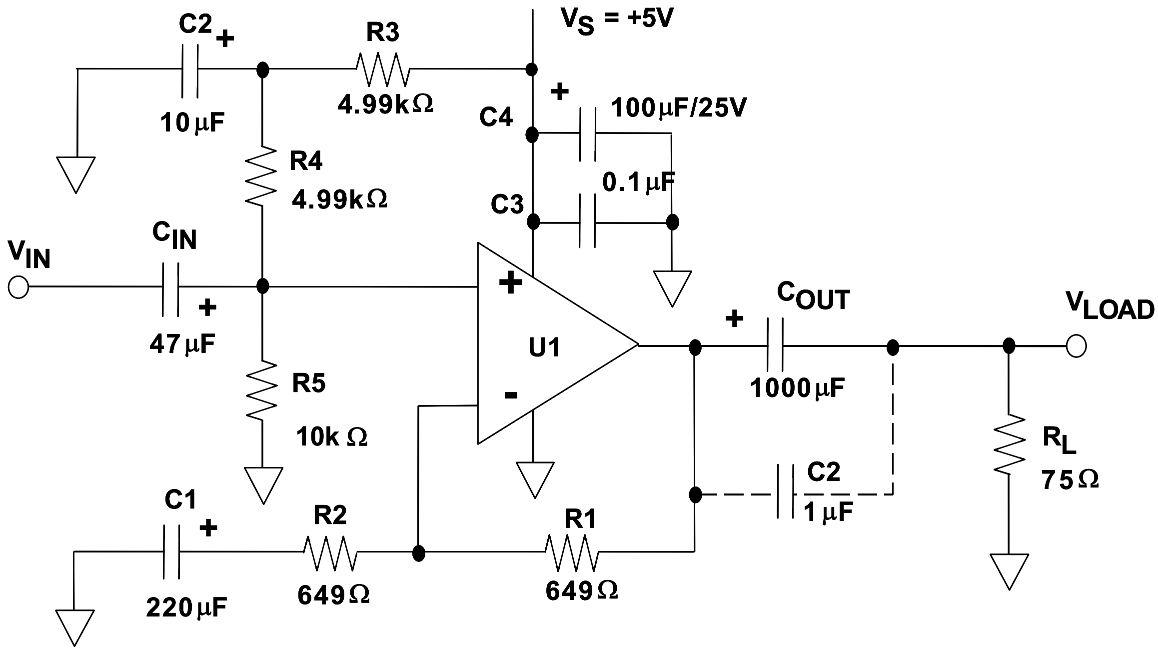


Figure 1.25: *Single Supply Biasing*

AC coupling is simply applying a high-pass filter and establishing a new reference level typically somewhere around the center of the supply voltage range. See Figure 1.25. The series capacitor will block the dc component of the input signal. The corner frequency (the frequency at which the response is 3 dB down from the midband level) is determined by the value of the components:

$$f_C = \frac{1}{2\pi\, R_{EQ}\, C} \qquad \text{Eq. 1-14}$$

where:

$$R_{EQ} = \frac{R4\ R5}{R4 + R5} \qquad \text{Eq. 1-15}$$

It should be noted that if multiple sections are ac coupled, each section will be 3 dB down at the corner frequency. So if there are two sections with the same corner frequency, the total response will be 6 dB down, three sections would be 9 dB down, etc. This should be taken into account so that the overall response of the system will be adequate. Also keep in mind that the amplitude response starts to roll off a decade, or more, from the corner frequency.

The AC coupling of arbitrary waveforms can actually introduce problems which don't exist at all in dc coupled systems. These problems have to do with the waveform duty cycle, and are particularly acute with signals which approach the rails, as they can in low supply voltage systems which are ac coupled.

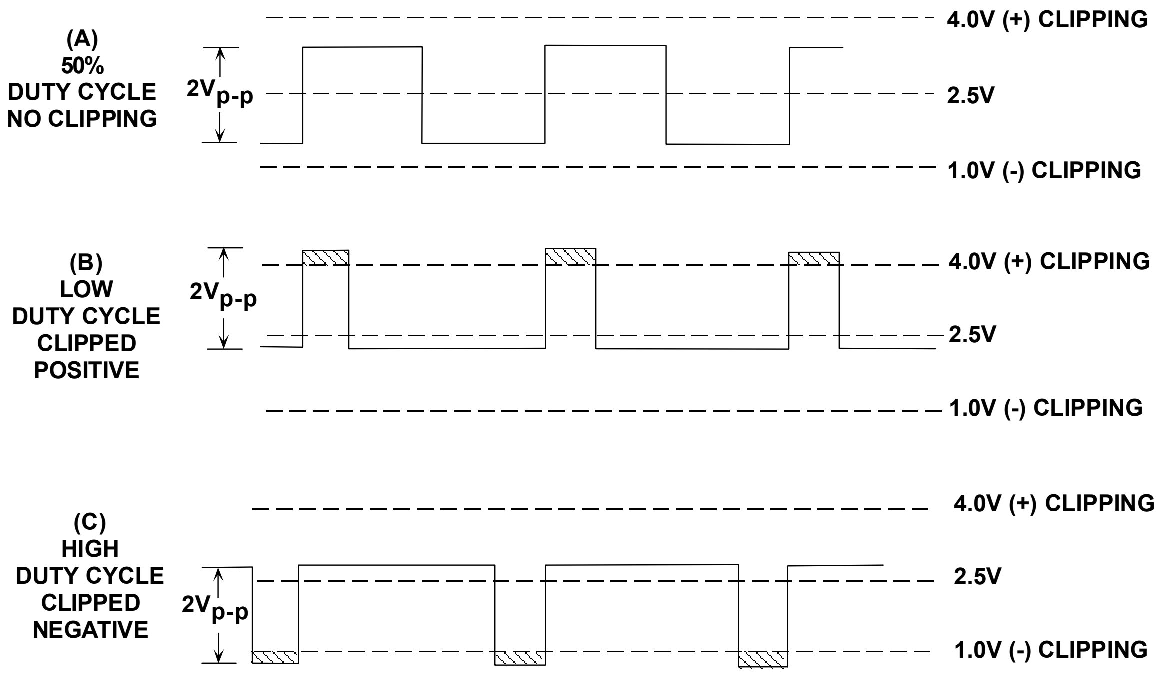


Fig. 1.26: *Headroom Issues with Single-Supply Biasing*

In an amplifier circuit such as that of Figure 1.25, the output bias point will be equal to the dc bias as applied to the op amp's (+) input. For a symmetric (50% duty cycle) waveform of a 2 V p-p output level, the output signal will swing symmetrically about the bias point, or nominally 2.5 V ±1 V (using the values give in Fig. 1.25). If, however, the pulsed waveform is of a very high (or low) duty cycle, the ac averaging effect of C_{IN} and R4 || R5 will shift the effective peak level either high or low, dependent upon the duty cycle. This phenomenon has the net effect of reducing the working headroom of the amplifier, and is illustrated in Figure 1.26.

In Figure 1.26 (A), an example of a 50% duty cycle square wave of about 2 V p-p level is shown, with the signal swing biased symmetrically between the upper and lower clip points of a 5 V supply amplifier. This amplifier, for example, (an AD817 biased similarly to Figure 1.25) can only swing to the limited dc levels as marked, about 1 V from either rail. In cases (B) and (C), the duty cycle of the input waveform is adjusted to both low and high duty cycle extremes *while maintaining the same peak-to-peak input level*. At the amplifier output, the waveform is seen to clip either negative or positive, in (B) and (C), respectively.

Rail-to-Rail

When the input and/or the output can swing very close to the supply rails, it is referred to as "rail-to-rail." There is no industry standard definition for this. At Analog Devices we have defined this at swinging to within 100 mV of either rail. For the output this is driving a standard load, since the actual maximum output level will depend on the output current. Note that not all amplifiers that are touted as single supply are rail-to-rail. And not all rail-to-rail amplifiers are rail-to-rail on input and output. It could be one or the other, or both, or neither. The bottom line is that you must read the data sheet. In no case can the output actually swing completely to the rails.

Phase Reversal

There is an interesting phenomenon that can occur when the common-mode range of the op amp is exceeded. Some internal nodes can turn off and the output will be pulled to the opposite rail until the input comes back into the operational range. Many modern designs take steps to eliminate this problem. Many times this is called out in the bullets on the cover page. See Figure 1.27. Phase reversal is most common when the amplifier us in the follower mode.

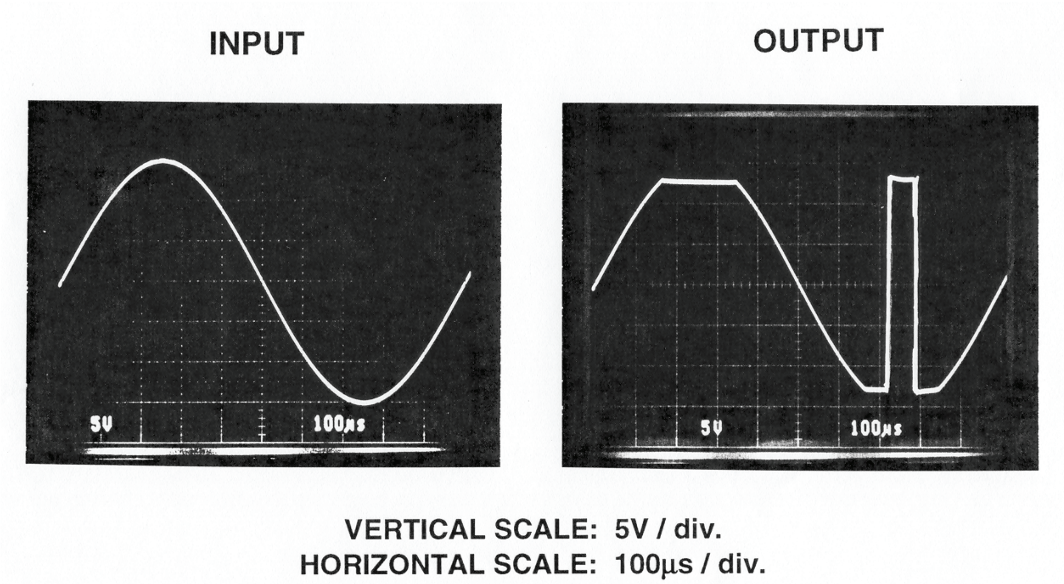


Figure 1.27: *Phase Reversal*

Low Power and Micropower

Along with the trend toward single supplies is the trend toward lower quiescent power. This is the power used by the amp itself. We have arrived at the point where there are whole amplifiers that can operate on the bias current of the 741.

However, low power involves some trade-offs.

One way to lower the quiescent power is to lower the bias current in the output stage. This amounts to moving more towards class B operation (and away from class A). The result of this is that the distortion of the output stage will tend to rise.

Another approach to lower power is to lower the standing current of the input stage. The result of this is to reduce the bandwidth and to increase the noise.

While the term “low power” can mean vastly different things depending on the application. At Analog Devices we have set a definition for op amps. Low power means the quiescent current is less than 1 mA per amplifier. Micropower is defined as having a quiescent current less than 100 μA per amplifier. As was the case with “rail-to-rail,” this is not an industry wide definition.

Processes

The vast majority of modern op amps are built using bipolar transistors.

Occasionally a junction FET is used for the input stage. This is commonly referred to as a Bi-Fet (for **Bi**polar-**FET**). This is typically done to increase the input impedance of the op amp, or conversely, to lower the input bias currents. The FET devices are typically used only in the input stage. For single-supply applications, the FETs can be either N-channel or P-channel. This allows input ranges extending to the negative rail and positive rail, respectively.

CMOS processing is also used for op amps. While historically CMOS hasn’t been that attractive a process for linear amplifiers, process and circuit design have progressed to the point that quite reasonable performance can be obtained from CMOS op amps.

One particularly attractive aspect of using CMOS is that it lends itself easily to mixed mode (analog and digital) applications. Some examples of this are the Digi-Trim and chopper stabilized op amps.

“Digi-Trim” is a technique that allows the offset voltage of op amps to be adjusted out at final test. This replaces the more common techniques of zener-zapping or laser trimming, which must be done at the wafer level. The problem with trimming at the wafer level is that there are certain shifts in parameters due to packaging, etc., that take place after the trimming is done. While the shift in parameters is fairly well understood and some of the shift can be anticipated, trimming at final test is a very attractive alternative. The Digi-trim amplifiers basically incorporate a small DAC used to adjust the offset.

Chopper stabilized amplifiers use techniques to adjust out the offset continuously. This is accomplished by using a dc precision amp to adjust the offset of a wider bandwidth amp. The dc precision amp is switched between a reference node (usually ground) and the input. This then is used to adjust the offset of the “main” amp.

Digi-Trim and chopper stabilized amplifiers are covered in more detail in Chapter 2.

Effects of Overdrive on Op Amp Inputs

There are several important points to be considered about the effects of overdrive on op amp inputs. The first is, obviously, damage. The data sheet of an op amp will give "absolute maximum" input ratings for the device. These are typically expressed in terms of the supply voltage but, unless the data sheet expressly says otherwise, maximum ratings apply only when the supplies are present, and the input voltages should be held near zero in the absence of supplies.

A common type of rating expresses the maximum input voltage in terms of the supply, $V_{SS} \pm 0.3$ V. In effect, neither input may go more than 0.3 V outside the supply rails, whether they are on or off. If current is limited to 5 mA or less, it generally does not matter if inputs do go outside ±0.3 V *when the supply is off* (provided that no base-emitter reverse breakdown occurs). Problems may arise if the input is outside this range when the supplies are turned on as this can turn on parasitic SCRs in the device structure and destroy it within microseconds. This condition is called *latch-up*, and is much more common in digital CMOS than in linear processes used for op amps. If a device is known to be sensitive to latch-up, avoid the possibility of signals appearing before supplies are established. (When signals come from other circuitry using the same supply there is rarely, if ever, a problem.) Fortunately, most modern IC op amps are relatively insensitive to latch-up.

Input stage damage will be limited if the input current is limited. The standard rule-of-thumb is to limit the current to 5 mA. Reverse bias junction breakdown should be avoided at all cost. Note that the common-mode and differential-mode specs may be different. Also, not all overvoltage damage is catastrophic. Small degradation of some of the specs can occur with constant abuse by overvoltaging the op amp.

A common method of keeping the signal within the supplies is to clamp the signal to the supplies with Schottky diodes as shown in Figure 1.28. This does not, in fact, limit the signal to ±0.3 V at all temperatures, but if the Schottky diodes are at the same temperature as the op amp, they will limit the voltage to a safe level, even if they do not limit it at all times to within the data sheet rating. This is easily accomplished if overvoltage is only possible at turn-on, and diodes and op amp will always be at the same temperature then. If the op amp may still be warm when it is repowered, however, steps must be taken to ensure that diodes and op amp are at the same temperature when this occurs.

Many op amps have limited common-mode or differential input voltage ratings. Limits on common-mode are usually due to complex structures in very fast op amps and vary from device to device. Limits on differential input avoid a damaging reverse breakdown of the input transistors (especially super-beta transistors). This damage can occur even at very low current levels. Limits on differential inputs may also be needed to prevent internal protective circuitry from over-heating at high current levels when it is conducting to prevent breakdowns—in this case, a few hundred microseconds of overvoltage may do no harm. One should never exceed any "absolute maximum" rating, but engineers should understand the reasons for the rating so that they can make realistic assessments of the risk of permanent damage should the unexpected occur.

If an op amp is overdriven *within* its ratings, no permanent damage should occur, but some of the internal stages may saturate. Recovery from saturation is generally slow, except for certain "clamped" op amps specifically designed for fast over-drive recovery. Over-driven amplifiers may therefore be unexpectedly slow.

Because of this reduction in speed with saturation (and also output stages unsuited to driving logic), it is generally unwise to use an op amp as a comparator. Nevertheless, there are sometimes reasons why op amps may be used as comparators. The subject is discussed in Reference 3 and Chapter 2.

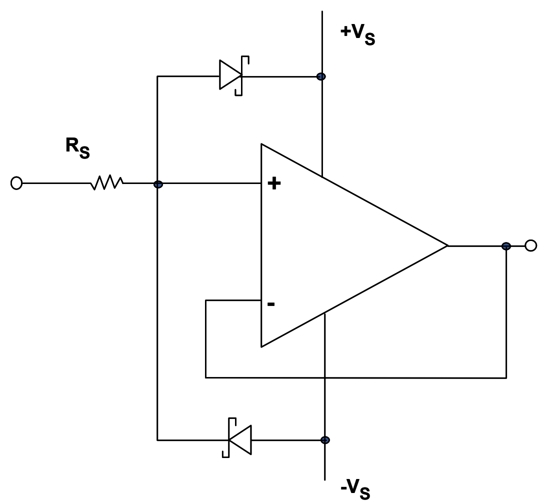


Figure 1.28: *Input Overvoltage Protection*

SECTION 2: OP AMP SPECIFICATIONS

Introduction

In this section, we will discuss basic op amp specs. The importance of any of these specs depends, of course, upon the application. For instance, offset voltage, offset voltage drift, and open-loop gain (dc specs) are very critical in precision sensor signal conditioning circuits, but may not be as important in high speed applications where bandwidth, slew rate, and distortion (ac specs) are typically the key specs.

Most op amp specs are largely topology independent. However, although voltage feedback (VFB) and current feedback (CFB) op amps have similar error terms and specs, the application of each part warrants discussing some of the specs separately. In the following discussions, this will be done where significant differences exist.

It should be noted that not all of these specs will necessarily appear on all data sheets. As the performance of the op amp increases, the more specs it has and the tighter the specs become. Also keep in mind the difference between typical and min/max. At Analog Devices, a spec that is min/max is guaranteed by test. Typ specs are generally not tested.

DC Specifications

Open-Loop Gain

The open-loop gain is the gain of the amplifier when the feedback loop is not closed. It is generally measured, however, with the feedback loop closed, although at a very large gain. In an ideal op amp, it is infinite with infinite bandwidth. In practice, it is very large (up to 160 dB) at dc. At some frequency (the dominant pole) it starts to fall at 6 dB/octave or 20 dB/decade. (An octave is a doubling in frequency and a decade is ×10 in frequency). This is referred to as a single-pole response. The dominant pole frequency will range from in the neighborhood of 10 Hz for some high precision amps to several kHz for some high speed amps. It will continue to fall at this rate until it reaches another pole in the response. This 2nd pole will double the rate at which the open-loop gain falls, that is to 12 dB/octave or 40 dB/decade. If the open-loop gain has gone below 0 dB (unity gain) before the amp hits the 2nd pole, the op amp will be unconditionally stable at any gain. This will be referred to as unity gain stable on the data sheet. If the 2nd pole is reached while the loop gain is greater than 1 (0 db), then the amplifier may not be stable under some conditions.

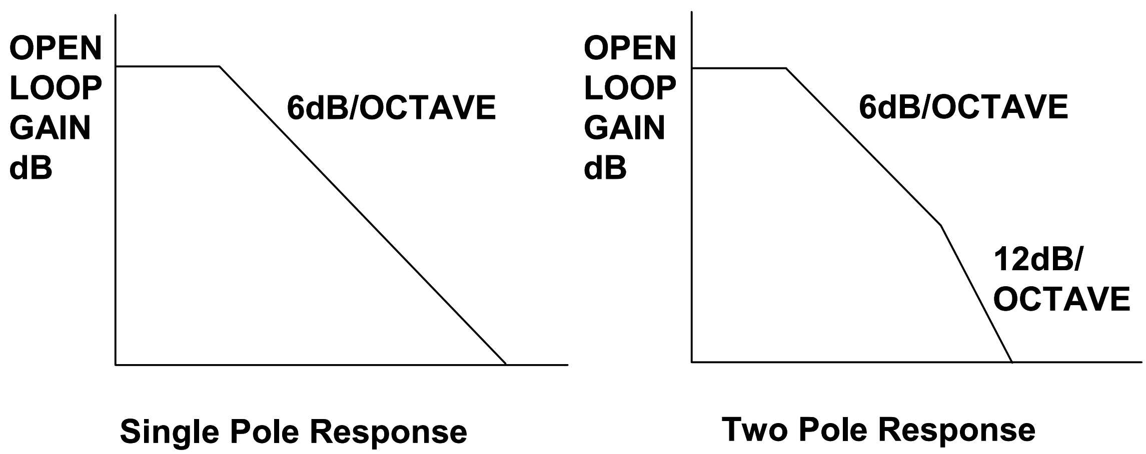


Figure. 1.29: *Open-Loop Gain*

Since the open-loop gain falls by half with a doubling of frequency with a single pole response, there is what is called a constant gain-bandwidth product. At any point along the curve, if the frequency is multiplied by the gain at that frequency, the product is a constant. For example, if an amplifier has a 1 MHz gain bandwidth product, the open-loop gain will be 10 (20 dB) at 100 kHz, 100 (40 dB) at 10 kHz, etc. This is readily apparent on a Bode plot, which plots gain vs. frequency on a log-log scale.

Since a voltage feedback op amp operates as a voltage in/voltage out device, its open-loop gain is a dimensionless ratio, so no unit is necessary. Data sheets sometimes express gain in V/mV or V/µV instead of V/V, for the convenience of using smaller numbers. Or voltage gain can also be expressed in dB terms, as gain in dB = $20 \times \log A_{VOL}$. Thus an open-loop gain of 1 V/µV (or 1000 V/mV or 1,000,000 V/V) is equivalent to 120 dB, and so on.

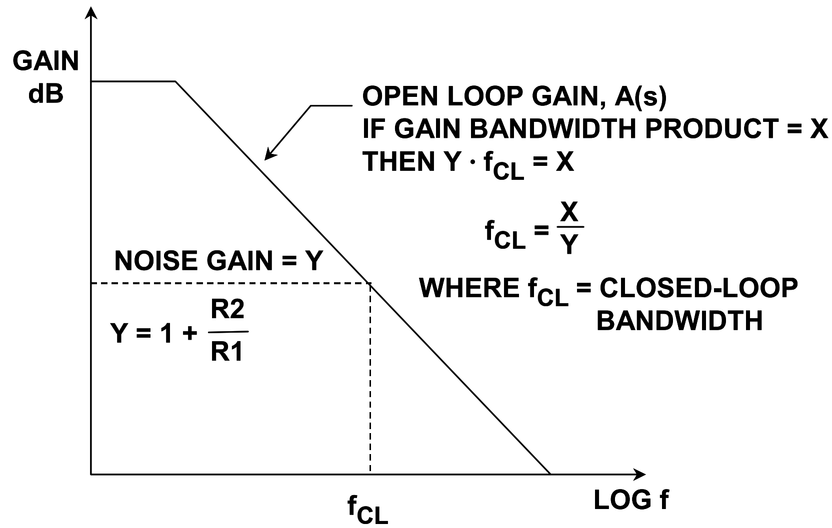


Figure 1.30: *Bode Plot (for VFB Amps)*

For very high precision work, the nonlinearity of the open-loop gain must be considered. Changes in the output voltage level and output loading are the most common causes of changes in the open-loop gain of op amps. A change in open-loop gain with signal level produces a *nonlinearity* in the closed-loop gain transfer function, which cannot be removed during system calibration. Most op amps have fixed loads, so A_{VOL} changes with load are not generally important. However, the sensitivity of A_{VOL} to output signal level may increase for higher load currents. See Figure 1.31.

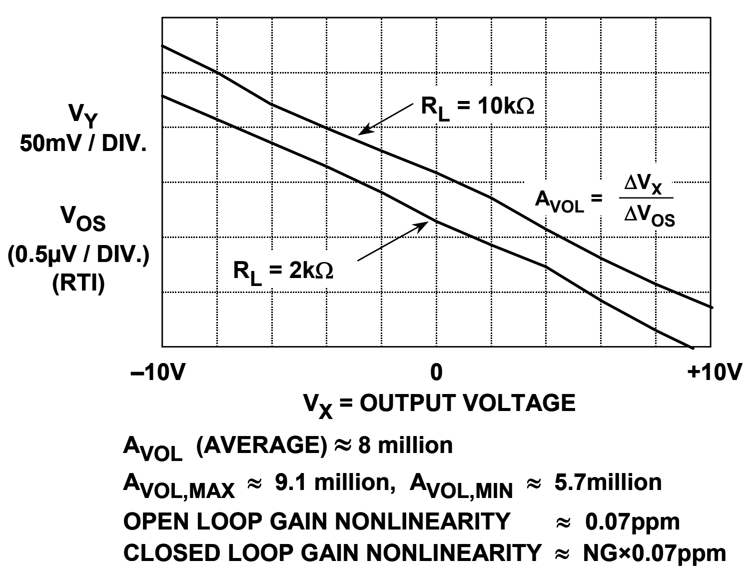


Figure 1.31: *Open-Loop Nonlinearity*

The severity of this nonlinearity varies widely from one device type to another, and generally isn't specified on the data sheet. The minimum A_{VOL} is always specified, and choosing an op amp with a high A_{VOL} will minimize the probability of gain nonlinearity errors. There is no way to compensate for A_{VOL} nonlinearity.

Open-Loop Transresistance of a CFB Op Amp

For current feedback amplifiers, the open-loop response is voltage out for a current in, so it is a *transresistance* (expressed in ohms) rather than a gain. This is generally referred to as a *transimpedance*, since there is an ac component as well as a dc term. The *transimpedance* of a CFB amp will usually be in the range of 500 kΩ to 1 MΩ.

A CFB op amp open-loop transimpedance does not vary in the same way as a VFB open-loop gain. Therefore, a CFB op amp will not have the same gain-bandwidth product as VFB amps. While there is some variation of frequency response with frequency with a CFB amp, it is nowhere near 6 dB/octave. See Figure 1.32.

When using the term *transimpedance amplifier*, there can be some confusion. An amplifier configured as a current to voltage (I/V) converter, typically in photodiode circuits, is also referred to as a transimpedance amplifier. But the photodiode application will generally use a FET input VFB amp rather than a CFB amp. This is because the current levels in the photodiode applications will be very low, not the most compatible with the low impedance input of a CDB op amp.

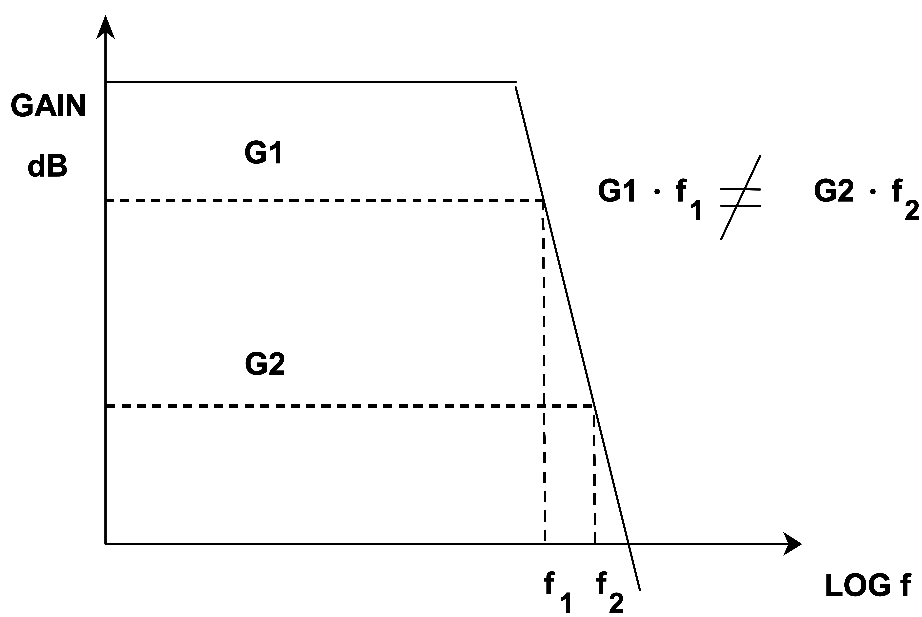


Figure 1.32: *Open-Loop Gain of a CFB Op Amp*

Offset Voltage

If both inputs of an op amp are at exactly the same voltage, then the output should be at zero volts, since a differential of 0 V should produce an output of 0 V. In practice, however, there will typically be some voltage at the output. This is known as the *offset voltage* or V_{OS}. The typical way to specify offset voltage is as the amount of voltage that must be added to the input to force 0 V out. This voltage, divided by the noise gain of the circuit, is the *input offset voltage* or *input referred offset voltage.* The offset voltage is usually input referred to eliminate the effect of circuit gain, which makes comparisons easier. The offset voltage is modeled as a voltage source, V_{OS}, in series with the inverting input of the op amp as shown in Figure 1.33 .

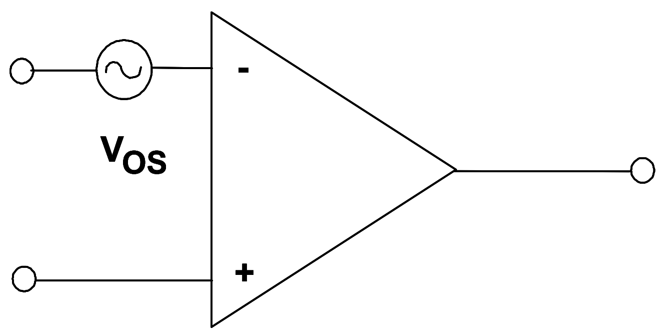


Figure 1.33: *Offset Voltage*

Offset Voltage Drift

The input offset voltage varies with temperature. Its temperature coefficient is known as TCV_{OS}, or more commonly, *drift*. Offset drift may be as low as 0.1 µV/°C (typical value for OP177F, a very high precision op amp). More typical drift values for a range of general purpose precision op amps lie in the range 1 µV/°C to 10 µV/°C. Most op amps have a specified value of TCV_{OS}, but some, instead, have a second value of maximum V_{OS} that is guaranteed over the operating temperature range. Such a spec is less useful, because there is no guarantee that TCV_{OS} is constant or monotonic.

Drift with Time

The offset voltage also changes as time passes, or *ages*. Aging is generally specified in µV/month or µV/1000 hours, but this can be misleading. Aging is not linear, but instead a nonlinear phenomenon that is proportional to the *square root* of the elapsed time. A drift rate of 1 µV/1000 hours therefore becomes about 3 µV/year (not 9 µV/year). *Long-term drift* of the OP177F is approximately 0.3 µV/month. This refers to a time period *after* the first 30 days of operation. Excluding the initial hour of operation, changes in the offset voltage of these devices during the first 30 days of operation are typically less than 2 µV. The long term drift of offset voltage with time is not always specified, even for precision op amps.

Correction for Offset Voltage

Early op amps typically had pins available for nulling out offset voltages. A potentiometer connected to these pins, and the wiper connected to one or the other of the supply voltages, allowed balancing the input stage, which, in turn, nulled out the offset voltage. See Figure 1.34.

Makers of high precision op amps, such as Analog Devices (ADI) and Precision Monolithics (PMI) employed circuit design tricks to internally balance the input structures. ADI used laser trimming of the input stage load resistors to achieve balance. PMI used a technique call zener zapping to accomplish basically the same thing.

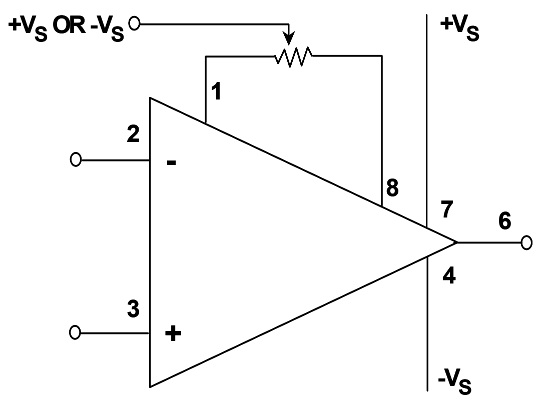


Figure 1.34: *Offset Adjustment Pins*

Laser trimming used lasers to eat away part of the collector resistors to adjust their value. Zener zapping involved having a string of resistors, each bypassed by a semiconductor structure that is basically a zener diode. By applying a pulse of voltage these zener diodes would be shorted out (zapped). This adjusts the value of the resistor string.

DigiTrim™ Technology

DigiTrim is a technique which adjusts circuit offset performance by programming digitally weighted current sources, in essence a DAC. This technique makes use of the mixed signal capabilities of the CMOS process. While, historically, CMOS would not be the first choice for precision amplifiers, recent process improvements combined with the DigiTrim technology result in a very reasonable precision performance. In this patented new trim method, the trim information is entered through existing analog pins using a special digital keyword sequence. The adjustment values can be temporarily programmed, evaluated and readjusted for optimum accuracy before permanent adjustment is performed. After the trim is completed, the trim circuit is locked out to prevent the possibility of any accidental re-trimming by the end user.

A unique feature of this technique is that the adjustment is done after the chip is packaged. With zener zapping and laser trimming, the offset must be adjusted at the die level. Subsequent processing, mounting the chip on a header and encapsulating in plastic cause a shift in the offset. This is due to both the mechanical stress of the mounting (strain gauge effect) and the heat of molding the package. While the amount of the shift is well profiled, the ability to trim at the package level versus the chip level is a distinct advantage.

The physical trimming, achieved by blowing polysilicon fuses, is very reliable. No extra pads or pins are required for this trim method and no special test equipment is needed to perform the trimming. The trimming is done through the input pins. A simplified representation of an amplifier with DigiTrim is shown in Figure 1.35. No testing is required at the wafer level assuming reasonable die yields. No special wafer fabrication process is required and circuits can even be produced by our foundry partners. All of the trim circuitry tend to scale with the process features so that as the process and the amplifier circuit shrink, the trim circuit also shrinks proportionally. The trim circuits are considerably smaller than normal amplifier circuits so that they contribute minimally to die cost. The trims are discrete as in link trimming and zener zapping but the required accuracy is easily achieved at a very small cost increase over an untrimmed part.

The DigiTrim approach could also support user trimming of system offsets with a different amplifier design. This has not yet been implemented in a production part, but it remains a possibility.

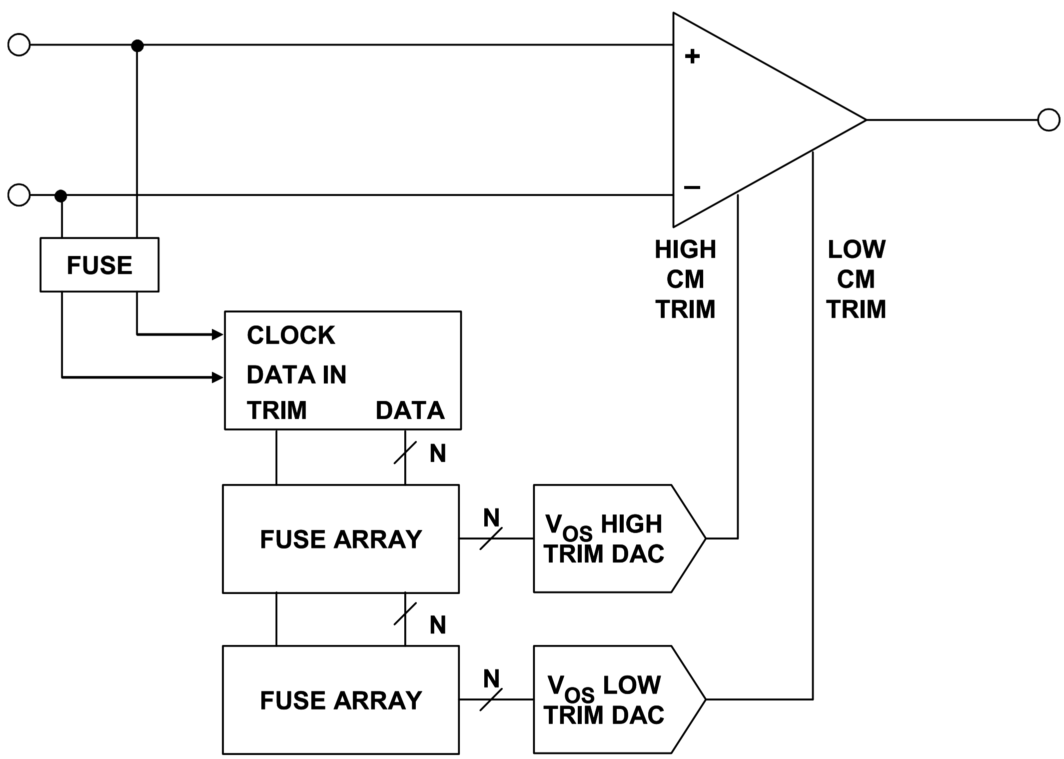


Figure 1.35: *Simplified Schematic of the DigiTrim Technology*

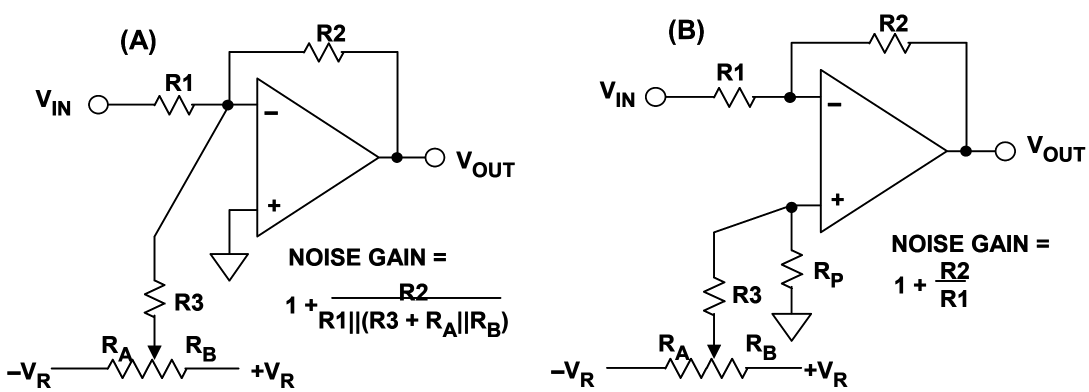
External Trim

The offset adjustment pins started to disappear with the advent of dual op amps since there weren't enough pins left for them in the 8-pin package. Therefore external adjustment techniques were required.

External trimming out offset involves basically adding a small voltage to the input to counteract the offset. See Figure 1.36. The polarity of the voltage applied to the offset potentiometer will depend on the process used to manufacture the part as well as the polarity of the input devices (NPN or PNP). The offset can be accomplished with potentiometers, digital potentiometers or DACs. The major problem with external trimming is that the temperature coefficients of the internal and external components will probably not match. This will limit the effectiveness of the adjustment over temperature.

In addition, the mechanical potentiometer is subject to aging and mechanical vibration.

There is an increase in noise gain due to the added resistance and the potentiometer resistance. The resulting increase in noise gain may be reduced by making R3 much greater than R1. Note that otherwise, the signal gain might be affected as the offset potentiometer is adjusted. The gain may be stabilized, however, if R3 is connected to a fixed low impedance reference voltage sources, $\pm V_R$.



$$V_{OUT} = -\frac{R2}{R1} V_{IN} \pm \underbrace{\frac{R2}{R3} V_R}_{\text{MAX OFFSET}}$$

$$V_{OUT} = -\frac{R2}{R1} V_{IN} \pm \underbrace{\left[1 + \frac{R2}{R1}\right] \left[\frac{R_P}{R_P + R3}\right] V_R}_{\text{MAX OFFSET}}$$

$R_P = R1||R2$ IF $I_{B+} \approx I_{B-}$

$R_P \leq 50\Omega$ IF $I_{B+} \neq I_{B-}$

Figure 1.36: External Offset Adjustment

The digital potentiometer and DAC however can be adjusted in circuit, under control of a microprocessor or microcontroller, which could mitigate aging and temperature effects.

If response to dc is not required, an alternative approach would be to use a circuit called a servo. See Figure 1.38. This circuit is basically an integrator, which is placed in a feedback loop around the main amplifier. A precision amplifier should be used for the integrator, it need not be fast enough to pass the full frequency spectrum that the main amplifier must. The circuit operates by taking the average dc level of the output and feeding it back to the main amplifier, in effect subtracting it from the signal.

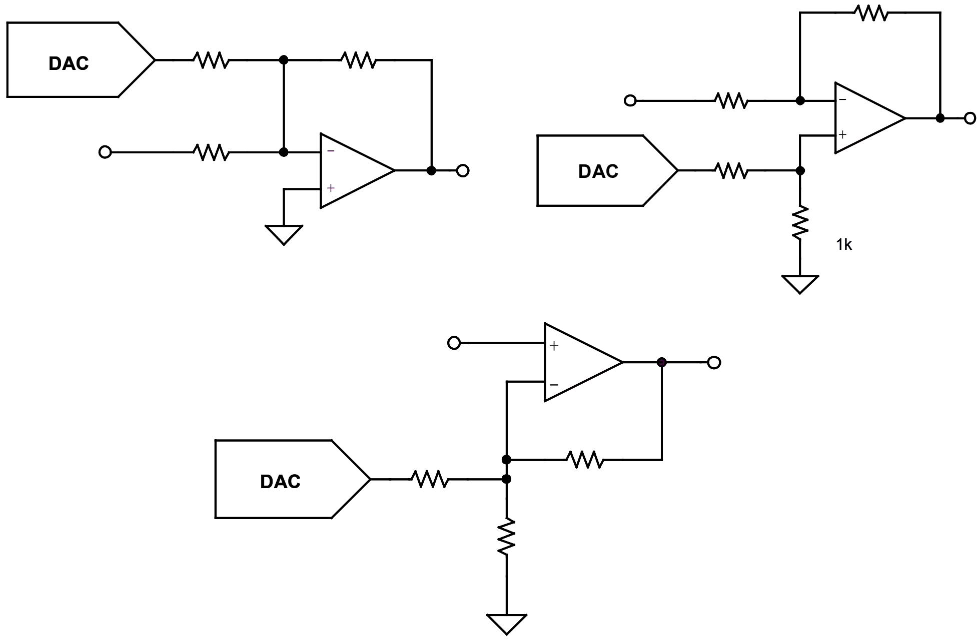


Figure 1.37: *Using a DAC to Control Offset*

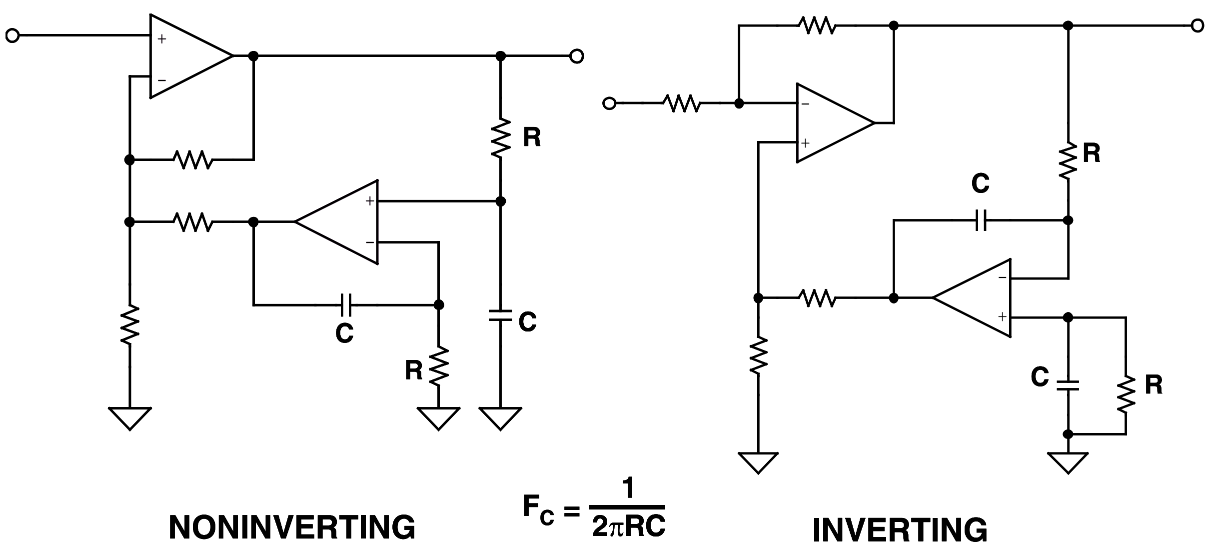


Figure 1.38: *Servo Controlled Offset*

Input Bias Current

In the ideal model of the op amp the inputs have infinite impedance and so no current flows into the input terminals. But since the most common input structure use bipolar junction transistors (BJTs), there is always some current required for operation, since the BJT is a current controlled device. This is referred to as *bias current* (I_B) or *input bias current*. In practice, there are always two *input bias currents*, I_{B+} and I_{B-} (see Figure 1.39), one for each of the inputs. Values of I_B range from 60 fA (about one electron every three microseconds) in the AD549 electrometer, to tens of microamperes in some high speed op amps. Due to the inherent nature of monolithic op amp fabrication processing, these bias currents tend to be equal, but this isn't guaranteed to be case. And in the case of current feedback amplifiers, the nonsymmetric nature of the inputs guarantees that the bias currents are different.

Input bias current is a problem to the op amp user because it flows in external impedances and produces offset voltages, which add to system errors. Consider a noninverting unity gain buffer driven from a source impedance of 1 MΩ. If I_B is 10 nA, it will introduce an additional 10 mV of error. Or, if the designer simply forgets about I_B and uses capacitive coupling, the circuit won't work at all! This is because the bias currents need a DC return path to ground. If the dc return path is not there, the input of the op amp will drift to one of the rails. Or, if I_B is low enough, it may work momentarily while the capacitor charges, giving even more misleading results. The moral here is not to neglect the effects of I_B, in any op amp circuit.

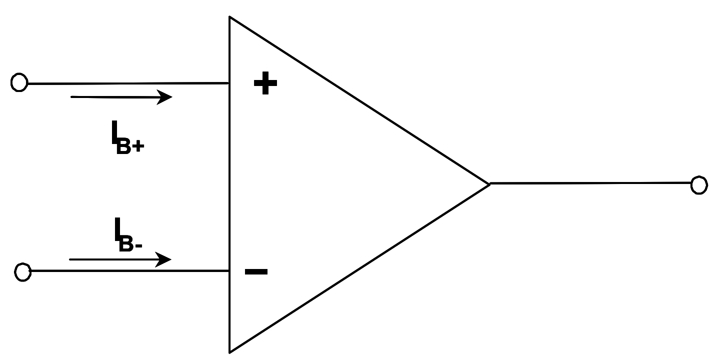


Figure 1.39: *Input Bias Current*

Input Offset Current

The difference in the bias currents is the input offset current. Normally the difference between the bias currents is small, so that the offset current is also small. In bias compensated op amps (see next section) the offset current is approximately equal to the bias current.

Compensating for Input Bias Current

There are several ways to compensate for bias currents. It can be addressed by the manufacturer, or external techniques can be employed.

There are basically two different ways that an IC manufacturer can deal with bias currents.

The first is the use a "super-beta" transistors for the input stage. Super-beta transistors are specially processed devices with a very narrow base region. They typically have a current gain (β) of thousands or tens of thousands (rather than the more usual hundreds for standard BJT transistors). Op amps with super-beta input stages have much lower bias currents, but they also have more limited frequency response. Since the breakdown voltages of super-beta devices are typically quite low, they also require additional circuitry to protect the input stage from damage caused by overvoltage on the input.

The second method of dealing with bias currents is to use a bias compensated input structure. See Figure 1.40. With a bias current compensated input, small current sources are added to the bases of the input devices. The idea is that the bias currents required by the input devices are provided by the current sources so that the net current seen by the external circuit is reduced considerably.

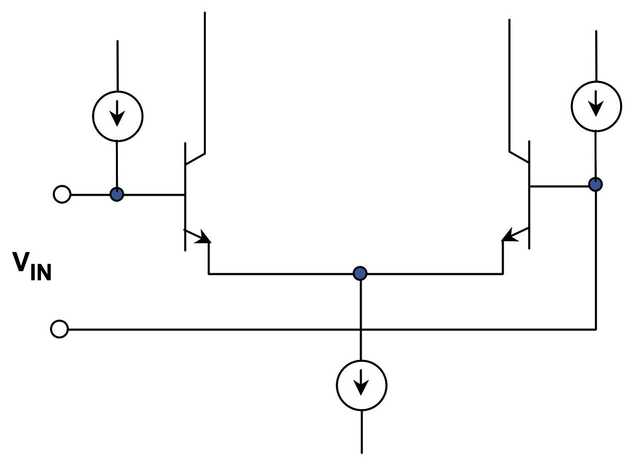


Figure 1.40: *Input Bias Current Compensation*

Bias current compensated input stages have many of the good features of the simple bipolar input stage, namely: low voltage noise, low offset, and low drift. Additionally, they have low bias current which is fairly stable with temperature. However, their current noise is not very good, since current sources are added to the input. And their bias current matching is poor. These latter two undesired side effects result from the external bias current being the *difference* between the compensating current source and the input transistor base current. Both of these currents inevitably have noise. Since they are uncorrelated, the two noises add in a root-sum-of-squares fashion (even though the dc currents subtract).

Note that this can easily be verified, by examining the *offset current* spec (the difference in the bias currents). If internal bias current compensation exists, the offset current will be of the same magnitude as the bias current. Without bias current compensation, the offset current will generally be at least a factor of 10 smaller than the bias current. Note that these relationships generally hold, regardless of the exact magnitude of the bias currents.

Since the resulting external bias current is the difference between two nearly equal currents, there is no reason why the net current should have a defined polarity. As a result, the bias currents of a bias-compensated op amp may not only be mismatched, they can actually flow in opposite directions! In most applications this isn't important, but in some it can have unexpected effects (for example, the droop (change of voltage in the hold mode) of a sample-and-hold amplifier (SHA) built with a bias-compensated op amp may have either polarity).

In many cases, the bias current compensation feature is not mentioned on an op amp data sheet. It is easy to determine if bias current compensation is being used by examining the bias current spec. If the bias current is specified as a "±" value, the op amp is most likely compensated for bias current.

The designer can compensate for the effects of the bias current by equalizing the impedances seen by the two inputs. See Figure 1.40. If the impedances are equal, then the bias currents (which will tend to also be equal) flowing through them will produce the same offset voltage, which will appear as a common-mode signal. Since it is a common-mode signal it would tend to not add to the error due to the common-mode rejection (CMRR, to be discussed later in this section) of the amplifier.

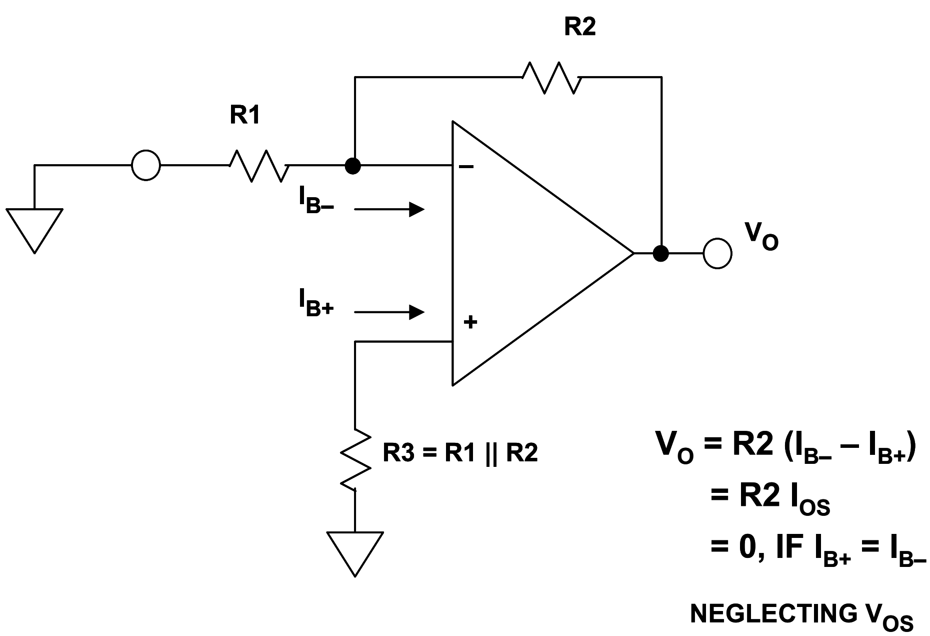


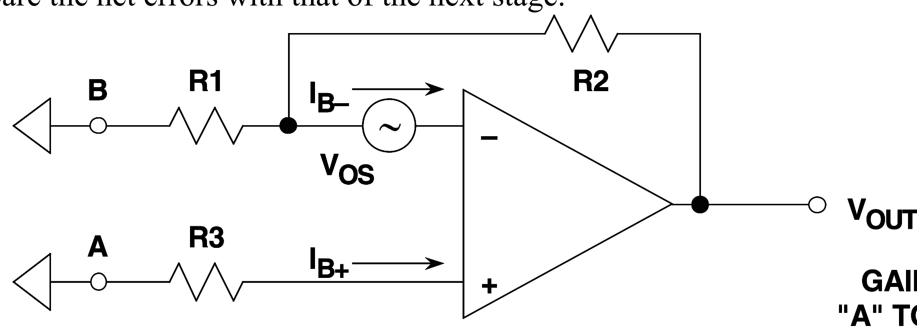
Figure 1.41: *Bias Current Compensation*

Care should be used when applying this technique. It obviously won't work with a bias compensated op amp, since the bias currents aren't equal. With FET input amps, the impedance levels tend to be high and the bias currents are small, so the added effects of the Johnson noise of the high input impedances might be worse than the effects of the bias current flowing through them. Analysis needs to be performed.

Calculating Total Output Offset Error Due to IB and VOS

The equations shown in Figure 1.42 below are useful in referring all the offset voltage and induced offset voltage from bias current errors to the either the input (RTI) or the output (RTO) of the op amp. The choice of RTI or RTO is a matter of preference.

The RTI value is useful in comparing the cumulative op amp offset error to the input signal. The RTO value is more useful if the op amp drives additional circuitry, to compare the net errors with that of the next stage.



GAIN FROM "A" TO OUTPUT = NOISE GAIN = $NG = 1 + \frac{R2}{R1}$

GAIN FROM "B" TO OUTPUT $= -\frac{R2}{R1}$

- $\text{OFFSET (RTO)} = V_{OS}\left[1 + \frac{R2}{R1}\right] + I_{B+} \bullet R3 \left[1 + \frac{R2}{R1}\right] - I_{B-} \bullet R2$
- $\text{OFFSET (RTI)} = V_{OS} + I_{B+} \bullet R3 - I_{B-}\left[\frac{R1 \bullet R2}{R1 + R2}\right]$

FOR BIAS CURRENT CANCELLATION:

$$\text{OFFSET (RTI)} = V_{OS} \quad \text{IF } I_{B+} = I_{B-} \text{ AND } R3 = \frac{R1 \bullet R2}{R1 + R2}$$

Figure 1.42: *Total Offset Voltage Calculations*

In any case, the RTO value is simply obtained by multiplying the RTI value by the stage noise gain, which is 1 + R2/R1.

There are some simple rules towards minimization offset voltage and bias current errors. First, keep input/feedback resistance values low, to minimize offset voltage due to bias current effects. Second, use bias compensation resistors. Bypass these resistors with fairly large values of capacitance. This gives the advantage of the resistors at dc for bias currents, but shorts out the resistances at higher frequencies to minimize noise at higher frequencies. Next, it is probably not wise to use this technique with FET input devices, since the value of the compensation resistor will likely add more noise than it will save in bias current compensation. If an op amp uses internal bias current compensation, *don't* use the compensation resistance, since the bias currents will not match. When necessary, use *external* offset trim networks, for lowest induced drift. Select an appropriate precision op amp specified for low offset and drift, as opposed to trimming.

Input Impedance

VFB op amps normally have both differential and common-mode input impedances specified. Current feedback op amps normally specify the impedance to ground at each input. Different models may be used for different voltage feedback op amps, but in the absence of other information, it is usually safe to use the model in Figure 1.43. In this model the bias currents flow into the inputs from infinite impedance current sources.

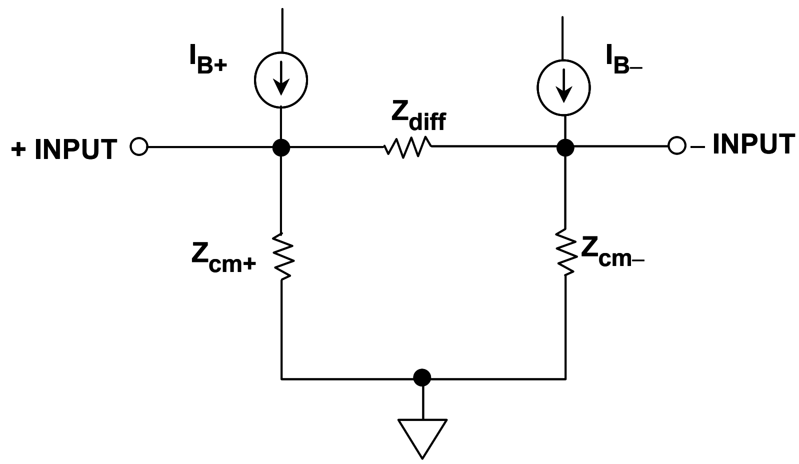


Figure 1.43: *Input Impedance*

The common-mode input impedance data sheet spec (Z_{cm+} and Z_{cm-}) is the impedance from either input to ground (NOT from both to ground). The differential input impedance (Z_{diff}) is the impedance between the two inputs. These impedances are usually resistive and high ($10^5\ \Omega$ to $10^{12}\ \Omega$.) with some shunt capacitance (generally a few pF, sometimes 20 pF to 25 pF). In most op amp circuits, the inverting input impedance is reduced to a very low value by negative feedback, and only Z_{cm+} and Z_{diff} are of importance.

A current feedback op amp is even more simple, as shown in Figure 1.44. Z+ is resistive, generally with some shunt capacitance, and high ($10^5\ \Omega$ to $10^9\ \Omega$.) while Z– is reactive (L r C, depending on the device) but has a resistive component of 10 Ω to 100 Ω, varying from type to type.

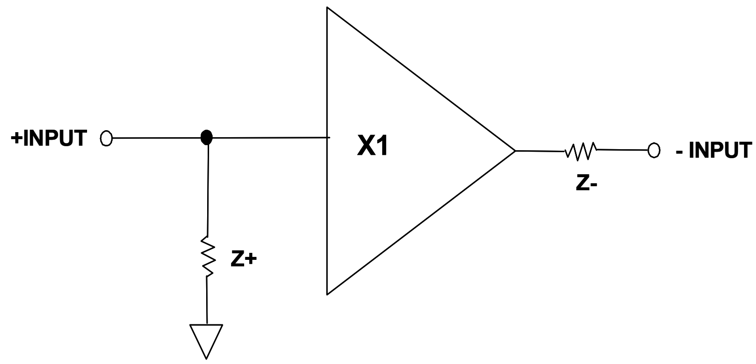


Figure 1.44: *Current Feedback Input resistance*

Input Capacitance

In general, the input capacitance is not an issue with high speed op amps. In certain applications, such as a photodiode amp, where the source impedance is high, it could come into play. With a very large source impedance, a relatively small capacitance could set up a zero in the transmission function. This could lead to instability. Since the noise gain of the amplifier is rising at 6 dB/octave, and the open-loop gain is falling at 6 dB/octave, the intersection will be at 12 dB/octave, which is unstable.

Another issue with FET input devices driven from a high impedance source in the noninverting configuration is the modulation of the input capacitance by the common-mode voltage. This leads to a level dependent distortion. To compensate for this effect, balancing the impedances as seen by the inputs is used. This is similar to the balancing used for input bias current, except that the balance is not just for dc.

Input Common-Mode Voltage Range

The input common-mode range is the allowable voltage on the input pins. It usually is not the full supply range. Classical system design used ±15 V supplies with an expected dynamic range of ±10 V, so the inputs really needed only to cover those ranges.

However, the current trend is to smaller and smaller supply voltages. This increases the need to maximize the input dynamic range. Many low voltage op amps utilize “rail-to-rail” inputs. While there is no industry-standard definition for “rail-to rail,” at Analog Devices it is defined as swinging within 100 mV of either rail. Note that not all devices marketed as single supply are rail-to-rail, and not all devices that are marketed as rail-to-rail are able to swing to the rails on both input and output. You must read the data sheet carefully.

Certain inputs, such as bias compensated and super beta op amps will further limit the input voltage range.

Differential Input Voltage

Certain input structures require limiting of differential input voltage to prevent damage. These op amps will generally have back-to-back diodes across the inputs. This will not always show up in the simplified schematics of the amps. It will show up, however, as a differential input voltage spec of ±700 mV maximum.

In addition, you may find a spec for the maximum input differential current. Some amps have current limiting resistors built in, but these resistors raise the noise, so for low noise op amps they are left off.

Supply Voltage

Classical system design was ±15 V supplies with an expected signal dynamic range of ±10 V. Most early op amps were designed to operate on these voltages. The supply voltage typically had a very wide range. On the data sheet a range of allowable supply voltages was generally listed. It could be something like ±4.5 V to ±18 V, which is the spec for the AD712. In general there are some small changes in the specs for the same op amp operated on different supplies. This usually shows up as multiple spec pages, each at a different set of conditions, which usually means different supplies.

Although the voltage spec was generally given as a symmetrical bipolar voltage, there is no reason that it had to be either symmetrical or bipolar. To the op amp a ±15 V supply is the same as a +30 V/0 V supply or a +20 V/−10 V supply, as long as the inputs are biased in the active region (within the common-mode range).

The current trend is to lower supply voltages. For high speed amps this is partially due to process limitations. Higher speeds imply small physical structures, which, in turn, imply lower breakdown voltages. Lower breakdown voltages imply lower supply voltages. Currently most high speed op amps require ±5 V or single +5 V supplies. For general purpose op amps, supplies are getting as low as +1.8 V. Note that the term single-supply is sometimes used to indicate lower supply voltages. The two concepts are related, but, as pointed out above, single-supply does not necessarily mean low voltage. Keep the concepts separate.

CMOS op amps are also generally operated with lower supplies. The trend in CMOS processes, again driven by digital circuits, emphasizes small and smaller geometries, with their attendant lower breakdown voltages.

Quiescent Current

The quiescent current is the current internally consumed by the op amp itself (no load). In general, high speed amps tend to draw more quiescent current than general purpose amps. In addition, for general purpose op amps, some performance parameters (noise and distortion in particular) tend to improve with higher current. On the other end of the spectrum, the lowest quiescent current amps have severely limited bandwidth. Currently the lowest quiescent current device from Analog Devices is the OP290 at 3.5 μA.

There is a strong demand for low quiescent current op amps. One driving application is battery powered equipment. While there is no industry standard for what "low power" means, at Analog Devices "low power" is defined as less than 1 mA of quiescent current. "Micropower" is defined as less than 100 μA quiescent current. Note that this is per amplifier, so a quad op amp will draw 4× this amount. Also note that this applies only to amplifiers. Low power can mean many things to many people. For instance a very high speed ADC may dissipate over 1 W! This can still be considered low power, since competing solutions can be over 4 W.

Output Voltage Swing (Output Voltage High/Output Voltage Low)

As pointed out above, classical system design used ±15 V supplies with an expected dynamic range of ±10 V. The standard output structure was an emitter follower (common collector) circuit. The base is a diode drop above the output. There must be some voltage above that for biasing the drive signal. So we need a spec on how much voltage we can expect from the output. If using reduced supply voltages this spec for overhead will remain constant. For example, if the spec is ±12 V (min) on a ±15 V supply, we should expect to achieve ±6 V on a ±9 V supply.

Again, as we shrink the supply voltage, we need to maximize the output dynamic range. After all, if we lose 3 V to each of the supply rails, as in the example above, and we are operating on a ±3 V supply, we will have a severely compressed dynamic range. What is typically done to increase the dynamic range is to change the configuration of the output stage from an emitter follower to a common emitter. The output will then be able to swing to within the V_{CEsat} of the output transistor.

Allowing the output to swing close to the rail is referred to as "rail-to-rail." As we discussed in the input voltage section there is no industry-standard rail-to-rail spec. At Analog Devices we define it, again, as being able to swing within 100 mV of either rail, with the added constraint of driving a 10 kΩ load. The value of the load is important, since the V_{CEsat} of the output transistor is dependent on output current. Remember not all "single-supply" op amps are "rail-to-rail" and not all "rail-to-rail" are so on both input and output. You must read the data sheet.

Output Current (Short-Circuit Current)

Most general-purpose op amps have output stages which are protected against short circuits to ground or to either supply. This is commonly referred to as "infinite" short-circuit protection, since the amplifier can drive that value of current into the short circuit indefinitely. The output current that can be expected to be delivered by the op amp is the output current. Typically the limit is set so that the op amp can deliver 10 mA for general purpose op amps.

If an op amp is required to have both high precision and a large output current, it is advisable to use a separate output stage (within the feedback loop) to minimize self-heating of the precision op amp. This added amplifier is often called a buffer, since it typically will have a voltage gain = 1.

There are some op amps that are designed to give large output currents. An example is the AD8534, which is a quad device that has an output current of 250 mA for each of the four sections. A word of warning—if you try to supply 250 mA from of all four sections at the same time, you will exceed the package dissipation spec. The amp will overheat, and could destroy itself. This problem gets worse with smaller packages, which have lower dissipation.

High speed op amps typically do not have output currents limited to a low value, since it would affect their slew rate and ability to drive low impedances. Most high speed op amps will source and sink between 50 mA and 100 mA, though a few are limited to less than 30 mA. Even for high speed op amps that have short-circuit protection, junction temperatures may be exceeded (because of the high short-circuit current) resulting in device damage for prolonged shorts.

AC Specifications

Noise

This section discusses the noise generated within op amps, not external noise which they may pick up. External noise is important, and is discussed in detail in other texts, but in this section we are concerned solely with internal noise.

There are three noise sources in an op amp: a voltage noise, which appears differentially across the two inputs and a current noise in each input. These sources are effectively uncorrelated (independent of each other). In fact, there is a slight correlation between the two noise currents, but it is too small to need consideration in practical noise analyses. In addition to these three internal noise sources, it is necessary to consider the Johnson noise of the external resistors, which are used with the op amp in the feedback network.

Voltage Noise

The voltage noise of different op amps may vary from under 1 nV/√Hz to 20 nV/√Hz, or even more. Bipolar op amps tend to have lower voltage noise than JFET amps. Voltage noise is specified on the data sheet, and it isn't possible to predict it from other parameters.

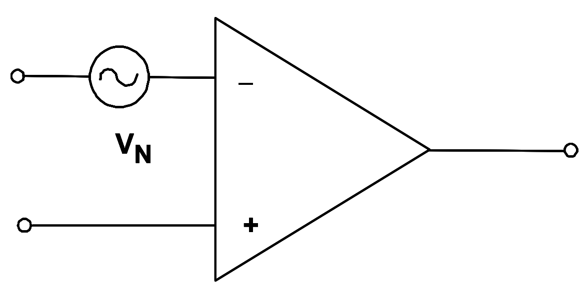


Figure 1.45: *Voltage Noise*

Until recently, JFET input amplifiers tended to have comparatively high voltage noise (though they have very low current noise), and were thus more suitable for low noise applications in high impedance rather than low impedance circuitry. The AD645 and AD743/AD745 have very low values of both voltage and current noise. The AD645 specs at 10 kHz are 10 nV/√Hz and 0.6 fA/√Hz, and the AD743/AD745 specs at 10 kHz are 2.9 nV/√Hz and 6.9 fA/√Hz. These make possible the design of low noise amplifier circuits, which have low noise over a wide range of source impedances. The cost of the lower voltage noise is large input devices, and hence large input capacitance.

Noise Bandwidth

When calculating the bandwidth of the noise contribution we always use a bandwidth of 1.57 f_C to calculate the noise. The reason for this is that a Gaussian (white) noise source passed through a single pole filter with a cutoff frequency of Fc has the same spectral energy as the same source passed through a brick wall filter with a cutoff frequency of 1.57 f_C. A brick wall filter has a flat response up to the cutoff frequency above which it has infinite attenuation. Similarly, a two pole filter has an apparent corner frequency of approximately 1.2 f_C. The error correction factor is usually negligible for filters having more than two poles.

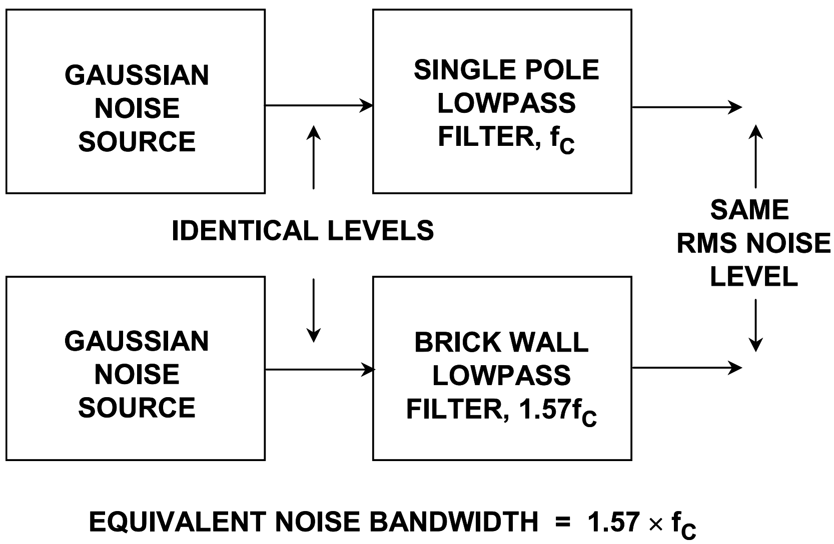


Figure 1.47: *Equivalent Noise Bandwidth*

Noise Figure

Noise figure is rarely used with op amps. The *noise figure* of an amplifier is the amount (in dB) by which the noise of the amplifier exceeds the noise of a perfect noise-free amplifier in the same environment. The concept comes from RF and TV applications, where 50 Ω or 75 Ω transmission lines and terminations are ubiquitous, but is useless for an op amp, which may be used with a wide variety of impedances. Voltage noise spectral density and current noise spectral density are much more useful specs.

Current Noise

Current noise can vary much more widely, from around 0.1 fA/√Hz (in JFET electrometer op amps) to several pA/√Hz (in high speed bipolar op amps). It is not always specified on data sheets, but may be calculated in cases (like simple BJT or JFET input devices) where all the bias current flows in the input junction, because in these cases it is simply the Schottky (or shot) noise of the bias current. It cannot be calculated for bias-compensated or current feedback op amps, where the external bias current is the *difference* of two internal current sources. The shot noise spectral density is simply $\sqrt{2I_bq}/\sqrt{Hz}$, where I_b is the bias current (in amps) and q is the charge on an electron (1.6×10^{-19} C).

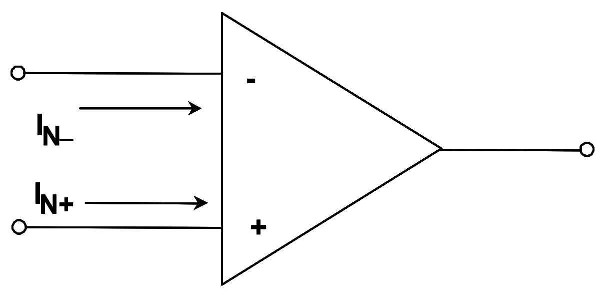


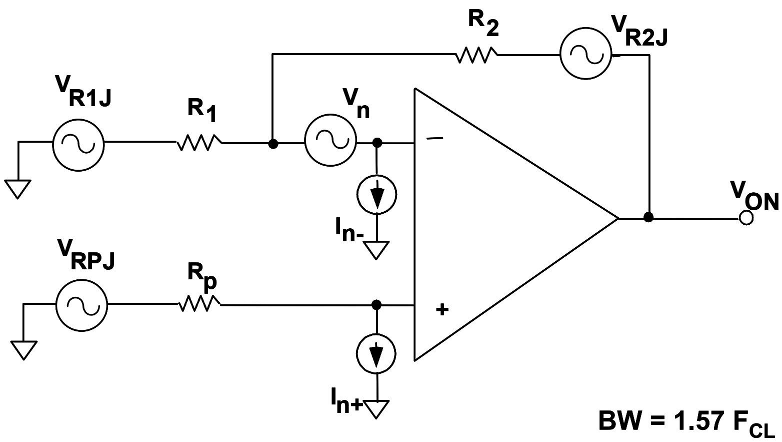
Figure 1.48: *Current Noise*

The current noise for the inputs of a VFB op amp are uncorrelated and roughly equal in value. In the simple input structures, the current noise is the shot noise of the input bias current. In a bias-compensated op amp, the current noise can not be calculated. Also, since the inputs of a CFB op amp are different, the current noise for the two inputs can be very different. The 1/f corners will typically not match either.

Current noise is only important when it flows in an impedance and generates a noise voltage. Therefore, the choice of a low noise op amp depends on the impedances around it. Consider an OP-27, a bias-compensated op amp with low voltage noise (3 nV/√Hz), but quite high current noise (1 pA/√Hz). With zero source impedance, the voltage noise will dominate. With a source resistance of 3 kΩ, the current noise (1 pA/√Hz flowing in 3 kΩ) will equal the voltage noise, but the Johnson noise of the 3 kΩ resistor is 7 nV/√Hz and so is dominant. With a source resistance of 300 kΩ, the current noise increases a hundredfold to 300 nV/√Hz, while the voltage noise continues unchanged, and the Johnson noise (which is proportional to the *square root* of the resistance) only increases tenfold. Here, current noise is dominant.

Total Noise (Sum of Noise Sources)

Uncorrelated noise voltages add in a "root-sum-of-squares" manner; i.e., noise voltages V_1, V_2, V_3 give a summed result of $\sqrt{(V_1^2 + V_2^2 + V_3^2)}$. Noise powers, of course, add normally. Thus, any noise voltage that is more than 3 to 5 times any of the others is dominant, and the others may generally be ignored. This simplifies noise assessment. Current noises flowing through resistance equal noise voltages



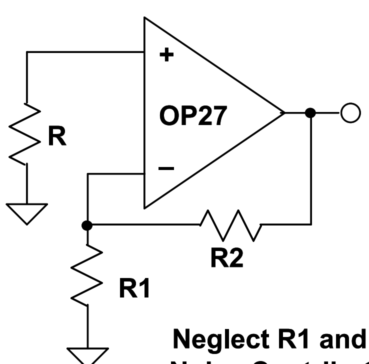
$BW = 1.57\ F_{CL}$

F_{CL} = CLOSED LOOP BANDWIDTH

$$V_{ON} = \sqrt{BW}\sqrt{[(I_{n-}^2)R_2^2]\,[NG] + [(I_{n+}^2)R_P^2]\,[NG] + V_N^2\,[NG] + 4kTR_2\,[NG-1] + 4kTR_1\,[NG-1] + 4kTR_P\,[NG]}$$

Figure 1.49: *Total Noise Calculation*

EXAMPLE: OP27
Voltage Noise = 3nV / √Hz
Current Noise = 1pA / √Hz
T = 25°C



Neglect R1 and R2 Noise Contribution

CONTRIBUTION FROM	VALUES OF R		
	0	3kΩ	300kΩ
AMPLIFIER VOLTAGE NOISE	**3**	3	3
AMPLIFIER CURRENT NOISE FLOWING IN R	0	3	**300**
JOHNSON NOISE OF R	0	**7**	70

RTI NOISE (nV / √Hz)
Dominant Noise Source is Highlighted

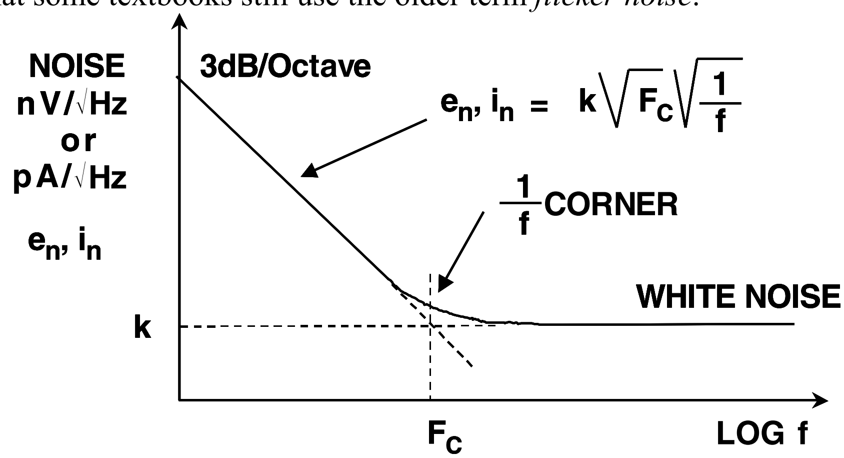
Figure 1.50: *Dominant Noise Source Determined by Input impedance*

The choice of a low noise op amp depends on the source impedance of the signal, and at high impedances, current noise always dominates.

For low impedance circuitry, amplifiers with low voltage noise, such as the OP-27, will be the obvious choice, since they are inexpensive, and their comparatively large current noise will not affect the application (see Figure 1.50). At medium resistances, the Johnson noise of resistors is dominant, while at very high resistances, we must choose an op amp with the smallest possible current noise, such as the FET input devices AD549 or AD645.

1/f Noise (Flicker Noise)

So far, we have assumed that noise is *white* (i.e., its spectral density does not vary with frequency). This is true over most of an op amp's frequency range, but at low frequencies the noise spectral density rises at 3 dB/octave, as shown in Figure 1.51. The power spectral density in this region is inversely proportional to frequency, and therefore the voltage noise spectral density is inversely proportional to the square root of the frequency. For this reason, this noise is commonly referred to as *1/f noise*. Note, however, that some textbooks still use the older term *flicker noise*.



- 1/f Corner Frequency is a figure of merit for op amp noise performance (the lower the better)
- Typical Ranges: 2Hz to 2kHz
- Voltage Noise and Current Noise do not necessarily have the same 1/f corner frequency

Figure 1.51: *1/f Noise bandwidth*

The frequency at which this noise starts to rise is known as the *1/f corner frequency* (F_C) and is a figure of merit—the lower it is, the better. The 1/f corner frequencies are not necessarily the same for the voltage noise and the current noise of a particular amplifier, and a current feedback op amp may have three 1/f corners: for its voltage noise, its inverting input current noise, and its noninverting input current noise.

The general equation which describes the voltage or current noise spectral density in the 1/f region is:

$$e_n, i_n = k\sqrt{F_C}\sqrt{\frac{1}{f}} \qquad \text{Eq. 1-16}$$

where k is the level of the "white" current or voltage noise level, and F_C is the 1/f corner frequency.

The best low frequency, low noise amplifiers have corner frequencies in the range 1 Hz to 10 Hz, while JFET devices and more general purpose op amps have values in the range 100 Hz to sometimes over 1 kHz. Very fast amplifiers, however, may make compromises in processing to achieve high speed which result in quite poor 1/f corners of several hundred Hz or even 1 kHz to 2 kHz. This is generally unimportant in the wideband applications for which they were intended, but may affect their use at audio frequencies, particularly in equalization circuits.

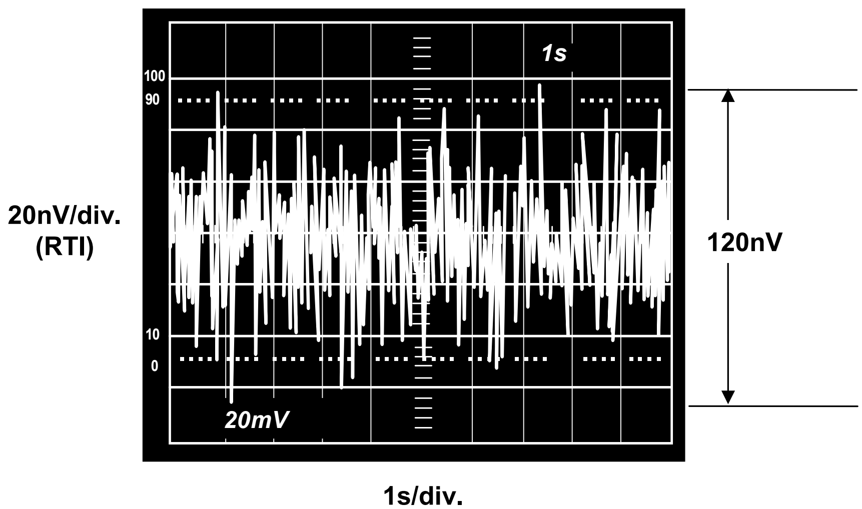


Figure 1.52: *Noise in the 0.1 Hz to 10 Hz. Bandwidth for the OP-213*

Popcorn Noise

Popcorn noise is so-called because when played through an audio system, it sounds like cooking popcorn. It consists of random step changes of offset voltage that take place at random intervals in the 10+ millisecond timeframe. Such noise results from high levels of contamination and crystal lattice dislocation at the surface of the silicon chip, which, in turn, results from inappropriate processing techniques or poor quality raw materials. When monolithic op amps were first introduced in the 1960s, popcorn noise was a dominant noise source. Today, however, the causes of popcorn noise are well understood, raw material purity is high, contamination is low, and production tests for it are reliable so that no op amp manufacturer should have any difficulty in shipping products that are substantially free of popcorn noise. For this reason, it is not even mentioned in most modern op amp textbooks or data sheets.

RMS Noise Considerations

As was discussed above, noise spectral density is a function of frequency. In order to obtain the rms noise, the noise spectral density curve must be integrated over the bandwidth of interest.

In the 1/f region, the rms noise in the bandwidth f_1 to f_2 is given by:

$$e_{rms} = \sqrt{\int_{f_1}^{f_2} \frac{df}{f}} = k\sqrt{\ln \frac{f_2}{f_1}} \qquad \text{Eq. 1-17}$$

where k is the noise spectral density at 1 Hz. The total 1/f noise in a given band is a function of the ratio of the low and high band edge frequencies, since the actual frequency cancels out. It is necessary, however, that the upper band edge is still in the 1/f region for the above formula to be accurate.

It is often desirable to convert rms noise measurements into peak-to-peak. In order to do this, one must have some understanding of the statistical nature of noise. For Gaussian noise and a given value of rms noise, statistics tell us that the chance of a particular peak-to-peak value being exceeded decreases sharply as that value increases—but this probability never becomes zero.

NOMINAL PEAK-TO-PEAK	% OF THE TIME NOISE WILL EXCEED NOMINAL PEAK-TO-PEAK VALUE
2 × rms	32%
3 × rms	13%
4 × rms	4.6%
5 × rms	1.2%
6 × rms	0.27%
6.6 × rms**	0.10%
7 × rms	0.046%
8 × rms	0.006%

**MOST OFTEN USED CONVERSION FACTOR IS 6.6

Figure 1.53: *RMS to Peak-to-Peak voltage Comparison Chart*

Thus, for a given rms noise, it is possible to predict the percentage of time that a given peak-to-peak value will be exceeded, but it is not possible to give a peak-to-peak value which will never be exceeded as shown in Figure 1.53.

Peak-to-peak noise specs, therefore, must always be given for a specified time limit. The most common choice is for the peak-to-peak noise to be 6.6 times the rms value, which means the peak-to-peak level will be exceeded only 0.1% of the time.

In many cases, the low frequency noise is specified as a peak-to-peak value within the bandwidth 0.1 Hz to 10 Hz. This is measured by inserting a 0.1 Hz to 10 Hz band-pass filter between the op amp and the measuring device. The measurement is often presented as a scope photo with a time scale of 1 s/div as shown in Figure 1.54 for the OP-213.

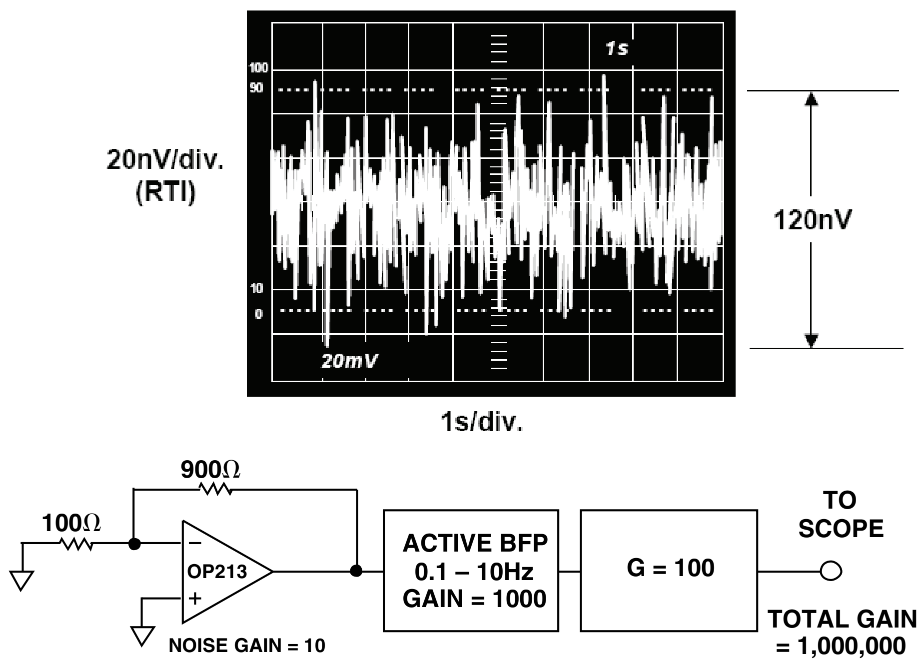


Figure 1.54: *The Peak-to-Peak Noise in the 0.1 Hz to 10 Hz Bandwidth for the OP213 is Less Than 120 nV*

In practice, it is virtually impossible to measure noise within specific frequency limits with no contribution from outside those limits, since practical filters have finite roll-off characteristics. Fortunately, the measurement error introduced by a single-pole low-pass filter is readily computed. See the previous section on noise bandwidth.

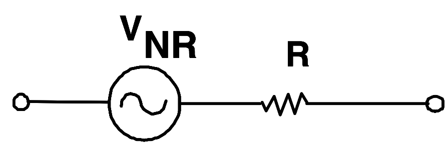
When computing rms noise for wide bandwidth op amps, 1/f noise becomes relatively insignificant. The dominant source of noise is *Gaussian*, or white noise. This noise has a relatively constant noise spectral density over a wide range of frequencies. The rms noise calculation is made by multiplying the noise spectral density by the square root of the equivalent noise bandwidth.

Total Output Noise Calculations

We have already pointed out that any noise source which produces less than one third to one fifth of the noise of some other source can be ignored. (Both noise voltages must be measured at the same point in the circuit.) To analyze the noise performance of an op amp circuit, we must assess the noise contributions of each part of the circuit and determine which are significant. To simplify the following calculations, we shall work with noise spectral densities, rather than actual voltages, to leave bandwidth out of the expressions (the noise spectral density, which is generally expressed in $\mu V/\sqrt{Hz}$, is equivalent to the noise in a 1 Hz bandwidth).

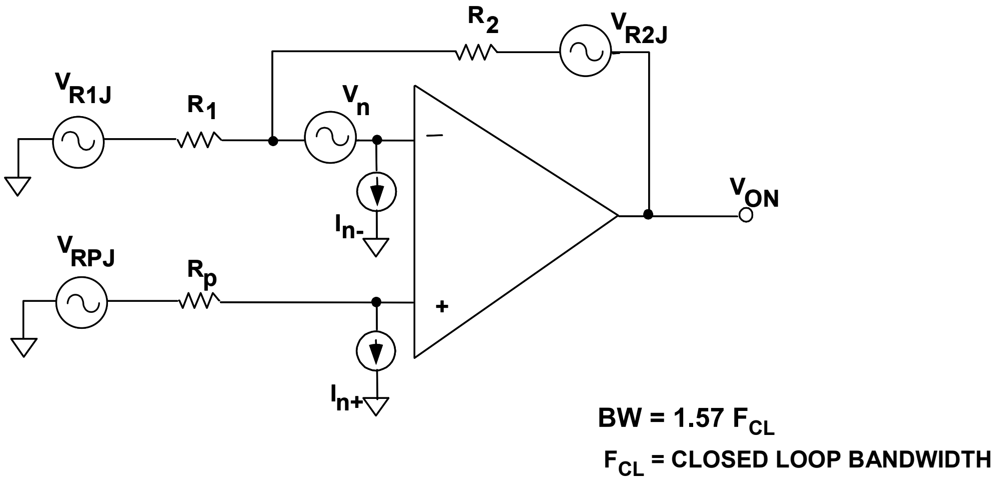
All resistors have a Johnson noise of $\sqrt{4kTBR}$, where k is Boltzmann's Constant (1.38×10^{-23}J/°K), T is the absolute temperature, B is the bandwidth, and R is the resistance. This is intrinsic—it is not possible to obtain resistors which do not have Johnson noise (unless operated a 0°K).

If we consider the circuit in Figure 1.56, which is an amplifier consisting of an op amp and three resistors (R_p represents the source resistance at node A), we can find six separate noise sources: the Johnson noise of the three resistors, the op amp voltage noise, and the current noise in each input of the op amp. Each has its own contribution to the noise at the amplifier output. (Noise is generally specified RTI, or *referred to the input*, but it is often simpler to calculate the noise at the output and then divide it by the *signal* gain (not the *noise* gain) of the amplifier to obtain the RTI noise).



- **ALL resistors have a voltage noise of $V_{NR} = \sqrt{(4kTBR)}$**
- **T = Absolute Temperature = T (°C) + 273.15**
- **B = Bandwidth (Hz)**
- **k = Boltzmann's Constant (1.38×10^{-23} J/K)**
- **A 1000Ω resistor generates 4 nV / √Hz @ 25°C**

Figure 1.55: *Resistor Noise*



$$V_{ON} = \sqrt{BW}\sqrt{[(In-^{2})R_2^{2}]\,[NG] + [(In+^{2})R_P^{2}]\,[NG] + V_N^{2}\,[NG] + 4kTR_2\,[NG-1] + 4kTR_1\,[NG-1] + 4kTR_P\,[NG]}$$

Figure 1.56: *Total Noise Calculation*

The circuit in Figure 1.57 represents a second-order system, where capacitor C_1 represents the source capacitance, stray capacitance on the inverting input, the input capacitance of the op amp, or any combination of these. C_1 causes a breakpoint in the noise gain, and C_2 is the capacitor which must be added to obtain stability. Because of C_1 and C_2, the noise gain is a function of frequency, and has peaking at the higher frequencies (assuming C_2 is selected to make the second-order system critically damped).

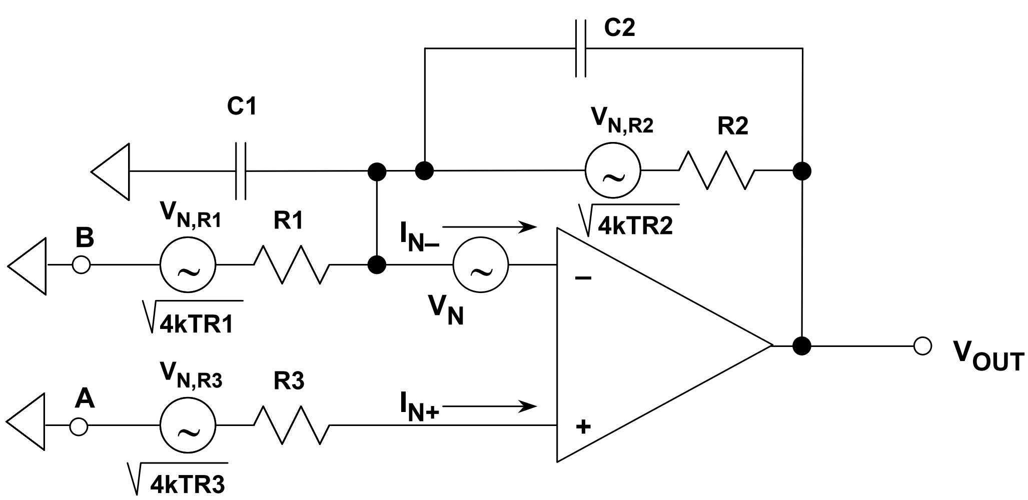


Figure 1.57: *Second Order Noise Model*

A dc signal applied to input A (B being grounded) sees a gain of:

$$1 + R_2/R_1 = \text{DC Noise Gain} \quad [1a] \qquad \text{Eq. 1-18}$$

At higher frequencies, the gain from input A to the output becomes:

$$1 + C_2/C_1 = \text{AC Noise Gain} \qquad \text{Eq. 1-19}$$

The closed-loop bandwidth f_{cl} is the point at which the Noise Gain intersects the open-loop gain.

A dc signal applied to B (A being grounded) sees a gain of:

$$-R_2/R_1 \qquad \text{Eq. 1-20}$$

with a high frequency cutoff determined by R_2C_2:

$$\text{Bandwidth (B to Output)} = 1/2\pi R_2C_2 \qquad \text{Eq. 1-21}$$

These are the noninverting and inverting gains and bandwidths, respectively, of the amplifier.

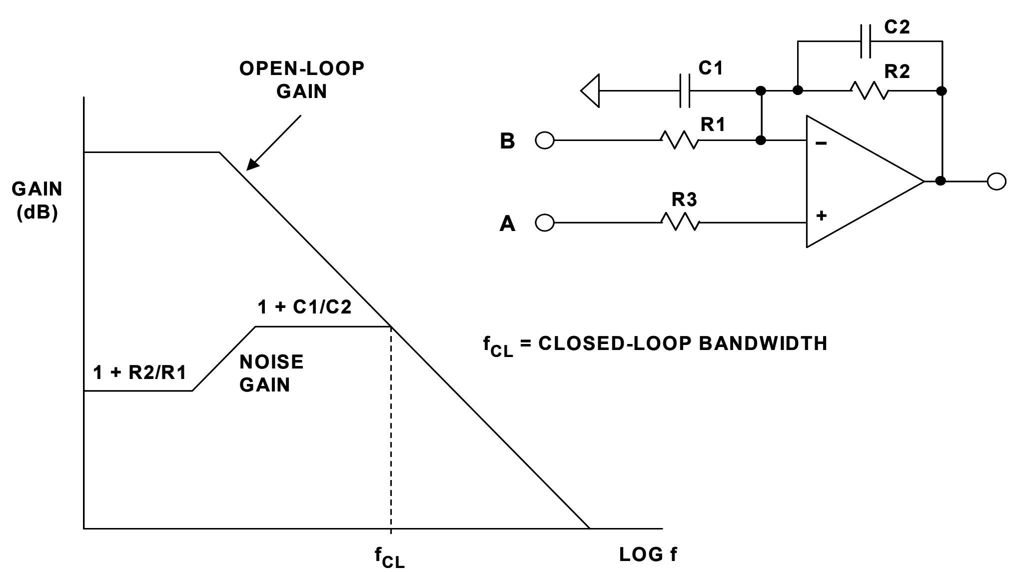


Figure 1.58: *Second-Order System Noise Gain*

The current noise of the noninverting input, I_{n+}, flows in R_p and gives rise to a noise voltage of $I_{n+}R_p$, which is amplified by [1a, 1b], as are the op amp noise voltage, V_n, and the Johnson noise of R_p, which is $\sqrt{4kTR_p}$. The Johnson noise of R_1 is amplified by [2a] over a bandwidth of $1/2\pi R_2C_2$ [2b], and the Johnson noise of R_2 is not amplified at all but is buffered directly to the output over a bandwidth of $1/2\pi R_2C_2$. The current noise of the inverting input, I_{n-}, does not flow in R_1, as might be expected—negative feedback around the amplifier works to keep the potential at the inverting input unchanged, so that a current flowing from that pin is forced, by negative feedback, to flow in R_2 only, resulting in a voltage at the amplifier output of $I_{n-}R_2$ over a bandwidth of $1/2\pi R_2C_2$ (we could equally well consider the voltage caused by I_{n-} flowing in the parallel combination of R_1 and R_2 and then amplified by the noise gain of the amplifier (see below), but the results are identical—only the calculations are more involved).

If we consider these six noise contributions, we see that if R_p and R_2 are low, then the effect of current noise and Johnson noise will be minimized, and the dominant noise will be the op amp's voltage noise. As we increase resistance, both Johnson noise and the voltage noise produced by noise currents will rise. If noise currents are low, then Johnson noise will take over from voltage noise as the dominant contributor. Johnson noise, however, rises with the square root of the resistance, while the current noise voltage rises linearly with resistance, so ultimately, as the resistance continues to rise, the voltage due to noise currents will become dominant.

These noise contributions we have analyzed are not affected by whether the input is connected to node A or node B (the other being grounded or connected to some other low impedance voltage source), which is why the noninverting gain $(1 + R_2/R_1)$, which is seen by the voltage noise of the op amp, V_n, is known as the "noise gain" of the amplifier.

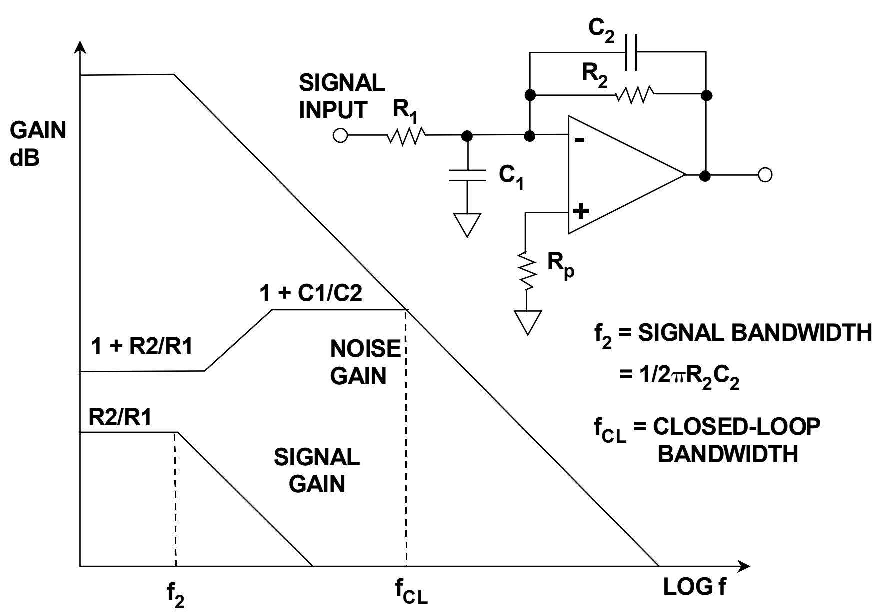
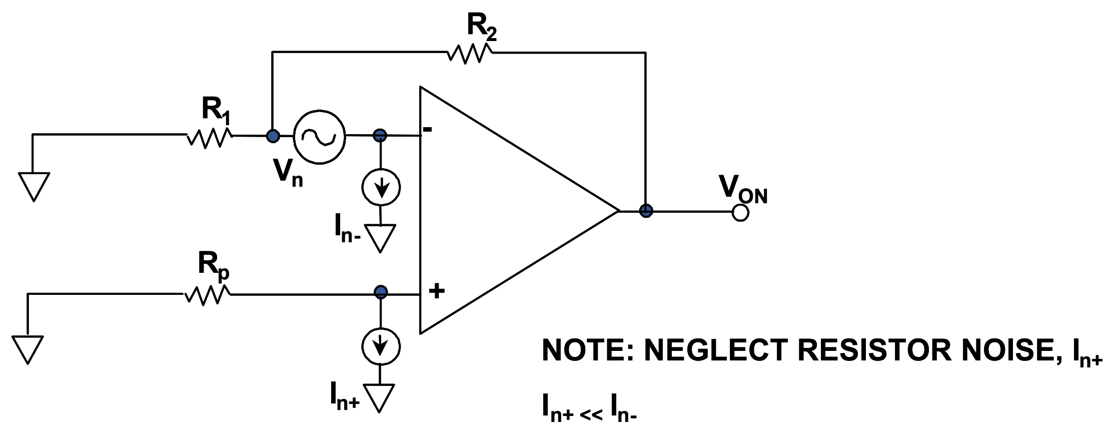


Figure 1.59: Noise and Signal Gain for a Second-Order System

Calculating the total output rms noise of the op amp requires multiplying each of the six noise voltages by the appropriate gain and integrating over the appropriate frequency. The root-sum-square of all the output contributions then represents the total rms output noise. Fortunately, this cumbersome exercise may be greatly simplified in most cases by making the appropriate assumptions.

The noise gain for a typical second-order system is shown in Figure 1.58. It is quite easy to perform the voltage noise integration in two steps, but notice that because of peaking, the majority of the output noise due to the input voltage noise will be determined by the high frequency portion where the noise gain is $1 + C_1/C_2$ This type of response is typical of second-order systems. The noise due to the inverting input current noise, R_1, and R_2 is only integrated over the bandwidth $1/2\pi R_2C_2$.

In high speed op amp applications, there are some further simplifications which can be made. The noise gain plot for a first-order system optimized for fast settling time is usually flat up to the closed-loop bandwidth frequency, with only a dB or so of gain peaking at the most. All noise sources may therefore be integrated over the closed-loop op amp bandwidth.



$$V_{ON} = \sqrt{1.57 f_{cl}}\ \sqrt{\left[V_n^2\left(1+\frac{R_2}{R_1}\right)\right]^2 + I_{n-}^2\, R_2^2}$$

f_{cl} = CLOSED LOOP BANDWIDTH

Figure 1.60: *Current Feedback Amp Noise Model*

In high speed current feedback op amp circuits, the input voltage noise and the inverting input current noise are the dominant contributors to the output noise as shown in Figure 1.60.

Distortion

Dynamic range of an op amp may be defined in several ways. One of the most common ways is to specify *harmonic distortion*, *total harmonic distortion* (THD), or *total harmonic distortion plus noise* (THD + N). Other related specs include *intermodulation distortion* (IMD), *intercept points* (IP), *spurious-free dynamic range* (SFDR), and *multitone power ratio* (MTPR), among others.

THD (Total Harmonic Distortion)

THD is the ratio of the harmonically related (2X, 3X, 4X, and so on the fundamental frequency) signal components caused by amplifier nonlinearity. Only the harmonically related signals are included in the measurement. The distortion components which make up total harmonic distortion are usually calculated by taking the square root of the sum of the squares of the first five or six harmonics of the fundamental. In many practical situations, however, there is negligible error if only the second and third harmonics are included since the higher order terms most often are greatly reduced in amplitude.

THD + N (Total Harmonic Distortion plus Noise)

THD + N is the residual signal with only the fundamental removed. It is important to note that the THD measurement does not include noise terms, while THD + N does. The noise in the THD + N measurement must be integrated over the measurement bandwidth. In narrow-band applications, the level of the noise may be reduced by filtering, in turn lowering the THD + N which increases the signal-to-noise ratio (SNR). Most times when a THD spec is quoted, it is really a THD + N spec, since most measurement systems do not differentiate harmonically related signals from the other signals. The THD measurement is generally made by notching out the fundamental signal and measuring the remaining signal (the residual). The definition of THD and THD + N is shown in Figure 1.60.

- **V_S = Signal Amplitude (RMS Volts)**
- **V_2 = Second Harmonic Amplitude (RMS Volts)**
- **V_n = nth Harmonic Amplitude (RMS Volts)**
- **V_{noise} = RMS value of noise over measurement bandwidth**
- $$\mathrm{THD + N} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2 + V_{noise}^2}}{V_S}$$
- $$\mathrm{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2}}{V_S}$$

Figure 1.61: *THD & THD + N Definitions*

Intermodulation Distortion (IMD)

Rather than simply examining the THD produced by a single tone sine wave input, it is often useful to look at the distortion products produced by two tones. As shown in Figure 1.61 two tones will produce intermodulation products. Intermodulation occurs when two (or more) signals are passed through a nonlinear system. And all systems are nonlinear, to some degree. Intermodulation products consist of sum and difference frequencies. The example shows the second and third order products produced by applying two frequencies, f_1 and f_2, to a nonlinear system. The second order products located at $f_2 + f_1$ and $f_2 – f_1$ are located relatively far away from the two tones, and may possibly be removed by filtering, depending on the bandwidth of the system. If the system is wideband, these distortion products may still be inband. The third order products located at $2f_1 + f_2$ and $2f_2 + f_1$ may likewise possibly be filtered. The third order products located at $2f_1 – f_2$ and $2f_2 – f_1$, however, are close to the original tones, and filtering them is difficult.

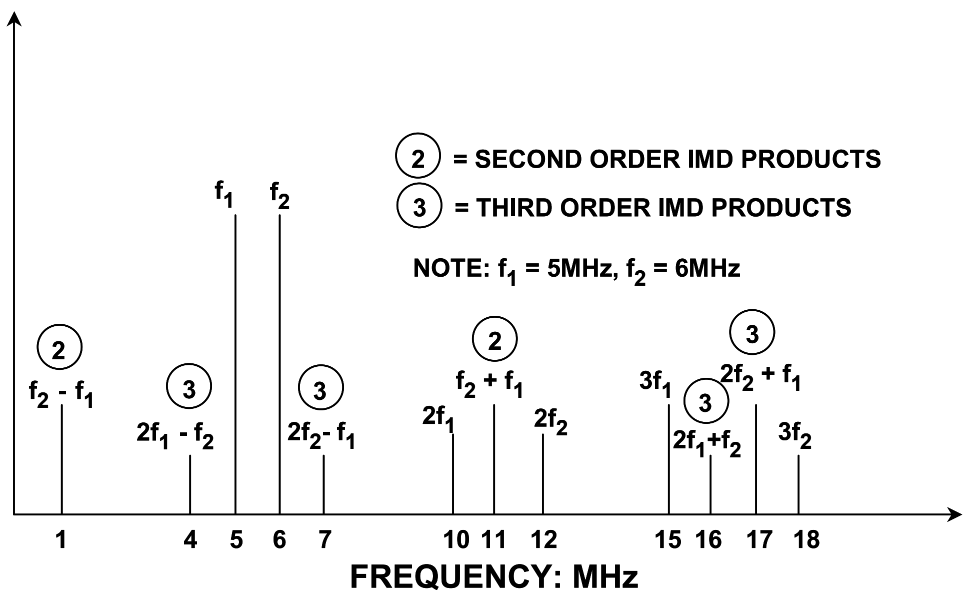


Figure 1.62: *Intermodulation Distortion Products*

Third-Order Intercept Point (IP3), Second-Order Intercept Point (IP2)

Intermodulation distortion products are of special interest in the RF area, and a major concern in the design of radio receivers. Third-order IMD products can mask out small signals in the presence of larger adjacent ones. Third order IMD is often specified in terms of the *third-order intercept point* (IP3) as shown in Figure 1.63.

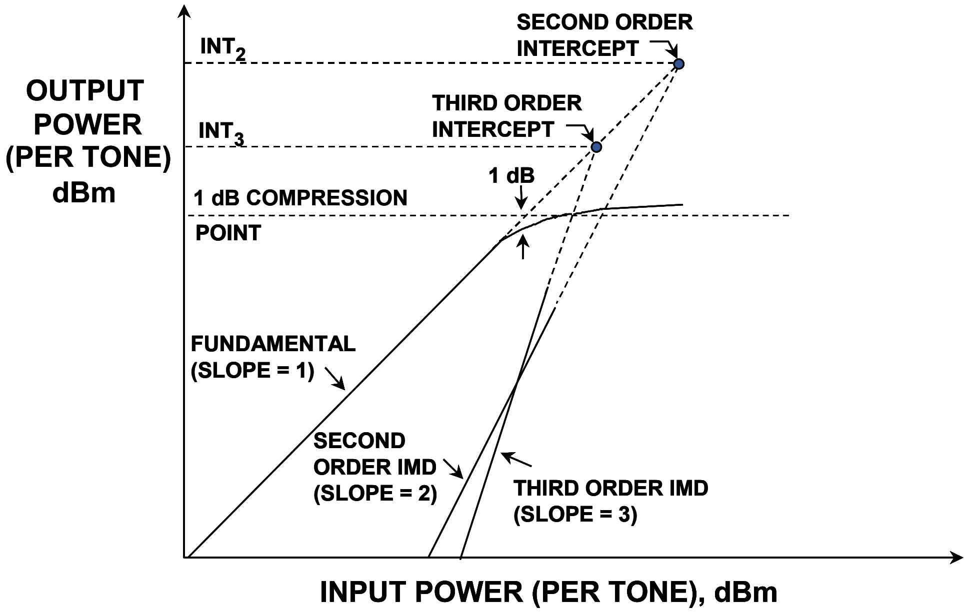


Figure 1.63: *IMD, Intercept Points, and Gain Compression*

If the system nonlinearity is approximated by a power series expansion, the second-order IMD amplitudes increase 2 dB for every 1 dB of signal increase. Similarly, the third-order IMD amplitudes increase 3 dB for every 1 dB of signal increase. Once the input reaches a certain level, however, the output signal begins to soft-limit, or compress due to things like power supply limits, output drive maximums and the like. But the second- and third-order intercept lines may be extended to intersect the extension of the output signal line. These intersections are called the *second-* and *third-order intercept points*, respectively. The values are usually referenced to the output power of the device expressed in dBm. So, while the IP3 point most often will never be reached in practice, it is still used as a figure of merit in high speed systems.

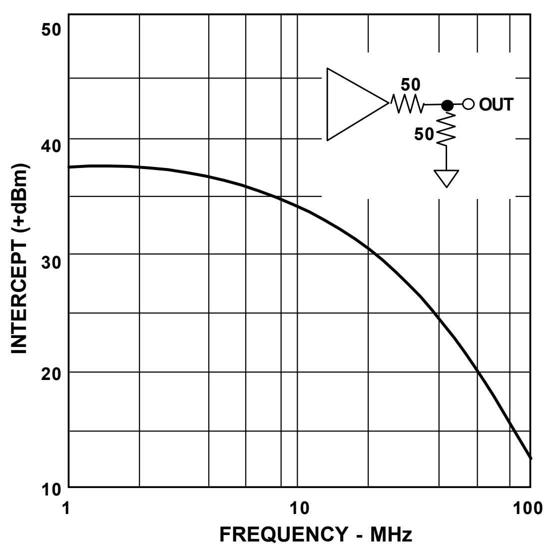


Figure 1.64: *Typical IP3 Variation with Frequency*

To determine the IP3 point, two spectrally pure tones are applied to the system. The output signal power of a single tone (in dBm) as well as the relative amplitude of the third-order products (referenced to a single tone) is plotted as a function of input signal power. With a low level (well below clipping) two-tone input signal, and two data points, draw the second and third order IMD lines as are shown in Figure 1.62, because one point and a slope determine each straight line. Where they intersect will be the *second-* and *third-order intercept points*, respectively.

Figure 1.64 shows the third-order intercept value as a function of frequency for a typical voltage feedback amplifier.

Assume the op amp output signal is 5 MHz and 2 V peak-to-peak into a 100 Ω load (50 Ω source and load termination). The voltage into the 50 Ω load is therefore 1 V peak-to-peak, corresponding to +4 dBm. The value of the third-order intercept at 5 MHz is 36 dBm. The difference between +36 dBm and +4 dBm is 32 dB. This value is then multiplied by 2 to yield 64 dB (the value of the third-order intermodulation products referenced to the power in a single tone). Therefore, the intermodulation products should be –64 dBc (dB below carrier frequency), or at a level of –60 dBm. Figure 1.62 shows the graphical analysis for this example.

1 dB Compression Point

Another parameter, which may be of interest, is the *1 dB compression point*. This is the point at which the output signal is compressed by 1 dB from the ideal input/output transfer function. This occurs when the dynamic range of the amplifier output is reached and the output will not increase no matter how much the input to the amplifier increases (i.e., clipping). This point is also shown in Figure 1.63.

SNR (Signal-to-Noise Ratio)

The signal-to-noise ratio is the dynamic range of the system, usually expressed in dB. The reference level is the maximum signal level and the rms level of the noise is the floor. The bandwidth of the measurement must be specified.

ENOB (Equivalent Number of Bits)

If we take the SNR of the op amp and express it in bits we have ENOBs. The conversion formula is:

$$\text{ENOB} = \frac{\text{SNR (in dB)} - 1.76}{6.02} \qquad \text{Eq. 1-22}$$

Although we would mainly think of bits in converter applications, it is sometimes used in the context of op amps. Again, the bandwidth of the measurement must be specified.

Spurious-Free Dynamic Range (SFDR)

SFDR is another measure of the dynamic range of the system. It can be measured two ways. The first is the difference between the maximum signal and the 1st distortion component of any type. It would be measured in dB. This would be the SFDR in dBFS. The other way to measure it is in relation to the actual signal strength. This would be the SFDR in dBc (meaning relative to the carrier). While this is again more commonly a converter spec, we sometimes see SFDR used in reference to op amps.

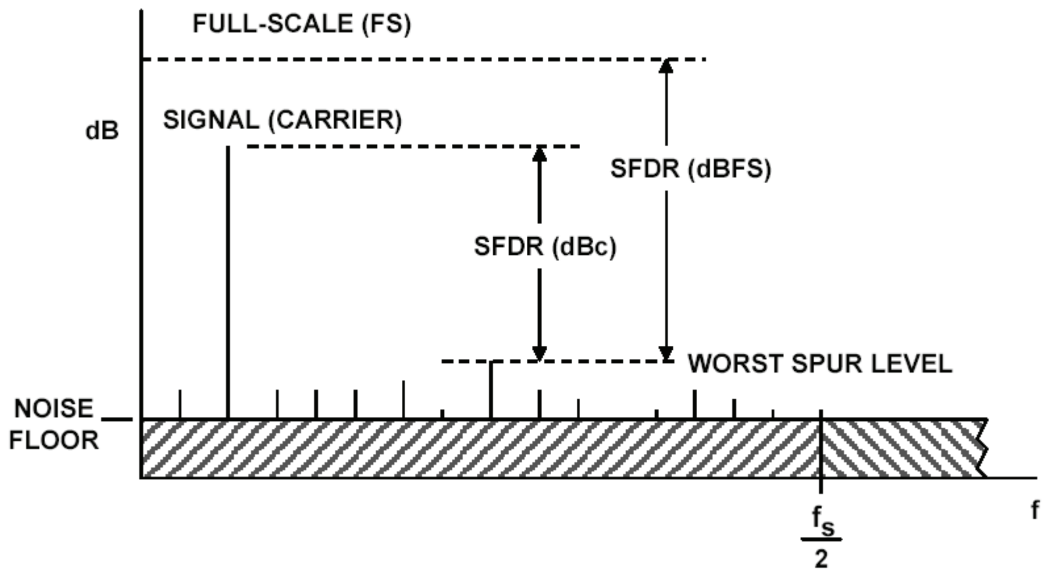


Figure 1.65: *Spurious-Free Dynamic Range (SFDR)*

Slew Rate

The slew rate of an amplifier is the maximum rate of change of voltage at its output. It is expressed in V/s (or, more probably, V/μs). Op amps may have different slew rates during positive- and negative going transitions, due to circuit design, but for this analysis we shall assume that good fast op amps have reasonably symmetrical slew rates.

If we consider a sine wave with a p-p amplitude of 2 V_p and frequency f, the expression for the output voltage is:

$$v(t) = V_p \sin 2\pi f t \qquad \text{Eq. 1-23}$$

This has a maximum slew rate:

$$\left.\frac{dv}{dt}\right|_{max} = 2\pi f V_p \qquad \text{Eq. 1-24}$$

One note here—many high speed amplifiers will have overshoot. This means the output will go beyond the final value and will then have a damped oscillation around the final value. This is call "ringing." The amount of overshoot and ringing will be an indication of the phase margin of the amplifier. The higher the overshoot and the more ringing, the less phase margin.

The slew rate is generally measured between 10% and 90% of the final value (although 20% to 80% is sometimes also used).

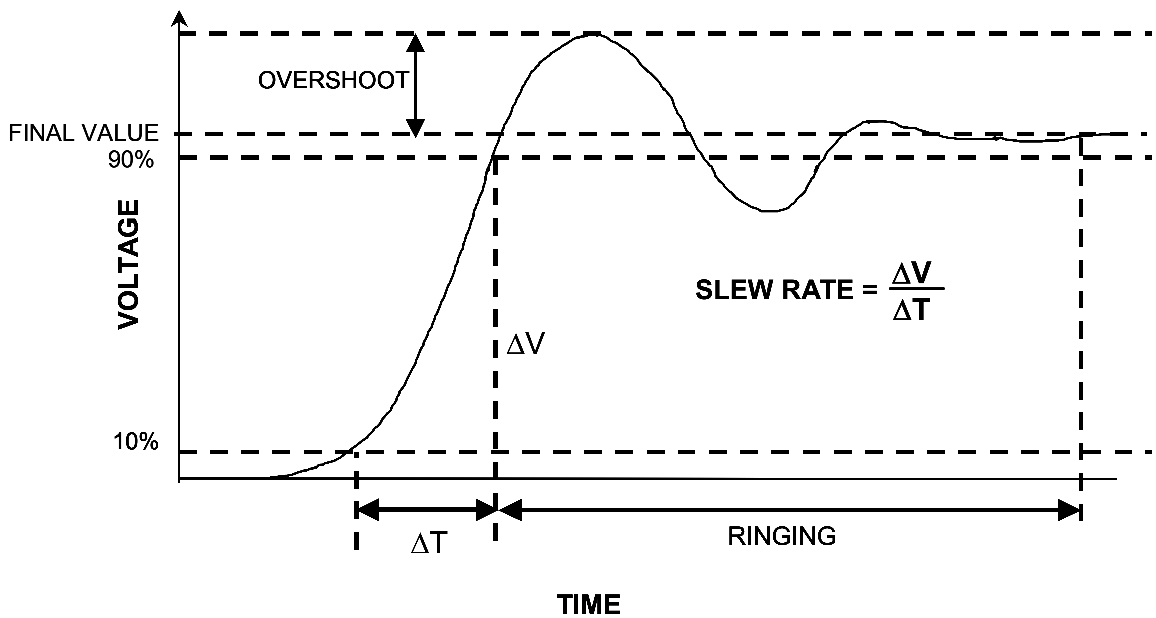


Figure 1.66: *Slew Rate*

Full Power Bandwidth

The maximum output frequency at which slew limiting *occurs* is directly proportional to slew rate and inversely proportional to the amplitude of the signal. This allows us to define the "full-power bandwidth" (FPBW) of an op amp.

$$FPBW = \text{Slew Rate}/2\pi Vp \qquad \text{Eq. 1-25}$$

It is important to realize that both slew rate and full-power bandwidth can also depend somewhat on the power supply voltage being used and the load the amplifier is driving (particularly capacitive).

In practice, the FPBW of the op amp should be approximately 5 to 10 times the maximum output frequency in order to achieve acceptable distortion performance.

Slew Rate = Maximum rate at which the output voltage of an op amp can change

Ranges: A few volts / μs to several thousand volts / μs

For a sinewave, $V_{out} = V_p \sin 2\pi f t$

$$dV/dt = 2\pi f V_p \cos 2\pi f t$$

$$(dV/dt)_{max} = 2\pi f V_p$$

If $2V_p$ = full output span of op amp, then

$$\text{Slew Rate} = (dV/dt)_{max} = 2\pi * \text{FPBW} * V_p$$

$$\text{FPBW} = \text{Slew Rate} / 2\pi V_p$$

Figure 1.67: *Slew Rate and Full Power Bandwidth*

−3 dB Small Signal Bandwidth

The –3 dB bandwidth of an op amp will almost always be greater than the full power bandwidth. This is because the signal doesn't have to swing as far. Since Vp is reduced the bandwidth is increased.

Bandwidth for 0.1 dB Flatness

In demanding applications such as professional video, it is desirable to maintain a relatively flat bandwidth and linear phase up to some maximum specified frequency. This is because a change in gain or phase of the system will affect the color intensity or hue.

Simply specifying the 3 dB bandwidth isn't enough. It has become customary to specify the *0.1 dB bandwidth*, or *0.1 dB bandwidth flatness*. This means there is no more than 0.1 dB ripple up to a specified 0.1 dB bandwidth frequency. Video buffer amplifiers generally have both the 3 dB and the 0.1 dB bandwidth specified. Figure 1.68 shows the frequency response of the AD8075 triple video buffer.

Note that the 3 dB bandwidth is approximately 400 MHz. This can be determined from the response labeled "GAIN" in the graph, and the corresponding gain scale is shown on the left-hand vertical axis (at a scaling of 1 dB/division). The response scale for "FLATNESS" is on the right-hand vertical axis, at a scaling of 0.1 dB/division in this case. This allows the 0.1 dB bandwidth to be determined, which is about 65 MHz in this case. The major difference in the applicable bandwidth between the 3 dB and 0.1 dB criteria. It requires a 400 MHz bandwidth amplifier (as conventionally measured) to provide the 65 MHz 0.1 dB flatness rating.

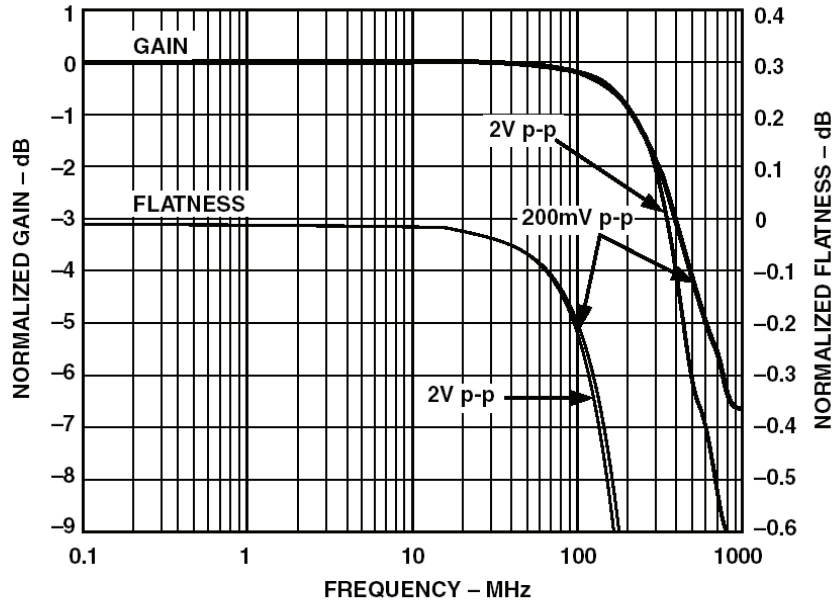


***Figure 1.68**: 0.1 dB Gain Flatness*

It should be noted that these specs hold true when driving a 75 Ω source and load terminated cable, which represents a resistive load of 150 Ω. Any capacitive loading at the amplifier output could cause peaking in the frequency response, and should be avoided.

Gain-Bandwidth Product

For a VFB amplifier, if the gain at any particular frequency is multiplied by that frequency, the product is a constant. This is because in a 1st order system a doubling of frequency causes a reduction in gain by a factor of 2. Therefore, this product becomes a useful figure of merit in comparing the bandwidth of op amps.

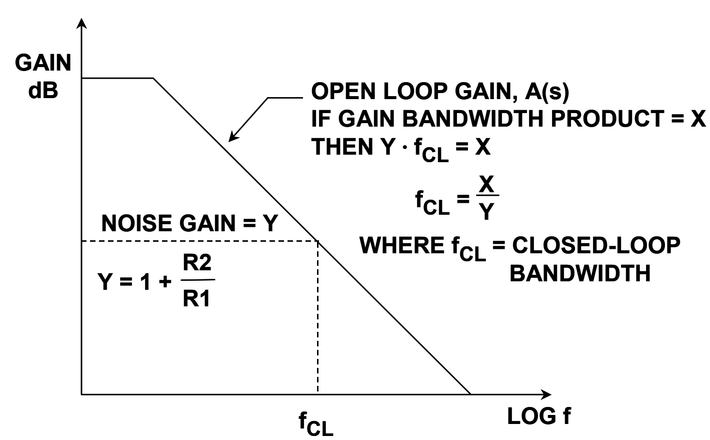


***Figure 1.69:** Gain-Bandwidth Product*

CFB Frequency Dependence

Current feedback op amps do not behave in the same way as voltage feedback types. They are not stable with capacitive feedback, nor are they so with a short circuit from output to inverting input. With a CFB op amp, *there is an optimum feedback resistance for maximum bandwidth.* Note that the value of this resistance may vary with supply voltage. If the feedback resistance is increased, the bandwidth is reduced. Conversely, if it is reduced, bandwidth increases, and the amplifier may become unstable.

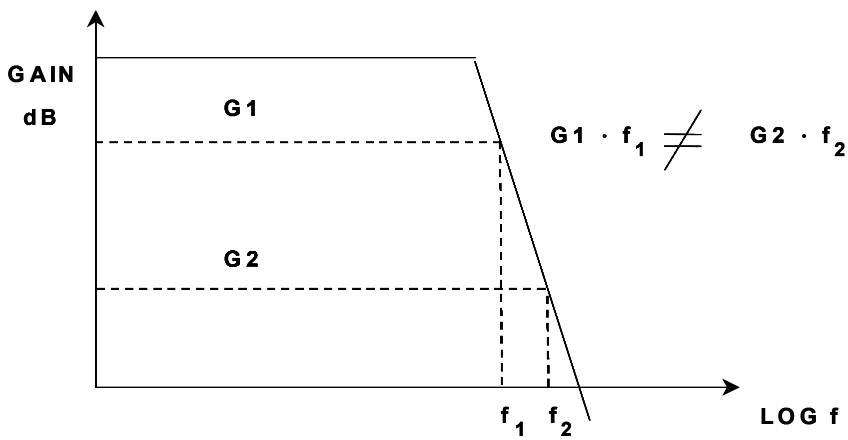


Figure 1.70: *CFB Op Amp Open-Loop Gain*

In a CFB op amp, for a given value of feedback resistance , *the closed-loop bandwidth is largely unaffected by the noise gain*, as shown in Figure 1.70. Thus it is not correct to refer to gain-bandwidth product, for a CFB amplifier, because of the fact that it is not constant. Gain is manipulated in a CFB op amp application by choosing the correct feedback resistor for the device, and then selecting the input resistor to yield the desired closed-loop gain. The signal gain (as determined by the feedback network) of a current feedback amplifier is identical to the case of a VFB op amp.

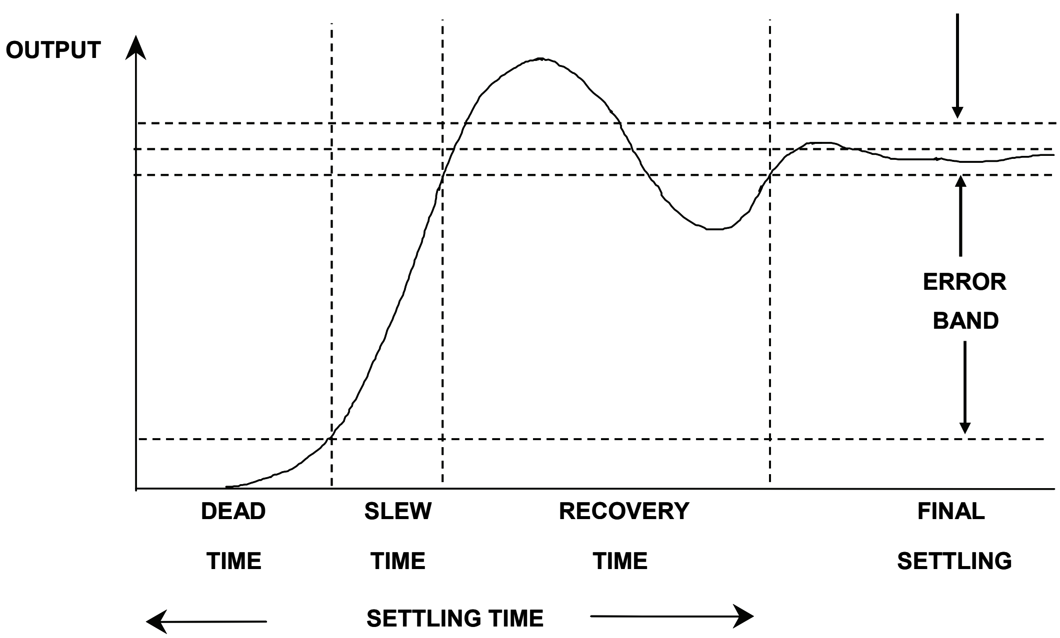
	AD8001AN (PDIP) Gain					AD8001AR (SOIC) Gain					AD8001ART (SOT-23-5) Gain				
Component	–1	+1	+2	+10	+100	–1	+1	+2	+10	+100	–1	+1	+2	+10	+100
R_F (Ω)	649	1050	750	470	1000	604	953	681	470	1000	845	1000	768	470	1000
R_G (Ω)	649		750	51	10	604		681	51	10	845		768	51	10
R_O (Nominal) (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9
R_S (Ω)	0					0					0				
R_T (Nominal) (Ω)	54.9	49.9	49.9	49.9	49.9	54.9	49.9	49.9	49.9	49.9	54.9	49.9	49.9	49.9	49.9
Small Signal BW (MHz)	340	880	460	260	20	370	710	440	260	20	240	795	380	260	20
0.1 db Flatness (MHz)	105	70	105			130	100	120			110	300	145		

Figure 1.71: *Recommended Feedback Resistor Values for the AD8001*

Typically, CFB op amp data sheets will provide a table of recommended resistor values, which provide maximum bandwidth for the device, over a range of gain, supply voltage and package type. It simplifies the design process considerably to use these tables.

Settling Time

The settling time of an amplifier is defined as the time it takes the output to respond to a step change of input and come within *and remain within* a defined error band, as measured relative to the 50% point of the input pulse (see Figure 1.72). There is no natural error band for an op amp (a DAC naturally has an error band of 1 LSB, or perhaps ±1 LSB), so one must be chosen and defined. What is chosen will depend on the performance of the op amp, but since the value chosen will vary from device to device, comparisons are very difficult. This is true because settling is not linear, and many different time constants may be involved. Examples are early op amps using dielectrically isolated (DI) processes. These had very fast settling to 1% of full-scale, but they took almost forever to settle to 10 bits (0.1%). Similarly, some very high precision op amps have thermal effects which cause settling to 0.001% or better to take tens of ms, although they will settle to 0.025% in a few μs.



Error band is usually defined to be a percentage of the step 0.1 % 0.05%, 0.01%, etc.

Settling time is non-linear; it may take 30 times as long to settle to 0.01% as to 0.1%.

Manufacturers often choose an error band which makes the op amp look good.

Figure 1.72: *Settling time*

It should also be noted that thermal effects could cause significant differences between short-term settling time (generally measured in nanoseconds) and long-term settling time (generally measured in microseconds or milliseconds). In many ac applications, long-term settling time is not important; but if it is, it must be measured on a much different time scale than short-term settling time.

Rise Time and Fall Time

For high speed op amps we might also have a spec for rise and fall times. While ideally they should be the same, there is typically some difference in practical op amps. Rise and fall times are measured by applying a square wave to the op amp and would be measured on the output waveform. This is closely related to slew rate. Also, as is done with slew rate, we generally measure between the 10% and 90% points, so that overshoot and ringing generally don't enter into the picture. The input wave generally will be full scale, but occasionally it is specified for a smaller input signal. Overall rise and fall times are a less revealing spec than slew rate and settling time.

Phase Margin

Phase margin is the amount of phase shift when the (voltage feedback) amplifier's gain passes through 0 dB. It is basically a measure of how close the 2nd pole of the system is to causing instability. Phase starts to change on the order of a decade before the corner frequency. The phase shift must be less than 180°. The phase margin is the 180°—the actual phase shift of the amplifier. Anything greater than 45° is usually acceptable. The higher the phase margin, the more stable the system. Capacitive loading will reduce the phase margin.

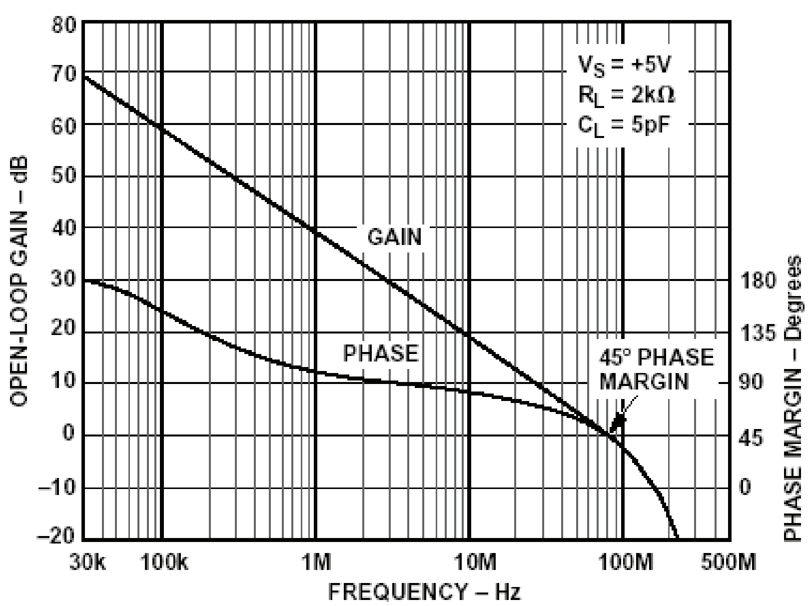


***Figure 1.73**: Phase Margin for the AD8054*

The graph in Fig. 1.73, taken from the data sheet for the AD8054, shows that when the open-loop gain (left scale) falls below 0 dB, the phase margin is around 45° (right scale). This is a respectable value for phase margin. In general, you should avoid phase margins below 20° to 25°.

CMRR (Common-Mode Rejection Ratio)

If a signal is applied equally to both inputs of an op amp, so that the differential input voltage is unaffected, the output should not be affected. In practice, changes in common-mode voltage will produce changes in output. The op amp *common-mode rejection ratio* (CMRR) is the ratio of the common-mode gain to differential-mode gain. For example, if a differential input change of Y volts produces a change of 1 V at the output, and a common-mode change of X volts produces a similar change of 1V, then the CMRR is X/Y. When the common-mode rejection ratio is expressed in dB, it is generally referred to as common-mode rejection (CMR). Typical LF CMR values can be between 70 dB and 120 dB, but at higher frequencies, CMR deteriorates. In addition to a CMRR numeric spec, many op amp data sheets show a plot of CMR versus frequency, as shown in Figure 1.74 for an OP177 op amp.

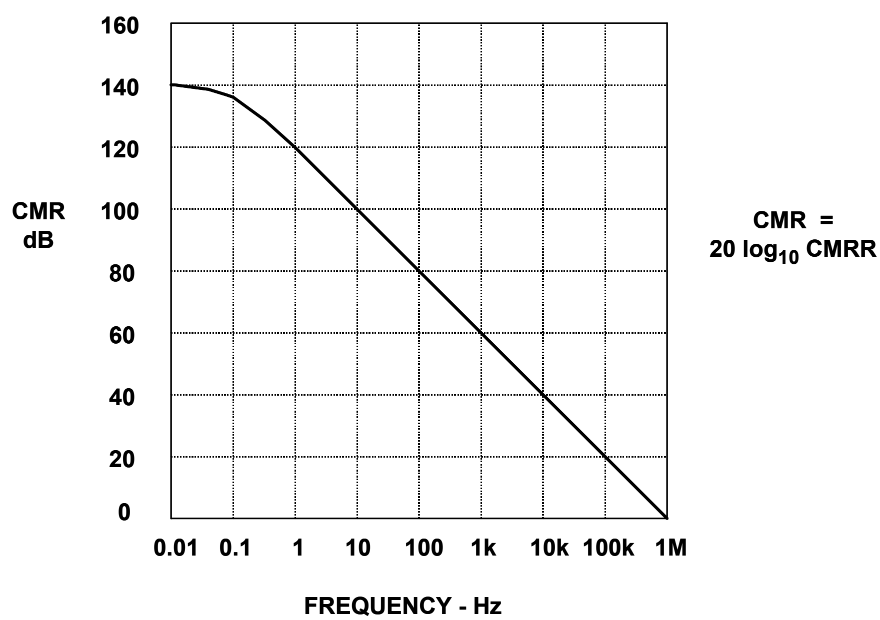


Figure 1.74: *CMRR for the OP177*

CMRR produces a corresponding output offset voltage error in op amps configured in the noninverting mode as shown in Figure 1.74

Note that inverting mode operating op amps will have less CMRR error. Since both inputs are held at a ground (or virtual ground), there is no CM dynamic voltage.

PSRR (Power Supply Rejection Ratio)

If the supply of an op amp changes, its output should not, but it typically does. The spec of *power supply rejection ratio* or PSRR is defined similarly to the definition of CMRR. If a change of X volts in the supply produces the same output change as a differential input change of Y volts, then the PSRR on that supply is X/Y. The definition of PSRR assumes that both supplies are altered equally in opposite directions, otherwise the change will introduce a common-mode change as well as a supply change, and the analysis becomes considerably more complex. It is this effect which causes apparent differences in PSRR between the positive and negative supplies.

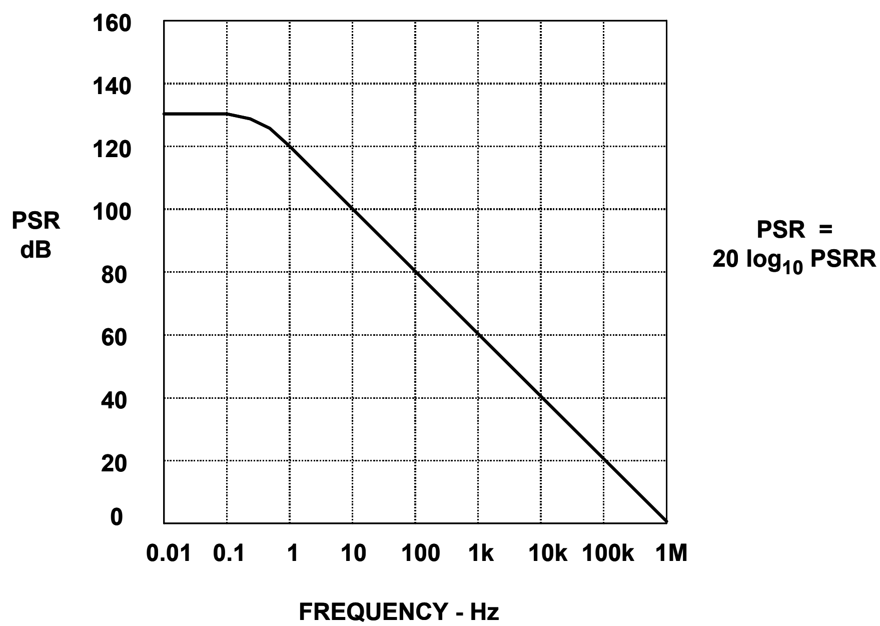


Figure 1.75: *Power Supple Rejection Ratio*

Because op amp PSRR is frequency dependent, op amp power supplies must be well decoupled. At low frequencies, several devices may share a 10 µF to 50 µF capacitor on each supply, provided it is no more than 10 cm (PC track distance) from any of them.

At high frequencies, each IC should have the supply leads decoupled by a low inductance 0.1 µF (or so) capacitor with short leads and PC tracks. These capacitors must also provide a return path for HF currents in the op amp load. Typical decoupling circuits are shown in Figure 1-76. Further bypassing and decoupling information is found in Chapter 12.

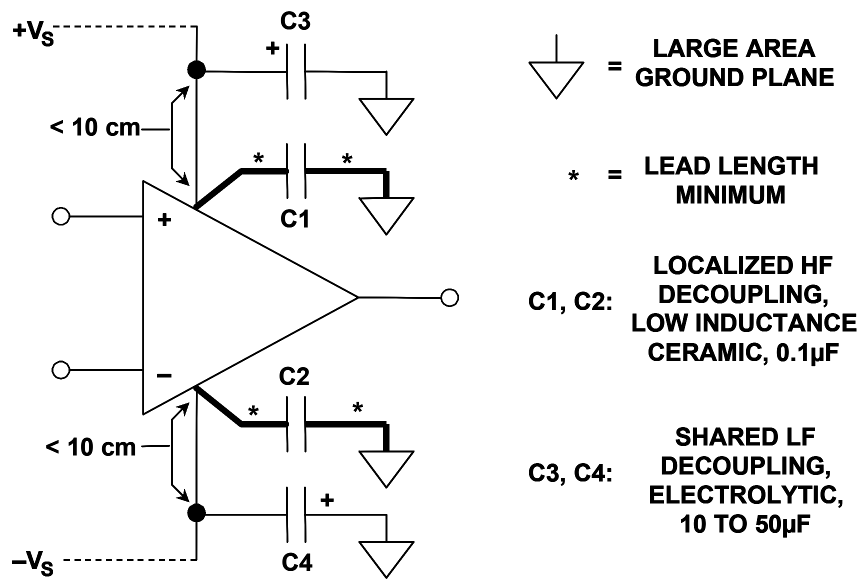


Figure 1.76: *Recommended Power Supply Decoupling*

Differential Gain

Differential gain is a spec that originated for video applications. In early video processing equipment it was found that there was sometimes a change in the gain of the amplifier with dc level. More correctly, differential gain is the change in the color saturation level (amplitude of the color modulation) for a change in low frequency luma (brightness) amplitude. This modulation is obviously a distortion, changing the intensity of the color. Professional video editing equipment commonly strives to keep the total differential gain of the system below 1%. Modern, high performance video op amps have differential gain specs of < .01%.

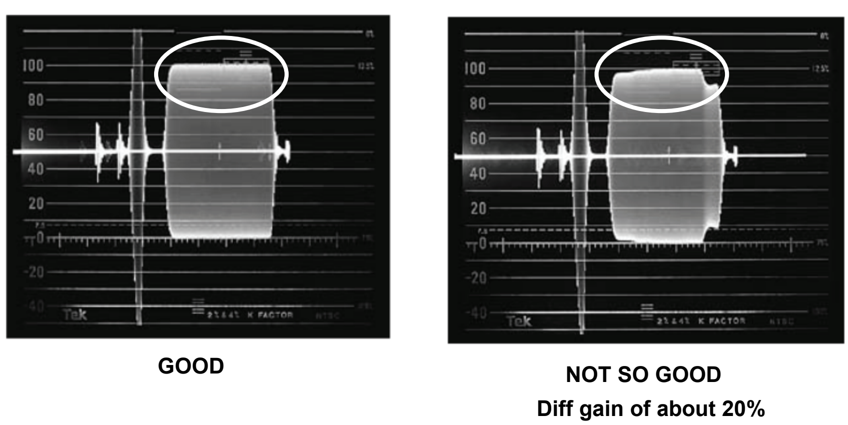


Figure 1.77: *Differential Gain Example*

AD829–SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

DIFFERENTIAL GAIN ERROR[3]	R_{LOAD} = 100 Ω C_{COMP} = 30 pF	±15 V	0.02	0.02	%
DIFFERENTIAL PHASE ERROR[3]	R_{LOAD} = 100 Ω C_{COMP} = 30 pF	±15 V	0.04	0.04	Degrees

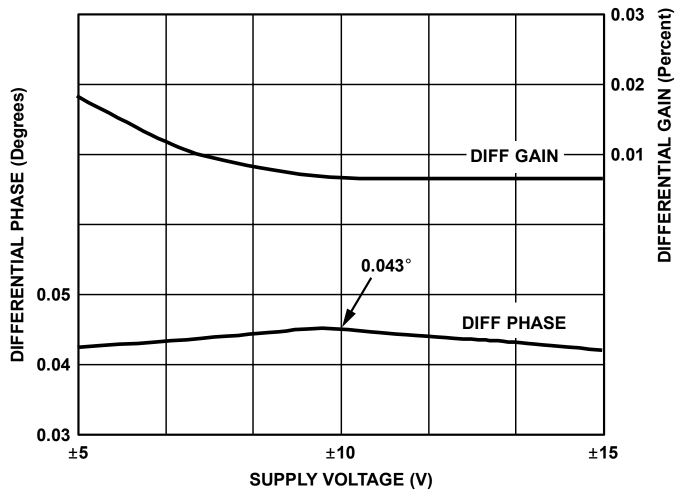


***Figure 1.78:** Differential Gain and Differential Phase Specifications*

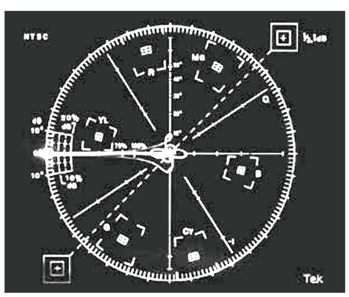


Figure 1.79: Vectorscope Display of a "Good" Signal

Note smearing of display line

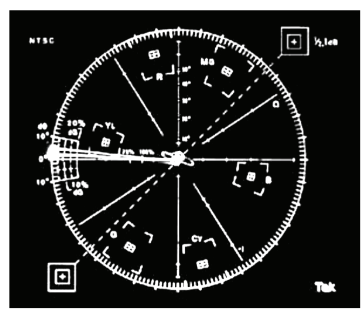


Figure 1.80: Vectorscope Display Showing ~15% Diff Gain

Note curve on display

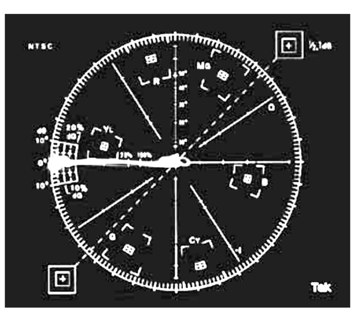


***Figure 1.81:** Vectorscope Display Showing ~5° Diff Phase*

Note both curving & smearing of display line

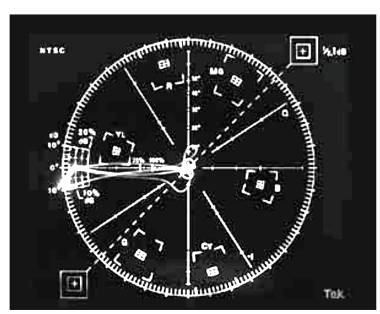


***Figure 1.82:** Vectorscope Display Showing~10% Diff Gain and ~9° Diff Phase*

Differential Phase

Differential phase is the change in hue (phase of the color modulation) for a change in low frequency luma (brightness) amplitude. This modulation is obviously a distortion, changing the hue of the color. Professional video editing equipment commonly strives to keep the total differential phase of the system below 1°. Modern, high performance video op amps have differential gain specs of < .01°.

Phase Reversal

Phase reversal is a problem that occurs in some op amp when the input common-mode of an op amp is exceeded. The mechanism is that one of the internal stages of the op amp no longer has a bias voltage across it and subsequently turns off. The effect is that the output waveform swings to the opposite rail until the input comes back into the common-mode range. See Figure 1.83. This became a big problem with the move toward lower supply voltages and single supplies. Advances in circuit design have resulted in op amps that do not suffer from phase reversal. If the op amp is designed to avoid phase reversal it is generally noted in the bullets or "Key Features" and not necessarily in the specification table.

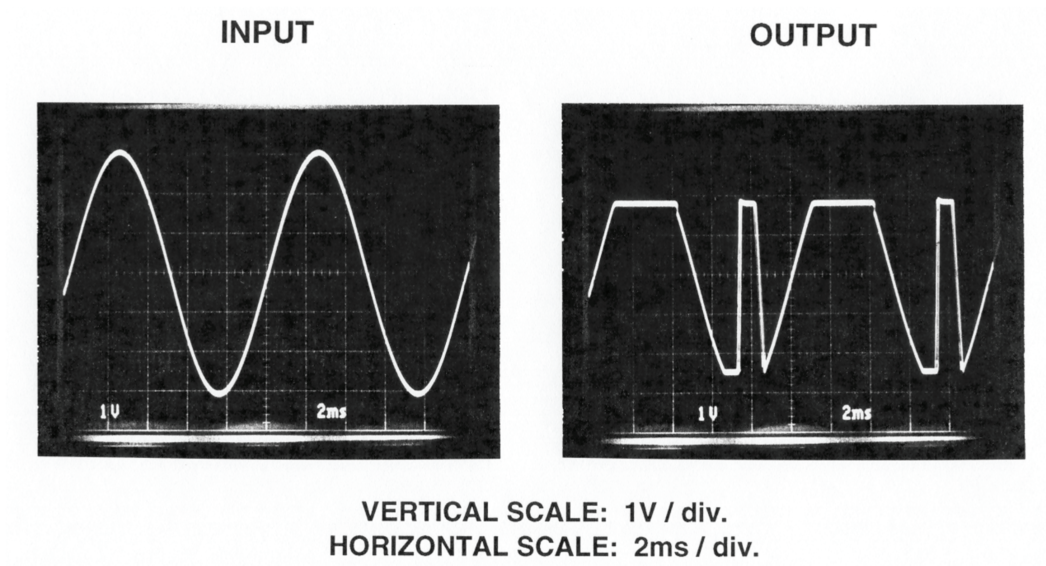


Figure 1.83: *Phase Reversal*

Channel Separation

Channel separation, otherwise known as crosstalk, is a signal that couples from one amplifier in a package to another amplifier in the same package. The path is typically through the power supply, which will typically be shared between the amplifiers. Careful layout of the op amp chip can minimize the crosstalk. Careful external bypassing of the power supplies can also help.

Absolute Maximum Ratings

The absolute maximum ratings are the voltage, current, and temperature limits of the op amp. Exceeding the absolute maximums can lead to the destruction of the op amp.

Applying overvoltage to input pins is one very common way to destroy an op amp. Overvoltage conditions can be broken into two groups, overvoltage and ESD.

ESD voltages typically run to the thousand of volts. Most of us have experienced ESD. Just shuffle your feet across a nylon carpet, especially in a dry environment, and touch a metal doorknob. Sparks will fly from your fingertips. CMOS circuits are especially prone to ESD.

Overvoltages occur when the maximum voltage allowed on the op amp are exceeded. The maximum allowable voltage is typically set by the supply voltage, although there are a few exceptions. An overvoltage on the inputs will typically cause the input devices to turn into an SCR (silicon controlled rectifier) type structure, usually through the substrate.
The failure mechanism is not the overvoltage per se, but instead the current that the overvoltage causes to flow. So if the current is limited, no catastrophic damage will be done. The general rule is to limit the current to 5 mA.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	12.6 V
Internal Power Dissipation @ 25°C[2]	
PDIP Package (N)	1.3 W
SOIC (R)	0.8 W
8-Lead CERDIP	1.1 W
SOT-23-5 Package (RT)	0.5 W
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	±1.2 V
Output Short Circuit Duration	Observe Power Derating Curves
Storage Temperature Range N, R	–65°C to +125°C
Operating Temperature Range (A Grade)	–40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Lead PDIP Package: θ_{JA} = 90°C/W
8-Lead SOIC Package: θ_{JA} = 155°C/W
8-Lead CERDIP Package: θ_{JA} = 110°C/W
5-Lead SOT-23-5 Package: θ_{JA} = 260°C/W

Figure 1.84: *Typical Absolute Maximum Ratings (from AD8001)*

While no catastrophic damage will be done, continually overstressing the inputs can cause a change in parameters like bias current and offset voltage. So even though you won't necessarily destroy the amp, overvoltage should be avoided.

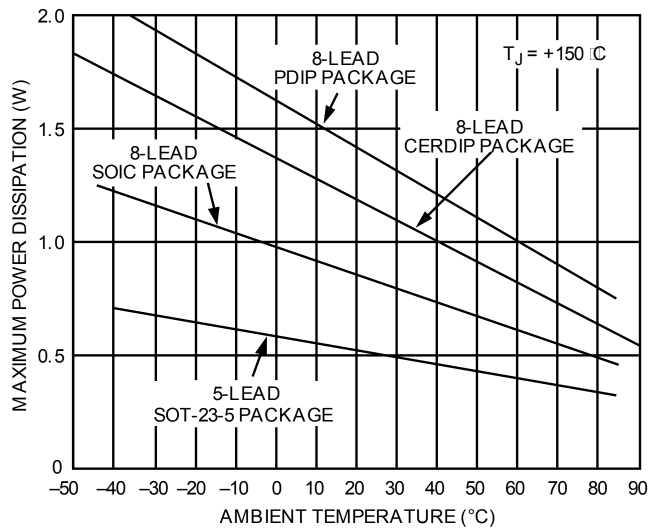


Figure 1.85: *Maximum Power Chart (from the AD8001)*

Protection for overvoltage can consist of diodes from the input pins to the supplies and current limiting resistors. The diodes are typically Schottky diodes, used because of their lower forward voltage (typically 300 mV versus 700 mV for silicon). Protection devices should be applied with caution though. Some diodes can be leaky, which causes issues similar to those of bias currents. Some can also have fairly high capacitance, which may limit frequency response. This is especially true for high speed amps. Current limiting resistors raise the noise floor. Some op amps, such as the OP-27, include protection diodes, but still require current limiting. If an op amp has protection diodes it will typically have a spec for maximum differential input current. The protection circuit should also show up on the simplified schematic.

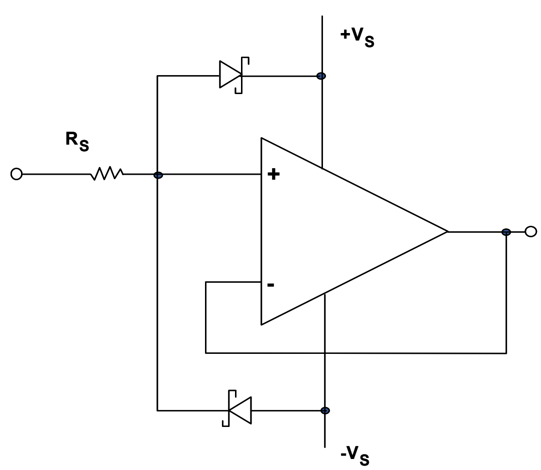


Figure 1.86: *Input Protection*

Some op amps also have back to back diodes across the inputs. These are not for input overvoltage protection, but to limit the differential voltage. If these exist, there will be an absolute maximum spec of ±700 mV for the differential input voltage.

The overriding spec for temperature is the maximum junction temperature of 150ºC. As this limit is approached the life expectancy of the amp (actually any semiconductor) goes down.

The temperature gradient between the junction and the case is based on the thermal resistance of the package, which is called θ_{JC}. There is also a thermal resistance, θ_{CA}, from the package to the ambient. These thermal resistances add up linearly, so the total thermal resistance, θ_{JA}, from the junction to the ambient is $\theta_{JC} + \theta_{CA}$.

The maximum operation temperature rating has more to do with the temperature performance range of the rest of the specs of the op amp rather than any potential damage.

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50) Data Sheet for **AD8551/AD8552/AD8554 Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Operational Amplifiers,** http://www.analog.com

51) Data Sheet for **AD8571/AD8572/AD8574 Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Operational Amplifiers**, http://www.analog.com

52) Data Sheet for **OP777/OP727/OP747 Precision Micropower Single-Supply Operational Amplifiers,** http://www.analog.com

53) Data Sheet for **OP1177/OP2177/OP4177 Precision Low Noise, Low Input Bias Current Operational Amplifiers,** http://www.analog.com

Notes:

SECTION 3: HOW TO READ A DATA SHEET

While there is not an industry standard concerning the format of data sheets, what they cover, what information is included and where that information is located, for the most part data sheets from various manufacturers generally are similar in construction. In this section we will take a look at several data sheets and try to give a feel for where to find certain information and how to interpret what is found.

As a demonstration we will look at five data sheets, a precision amp (OP1177/OP2177/OP4177), a single supply amp (AD8531/AD8532/AD8534), a high speed VFB amp (AD8051/AD8052/AD8054), a CFB amp (AD8001) and the AD847. The part numbers chosen are arbitrary, they were chosen only to give a range of parts.

The Front Page

This page is designed to give you the basic information you might need to choose the part. Referring to Figure 1.87, we can break the front page up into 3 sections.

Section 1 is the features. These bullet points are what are considered by the manufacturer to be the more important parameters of the product for its intended application. The targeted applications are typically listed as well.

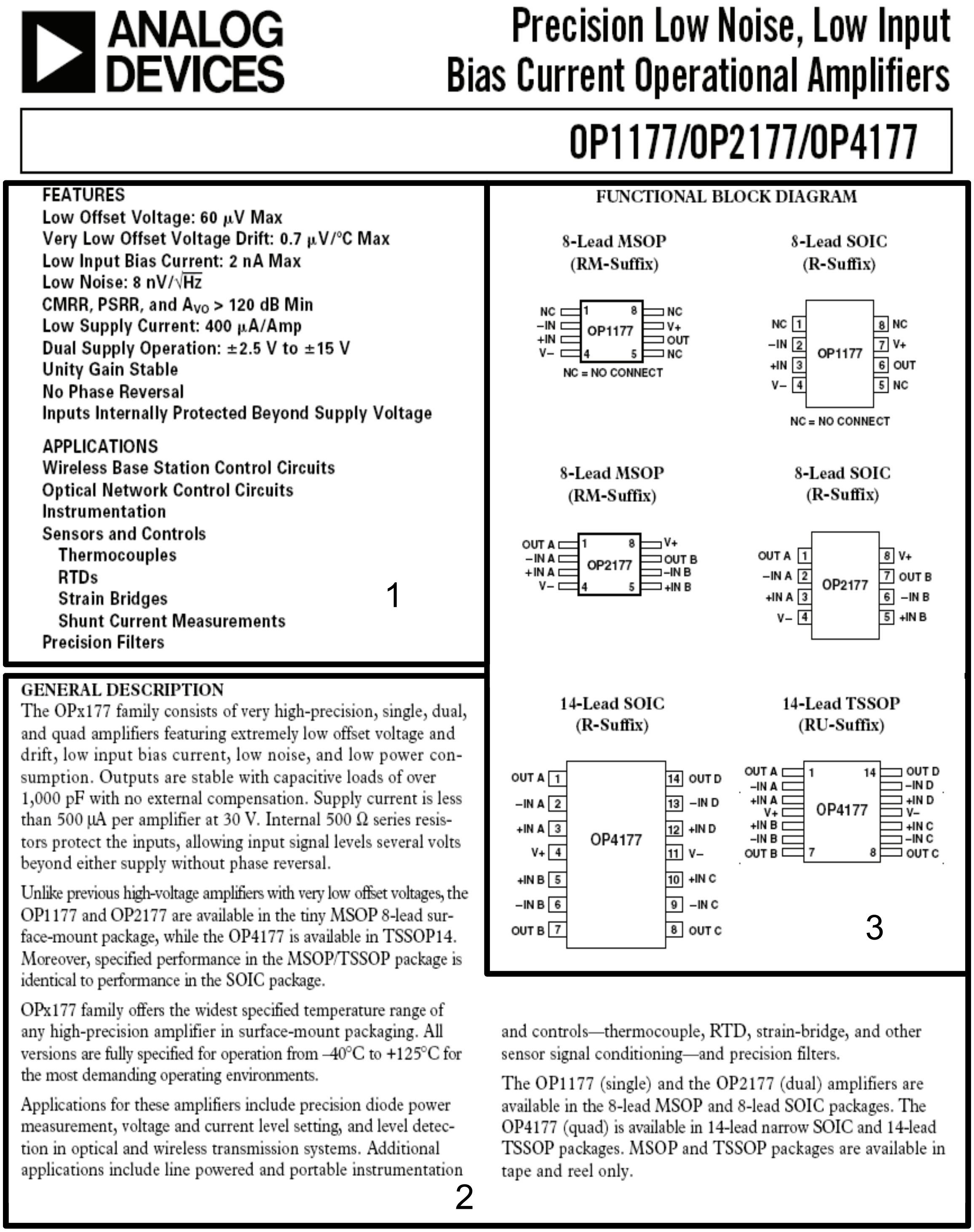
Section 2 is the product description. This typically covers some of what the manufacturer considers to be the salient features of the op amp.

The 3rd section is the functional block diagram. For an op amp, this is typically the pin out of the various packages. For more complex parts, it will truly be a block diagram.

The Specification Tables

There are an unlimited number of conditions possible when measuring any given spec. Obviously, it is not possible to test all possible conditions. So a representative set of conditions are chosen. The test conditions are specified (1 in Figure 1.86). Occasionally if further clarification of or modification to the conditions are required, they are handled as footnotes (2 in Figure 1.86).

In some cases, when the op amp is specified over a large range of conditions, there may be several spec pages. Each would have a different set of conditions. For instance, an op amp may be specified with a ±15 V power supply, a ±5 V power supply or a +5 V only supply. See the AD8051/AD8052/AD8054 data sheet as an example.



ANALOG DEVICES

Precision Low Noise, Low Input Bias Current Operational Amplifiers

OP1177/OP2177/OP4177

FEATURES
Low Offset Voltage: 60 μV Max
Very Low Offset Voltage Drift: 0.7 μV/°C Max
Low Input Bias Current: 2 nA Max
Low Noise: 8 nV/√Hz
CMRR, PSRR, and A_{VO} > 120 dB Min
Low Supply Current: 400 μA/Amp
Dual Supply Operation: ±2.5 V to ±15 V
Unity Gain Stable
No Phase Reversal
Inputs Internally Protected Beyond Supply Voltage

APPLICATIONS
Wireless Base Station Control Circuits
Optical Network Control Circuits
Instrumentation
Sensors and Controls
Thermocouples
RTDs
Strain Bridges
Shunt Current Measurements
Precision Filters

1

FUNCTIONAL BLOCK DIAGRAM

3

GENERAL DESCRIPTION

The OPx177 family consists of very high-precision, single, dual, and quad amplifiers featuring extremely low offset voltage and drift, low input bias current, low noise, and low power consumption. Outputs are stable with capacitive loads of over 1,000 pF with no external compensation. Supply current is less than 500 μA per amplifier at 30 V. Internal 500 Ω series resistors protect the inputs, allowing input signal levels several volts beyond either supply without phase reversal.

Unlike previous high-voltage amplifiers with very low offset voltages, the OP1177 and OP2177 are available in the tiny MSOP 8-lead surface-mount package, while the OP4177 is available in TSSOP14. Moreover, specified performance in the MSOP/TSSOP package is identical to performance in the SOIC package.

OPx177 family offers the widest specified temperature range of any high-precision amplifier in surface-mount packaging. All versions are fully specified for operation from –40°C to +125°C for the most demanding operating environments.

Applications for these amplifiers include precision diode power measurement, voltage and current level setting, and level detection in optical and wireless transmission systems. Additional applications include line powered and portable instrumentation and controls—thermocouple, RTD, strain-bridge, and other sensor signal conditioning—and precision filters.

2

The OP1177 (single) and the OP2177 (dual) amplifiers are available in the 8-lead MSOP and 8-lead SOIC packages. The OP4177 (quad) is available in 14-lead narrow SOIC and 14-lead TSSOP packages. MSOP and TSSOP packages are available in tape and reel only.

Figure 1.87: *Example Data Sheet Front Page*

AD847–SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted) 1

3

Model	Conditions	V_S	AD847J Min	AD847J Typ	AD847J Max	AD847AR Min	AD847AR Typ	AD847AR Max	Units
INPUT OFFSET VOLTAGE[1]		±5 V		0.5	**1**		0.5	**1**	mV
	T_{MIN} to T_{MAX}				3.5			4	mV
Offset Drift				15			15		μV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	**6.6**		3.3	**6.6**	μA
	T_{MIN} to T_{MAX}				7.2			10	μA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	**300**		**50**	**300**	nA
	T_{MIN} to T_{MAX}				400			500	nA
Offset Current Drift				0.3			0.3		nA/°C
OPEN-LOOP GAIN	V_{OUT} = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		2	3.5		2	3.5		V/mV
	T_{MIN} to T_{MAX}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		3	5.5		3	5.5		V/mV
	T_{MIN} to T_{MAX}		1.5			1.5			V/mV
DYNAMIC PERFORMANCE									
Unity Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_{OUT} = 5 V p-p								
	R_{LOAD} = 500 Ω,	±5 V		12.7			12.7		MHz
	V_{OUT} = 20 V p-p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 1 kΩ	±5 V		200			200		V/μs
		±15 V	225	300		225	300		V/μs
Settling Time									
to 0.1%, R_{LOAD} = 250 Ω	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step, A_V = −1	±15 V		65			65		ns
to 0.01%, R_{LOAD} = 250 Ω	−2.5 V to +2.5 V	±5 V		140			140		ns
	10 V Step, A_V = −1	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD}= 1 kΩ			50			50		Degree
Differential Gain	f = 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.04			0.04		%
Differential Phase	f = 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.19			0.19		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	**78**	95		**78**	95		dB
	V_{CM} = ±12 V	±15 V	**78**	95		**78**	95		dB
	T_{MIN} to T_{MAX}		75			75			dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		**75**	86		**75**	86		dB
	T_{MIN} to T_{MAX}		72			72			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		15			15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 1 kΩ	±15 V	**12**			**12**			±V
	R_{LOAD} = 500 Ω	±15 V	**10**			**10**			±V
Short-Circuit Current		±15 V		32			32		mA
INPUT RESISTANCE				300			300		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		±5 V		4.8	**6.0**		4.8	**6.0**	mA
	T_{MIN} to T_{MAX}				7.3			7.3	mA
		±15 V		5.3	**6.3**		5.3	**6.3**	mA
	T_{MIN} to T_{MAX}				7.6			7.6	mA

NOTES
[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[3]Slew Rate is measured on rising edge.
All min and max specifications are guaranteed. Specifications in **boldface** are 100% tested at final electrical test.
Specifications subject to change without notice.

2

Figure 1.88: *Example Specification page*

AD8051/AD8052/AD8054

SPECIFICATIONS (@ T_A = 25°C, $\boxed{V_S = 5\ V}$, R_L = 2 kΩ to 2.5 V, unless otherwise noted.)

Parameter	Conditions	AD8051A/AD8052A			AD8054A			Unit
		Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		80	150		MHz
	G = –1, +2, V_O = 0.2 V p-p		50			60		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω to 2.5 V, R_F = 806 Ω for AD8051A/ AD8052A		20					MHz
	R_F = 200 Ω for AD8054A					12		MHz
Slew Rate	G = –1, V_O = 2 V Step	100	145		140	170		V/μs
Full Power Response	G = +1, V_O = 2 V p-p		35			45		MHz
Settling Time to 0.1%	G = –1, V_O = 2 V Step		50			40		ns
NOISE/DISTORTION PERFORMANCE								
Total Harmonic Distortion*	f_C = 5 MHz, V_O = 2 V p-p, G = +2		–67			–68		dB
Input Voltage Noise	f = 10 kHz		16			16		nV/√Hz
Input Current Noise	f = 10 kHz		850			850		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.09			0.07		%
	R_L = 1 kΩ to 2.5 V		0.03			0.02		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.19			0.26		Degrees
	R_L = 1 kΩ to 2.5 V		0.03			0.05		Degrees
Crosstalk	f = 5 MHz, G = +2		–60			–60		dB
DC PERFORMANCE								
Input Offset Voltage			1.7	10		1.7	12	mV
	T_{MIN}–T_{MAX}			25			30	mV
Offset Drift			10			15		μV/°C
Input Bias Current			1.4	2.5		2	4.5	μA
	T_{MIN}–T_{MAX}			3.25			4.5	μA
Input Offset Current			0.1	0.75		0.2	1.2	μA
Open-Loop Gain	R_L = 2 kΩ to 2.5 V	86	98		82	98		dB
	T_{MIN}–T_{MAX}		96			96		dB
	R_L = 150 Ω to 2.5 V	76	82		74	82		dB
	T_{MIN}–T_{MAX}		78			78		dB
INPUT CHARACTERISTICS								
Input Resistance			290			300		kΩ
Input Capacitance			1.4			1.5		pF
Input Common-Mode Voltage Range			–0.2 to +4			–0.2 to +4		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3.5 V	72	88		70	86		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 10 kΩ to 2.5 V		0.015 to 4.985			0.03 to 4.975		V
	R_L = 2 kΩ to 2.5 V	0.1 to 4.9	0.025 to 4.975		0.125 to 4.875	0.05 to 4.95		V
	R_L = 150 Ω to 2.5 V	0.3 to 4.625	0.2 to 4.8		0.55 to 4.4	0.25 to 4.65		V
Output Current	V_{OUT} = 0.5 V to 4.5 V		45			30		mA
	T_{MIN}–T_{MAX}		45			30		mA
Short-Circuit Current	Sourcing		80			45		mA
	Sinking		130			85		mA
Capacitive Load Drive	G = +1 (AD8051/AD8052)		50					pF
	G = +2 (AD8054)					40		pF
POWER SUPPLY								
Operating Range		3		12	3		12	V
Quiescent Current/Amplifier			4.4	5		2.75	3.275	mA
Power Supply Rejection Ratio	ΔV_S = ±1 V	70	80		68	80		dB
OPERATING TEMPERATURE RANGE	RT, RU, RN-14	–40		+85	–40		+85	°C
	RM, RN-8	–40		+125				°C

*Refer to TPC 13.

Specifications subject to change without notice.

Figure 1.89: *Example Specification page 2*

AD8051/AD8052/AD8054

SPECIFICATIONS (@ T_A = 25°C, $\boxed{V_S = 3\ V,}$ R_L = 2 kΩ to 1.5 V, unless otherwise noted.)

Parameter	Conditions	AD8051A/AD8052A Min	Typ	Max	AD8054A Min	Typ	Max	Unit
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		80	135		MHz
	G = –1, +2, V_O = 0.2 V p-p		50			65		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p,							
	R_L = 150 Ω to 2.5 V,							
	R_F = 402 Ω for AD8051A/AD8052A		17					MHz
	R_F = 200 Ω for AD8054A					10		MHz
Slew Rate	G = –1, V_O = 2 V Step	90	135		110	150		V/μs
Full Power Response	G = +1, V_O = 1 V p-p		65			85		MHz
Settling Time to 0.1%	G = –1, V_O = 2 V Step		55			55		ns
NOISE/DISTORTION PERFORMANCE								
Total Harmonic Distortion*	f_C = 5 MHz, V_O = 2 V p-p,							
	G = –1, R_L = 100 Ω to 1.5 V		–47			–48		dB
Input Voltage Noise	f = 10 kHz		16			16		nV/$\sqrt{Hz}$
Input Current Noise	f = 10 kHz		600			600		fA/$\sqrt{Hz}$
Differential Gain Error (NTSC)	G = +2, V_{CM} = 1 V							
	R_L = 150 Ω to 1.5 V,		0.11			0.13		%
	R_L = 1 kΩ to 1.5 V		0.09			0.09		%
Differential Phase Error (NTSC)	G = +2, V_{CM} = 1 V							
	R_L = 150 Ω to 1.5 V		0.24			0.3		Degrees
	R_L = 1 kΩ to 1.5 V		0.10			0.1		Degrees
Crosstalk	f = 5 MHz, G = +2		–60			–60		dB
DC PERFORMANCE								
Input Offset Voltage			1.6	10		1.6	12	mV
	T_{MIN}–T_{MAX}			25			30	mV
Offset Drift			10			15		μV/°C
Input Bias Current			1.3	2.6		2	4.5	μA
	T_{MIN}–T_{MAX}			3.25			4.5	μA
Input Offset Current			0.15	0.8		0.2	1.2	μA
Open-Loop Gain	R_L = 2 kΩ	80	96		80	96		dB
	T_{MIN}–T_{MAX}		94			94		dB
	R_L = 150 Ω	74	82		72	80		dB
	T_{MIN}–T_{MAX}		76			76		dB
INPUT CHARACTERISTICS								
Input Resistance			290			300		kΩ
Input Capacitance			1.4			1.5		pF
Input Common-Mode Voltage Range			–0.2 to +2			–0.2 to +2		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1.5 V	72	88		70	86		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 10 kΩ to 1.5 V		0.01 to 2.99			0.025 to 2.98		V
	R_L = 2 kΩ to 1.5 V	0.075 to 2.9	0.02 to 2.98		0.1 to 2.9	0.35 to 2.965		V
	R_L = 150 Ω to 1.5 V	0.2 to 2.75	0.125 to 2.875		0.35 to 2.55	0.15 to 2.75		V
Output Current	V_{OUT} = 0.5 V to 2.5 V		45			25		mA
	T_{MIN}–T_{MAX}		45			25		mA
Short-Circuit Current	Sourcing		60			30		mA
	Sinking		90			50		mA
Capacitive Load Drive	G = +1 (AD8051/AD8052)		45					pF
	G = +2 (AD8054)					35		pF
POWER SUPPLY								
Operating Range		3		12	3		12	V
Quiescent Current/Amplifier			4.2	4.8		2.625	3.125	mA
Power Supply Rejection Ratio	ΔV_S = 0.5 V	68	80		68	80		dB
OPERATING TEMPERATURE RANGE	RT, RU,							
	RN-14	–40		+85	–40		+85	°C
	RM, RN-8	–40		+125				°C

*Refer to TPC 13.

Specifications subject to change without notice.

Figure 1.90: *Example Specification page 3*

AD8051/AD8052/AD8054

SPECIFICATIONS (@ T_A = 25°C, V_S = ±5 V, R_L = 2 kΩ to Ground, unless otherwise noted.)

Parameter	Conditions	AD8051A/AD8052A Min	Typ	Max	AD8054A Min	Typ	Max	Unit
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	70	110		85	160		MHz
	G = –1, +2, V_O = 0.2 V p-p		50			65		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω, R_F = 1.1 kΩ for AD8051A/AD8052A		20					MHz
	R_F = 200 Ω for AD8054A					15		MHz
Slew Rate	G = –1, V_O = 2 V Step	105	170		150	190		V/µs
Full Power Response	G = +1, V_O = 2 V p-p		40			50		MHz
Settling Time to 0.1%	G = –1, V_O = 2 V Step		50			40		ns
NOISE/DISTORTION PERFORMANCE								
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = +2		–71			–72		dB
Input Voltage Noise	f = 10 kHz		16			16		nV/√Hz
Input Current Noise	f = 10 kHz		900			900		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω		0.02			0.06		%
	R_L = 1 kΩ		0.02			0.02		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω		0.11			0.15		Degrees
	R_L = 1 kΩ		0.02			0.03		Degrees
Crosstalk	f = 5 MHz, G = +2		–60			–60		dB
DC PERFORMANCE								
Input Offset Voltage			1.8	11		1.8	13	mV
	T_{MIN}–T_{MAX}			27			32	mV
Offset Drift			10			15		µV/°C
Input Bias Current			1.4	2.6		2	4.5	µA
	T_{MIN}–T_{MAX}			3.5			4.5	µA
Input Offset Current			0.1	0.75		0.2	1.2	µA
Open-Loop Gain	R_L = 2 kΩ	88	96		84	96		dB
	T_{MIN}–T_{MAX}		96			96		dB
	R_L = 150 Ω	78	82		76	82		dB
	T_{MIN}–T_{MAX}		80			80		dB
INPUT CHARACTERISTICS								
Input Resistance			290			300		kΩ
Input Capacitance			1.4			1.5		pF
Input Common-Mode Voltage Range			–5.2 to +4			–5.2 to +4		V
Common-Mode Rejection Ratio	V_{CM} = –5 V to +3.5 V	72	88		70	86		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 10 kΩ		–4.98 to +4.98			–4.97 to +4.97		V
	R_L = 2 kΩ	–4.85 to +4.85	–4.97 to +4.97		–4.8 to +4.8	–4.9 to +4.9		V
	R_L = 150 Ω	–4.45 to +4.3	–4.6 to +4.6		–4.0 to +3.8	–4.5 to +4.5		V
Output Current	V_{OUT} = –4.5 V to +4.5 V		45			30		mA
	T_{MIN}–T_{MAX}		45			30		mA
Short-Circuit Current	Sourcing		100			60		mA
	Sinking		160			100		mA
Capacitive Load Drive	G = +1 (AD8051/AD8052)		50					pF
	G = +2 (AD8054)					40		pF
POWER SUPPLY								
Operating Range		3		12	3		12	V
Quiescent Current/Amplifier			4.8	5.5		2.875	3.4	mA
Power Supply Rejection Ratio	ΔV_S = ±1 V	68	80		68	80		dB
OPERATING TEMPERATURE RANGE	RT, RU, RN-14	–40		+85	–40		+85	°C
	RM, RN-8	–40		+125				°C

Specifications subject to change without notice.

Figure 1.91: *Example Specification page 4*

On many op amps some individual specs may have multiple entries. This is for different performance levels. It can also be for different temperature ranges (usually commercial, industrial, or military). This can be seen in Figure 1-84 (3).

Note that there are typically three possibilities for the specs, Min, Typ, and Max. See Figure 1-84 (3). At Analog Devices any spec in the min (minimum) and max (maximum) columns will be guaranteed by test. This can be a direct test, or, in some instances, testing one parameter will guarantee another. A typ (typical) spec is just that, typical. Depending on the particular spec, the deviation from the typical can be substantial. And you have no way of knowing what the range of variation on the typ spec is. Sometimes you will find a typ and a min (or max) for the same spec. This tells you that although the test limits are at a particular level (min or max) the typicals tend to run much better than the test limits. When designing, using typs is risky. You are much better off using mins or maxes for error budget analysis.

Testing is one of the most expensive steps in the manufacturing of op amps. Therefore a more highly specified part will typically cost more than a less completely specified part. But, in your system, the higher specified part may be required to guarantee the circuit performance.

The Absolute Maximums

There is always a section just after the spec tables that contains the absolute maximum ratings. These are typically voltage and temperature related.

The process used to fabricate the op amp will typically determine the maximum supply voltage. Maximum input voltages typically are limited to the supply voltages. It should be pointed out that the supply voltage is the instantaneous value, not the average, or final value. So if an op amp has voltages on its input but the supply voltage is not present. (which could occur during power up when one section of the system is powered but others aren't) the op amp is overvoltaged, even if when the op amp power is applied, everything is within operational limits.

Looking at Figure 1.92, the maximum input voltage spec is GND to V_S. The Differential input voltage maximum is ±6 V. Note that both of these conditions must be met. So the input pins of the op amp must be between GND and V_S AND no more than 6 V from each other.

The primary concern for semiconductor reliability is to keep the junction temperature below 150°C. There will be a θ_{ja} given for the various package options. This is the thermal resistance. The units are °C/Watt. See Figure 1.92. To use this information first determine the power dissipation of the package. This would be the quiescent current times the supply voltage. Then take the maximum dissipation generated by the output stage (output current times the difference between the output voltage and the supply voltage). Add these two together and you will have the total package dissipation, in Watts. Multiply the thermal resistance by the dissipation and you have the temperature rise. Start with the ambient temperature (in °C), take the rise calculated above and that will give you the junction temperature. Remember that the ambient temperature should be in operation. Circuits packaged in an enclosure, which is in turn placed in a rack with other equipment will have an internal ambient temperature that could be significantly above the air temperature where it is located. This must be considered.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	12.6 V
Internal Power Dissipation[2]	
Plastic DIP Package (N)	1.3 W
Small Outline Package (R)	0.9 W
SOT-23-5 Package (RT)	0.5 W
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	±1.2 V
Output Short Circuit Duration	Observe Power Derating Curves
Storage Temperature Range N, R	–65°C to +125°C
Operating Temperature Range (A Grade)	–40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	+300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Lead Plastic DIP Package: θ_{JA} = 90°C/W
8-Lead SOIC Package: θ_{JA} = 155°C/W
8-Lead Cerdip Package: θ_{JA} = 110°C/W
5-Lead SOT-23-5 Package: θ_{JA} = 260°C/W

Figure 1.92: *Typical Absolute Maximum Ratings*

As an example, let's take the AD8534. We will assume that it is being used as a line driver. The required output voltage range is 500 mV to 5 V. The maximum output current we expect from each of the four sections is 100 mA at a maximum output voltage of 5 V. This equates to a load of 50 Ω. Let us say the circuit will operate on a supply of 5.5 V. This allows for a bit of headroom for the driver. If you plot the output voltage versus output current for an amplifier with a resistive load the maximum dissipation is approximately 55% of the maximum (see Figure 1.93). This is due to the fact that as the output voltage increases, the dissipation voltage (the difference between the output voltage and the supply voltage) decreases, even though the current keeps increasing. Remember it's the power dissipation of the package, not the load, which will rise with increasing output voltage. The quiescent current (Iq) is 1.75 mA max over temperature per amplifier. For the four amplifiers, then, the total quiescent dissipation is: 38.5 mW (Iq × Vs × 4). The maximum output dissipation is calculated from the following equation:

$$P_D = \frac{(V_S - .55 * V_O(max))^2}{R_{LOAD}} \qquad \text{Eq. 1-26}$$

which calculates to 150 mW per amplifier or 600 mW total. The total dissipation is therefore 638.5 mW.

We chose a TSSOP package because it was the smallest available. The θ_{ja} for this package is 240°C/W. This gives a temperature rise of 154°C (240° C/W × 638.5 mW). If the ambient temperature is assumed to be 25°C (the usual value given for room temperature), the junction temperature would be 179°C! This is a problem. So we can see that even though we are operating the AD8534 below what would seem to be its maximum output current rating (which is 250 mA), the part will not be reliable since the junction temperature (150°C) will be exceeded.

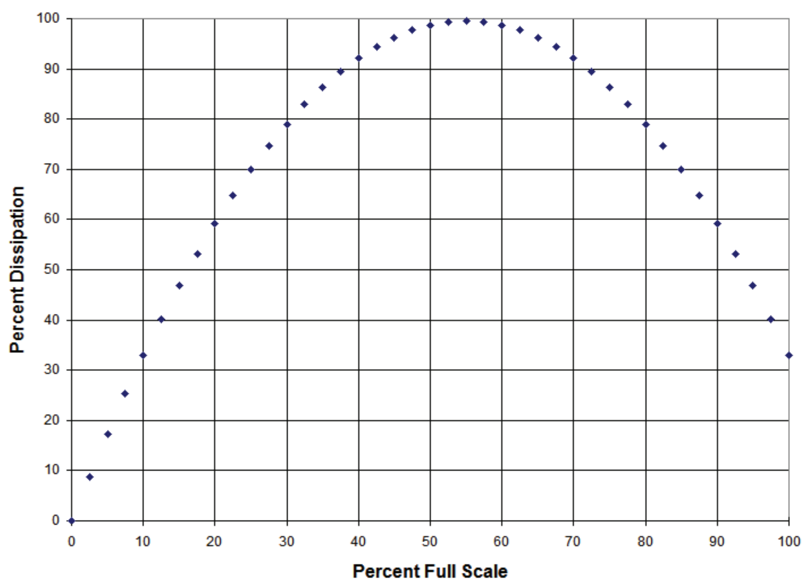


Figure 1.93: *Power Dissipation vs. Percent Full Scale*

θja actually has two components, θ_{jc} (the thermal resistance from the junction to the case) and θ_{ca} (the thermal resistance from the case to the ambient). They add linearly. We can't do anything about the θ_{jc}, but by adding a heat sink we can change θ_{ca} to some degree. Most of the time with op amps, this is not an issue, but it could help for a high current output op amp in a small package as in the example above.

The Ordering Guide

Many op amps are available in multiple packages and/or multiple temperature ranges. Each of the various combinations of package and temperature range requires a unique part number. This is spelled out in the ordering guide. See Figure 1.94.

Just as a note, in the case of op amps, the commercial (0°C to 70°C) temperature range has become much less common. The reason for this is that most circuits yield to the industrial temperature range. It is less expensive to support fewer part types. Each discrete part number requires a separate test program, separate inventorying, etc. An exception to this rule is for parts designed for a specific application which is, by definition, commercial. Examples of this are consumer applications, such as audio. Wider temperature range for these parts offers no advantage.

The industrial temperature range can also mean different things. The standard industrial temperature range is −40°C to +85°C. A common variant on this is what is commonly called the automotive temperature range −40°C to +105°C. 0°C to 100°C is also common.

The military temperature range is −55°C to +125°C.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information
AD8531AKS*	–40°C to +85°C	5-Lead SC70	KS-5	A7B
AD8531AR	–40°C to +85°C	8-Lead SOIC	SO-8	
AD8531ART*	–40°C to +85°C	5-Lead SOT-23	RT-5	A7A
AD8532AR	–40°C to +85°C	8-Lead SOIC	SO-8	
AD8532ARM*	–40°C to +85°C	8-Lead MSOP	RM-8	ARA
AD8532AN	–40°C to +85°C	8-Lead Plastic DIP	N-8	
AD8532ARU*	–40°C to +85°C	8-Lead TSSOP	RU-8	
AD8534AR	–40°C to +85°C	14-Lead SOIC	SO-14	
AD8534AN	–40°C to +85°C	14-Lead Plastic DIP	N-14	
AD8534ARU*	–40°C to +85°C	14-Lead TSSOP	RU-14	

*Available in reels only.

Figure 1.94: *Typical Ordering Guide*

The Graphs

Many specs vary over the operational range of the op amp. An example is the variation of open-loop gain with frequency. See Figure 1.94. So to completely specify the open-loop gain of a part there would be an open-loop gain spec at dc, which typically would appear in the spec table, and a graph showing variation with frequency. The information presented in the graphs is not uniform from vendor to vendor or even from part to part from the same manufacturer. Higher performance parts tend to be more completely specified. For the most part the graphs will tend to be typical values.

The Main Body

The main body of the data sheet contains detailed information on the operation and applications of the op amp.

The main body typically starts off with a section on the theory of operation of the part.

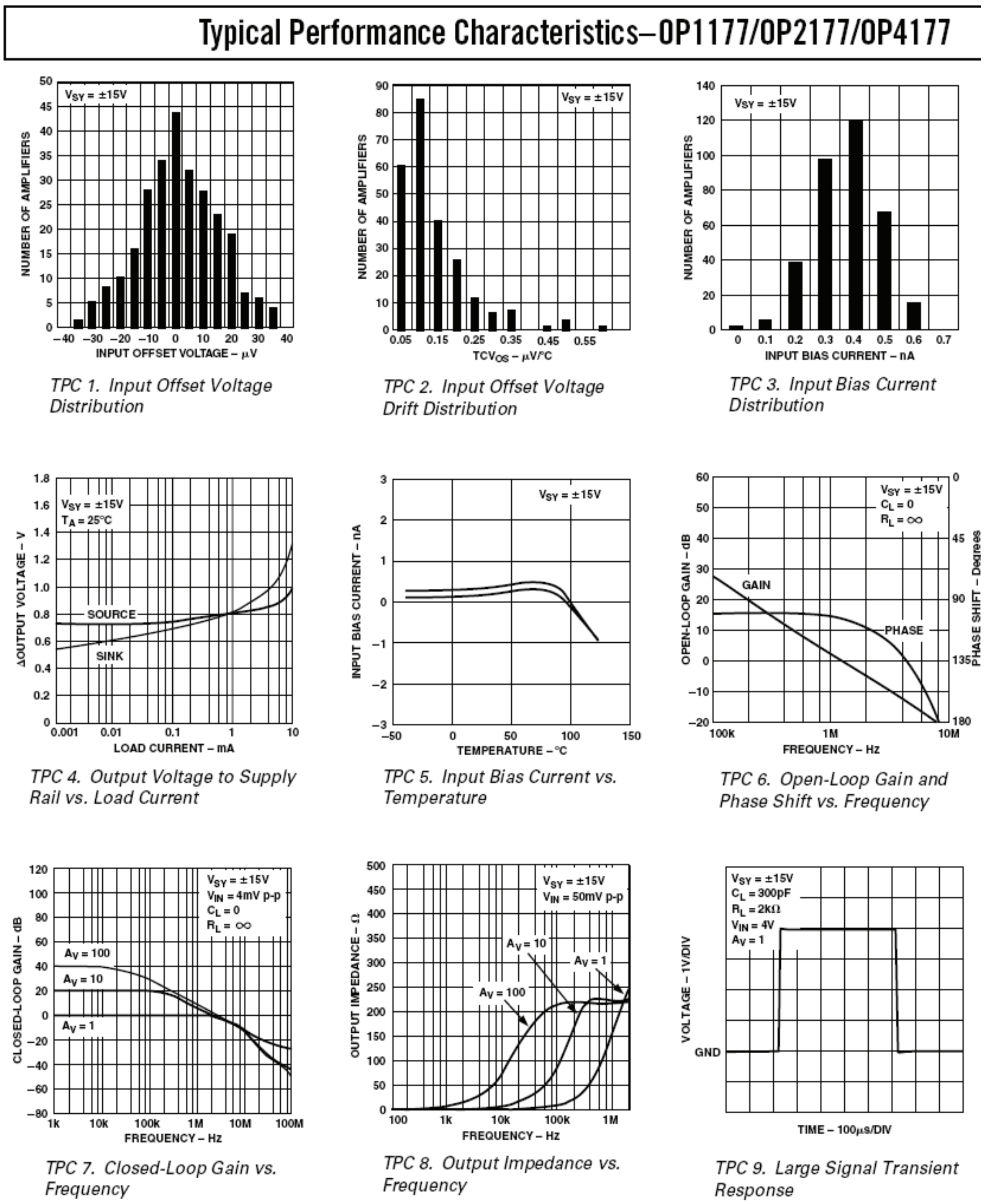


Figure 1.95: *Typical Performance Graphs*

This is usually a short description of the various specs that are particularly to build was not the best approach.

Typically simple calculations, noise for example, are worked out as examples.

The rest of the body of the data sheet contains application information. Since its founding Analog Devices determined that just giving someone an amplifier and letting them go off on their own to try to build whatever it is that they want. Therefore, Analog Devices includes application information with the data sheet appropriate for the specific op amp. For instance, a precision op amp will emphasize offset and noise, while a high speed op amp will emphasize bandwidth and speed.

Much of the information in the applications section is more relevant to other op amps than the one that it appears in.

The last thing that is typically included in the data sheet is the package drawings.

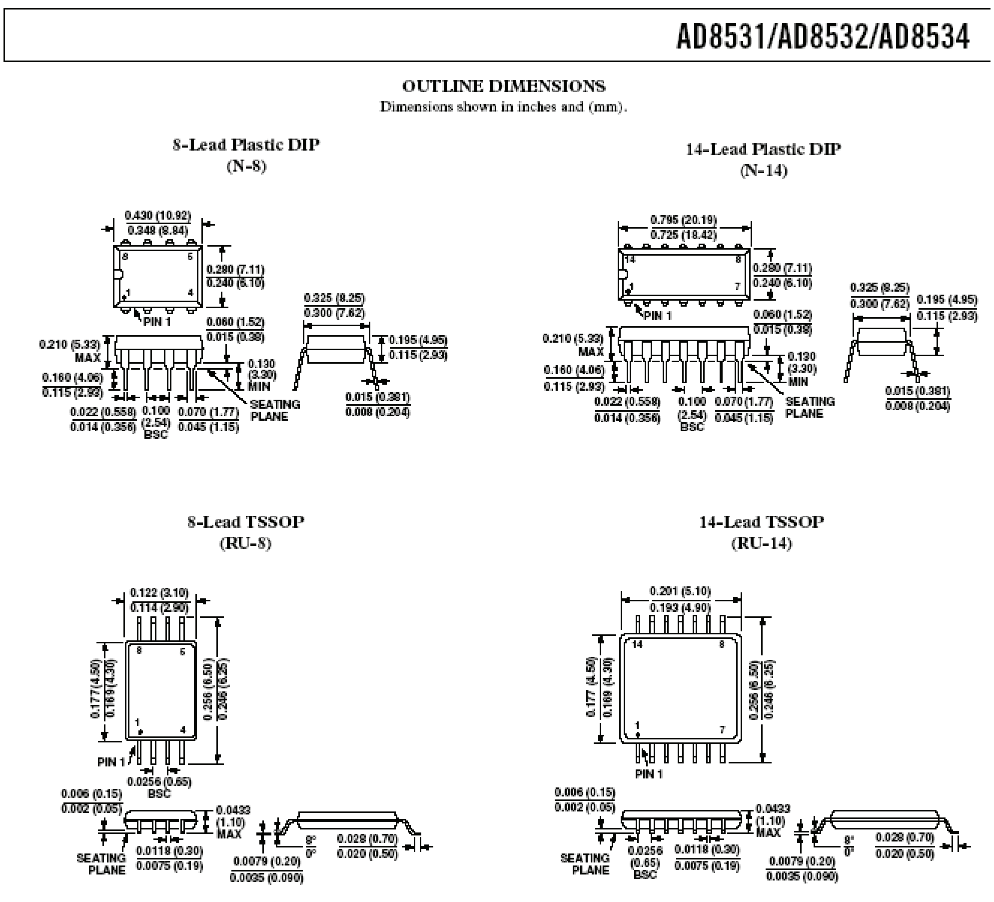


Figure 1.96: *Typical Package Dimension Drawing*

SECTION 4: CHOOSING AN OP AMP

As we have seen in the previous sections, an op amp can have many specs. Now that we have gone over what those specs mean and how to read a data sheet we are ready to proceed to the next step. How, then, do you determine which amp best suits your needs?

Step 1: Determine the Parameters

The first step in the process is to determine what parameters are important to your design. To do this you must have a clear idea of:

1) The input signal.
    a. Is it a voltage or a current?
    b. What are the frequency and the amplitude ranges?
    c. What is the impedance level of the surrounding circuit?
2) The accuracy requirements.
3) The output signal.
    a. What are the frequency and the amplitude ranges?
    b. What will the circuit be driving (another op amp stage, an ADC, a cable, etc.)?
4) The physical environment.
    a. What is the operational temperature range?
    b. What is the size limitation?
    c. What power supplies are available?

For instance, if you are designing a single-supply system that is going to be capacitively coupled, offsets probably aren't a concern. If you are designing a system to interface to a low level physical sensor, then noise, dc precision, and closed-loop gain are important, but bandwidth is probably of less importance, since the bandwidth of most physical sensors are relatively low. However, you do need enough bandwidth to support the required closed loop gain.

Part of this process is determining the values for the various parameters. In doing this you should determine both an optimum value and an acceptable range. For example, you may have a target value of 500 µV for the offset voltage, but you may be able to live with 1 mV and be relaxing this spec, a better overall fit could be made. The operating temperature range that the circuit will be required to operate in will affect this as well. The physical size of the package and the cost, as always, should be considered. It is also good practice to allow a little margin on the specs so that aging effects, etc., don't cause the circuit to go out of spec.

Step 2: Prioritize the Parameters

The next step is to prioritize these parameters. Typically one or two parameters are critical. A few more may be desirable but not required. Try not to overspecify the part. Remember that the more specified a part is the harder it will be to find an exact match, and the tighter the specs, the more expensive the part is likely to be.

Step 3: Selecting the Part

The next step is to finally select the part. The brute force method would be to gather data books and randomly start to look at the specs for each of the parts individually. This would quickly get out of hand. There are several tools that make the job much easier.

The first is to use a selection guide. These appear frequently in magazine ads and promotional mailers. The problem with using these guides is that, in many instances, the lists are not all inclusive, but instead are usually focused on specific sub group, such as new products, single supply, or the like. The narrow focus may cause you to miss some otherwise acceptable options.

ADI provides a piece of literature called *The Short Form Designers Guide* which is much better suited to the purpose. It contains all of ADI's current product offering, sorted by function and performance. Two of the main parts of the short form are the product trees and selection guides.

Using the amplifier section as an example, we can choose between several possibilities, each of which are expanded further in subsequent trees. This allows the designer to drill down to a particular amp which will be acceptable in his application. Fig. 1.90 to Fig. 1.92 shows part of the amplifier selection tree.

The selection trees generally only give one, or maybe two, specs. It is designed to be the start of the selection process. More detailed specs are given in the selection guides, which will take a particular category corresponding to one of the sections of the selection trees, and then sort the parts by the relevant parameter. For example, single-supply precision amps would be sorted by open-loop gain, highest open-loop gain first. If there is more than one amp with the same open-loop gain, then the amps would be further sorted by the next parameter, in this case offset voltage.

For high speed amplifiers the primary sorting spec is bandwidth, since this is the primary criteria of interest.

In addition to the specs on which the parts are sorted, there are several other specs given. These include package size and cost. The cost quoted is generally the 1000 piece price for the base grade of the amplifier. It should be used for comparison purposes. Small quantities will typically be priced higher; higher quantities will generally be lower.

An alternative is the parametric search engine. Here you enter the relevant parameters for your design. The op amp search is shown in Figures 1.96 – 1.99. You can also prioritize the selection by clicking on the "priority" box. The search engine will then search the database of parts and it will come up with 10 alternatives.

A particularly nice feature of the search engine is that if it can't meet your selection criteria exactly, it will give a selection of parts that come close to matching your criteria. Where there is not a match the parameter is presented in red. This allows the designer the chance to evaluate how well his application lines up with available components.

Design aids are covered in more detail in Chapter 13.

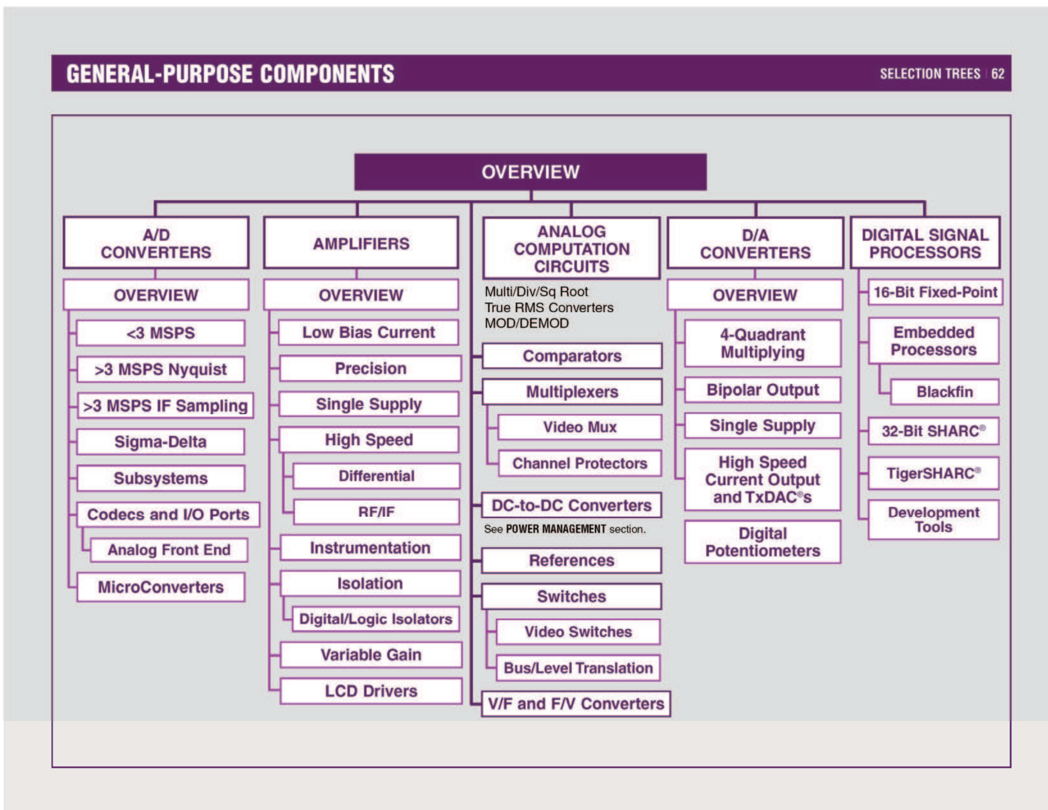


Figure 1.97: Selection Tree Top Level

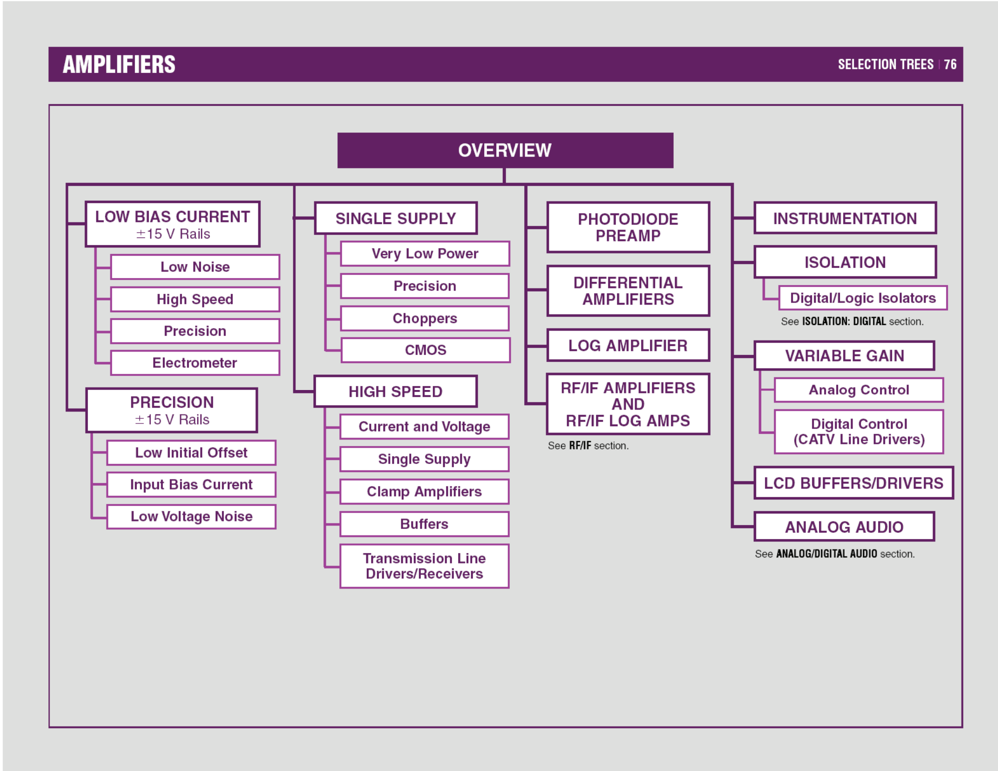


Figure 1.98: *Selection Tree, Amplifier, Top Level*

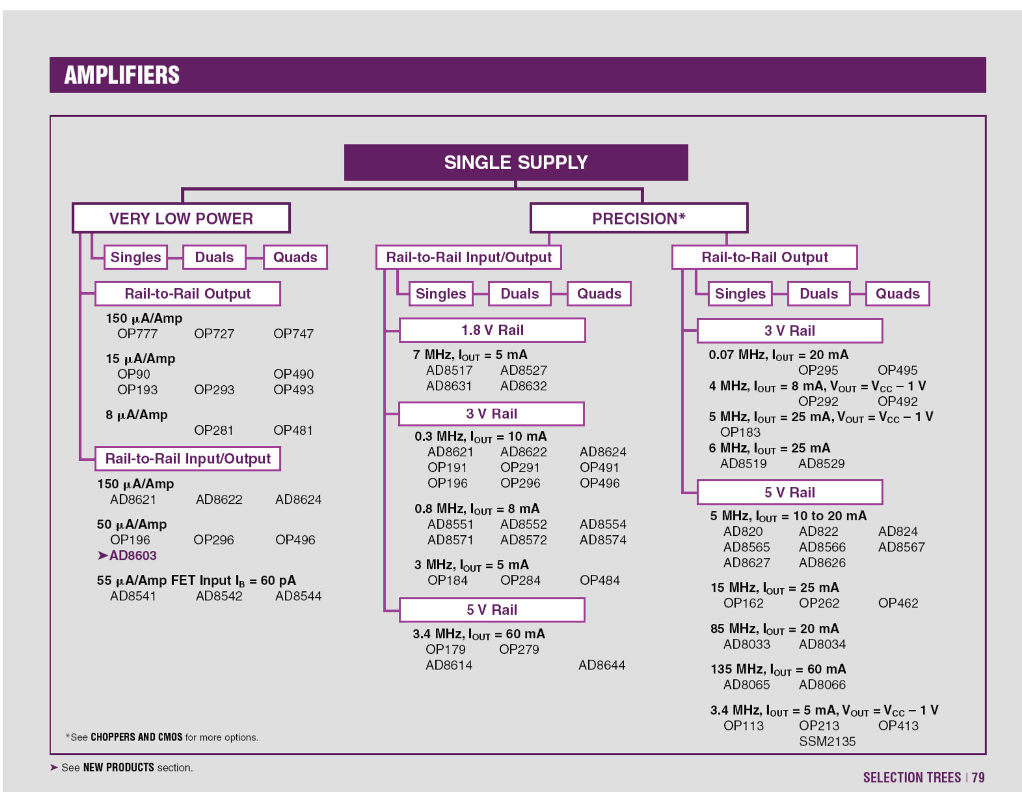


Figure 1.99: *Selection Guide, Amplifier example Page*

AMPLIFIERS

Single Supply, Precision

Rail-to-Rail Output

Model	V_{SUPPLY} Specs @ 5 V Min/Max	Open-Loop Gain V/μV	CMRR dB	Unity Gain BW MHz	Slew Rate V/μs	Initial Offset E_{OS} ±mV Max	E_{OS} vs. Temp ±μV/°C	I_B 25°C Max ±nA	I_Q 25°C Max mA	I_{OUT} mA	Smallest Available Package	Lowest Grade Price 100s	Comments	Eval Board Avail
Singles														
OP113	5/36	2	90	3.4	0.6	0.175	4	650	3	30	8 SOIC	$ 1.76	$V_{OUT} = V_{CC} - 1$ V	
OP162	2.7/12	0.03	70	15	10	0.325	8	600	0.65	25	8 TSSOP	$ 1.65	Fast, Low Power	
AD8065	5/24	0.1	80	135	200	1	2.5	1 pA	6.5	60	5 SOT	$ 1.59	JFET Input	
AD8627	5/26	0.08	65	5	5	1	2	10 pA	0.7	10	5 SOT	$ 1.69	No Phase Reversal	
OP183	3/36	0.1	70	5	5	1	20	600	1.5	25	8 SOIC	$ 1.74	$V_{OUT} = V_{CC} - 2$ V	
AD820	3/36	0.3	60	1.8	3	1	20	25 pA	0.8	10	8 SOIC	$ 1.65	CMV Range = $V_{CC} - 2$ V	
AD8519	2.7/16	0.02	55	6	1.5	1.4	5	300	1.1	25	5 SOT	$ 0.92	Low Offset, 125°C Operation	
AD8565	4.5/16	0.03	54	4	4	10	5	600	0.85	35	5 SC70	$ 0.68*	LCD REF Driver	
AD8033	4/24	0.03	90	75	80	6	5	1 pA	3.3	20	5 SC70	$ 1.19	CMV Range = $V_{CC} - 3$ V	
Duals														
OP213	5/36	2	90	3.4	0.6	0.175	4	650	6	30	8 SOIC	$ 2.09	$V_{OUT} = V_{CC} - 1$ V	
OP295	3/36	0.75	90	0.075	0.03	0.300	5	20	0.3	10	8 SOIC	$ 2.53	Low Offset	
OP262	2.7/12	0.03	70	15	10	0.325	8	600	1.3	25	8 TSSOP	$ 2.38	Fast, Low Power	
OP292	5/33	0.025	75	4	1.5	0.8	15	700	2.4	5	8 SOIC	$ 1.53	$V_{OUT} = V_{CC} - 1$ V	
AD8066	5/24	0.1	80	135	200	1	2.5	1 pA	6.5	60	8 MSOP	$ 2.29	FastFET	
AD822	3/36	0.3	60	1.8	3	1	20	25 pA	1.6	10	8 SOIC	$ 2.64	JFET	
AD8626	5/26	0.08	65	5	5	1	2	10 pA	1.4	10	8 MSOP	$ 1.59	No Phase Reversal	
AD8529	2.7/16	0.02	55	6	1.5	1.4	5	300	2.2	25	8 MSOP	$ 1.22	125°C Operation	
AD823	3.3/36	0.015	54	12	13	1.5	20	25 pA	5.7	25	8 SOIC	$ 2.91	JFET	
AD8566	4.5/16	0.03	54	4	4	10	5	600	1.7	35	8 MSOP	$ 0.98*	LCD REF Driver	
AD8034	4/24	0.03	90	75	80	6	5	1 pA	6.6	20	8 SOT	$ 1.05	FastFET	
SSM2135	4/36	2	87	3.5	0.6	2	ns	7570	6	10	8 SOIC	$ 2.59	Audio Quality	
Quads														
OP495	3/36	0.75	90	0.075	0.03	0.3	5	20	0.3	11	14W SOIC	$ 4.52	Low Offset	
OP462	2.7/12	0.03	70	15	10	0.325	8	600	2.6	25	14 TSSOP	$ 3.02	Fast, Low Power	
OP413	5/36	2	90	3.4	0.6	0.325	5	650	12	30	14N SOIC	$ 3.85	$V_{OUT} = V_{CC} - 1$ V	
OP492	5/33	0.025	75	4	1.5	0.8	15	700	4.8	5	14N SOIC	$ 2.71	$V_{OUT} = V_{CC} - 1$ V	
AD824	3/36	0.25	60	1.8	3	1	20	25 pA	1.6	8	14N SOIC	$ 4.13	JFET	
AD8567	4.5/16	0.03	54	4	4	10	5	600	3.4	35	14 TSSOP	$ 1.38*	LCD REF Driver	
AD8625	5/26	0.08	65	5	5	1	2	10 pA	2.8	10	14 TSSOP	$ 4.75	No Phase Reversal	

Figure 1.100: *Typical Amplifier Selection Guide Page*