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# A 10 V programmable Josephson voltage standard circuit with a maximum output voltage of 20 V

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**Abstract**

A 10 V programmable Josephson voltage standard (PJVS) circuit with a maximum output voltage of 20 V and a microwave bias of 18.5 GHz was designed and fabricated. Although an attempt was made to improve the fabrication yield for the 10 V PJVS circuit, it was not sufficiently large to reproducibly fabricate a perfect chip without any defects. The redundant arrays were additionally integrated to increase the maximum output voltage, which contributed to an increase in the number of available chips under the limited fabrication yield. Fortunately, most of the defective arrays had a zeroth Shapiro step, while the first step was very small or zero. If the array was not dc biased, it did not generate any voltage, because it worked as a superconductive wiring. In this case, the maximum output voltage became smaller than that of a perfect chip, but it functioned as a 10 V PJVS, due to the back-up arrays.

## 1. Introduction

Josephson voltage standards are based on the ac Josephson effect, in which a microwave field of frequency $f$ produces quantized voltages $V = nf/K_{J-90}$, where $n$ is an integer and $K_{J-90} = 483\,597.9$ GHz V$^{-1}$ is the Josephson constant; namely, the Josephson junction is used as a frequency-to-voltage converter [1]. Because frequencies can be measured to high accuracy, the Josephson effect provides an accurate and reproducible method of generating the voltage [2, 3]. A programmable Josephson voltage standard (PJVS), in which an array of nonhysteretic junctions is divided into a binary sequence of array segments, has a rapid settling time and inherent step stability [4]. Furthermore, the large critical currents of superconductor–normal-metal–superconductor (SNS) junctions enhance the operating margin and noise immunity [5]. In addition, despite temperature fluctuations, operation cooled with a cryocooler is possible due to these advantages [6–8]. Niobium nitride (NbN) junctions have a higher critical temperature $T_c$ than niobium (Nb); therefore, it is possible to use a more compact cryocooler, which means a reduction in volume, power consumption, and total cost of the PJVS system. While an output voltage of 10 V is necessary to replace a conventional Josephson voltage standard [9, 10], it is challenging to fabricate a perfect 10 V PJVS chip without any defects. The Physikalisch Technische Bundesanstalt (PTB) has demonstrated a 10 V PJVS with 69 120 Josephson junctions driven at 70 GHz [11]. At the National Institute of Advanced Industrial Science and Technology (AIST), the microwave frequency for the PJVS circuit is designed to be lower than 20 GHz, because it is easier to handle and the cable and oscillator costs are lower. Since the Shapiro step voltage is proportional to the frequency, a larger number of Josephson junctions, that is more than 300 000, is required to generate 10 V with a microwave bias of 16 GHz. Vertically stacked Josephson junctions are effective for enlargement of the output voltage with a practical chip size of 10 to 20 mm [12]. While the National Institute of Standards and Technology (NIST) has demonstrated a vertical ten Josephson junction stack in Nb [13], at present, double NbN Josephson junctions may the only practical approach with sufficient uniformity and reproducibility for a large circuit.

Since most of the chips fabricated at AIST have had a smaller output voltage than that designed, due to defective arrays, two imperfect chips were used to generate an output voltage of 10 V [14]. While the dual chip system was shown to

 

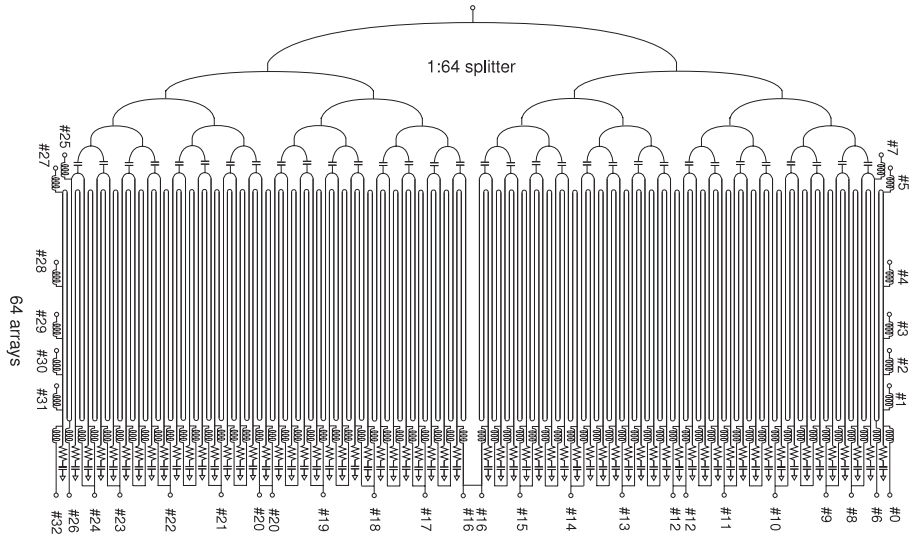


**Figure 1.** Equivalent circuit of the PJVS circuit.

**Table 1.** Specifications.

| | |
|---|---|
| Chip size | 15.28 mm × 14.70 mm |
| Number of junctions | 524 288 |
| Junction size | 3.4 $\mu$m square |
| Minimum line and space | 1.6 $\mu$m |
| Resolution of DAC | 12 bit × 2 channel |

**Table 2.** Required number of cells for the 10 V PJVS.

| Frequency, $f$ (GHz) | Cell voltage, $V_{\rm cell}$ (mV) | Maximum voltage, $V_{\rm max}$ (V) | Required cells, $N_{10}$ |
|---|---|---|---|
| 14.0 | 948.6 | 15.2 | 11 |
| 16.0 | 1084.1 | 17.3 | 10 |
| 18.0 | 1219.7 | 19.5 | 9 |
| 18.5 | 1253.5 | 20.1 | 8 |

have sufficient precision, the costs for the microwave oscillator and microwave cables were doubled. In this paper, we will describe an approach for obtaining an output voltage of 10 V with a single PJVS chip under limited fabrication yield.

## 2. Circuit design

Figure 1 shows the equivalent circuit for the PJVS circuit, in which two identical 10 V 12-bit digital-to-analogue converter (DAC) circuits are integrated on one chip. While one channel is intended to be used as a back-up if the arrays are defective, the chip with two functional arrays would enable waveform synthesis of two independent waves with different phases [15, 16]. Independent channels for current and voltage are also required for a 60 Hz power standard [17].

The specifications for the chip are summarized in table 1. The size of the NbN/TiN$_x$/NbN/TiN$_x$/NbN double-SNS junction stacks is 3.4 $\mu$m × 3.4 $\mu$m, and the minimum line and space is 1.6 $\mu$m. The critical current density of the Josephson junction is typically $7 \times 10^8$ A m$^{-2}$. The design of the DAC chip is based on our prototype designed by NIST [18], and has been optimized for the NbN film, which has a larger magnetic penetration depth than Nb. Furthermore, the size of the microwave circuits has been shrunk and the density of Josephson junctions has been increased. The microwave is launched to one tap, and is equally split between the 64 arrays through a coplanar network circuit and dc blocking capacitors. A quarter-wavelength coplanar waveguide (CPW) with a specific impedance of 36 Ω is connected to two 50 Ω CPWs, which function as two-way splitters. Six consecutive stages of the two-way splitters are connected in series in order to divide the microwave power into the $64 (= 2^6)$ arrays. The CPWs are optimized using an electromagnetic field simulator, taking into account the kinetic inductance of the NbN film. Sixty four 50 Ω resistors and capacitors are used for termination of the microwave and dc block, respectively.

In the chip, 262 144 NbN/TiN$_x$/NbN/TiN$_x$/NbN double-junction stacks (524 288 Josephson junctions) are divided into 64 parallel arrays, and the dc bias pads are connected to every four arrays. Thus, the junction arrays are divided into 16 cells, each containing 32 768 Josephson junctions. Two of the cells contain sub-arrays for the DAC function. The numbers of junctions in each sub-array are 128, 128, 256, 512, 1024, 2048, 4096, 8192, and 16 384. The dc bias currents are supplied to each cell through low-pass filters.

The required number of cells to generate an output voltage of 10 V as a function of the drive frequency is summarized in table 2. The output voltage is given by $V = Nf/K_{J-90}$, where $N$ is the number of Josephson junctions. The cell voltage $V_{\rm cell}$ for 32 768 junctions is given by $V_{\rm cell} = 32\,768 f/K_{J-90}$. The maximum output voltage $V_{\rm max}$ is the total voltage of 16 cells. The required number of cells $N_{10}$ is given by $10/V_{\rm cell}$. When the circuit is driven with 18.5 GHz microwaves, the maximum output voltage is 20.1 V. Eight of the 16 cells, which is equivalent to a yield of 50%, are required for an output voltage of 10 V.

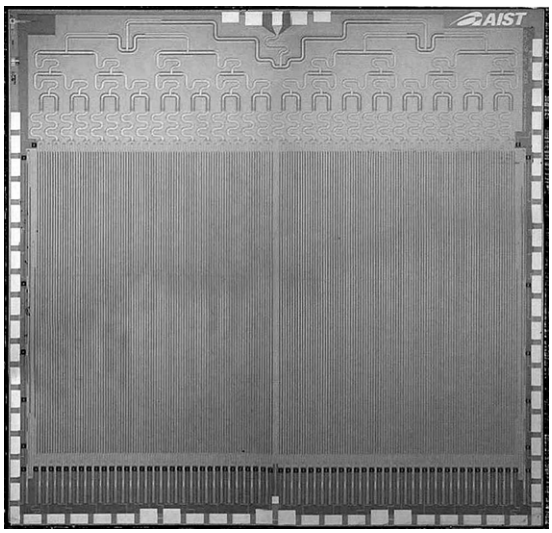


**Figure 2.** Photograph of the fabricated 10 V PJVS chip with a maximum output voltage of 20 V. The size is 15.28 mm × 14.70 mm.

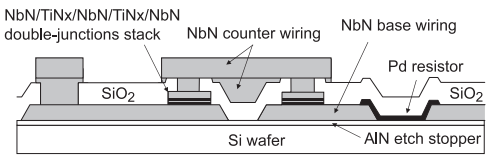


**Figure 3.** Cross-sectional schematic view of the array.

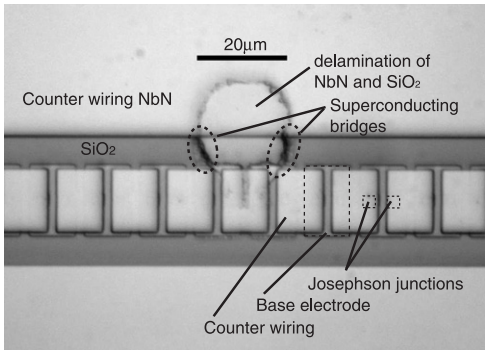


**Figure 4.** Optical micrograph showing the typical short circuit problem caused by delamination. The diameter of the hole due to delamination of both the counter NbN and $SiO_2$ films is approximately 20 $\mu$m.

**Table 3.** Layer summary.

| Layer | Material | Thickness (nm) |
|---|---|---|
| Etch stop | AlN | 2 |
| Base electrode | NbN | 200 |
| First barrier | $TiN_x$ | 25 |
| Middle electrode | NbN | 40 |
| Second barrier | $TiN_x$ | 25 |
| Counter electrode | NbN | 200 |
| Resistor | Pd | 50 |
| Isolation | $SiO_2$ | 400 |
| First wiring | NbN | 600 |
| CMP planarization | NbN | −200 |
| Second wiring | NbN | 400 |
| Passivation | $SiO_2$ | 200 |

## 3. Fabrication

Figure 2 shows a photograph of the fabricated chip. The size is 15.28 mm × 14.70 mm. Figure 3 shows a cross-sectional view of the array, although the passivation layer is not illustrated for simplicity. The typical thickness of each layer is summarized in table 3. The fabrication process was somewhat modified from that previously reported [12]. An AlN film was deposited by reactive rf sputtering instead of an Al film as an etch stop, because this decreased the risk of delamination for an isolation layer, although the reason for this was unclear.

For many years, we have struggled with a short circuit problem between the arrays and the ground. The problem was supposed as occurring at the capacitor or the CPW. Although effort was made to reduce the number of pin holes in the $SiO_2$ film, the problem was not completely resolved. Recently, it was found that delamination of the NbN film for the counter wiring damaged the isolation layer of the $SiO_2$ film. Figure 4 shows the typical short circuit problem caused by delamination. In order to avoid significant reduction in the wiring critical currents, the surface of the first NbN film was planarized by chemical–mechanical polishing (CMP), and the second NbN film was then deposited. The figure shows that the delamination of both the first NbN and $SiO_2$ films occurred before the CMP planarization, and the second NbN film remained along the contour of the hole as a superconducting bridge between the array and the ground. Some causes for the delamination may be stress in the NbN film, thermal stress after the film deposition, damage during CMP planarization, contamination of the $SiO_2$ film surface, and so on. Since the stress in the NbN film is dependent on the pressure during film deposition, it is possible to reduce it [19]. However, the pressure was optimized for the critical temperature $T_c$, and the stress in the NbN film was not reduced. Thus, the rapid temperature change of the film after deposition was avoided, because the delamination tended to occur as a result of thermal stress. The delamination shown in figure 4 occurred before the CMP planarization, because some contours of the hole on top of the junction were seen as having been planarized. However, the CMP planarization may also be one of the major causes for the damage to the layers, while it is necessary to avoid reduction of the critical current for the wiring. To avoid damage during CMP planarization, particles on the polishing table should be completely removed. Furthermore, to reduce contamination on the film surface, an *N*-methyl-2-pyrrolidone (NMP) jet was introduced to remove the photo-resist after patterning by reactive ion etching (RIE).

Due to such technical efforts, the fabrication yield was sufficiently improved for fabrication of a PJVS chip that contained up to approximately 100 000 Josephson junctions. The fabrication yield is defined by the ratio between the number of perfect chips and measured chips. The number of Josephson junctions and the density of the PJVS chip fabricated at AIST is summarized in table 4. The typical fabrication yield of the 1 V PJVS chip containing 32 768

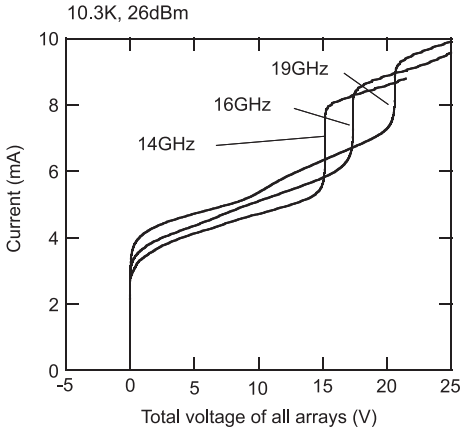


**Figure 5.** Current versus total voltage of 16 cells for various frequencies at 10.3 K. The source power of the microwave was 26 dBm.

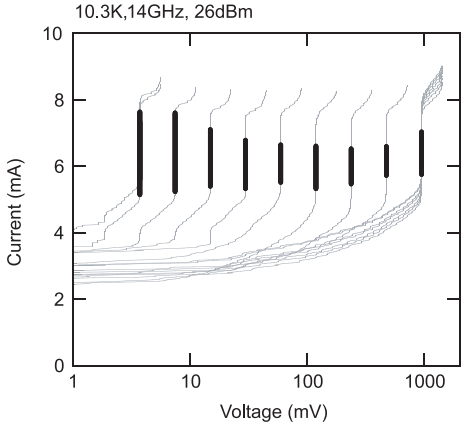


**Figure 6.** Current–voltage characteristics of the sub-arrays driven at 10.3 K. The frequency and source power of the microwave was 14 GHz and 26 dBm, respectively.

**Table 4.** Density of Josephson junctions.

| Year | Voltage (V) | Chip size (mm × mm) | Number of junctions | Junction density (junctions mm$^{-2}$) |
|---|---|---|---|---|
| 2003 | 1 | 14.7 × 4.7 | 32 768 | 474 |
| 2007 | 4 | 14.7 × 4.7 | 131 072 | 1879 |
| 2005 | 10 | 15.28 × 15.28 | 327 680 | 1403 |
| 2008 | 20 | 15.28 × 14.70 | 524 288 | 2334 |

Josephson junctions [6] was more than 50%. That of the 4 V PJVS chip, which contains 131 072 Josephson junctions [16], was decreased to approximately 30%. On the other hand, that of the 10 V PJVS chip, which contains more than 300 000 Josephson junctions [12], was not zero, but was very small. The fabrication yield tended to be dependent on both the chip size and density of the junctions, and it was not sufficiently large for fabrication of a perfect 10 V PJVS chip with under one million junctions.

The defects were categorized into four major classifications; M: insufficient margin or incorrect step voltage, due to a lack of Josephson junctions, D: disconnection in the array, R: resistive zeroth step, L: short circuit or leak between the array and the ground. Fortunately, most of the defective arrays had a zeroth Shapiro step, while the first Shapiro step was very small or zero, which was categorized as type M. If the array was not dc biased, it did not generate any voltage, because it worked as a superconductive wiring. In this case, the maximum output voltage became smaller than that of a perfect chip, but such an imperfect chip was expected to have sufficient precision. Therefore, an enlargement of the maximum output voltage may be one of the efficient ways to increase the number of available chips.

## 4. Measurement

### *4.1. Current–voltage characteristics*

The fabricated chip was mounted on a chip carrier and cooled with a cryocooler. Figure 5 shows the total voltage of all 16 cells at 10.3 K. The frequency of the applied microwave was 14, 16, and 19 GHz and the microwave power measured at the output terminal of the microwave source was 26 dBm. A summary of the current margins of each cell having 32 768 Josephson junctions at 14 GHz is presented in table 5. The upper margin of the zeroth step is equivalent to the critical current under microwave radiation. The margin of the first step is the width between the lower and upper margins. Precise measurement revealed that two cells did not have flat first steps. These are denoted by N/A at pads #21–#22 and #22–#23 in table 5. Although this chip contained two defective cells, their zeroth steps were flat and the total voltage of the other 14 cells was greater than 10 V. At least 11 cells were required for the output voltage of 10 V, as shown in table 2; therefore, this chip was considered as being available for the 10 V PJVS.

**Table 5.** Margin of 16 cells, each having 32 768 Josephson junctions.

| Pads | Number of junctions | Zeroth upper margin (mA) | First lower margin (mA) | First upper margin (mA) | First margin (mA) |
|---|---|---|---|---|---|
| #0–#9 | 32 768 | 2.03 | 5.85 | 6.55 | 0.70 |
| #9–#10 | 32 768 | 1.96 | 5.75 | 6.66 | 0.91 |
| #10–#11 | 32 768 | 2.04 | 5.95 | 6.83 | 0.88 |
| #11–#12 | 32 768 | 2.10 | 6.14 | 6.72 | 0.58 |
| #12–#13 | 32 768 | 2.07 | 6.19 | 6.84 | 0.65 |
| #13–#14 | 32 768 | 2.13 | 6.30 | 6.79 | 0.49 |
| #14–#15 | 32 768 | 2.16 | 6.40 | 6.90 | 0.50 |
| #15–#16 | 32 768 | 2.32 | 6.39 | 7.04 | 0.65 |
| #16–#17 | 32 768 | 2.30 | 6.53 | 6.97 | 0.44 |
| #17–#18 | 32 768 | 2.41 | 6.71 | 7.13 | 0.42 |
| #18–#19 | 32 768 | 2.31 | 6.59 | 6.96 | 0.37 |
| #19–#20 | 32 768 | 2.49 | 6.86 | 7.14 | 0.28 |
| #20–#21 | 32 768 | 2.51 | 6.82 | 7.02 | 0.20 |
| #21–#22 | 32 768 | 2.39 | N/A | N/A | 0.00 |
| #22–#23 | 32 768 | 2.39 | N/A | N/A | 0.00 |
| #23–#32 | 32 768 | 2.45 | 6.97 | 7.12 | 0.15 |

Figure 6 shows the $I$–$V$ characteristics of sub-arrays at 10.3 K. All $I$–$V$ curves were measured with microwave radiation at 14 GHz and 26 dBm. The bold lines are the

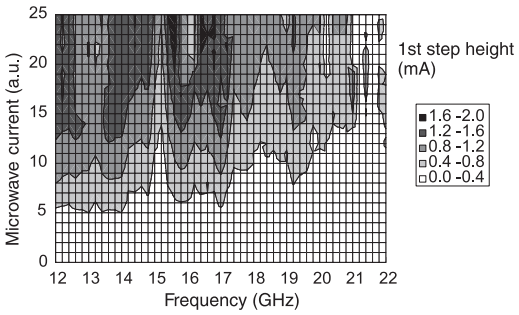


**Figure 7.** The first current margin as a function of the microwave current and frequency measured for a cell containing 32 768 Josephson junctions.

**Table 6.** Margins of sub-arrays.

| Pads | Number of junctions | Zeroth upper margin (mA) | First lower margin (mA) | First upper margin (mA) | First margin (mA) |
|---|---|---|---|---|---|
| #0–#1 | 128 | 2.81 | 5.59 | 7.34 | 1.75 |
| #1–#2 | 128 | 3.25 | 5.14 | 7.64 | 2.50 |
| #2–#3 | 256 | 3.28 | 5.23 | 7.61 | 2.38 |
| #3–#4 | 512 | 2.81 | 5.39 | 7.11 | 1.72 |
| #4–#5 | 1 024 | 2.58 | 5.32 | 6.79 | 1.47 |
| #5–#6 | 2 048 | 2.41 | 5.51 | 6.65 | 1.14 |
| #6–#7 | 4 096 | 2.08 | 5.32 | 6.61 | 1.29 |
| #7–#8 | 8 192 | 2.00 | 5.46 | 6.53 | 1.07 |
| #8–#9 | 16 384 | 2.09 | 5.72 | 6.60 | 0.88 |

constant-voltage steps that were defined using a 2 $\mu$V wide threshold. The multiple overlapping $I$–$V$ curves in the figure was the largest voltage step, corresponding to 13 array cells having 32 768 Josephson junctions each. A summary of the current margins of each sub-array is presented in table 6. Since no defective array was present in the sub-array, the DAC function was also available.

### *4.2. Frequency dependence*

Figure 7 is the measured first step height as a function of the frequency and microwave current for one of the largest cells containing 32 768 junctions; the dc bias current was supplied between the dc bias taps #9 and #10, and these numbers are marked in figure 1. The temperature was fixed at 10.3 K. The voltage was measured between the dc bias taps #0 and #32. The margin at low frequency tended to be larger than that at high frequency. In addition, as the frequency increased, a larger microwave current was required to obtain the same step heights. Even though the microwave circuit was designed to be driven by 16 GHz microwaves, the margin was obtained not only at 16 GHz, but also in a wide frequency range from 12 to 21 GHz. Since the higher frequency provided a larger output voltage, the required yield should become smaller. However, a high frequency is not necessarily good, because the margin is contrastingly small. Therefore, the drive frequency must be selected by taking both the yield and margin into account.

## 5. Conclusion

In summary, a 10 V PJVS circuit using double-barrier Josephson junctions with a maximum output voltage of 20 V was successfully demonstrated with cooling by a cryocooler at approximately 10 K. It has been shown that a chip having defective arrays is able to generate an output voltage of 10 V due to the back-up arrays. Although it is not easy to further improve the fabrication yield at present, the back-up arrays significantly increase the number of available PJVS chips, which is equivalent to an improved fabrication yield and will contribute to a reduction in chip fabrication costs.

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## References

[1] Barone A and Paterno G 1982 *Physics and Applications of the Josephson Effect* (New York: Wiley)
[2] Pöpel R 1992 The Josephson effect and voltage standard *Metrologia* **29** 153–74
[3] Gallop J 2005 The quantum electrical triangle *Phil. Trans. R. Soc.* A **363** 2221–47
[4] Hamilton C A, Burroughs C J and Kautz R L 1995 Josephson D/A converter with fundamental Accuracy *IEEE Trans. Instrum. Meas.* **44** 223–5
[5] Benz S P 1995 Superconductor–normal–superconductor junctions for programmable voltage standards *Appl. Phys. Lett.* **67** 2714–6
[6] Shoji A, Yamamori H, Ishizaki M, Benz S P and Dresselhaus P D 2003 Operation of a NbN-based programmable Josephson voltage standard chip with a compact refrigeration system *IEEE Trans. Appl. Supercond.* **13** 919–21
[7] Burroughs C J, Webber R J, Dresselhaus P D and Benz S P 2003 4 K cryocooler implementation of a DC programmable voltage standard *IEEE Trans. Appl. Supercond.* **13** 922–5
[8] Sasaki H, Yamamori H and Shoji A 2005 Suppression of temperature variation of a Josephson voltage standard chip mounted on a cryocooler *Extended Abstracts of 10th Int. Superconductive Electronics Conf.* vol 10, p PR02
[9] Pöpel R, Niemeyer J, Fromknecht R, Meier W and Grimm L 1990 1- and 10 V series array Josephson voltage standards in Nb/$Al_2O_3$/Nb technology *J. Appl. Phys.* **68** 4294–303
[10] Sakamoto Y, Yoshida H, Sakuraba T, Odawara A, Murayama Y and Endo T 1991 Josephson junction array voltage standard at the ETL *IEEE Trans. Instrum. Meas.* **40** 312–6
[11] Schulze H, Behr R, Kohlmann J, Müller F and Niemeyer J 2000 Design and fabrication of 10 V SINIS Josephson arrays for programmable voltage standards *Supercond. Sci. Technol.* **13** 1293–5
[12] Yamamori H, Ishizaki M, Shoji A, Dresselhaus P D and Benz S P 2006 10 V programmable Josephson voltage standard circuits using NbN/$TiN_x$/NbN/$TiN_x$/NbN double-junction stacks *Appl. Phys. Lett.* **88** 042503

[13] Nicolas H, Dresselhaus P D, Chong Y, Benz S P and Bonevich J E 2005 Fabrication and measurement of tall stacked arrays of SNS Josephson Junctions *IEEE Trans. Appl. Supercond.* **15** 110–3

[14] Yamada T, Sasaki H, Yamamori H and Shoji A 2008 Demonstration of a 10 V programmable Josephson voltage standard system based on a multi-chip technique *Supercond. Sci. Technol.* **21** 035002–5

[15] Budovsky I 1995 Very low frequency ac–dc transfer standard *IEEE Trans. Instrum. Meas.* **44** 367–9

[16] Sasaki H, Yamamori H, Yamada T, Fujiki H and Shoji A 2008 Evaluation of low-frequency characteristic of a thermal converter using a programmable Josephson voltage standard *CPEM 2008 Conf. Digest (Broomfield, June 2008)* pp 654–5

[17] Burroughs C J *et al* 2007 Development of a 60 Hz power standard using SNS programmable Josephson voltage standards *IEEE Trans. Instrum. Meas.* **56** 289–94

[18] Yamamori H, Itoh M, Sasaki H, Shoji A, Benz S P and Dresselhaus P D 2001 All-NbN digital-to-analog converters for a programmable voltage standard *Supercond. Sci. Technol.* **14** 1048–51

[19] Kiryu S, Shoji A, Kohjiro S and Kodaira S 1993 Stress in $NbC_xN_{1-x}$ films prepared by reactive Rf magnetron sputtering *Japan. J. Appl. Phys.* **32** L834–6