A cryogenic analog to digital converter operating from 300 K down to 4.4 K

Burak Okcan,[1,2] Patrick Merken,[1] Georges Gielen,[1,2] and Chris Van Hoof[1,2]
[1]*IMEC, Kapeldreef 75, B-3001 Leuven, Belgium*
[2]*K. U. Leuven, Department of Electrical Engineering – ESAT, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium*

(Received 23 September 2009; accepted 17 January 2010; published online 22 February 2010)

This paper presents a cryogenic successive approximation register (SAR) based analog to digital converter (ADC) implemented in a standard 0.35 μm complementary metal oxide semiconductor (CMOS) process. It operates from room temperature down to 4.4 K, achieving 10.47 effective number of bits (ENOB) at room temperature. At 4.4 K, the ADC achieves 8.53 ENOB at 50 kS/s sampling rate with a current consumption of 90 μA from a 3.3 V supply. The ADC utilizes an improved comparator architecture, which performs offset cancellation by using preamplifiers designed for cryogenic operation. The conventional offset cancellation algorithm is also modified in order to eliminate the effect of cryogenic anomalies below freeze-out temperature. The power efficiency is significantly improved compared to the state of the art semiconductor ADCs operating in the same temperature range. © *2010 American Institute of Physics.* [doi:10.1063/1.3309825]

I. INTRODUCTION

Advanced space observatory systems developed for the mid- and far-infrared wavelength region (5–210 μm) require the cooling of the sensing elements below ~5 K, in order to avoid the thermal interferences that overwhelm the signal coming from the astronomical sources.[1] These systems therefore require ultra-low-temperature front-end electronics, which are located in close proximity to the sensor arrays and cooled down to the same temperature level. Such high-performance front-end readout electronics with analog output and operating in the desired cryogenic temperature range have successfully been developed and presented in the literature.[2,3]

In current cryogenic sensor systems, however, the transmission of the analog output from the front-end electronics to the digital section, which operates at room temperature, is performed through long shielded cables resulting in electromagnetic interference and noise coupling problems. The signal integrity of the system will be improved by enabling digital data transmission, which raises the demand for an ultra-low-temperature analog to digital converter (ADC) close to the sensors. A wide temperature range of operation is also an essential feature, as it provides the possibility of fast system functionality tests at room temperature and increased flexibility.

Superconductor-based ADCs can provide high resolution (~16 bits) at very high sampling frequencies (>100 GHz) at cryogenic temperatures.[4] However, the maximum operating temperature of this type of converters is limited to a level of about 15 K.

Cryogenic ADCs developed in standard CMOS technologies are also reported in the literature.[5,6] The first one has an 8-bit successive approximation architecture,[5] while the second one is a flash ADC providing faster operation but consuming higher power for the same resolution level.[6] These converters are functional from room temperature down to 4.2 K.

The standard CMOS successive approximation ADC presented in this paper achieves a higher effective number of bits (ENOB) at a higher sampling rate and consumes less power than the cryogenic ADCs in the literature. This improvement is achieved by the development of a comparator architecture, which performs offset cancellation by using differential preamplifiers designed for cryogenic operation. The conventional offset cancellation algorithm is also modified in order to compensate for the anomalies in the transistor behavior at cryogenic temperatures.

The remainder of the paper is organized as follows. Section II describes the anomalies observed in CMOS transistor characteristics at cryogenic temperatures. In Sec. III, the challenges in achieving a high-resolution cryogenic ADC and the proposed solution are explained. Section IV demonstrates the implementation and the test results of the developed ADC. Finally, a summary is provided in Sec. V.

II. CMOS BEHAVIOR AT CRYOGENIC TEMPERATURES

The freeze-out temperature of silicon, i.e., the temperature at which the dopants cannot ionize due to the lack of thermal energy, is reported to be 30 K for the doping level of standard CMOS technologies.[7] The freeze-out effect does not prevent the conduction in a MOS transistor, since the carriers in the inversion channel are supplied by the degenerately doped source and drain regions. However, anomalous dc and transient behavior is observed in the I-V characteristics of MOS transistors operating below the freeze-out temperature.

Figure 1 shows the drain to source current (I_{DS}) versus drain to source voltage (V_{DS}) plot of an NMOS transistor in a 0.35 μm standard CMOS technology, measured at 4.4 K for two different V_{GS} voltages. In the saturation region where V_{DS} is higher than the midsupply voltage, the I_{DS} of the

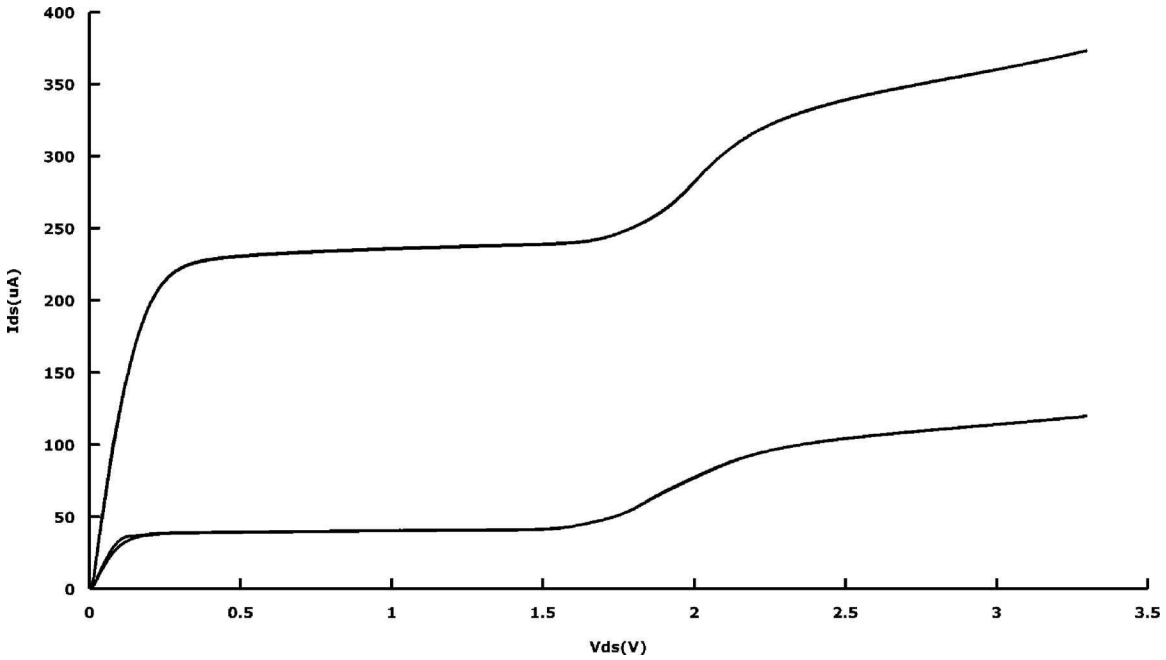

FIG. 1. I_{DS} vs V_{DS} curve of an NMOS transistor for two different V_{GS} values measured at 4.4 K in a standard 0.35 μm CMOS technology.

transistor suddenly increases with increasing V_{DS}, which is called the kink effect. The reason of this effect is the self-polarization of the bulk silicon due to the injection of the excess carriers into the substrate by the impact ionization at the drain. At low temperatures the impact ionization is observed at a lower V_{DS} due to the increased multiplication factor. The excess carriers injected into the substrate cannot be collected effectively by the substrate contact, since the resistance of the bulk silicon significantly increases due to the impurity freeze out.[8] As a result, the threshold voltage of the channel decreases with increasing V_{DS}, causing an increase in I_{DS}. For p-type transistors a similar characteristic is observed, but the kink effect occurs at a higher V_{DS} level.

The second anomaly is the hysteresis of the I-V curve at the transition between the linear and the saturation region. This phenomenon is explained by the slow recharging of the traps between the gate oxide and the silicon substrate, because of the small ionization rate at low temperature levels.[9] During the transition from the linear to the saturation region, the formation of the depletion layer is delayed, resulting in a further increase in the current until a sufficient amount of V_{DS} is achieved. After this point, the current drops to its stable saturation value, which is equal to the value during the high to low V_{DS} sweep. Although the amount of hysteresis observed in a 0.35 μm CMOS technology is not as large as the values reported before for other technologies, it is still critical for a high-resolution ADC application and must be taken into account during the converter design.

The anomalies explained above can be modeled analytically.[10] There are however no real circuit simulation models available for the complete behavior of the transistor in the freeze-out temperature region. The design methodology followed in the previous studies is based on the prevention of the transistors operating in the anomalous region of the I-V characteristics.[2,5,6] In this work a similar technique is used to prevent the kink effect, while the hysteresis is compensated by a modified offset cancellation algorithm. Transistor dimensions are determined according to SPICE simulations using the mobility and the threshold voltage values at cryogenic temperatures, which have been extracted from individual device measurements.

III. CRYOGENIC ADC DESIGN

The successive approximation register (SAR) algorithm has been proven to be a power-efficient analog to digital conversion technique, providing effective resolutions around 10 bits at sampling rates up to 100 kS/s.[10,11] Figure 2 shows a fully differential low-power SAR ADC architecture consisting of a fully passive capacitive feedback digital to analog converter (DAC), a digital circuit and a high-resolution comparator. This architecture suits the cryogenic applications, as the passive components and the digital circuits are

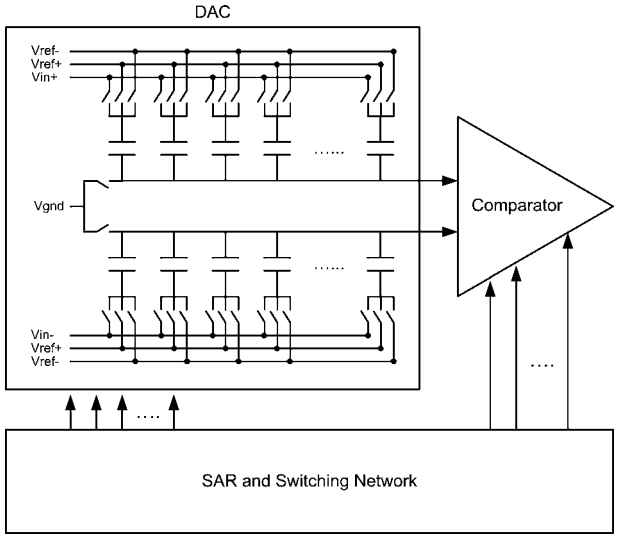

FIG. 2. Fully differential low-power SAR ADC architecture.

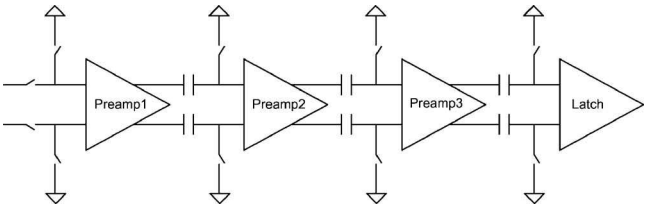

FIG. 3. Circuit diagram of a comparator composed of low-gain preamplifiers and a latch.

still functional at very low temperatures. The most challenging building block in this topology is the high-resolution comparator. This is difficult to design for cryogenic temperatures, not only because of the mentioned anomalies, but also because of the extra mismatch of the transistor parameters yielding a higher offset. In order to overcome this high offset, a preamplification and offset cancellation technique is used. The traditional preamplifier circuit architecture and the offset cancellation algorithm are also adapted to the cryogenic temperature operation.

Figure 3 shows the circuit diagram of the comparator composed of low-gain preamplifiers and a latch. The output offset storage based autozeroing technique has been proven to be an efficient way of implementing low-offset preamplification for high-resolution comparators.[12] In this technique the preamplifier inputs are connected to a reference voltage, which is typically the input common-mode voltage level, and the output offset voltage is stored on the coupling capacitors. During the amplification, the offset voltages stored on the capacitors are subtracted from the output of each preamplifier stage and the output is transferred into the next stage without any offset.

Low-gain preamplifiers can be implemented by a single-stage differential amplifier with diode-connected load transistors. However, at cryogenic temperatures a simple differential amplifier does not operate properly due to the kink effect. The voltage increase on the drain terminal of one of the input-pair transistors causes a steep increase in the current, which affects the voltage to current conversion of the input pair and causes malfunction. A solution to this problem is the implementation of a cascode stage in order to limit the drain to source voltages of the input-pair transistors. The drain to source voltage limitation avoids the input-pair transistors entering the kink region.

In the conventional low-power SAR architecture, the offset storage is performed in the beginning of the conversion process, which is followed by the bit cycling.[11] This method is however not reliable for cryogenic temperatures due to the hysteresis in the preamplifier operation. For large DAC outputs, one of the input-pair transistors turns off during a comparison cycle. When the transistor turns on in the next cycle, the offset voltage of the differential amplifier is going to be different than that of the previous cycle because of the hysteresis in the operating point of the transistors. Therefore, the autozeroing is performed after each comparison in order to store and subtract the new offset voltage.

Figure 4(a) shows the circuit diagram of the first preamplifier including the switches, the autozero capacitors, and the timing signals. The "amplify" signal is used to drive the switch, which connects the first stage to the feedback DAC. This signal must be disabled before the autozero cycle starts, in order to avoid a distortion in the DAC output. Therefore, the "autozero" and the "amplify" signals must be nonoverlapping signals. A critical error source of this configuration is the charge injection from the autozero switches to the coupling capacitor. Although the differential error depends on

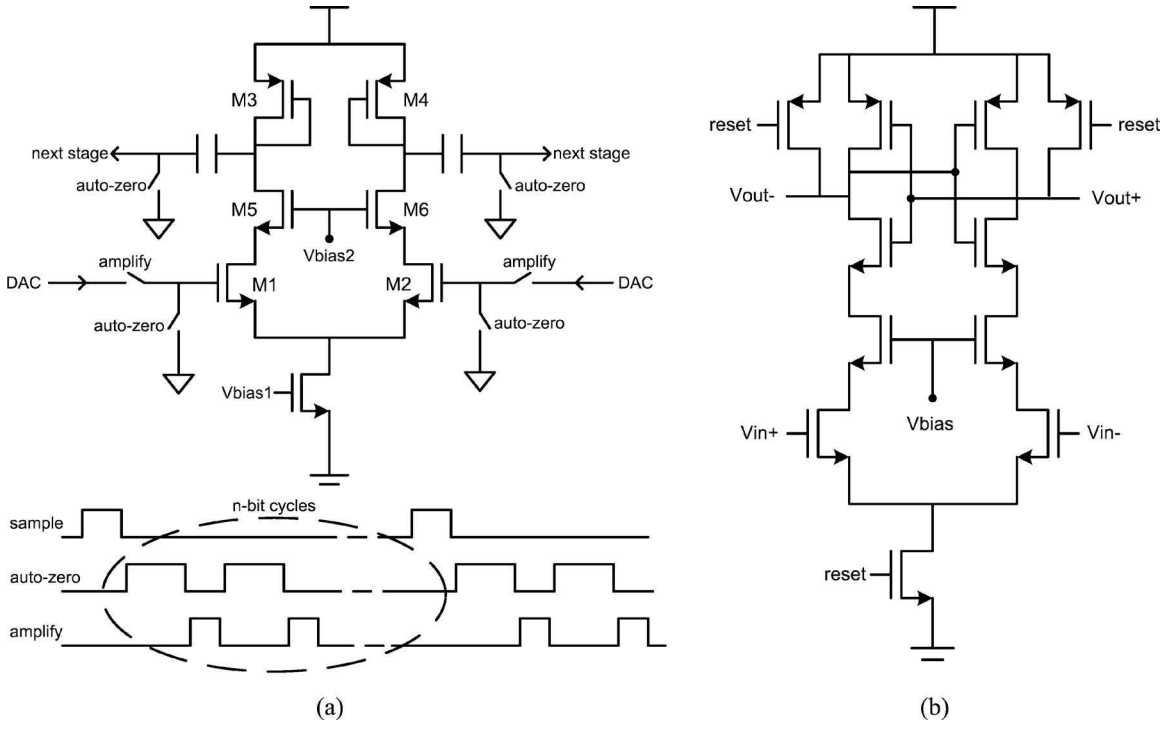

FIG. 4. (a) Circuit diagram of the first preamplifier including the switches, the autozero capacitors, and the timing signals. (b) Circuit diagram of the latch.

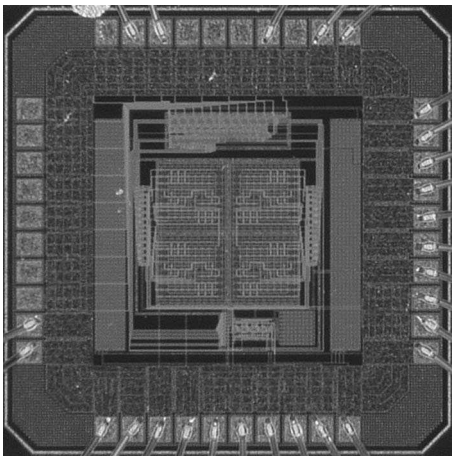

FIG. 5. Photograph of the fabricated ADC chip. The chip measures 1650 $\times 1600$ μm^2.

the matching of the switches and the coupling capacitors, which can be reduced by proper layout techniques, it can be further reduced by sequentially opening the autozero switches starting from the first preamplifier. This timing scheme allows every stage to store and cancel the charge injection of the preceding stages. Figure 4(b) shows the circuit diagram of the latch.

The three-stage preamplifier gain has been determined by assuming a latch offset of 90 mV at 4.4 K, which has been measured from a previous test run. The gain is adjusted to give an input-referred offset voltage of 400 μV, which corresponds to the half-LSB level of 12-bit resolution for a signal swing of 3.3 V. The dc gain and the 3-dB bandwidth of the preamplifier are given by

$$A_{\mathrm{dc}} = \frac{gm_{1,2}}{gm_{3,4}}, \quad \mathrm{BW} = \frac{gm_{3,4}}{2\pi C_L}, \tag{1}$$

where the transconductance gm is a temperature-dependent parameter due to its dependence on the mobility

$$gm = \sqrt{2\mu C_{\mathrm{ox}} I_D \frac{W}{L}}. \tag{2}$$

The electron and hole mobility values increase with decreasing temperature.[13,14] In addition, since the increase in the mobility of electrons is higher than that of holes, both the gain and the bandwidth of the preamplifier are expected to increase at cryogenic temperatures. Therefore, transistor dimensions and bias currents are determined using room temperature parameters, which give the minimum gain and bandwidth in the whole range from room temperature down to 4.4 K. Another important issue that has to be considered in the preamplifier design is the increase in the threshold voltage with decreasing temperature. In order to keep the transistors in the correct operating region over the whole temperature range, proper design margins have to be considered.

IV. CHIP IMPLEMENTATION AND TEST RESULTS

The ADC has been implemented in a conventional 0.35 μm double-poly, five-metal CMOS process. The feedback DAC is realized by using poly-poly-capacitors, where the digital section is implemented by the standard library of the technology. All the bias signals and the clock signal are connected to input pads in order to be applied externally, since there are no cryogenic bias circuits or clock generators available for CMOS technologies. Figure 5 shows the photograph of the fabricated chip, which measures 1650 $\times 1600$ μm^2.

The performance of the ADC has been tested first with a tone test at room temperature. A fully differential sinusoidal signal with a frequency of 830 Hz is applied to the ADC sampling at 50 kS/s. The sinusoidal signal has been applied from a DS360 ultra low distortion function generator, which provides sufficiently low jitter distortion and high frequency accuracy for the targeted specifications. The output spectrum is obtained by the fast Fourier transform of 65 536 output

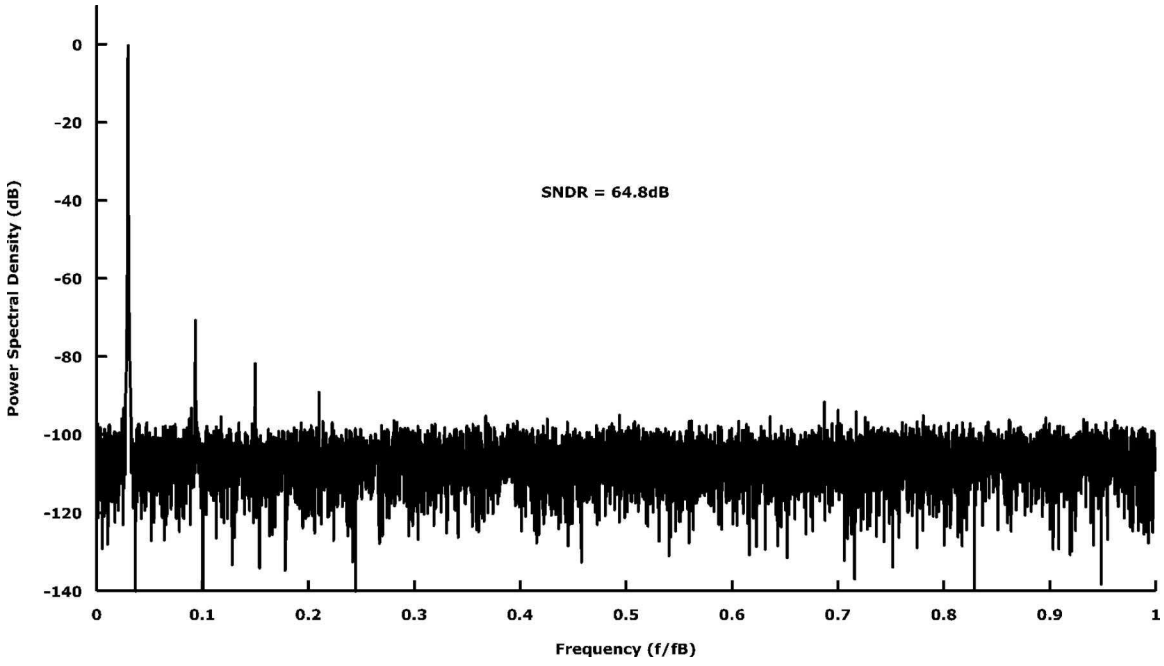

FIG. 6. Output spectrum of the ADC at room temperature.

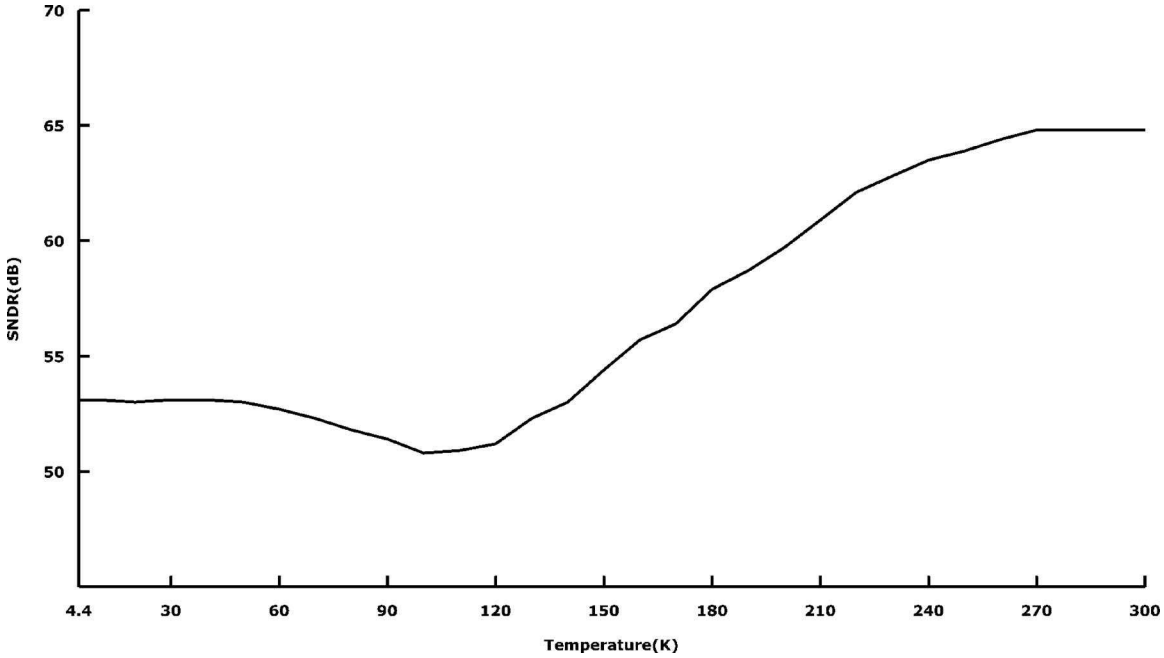

FIG. 7. SNDR vs temperature characteristic of the ADC.

samples. Figure 6 shows the output spectrum of the ADC at room temperature. The signal-to-noise-plus-distortion ratio (SNDR) is calculated as 64.8 dB, which corresponds to an ENOB of 10.47 bits according to the following formula:

$$\text{ENOB} = \frac{\text{SNDR(dB)} - 1.76}{6.02}. \tag{3}$$

In order to investigate the low-temperature performance, the tone test has been repeated at different temperature levels down to 4.4 K. Low-temperature tests are performed using a bath cryostat, which provides cooling using a constant liquid helium flow. The cryostat allows temperature control between room temperature and 4.4 K with an accuracy of 0.1 K. Figures 7 and 8 show the measured SNDR versus temperature characteristic and the output spectrum of the ADC at 4.4 K, respectively. The SNDR is 53.1 dB at 4.4 K, which is equivalent to 8.53 bits of ENOB. The total current consumption is measured as 90 μA from a 3.3 V supply.

According to Fig. 7, the performance of the ADC does not drop in the freeze-out temperature region, i.e., below 30 K, which means that the cryogenic anomalies are successfully eliminated. On the other hand, the ADC performance reduces with respect to room temperature, which is due to a higher comparator offset caused by dynamic errors. With de-

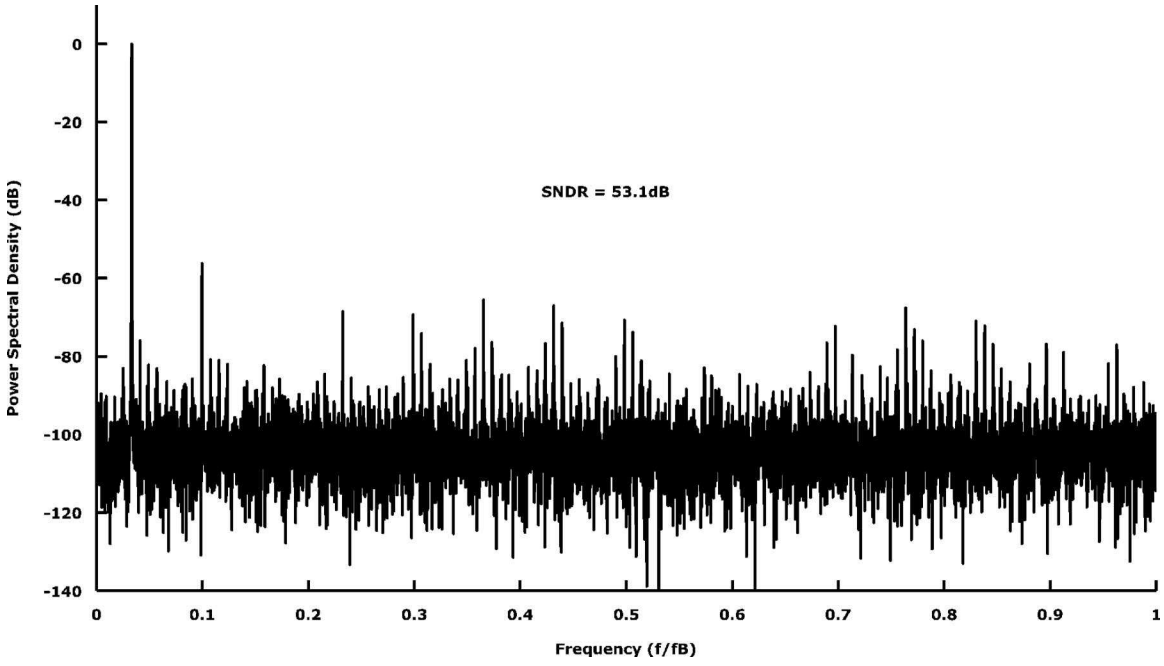

FIG. 8. Output spectrum of the ADC at 4.4 K.

TABLE I. Comparison of the proposed ADC with the state-of the art ADCs that operate from room temperature down to cryogenic temperatures.

Reference no.	Sampling rate (kS/s)	Resolution (bits)	Power dissipation (μW)	FOM (pJ/step)
5	3	8	350	455.7
6	12.5	8	5000	1562.4
This Work	**50**	**8.53**	**297**	**16.1**

creasing temperature, the charge injections of the switches increase with the increasing mobility. In addition, the deterioration of the device matching enhances the effect of charge injection on the latch offset. Consequently, the actual latch offset will be higher than the expected value based on individual device measurements. Similarly, the observed spurious high-frequency signals likely arise from distortion in the feedback DAC, which is caused by the floating switches connecting the DAC and the comparator. This explanation is also supported by the SNDR versus temperature curve shown in Fig. 7. The SNDR drops to its minimum value around 100 K, where the carrier mobilities are expected to be around their maximum values,[14] hence resulting in the maximum amount of charge injection. A possible solution to avoid the DAC distortion is the implementation of a buffer stage between the DAC and the comparator. The excessive latch offset can also be compensated by increasing the preamplification gain.

To the best of the authors' knowledge, the proposed ADC architecture shows the most energy efficient performance compared to state-of-the-art cryogenic ADCs operating over the same temperature range. This comparison is based on the conventional figure of merit (FOM) that quantifies the average energy per effective conversion step,[10,11]

$$\mathrm{FOM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \cdot f_s}. \tag{4}$$

Table I shows a performance comparison of this work with the state-of-the-art ADCs present in the literature that operate from room temperature down to cryogenic temperatures.[5,6] The proposed ADC performs the highest sampling rate at the lowest power dissipation, hence achieving the best FOM of 16.1 pJ/step.

V. SUMMARY

A cryogenic successive approximation ADC has been designed and implemented in a standard CMOS technology. It operates from room temperature down to 4.4 K. The ADC achieves significantly improved power efficiency compared to the state-of-the-art ADCs operating over the same temperature range. A drop in performance has been observed at cryogenic temperatures with respect to room temperature. In future designs this can be improved by some design modifications. It can be concluded that the proposed ADC architecture is very promising for high-resolution cryogenic ADC implementations.

[1] B. Swinyard and T. Nakagawa, Exp. Astron. **23**, 193 (2009).
[2] Y. Creten, O. Charlier, P. Merken, J. Putzeys, and C. Van Hoof, J. Phys. IV **12**, 203 (2002).
[3] H. Nagata, H. Shibai, T. Hirao, T. Watabe, M. Noda, Y. Hibi, M. Kawada, and T. Nakagawa, IEEE Trans. Electron Devices **51**, 270 (2004).
[4] O. A. Mukhanov, D. Gupta, A. M. Kadin, and V. K. Semenov, Proc. IEEE **92**, 1564 (2004).
[5] Y. Creten, P. Merken, W. Sansen, R. Mertens, and C. Van Hoof, Proceedings of the IEEE International Solid-State Circuits Conference, 2007 (unpublished), pp. 468–469.
[6] Y. Creten, P. Merken, W. Sansen, R. Mertens, and C. Van Hoof, IEEE J. Solid-State Circuits **44**, 2019 (2009).
[7] B. Dierickx, L. Warmerdam, E. Simoen, J. Vermeiren, and C. Claeys, IEEE Trans. Electron Devices **35**, 1120 (1988).
[8] G. Ghibaudo and F. Balestra, Proceedings of the 20th International Conference on Microelectronics, 1995 (unpublished), pp. 613–622.
[9] V. S. Lysenko, I. P. Tyagulski, Y. V. Gomeniuk, and I. N. Osiyuk, Semicond. Phys., Quantum Electron. Optoelectron. **4**, 75 (2001).
[10] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, Proceedings of the IEEE International Solid-State Circuits Conference, 2008 (unpublished), pp. 246–247.
[11] N. Verma and A. P. Chandrakasan, IEEE J. Solid-State Circuits **42**, 1196 (2007).
[12] E. Shirai, IEEE Trans. Circuits Syst., II: Express Briefs **54**, 166 (2007).
[13] W. F. Clark, B. El-Kareh, R. G. Pires, S. L. Titcomb, and R. L. Anderson, IEEE Trans. Compon., Hybrids, Manuf. Technol. **15**, 397 (1992).
[14] D. P. Foty and S. L. Titcomb, IEEE Trans. Electron Devices **34**, 107 (1987).