# "The CMOS Inverter" as a comparator in ADC designs

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**Abstract--This paper introduces a single-ended non-offset-cancelled flash ADC architecture, the "Threshold Inverter Quantizer" (TIQ). The TIQ is based on a CMOS inverter cell, in which the voltage transfer characteristics (VTC) are changed by  systematic transistor sizing.  As a result, a significant  improvement of speed and reduction of area and power consumption is achieved.**

## I. INTRODUCTION

Although the full-flash type A/D converter architecture is the most attractive solution for high-speed A/D converter designs, from a power dissipation and area perspective it is not efficient for the resolution of more than 8-bits. As long as the resolution level is kept small, the comparator count will be reasonable, and its offsets are not critical. Therefore the comparator structure is the most critical part in full-flash type architectures. There are primarily three types of comparator structures used in A/D converter designs in the literature. The differential amplifier type, dynamic (auto-zero), and the fully differential latch-type comparators are commonly used structures in CMOS flash A/D converter designs [1], [2], [3], [4].

Some of the main problems of the conventional comparator structures used in A/D designs can be listed as follows:
1. large transistor area for higher accuracy
2. DC bias requirement
3. charge injection errors
4. metastability errors
5. high power consumption
6. resistor or capacitor array requirement

In this paper, however, a new approach, the Threshold Inverter Quantizer (TIQ), based on systematic transistor sizing of a CMOS inverter in a full-flash scheme, eliminates the resistor array implementation of conventional comparator array flash designs. Therefore no static power consumption is required for quantizing the analog input signal, making the idea very attractive for battery-powered applications. However there are five main disadvantages of the TIQ approach:
1. It is a single-ended structure.
2. It requires $2^n$ -1 number of different area-sized quantizer designs.
3. It requires a separate 5V reference power supply voltage for analog part only due to poor power supply rejection ratio.
4. It has slight changes in linearity measures (DNL, INL) and the maximum analog input signal range due to process parameter variations. These problems can easily be handled by front end signal conditioning circuitry.
5. It requires a S/H at the analog input to increase the performance and to reduce the power consumption during metastable stage.

The following sections include the simulation (0.8-micron simulation only) and test (2-micron fabricated) results for the TIQ approach.

## II.  THE TIQ STRUCTURE

The TIQ consists of two cascaded CMOS inverters as shown in Fig. 1 (a). The analog input signal quantization level is set in the first stage by changing the voltage transfer curve (VTC) by means of transistor sizing [5]. Since the transistor channel length, L, is more effective than the channel width, W, in controlling the performance ($f_T \propto 1/L^2$), L is kept constant and only W is changed during the design process.

The second inverter stage is used for increased gain and logic level inversion so that the circuit behaves as an internally set comparator circuit. The key point with the second stage is that the second stage must be exactly the same as the first stage to maintain the same DC threshold levels, and to keep the linearity in balance for the voltage rising and falling intervals of high frequency input signals.

It can be shown that the Vth point on the VTC of a CMOS inverter, which is shown in Fig. 1 (b), can approximately be given by the following equation [6],[7]:

$$Vth = \frac{Vdd - |Vtp| + Vtn\sqrt{Kn / Kp}}{1 + \sqrt{Kn / Kp}}$$

where Vtn and Vtp are the threshold voltages for NMOS and PMOS devices, respectively;  and
$Kn = (W/L)_n$ . $\mu n\, Cox$

$Kp = (W/L)_p \cdot \mu p \, Cox.$

However due to non-ideal effects such as short channel and narrow channel effects, the above equation cannot be practical for the design process, therefore higher level MOS transistor model equations are necessary. In this study, the BSIM3 [8] model in which the effective threshold voltages are re-calculated after the transistor sizing processs to handle these non-ideal effects such as narrow channel effects [8]. The HSPICE circuit simulation is used to determine the proper transistor sizes together with a computer program automatically.
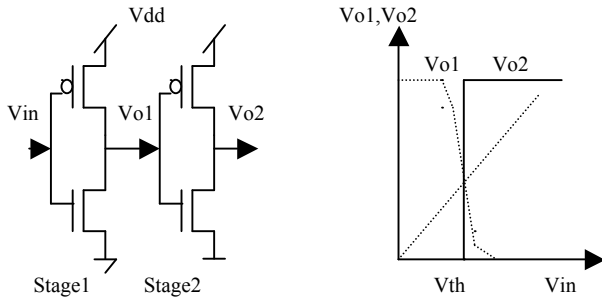


Fig. 1 (a)  TIQ schematic    (b) Voltage transfer curve (VTC)

The design steps obtained from a computer program can be explained by referring to Fig. 2 as follows:

1.  Design a minimum size inverter and verify the threshold voltage value of the midpoint quantizer, Qn, using the HSPICE circuit simulator by substituting BSIM3 (Level 49) spice model test parameters obtained from a vendor for a specific technology. Note that the channel length is kept at the minimum value during the entire design process.

2.  Estimate a safe analog input voltage range as follows:
    *Analog range = Vdd - (VTN + | VTP|),* where *VTN* and *VTP* are the threshold voltages for large NMOS and PMOS devices, namely the VTHO value from the model parameter data set used during the entire design process.
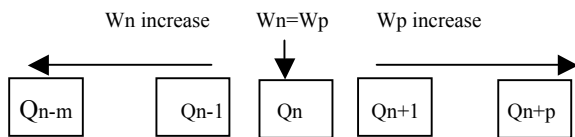


Fig. 2  Block diagram of the design process

3.  Calculate the LSB value as follows:
    *LSB = Analog range/ $2^n$.*

4.  Calculate the ideal threshold points for each quantizer ($Q_{n-m}$ … $Q_{n+p}$) accordingly, assuming the midpoint value for Qn is in the center.
5.  Run the HSPICE simulator to obtain the corresponding closest possible channel widths. Note that for the quantizers of $Q_{n+1}$ … $Q_{n+p}$), the so-called PMOS side, (W/L)n is kept at minimum value, but only the channel widths of the PMOS transistors are changed to minimize the current flow during the transition of VTC (metastable region). This process is applied to the NMOS side in the opposite way.
6.  Lay out the entire circuit.
7.  Replicate this entire quantizer block and complete the interconnections to obtain the cascaded structure, which will be the analog part of the entire A/D converter.

One can easily conclude that the designer cannot achieve the desired theoretical ratios by having a minimum sensitivity of only one lambda unit area change on the layout and also due to possible errors during fabrication process. Hence the analog input range and the linearity measures (DNL and INL) are affected by these nonideal factors. However the monotonicity of the converter is expected to be maintained.

## III. RESULTS FOR TIQ4 DESIGNS THE SIMULATION AND TEST

The design process explained above has been applied to design the TIQ4 in two different technology, 2μ (fabricated) and 0.8μ (simulation only) CMOS n-well. Fig.3 shows the DC simulation results for the TIQ4 in 0.8μ design. Simulation results include 0.27 LSB of DNL and 0.18 LSB of INL for the design of TIQ4 in 2μ CMOS n-well technology, and 0.33 LSB of DNL and 0.22LSB of INL in 0.8μ CMOS n-well technology. These results neglect additional linearity errors, which may occur in the digital part of the complete converter. The largest transistor size in the TIQ4 is only (W/L)n= (24μ/2μ) in the 2μ design.

In AC operation, by employing a S/H at the input, a Nyquist sampling rate of 300 MHz for TIQ4 has been



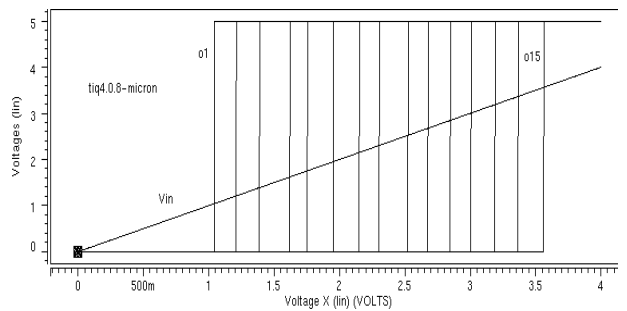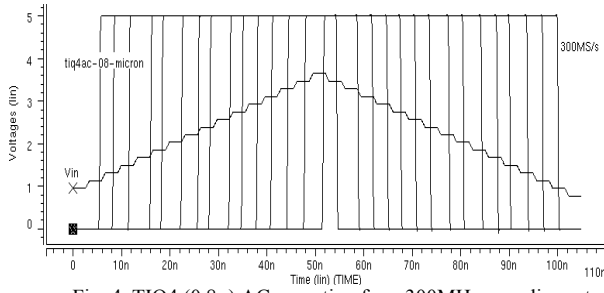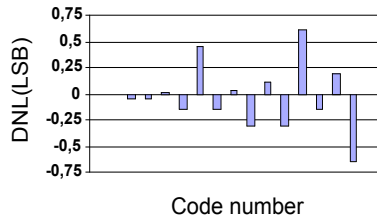Fig. 3 TIQ4 (0.8μ) threshold levels

Fig. 4 TIQ4 (0.8μ) AC operation for a 300MHz sampling rate

achieved. This maximum sampling rate reduces to 100 MHz for the 2μ design. Simulation measurements are taken under ideal sampling conditions. In fact, the S/H circuit design is not included in this study. Fig. 4 shows the AC operation at the maximum sampling rate for the TIQ4. The DC and the AC results are also tabulated in Table I.
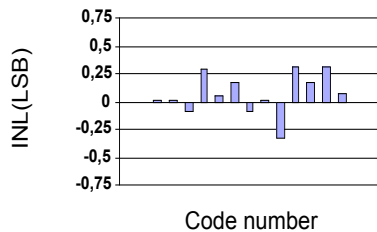
### TABLE I SIMULATION RESULTS FOR TIQ4 (ANALOG PART ONLY)

|                     | TIQ4(2μ) | TIQ4(0.8μ) |
|---------------------|----------|------------|
| DNL (LSB)           | 0.27     | 0.33       |
| INL (LSB)           | 0.18     | 0.22       |
| Sampling Rate (MHz) | 100      | 300        |
| Avg. Power (mW)     | 3.35     | 4.86       |
| Chip area (mm2)     | 0.035    | 0.006      |
| Analog Range (Vpp)  | 1.72     | 2.7        |

Fig. 5 and Table II show the worst case linearity plots (INL and DNL) and performance summary for the fabricated four sample TIQ4 (in 2μ n-well CMOS) chips, respectively.



(a)



(b)

Fig.5 (a) Differential non-linearity plot (b) Integral non-linearity plot

### TABLE II. COMPLETE TIQ4 BASED ADC SUMMARY (TEST RESULTS)

| | |
|---|---|
| DNL | 0.65 LSB |
| INL | 0.34 LSB |
| Input Voltage Range | 1.65Vpp |
| Static power dissipation | 0.4mW |
| Active chip area | 0.4mm2 |
| Sampling rate | 100 MHz |
| Technology | 2-micron CMOS n-well |
| Power supply | 5V |

The layout photo for the complete ADC is shown in Fig.6.



Fig.6 Layout photo of TIQ4 based ADC

## IV. THE DESIGN OF TIQ6 AND SIMULATION RESULTS

In the design process explained previously, keeping the one side transistors sizes at their minimum value simplifies the design process and reduces the power consumption. However after substituting a typical process parameter data set in Equation 1, one will see that the maximum resolution level that can be achieved is only 4-bits. This is because only one lambda-unit channel width change between mid-point quantizer (where Wn is equal to Wp) and its neighbors results in about 150 milivolts of minimum achievable voltage step, namely the Least Significant Bit (LSB) value.

We next introduce a modification of the TIQ design process, in which basically the both transistor channel widths are allowed to change at the same time to obtain the closest threshold point to the desired one. This leads to a maximum achievable resolution level of 8-bits. The new design methodology is obviously more complicated than the former one, and requires larger transistor sizes, and surely consumes more power. However the design has automatically been done by a developed computer optimization program [5]. Figs. 7 and 8 show the DC and AC simulation results of the TIQ6 design as an example. Note that the TIQ6 has peak current of 15mA at maximum sampling rate.
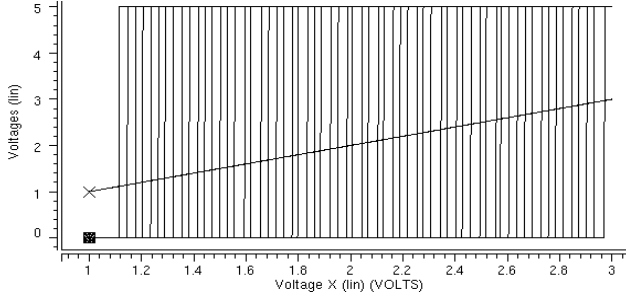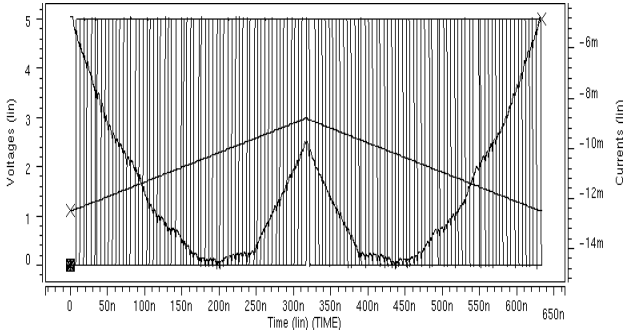
Fig. 7 The TIQ6 threshold levels



Fig. 8 The TIQ6 AC operation for 200MHz sampling

## V. ANALYSIS OF PROCESS PARAMETER VARIATIONS

It seems that the main drawback with the TIQ approach is that it is process parameter dependent. To analyze this effect the three critical size inverters (N-size maximum, N and P-size minimum, and P-size maximum) are chosen and simulated for six different 0.8μ Spice parametric test results obtained from the vendor. Fig. 9 shows the random changes on the corresponding three different threshold points. The simulation results shows that the maximum deviation due to process parameters is in the range of 90mV, and occurs in the minimum size inverter.

To analyze the effect of this change on the linearity measures, the original design of TIQ6 has also been simulated for the process parameters provided by a vendor for six other Spice parametric test results without making any changes in the beginning TIQ6 layout.
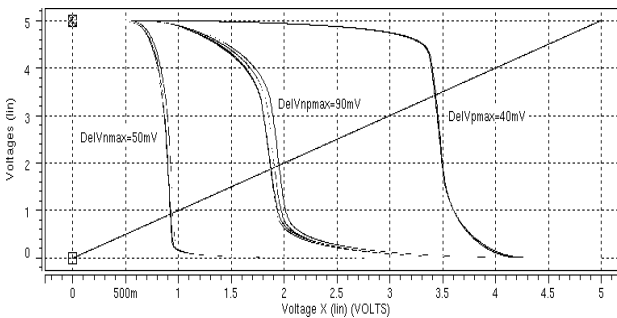


Fig. 9 Process parameter change

These simulation results show that the analog input range is affected only by process parameter changes. However the linearity measures are still in an acceptable range, which keeps the converter monotonic. This is because a converter is always monotonic as long as the INL is maintained at less than 0.5 LSB [9].

The second important issue is of course the matching properties on the wafer. Due to non uniform distribution of the dopant atoms in the bulk, threshold voltage mismatch in both PMOS and NMOS devices of large and small geometry must also be considered [10] . In fact, according to the DC linearity test measures taken on four different fabricated sample chips, matching non-idealities are less important in this new approach as long as the resolution is kept at small levels (currently less than 7-bit) as shown in Fig.10, in which the maximum deviation of threshold points due to mismatching is less than 20mV.
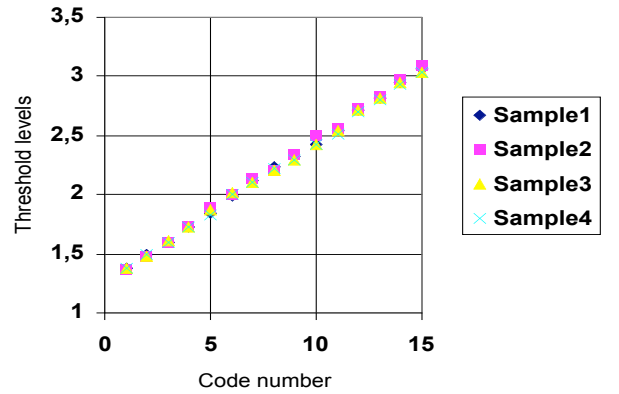


Fig. 10  TIQ4 matching test results over four sample chips

Finally, temperature effects have also been investigated, and the simulation result indicate a safe temperature range of between -40 and 85  C [5]. The temperature effect becomes important for more than 7-bits resolution levels.

## VI. CONCLUSION

A new analog technique so called TIQ for FLASH type A/D converters has been developed and simulated in two different technologies (0.8μ and 2μ CMOS n-well), and also 3-bit and 4-bit versions of TIQ based A/D converters have been fabricated in 2μ CMOS n-well technology as a supporting work for the new approach. Simulation and test results show that this technique is much more area and power efficient when compared to conventional comparator-array structures of comparable performance [2], [4], [11], [12], [13], [14], [15]. Traditional methods have been applied to the remaining (digital) part of the converter.

In conclusion, this proposed scheme has the following advantages when compared to traditional comparator based designs:

1. There is very little static power consumption excluding the S/H at the input. This makes the idea very attractive for battery-powered applications.
2. If a S/H is employed at the input, the TIQ is a more power and performance efficient method.
3. The TIQ doesn't require a resistor array implementation.
4. A significant amount of area reduction can be obtained.
5. Monotonicity is always expected to be maintained.

TIQ3 and TIQ4 can be used as a building block for semi-flash [2], pipeline [3], [4], [15],[16] or folding [11], [17] types of fast A/D converter architectures. As a result, significant reductions of power and area can be achieved even higher than 8-bit resolution levels. It is also projected that a TIQ-based complete A/D converter library cell could be put on a microprocessor chip, leading to a more compact DSP VLSI integration.

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