# Experimental Characterization of Bit Error Rate and Pulse Jitter in RSFQ Circuits

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***Abstract*— Rapid Single Flux Quantum (RSFQ) logic is well-known for its ultra-high switching speed and extremely low power consumpition. In this paper, we present two original experiments to demonstrate that it's also a reliable technology and its reliability is sufficient even for such a large-scale system as a proposed petaflops-scale HTMT computer. We have measured the bit error rate (BER) for a circular register of inverters representing a critical path of a 64-bit integer adder, and timing jitter in a 200 Josephson junction (JJ) long transmission line, imitating a branch of a clock distribution tree, both being important and representative building blocks of the HTMT computer. For the adder critical path we have demonstrated the highest clock frequency of 17 GHz, latency of 860 ps and BER of $10^{-19}$ for $3.5\mu m$ technology of HYPRES, Inc. The value of timing jitter was 200 fs per JJ for $1.5\mu m$ technology of TRW, Inc. These figures are in good agreement with our simulations.**

## I. Introduction

Recent development of an advanced $1.5\mu m$ Nb-trilayer RSFQ technology [1], and of a new microprocessor architecture optimized for RSFQ implemenation [2], opens bright perspectives for RSFQ digital design. As two of the most important and representative components of a microprocessor are the clock distribution tree and the arithmetic-logic unit (ALU), special attention must be payed to the reliability of these two components.

In [3], we described the design and simulation results for an RSFQ integer 64-bit carry look-ahead (CLA) adder, which has ca. 60,000 JJs and is an important ALU component. As a first step, we resorted to testing just its critical path which consists of 10 stages of inverters with intermediate splitters and mergers (about 300 JJs) using a circular register type of experiment, similar to "ring oscillator" experiments used by semiconductor designers to determine the highest operating frequency and error rate of logic circuits. The goals of this experiment were to verify the correctness of our library cells and of our approach to connecting them together in relatively large circuits and to measure the operating frequency, latency and BER of the complete circuit [1]. To our knowledge this is the first experiment which measured the BER of such a complex RSFQ circuit. It is described in Section II.

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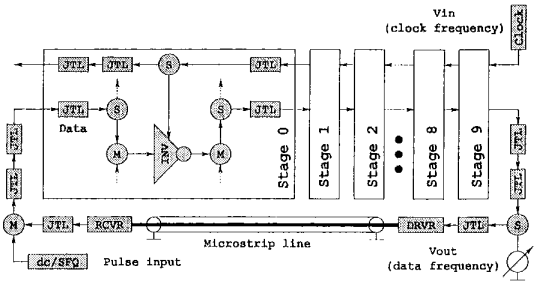


Fig. 1. 64-bit integer adder critical path (HF experiment).

Consistent operation of all logic gates and registers at high speed strongly depends of accurate and timely delivery of clock SFQ pulses. The main cause of clock distortion is timing jitter in Josephson junctions. To directly measure the timing jitter, we have designed an original interferometric experiment where a high-speed RSFQ circuit (pulse merger) is used as a sampling tool. This experiment is described in Section III.

## II. 64-bit CLA Critical Path Experiment

The schematics of the experiment is presented in Fig. 1. It is a ring which incorporates a chain of stages and a feedback path (implemented as a microstip line). Each stage consists of an inverter, two splitters and two mergers ("INV", "S" and "M") in the data path and a splitter in the clock path. Stages are interconnected using Josephson Transmission Line (JTL) segments of two JJs each. Since this is just a one-bit critical path of a complete adder, one port of each merger/splitter is not used. A 64-bit CLA needs $log_2(64) = 6$ stages to compute all carry "propagate" and "generate" signals and 4 more to compute the initial "propagate"/"generate" bits and the final sum (2 stages each). Thus, our circuit incorporates 10 stages.

All inverters are clocked using a counterflow clock generated by an overbiased Josephson junction, the average

[1] It is important to notice that an arbitrary Boolean function can be implemented in a similar fashion with a circuit consisting only of RSFQ mergers, splitters and inverters.

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voltage on this junction $V_{in}$ determines the clock frequency. We also have an ability to inject a data pulse into the first stage using a dc/SFQ converter and measure the average voltage on the data line $V_{out}$ which corresponds to data circulation frequency. Switching off the power supply current in the microstrip line receiver disables pulse propagation in feedback path and clears the circuit.

A corresponding low-frequency experiment has a dc/SFQ converter instead of a clock generator and an SFQ/dc converter to monitor the data pulse in place of $V_{out}$ connection. This experiment allows us to verify circuit correctness and measure the operating margins of the circuit at low frequency.

### A. *Circuit behavior*

If the feedback path power supply is switched off, the next 10 clock pulses bring the circuit to its initial state, so that the first inverter is always in state "0" and generates "1", the second inverter is in state "1" and generates "0", *etc.* Since we have an even number of stages in the chain the right-most inverter will always be in state "1" and generate "0". At this point the feedback path power can be switched on, clock pulses maintain the same bit pattern and $V_{out} = 0$.

If a pulse is injected in the first inverter using the dc/SFQ converter, it propagates through the inverter chain and eventually shows up at the output, returns to the first inverter via the feedback path and circulates this way until an error occurs [2]. In this state, we will see non-zero $V_{out}$ (in the high-frequency experiment) or observe data monitor switching every 10th clock pulse (in the low-frequency experiment). We can also inject more data pulses and see them circulating in the loop. Notice that because the bit pattern within the inverter chain is alternating, this experiment tests both $1 \rightarrow 0$ and $0 \rightarrow 1$ transitions in the inverters.

The analysis above was performed under the assumption that the clock period is larger than the longest propagation delay between stages (the one that includes the return microstrip line). This should not necessarily be the case. Our RSFQ asynchronous elements (splitters, mergers and JTLs) buffer SFQ pulses, so that several data pulses can exist within one stage at a time. The circuit should work at clock periods slightly larger than factors of data propagation delay down to the minimal period determined by the sum of latches hold and setup times.

The differences between the delays in different stages limit valid *counterflow* clock frequencies in this experiment: circuit only works at clock periods which are the factors of *all* stage delays. This is hard to achieve if the delays differ substantially but not by an integer number of clock periods. Our original CLA design [3] used *co-flow* clocking which does not suffer from this problem, but requires adding matching delays in clock lines for each stage.

[2] An alternative view of our 10-stage inverter chain is that it is a chain of 5 master-slave D-flip-flops. This makes it easier to see why our chain works as a shift register.

### B. *Experimental verification*

We have layed out three different experiments of this type fabricated in HYPRES using their $3.5\mu m$ technology [4]. One has the exact structure shown in Fig. 1, another has several extra splitters in all clock paths (to simulate clock distribution trees), and in the third, splitters and mergers in the internal stages are replaced by JTL segments. We have used a library-based approach to circuit layout. All our elementary cells were carefully optimized for interconnectivity, they have layouts with all I/O junctions on cell's corners easily accessible from two directions and connected with inductive stretches semi-automatically since the value of interconnecting inductance is not particularly important.

Though the fabrication run was not considered successful, the low-frequency parts of all three chips worked from the first attempt with large power supply voltage margins and verified our library cells' correctness and our approach to connecting them together. The inverter chain power supply margins on one chip were $1.7 \ldots 2.9$mV ($\pm 26\%$) while the designed value of power supply voltage was 2.6mV. It is interesting to note that the middle operating point (2.3mV) is $\approx 13\%$ off the designed value which is in good agreement with the data about that particular wafer reported by HYPRES: the wafer had 2% lower critical current density and 16% lower sheet resistance.

The high-frequency experiments were performed only for the least complex chip (unfortunately, the voltage pick-up resistors on the other two were accidently burnt out).

To verify the high-frequency behavior of our circuit we applied a relatively low frequency clock (ca. 7 GHz). We injected the data pulses and verified that $V_{out}$ voltage jumps for each new data bit. Our input data pulses (coming from slow room-temperature electronics) were not synchronized with clock pulses and sometimes we could not insert a data pulse in the loop because it arrived in the wrong position relative to the clock on the first inverter. This was a limitation of our simple experiment.

When we switched the return path voltage off to clear the register, the output voltage went back to zero and stayed zero until we injected the next data bit.

Then we increased clock frequency (while verifying the correctness of circuit behavior) and found out that the circuit works up to 10 GHz. Measurements of the $V_{out}$ voltage (0.0024 mV) gave us the latency of the circuit of 860 ps. Translated from present-day HYPRES technology to the HTMT target $0.8\mu m$ technology, it becomes approximately 290 ps which is in good agreement with 276 ps predicted in [3].

We also found a higher frequency for which our circuit works which is slightly less than 17 GHz and corresponds to one pulse in flight between two stages while the oth-

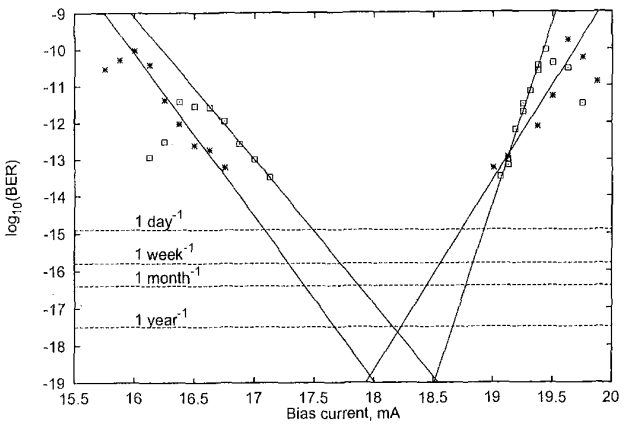


Fig. 2. BER in a 64-bit integer adder critical path versus power supply bias current. Stars correspond to 9.2 ... 9.6 GHz clock, boxes correspond to 16.5 ... 16.8 GHz clock.

ers are read-out from the latches. The data bit propagated with the same speed in this case and measured $V_{out}$ was the same, but the inverters clicked at higher frequency producing and removing data pulses internally. We have also tried the 25 GHz clock frequency when the circuit showed some correct behavior but the operating margins for this frequency were too narrow, and it was much harder to inject pulses in the circuit (since the clock frequency is so high the probability of data pulse collision with the clock is also higher).

The highest operating frequency for which our circuit works reliably is 17 GHz, when translated to $0.8\mu m$ technology, it becomes 51 GHz which is in good agreement with 52 GHz predicted in [3], assuming 3% JJ spread.

### C. BER measurements

The BER measurements were performed for approximately 9.5 GHz and 16.5 GHz clock frequency (the frequency drifted during long measurement runs). We injected an SFQ pulse in the loop and waited for an error which was signified by a decrease (pulse lost) or increase (extra pulse appeared) of $V_{out}$ voltage.

Our equipment did not allow to reliably measure voltage in the $\mu V$ range for long periods of time. Therefore, if an error did not occur in any given 10 seconds, we would stop the experiment, recalibrate the voltmeter and inject the pulse again. We were measuring for 180 10-seconds intervals to be able to detect at least one error in 1/2 hour.

The mean time between failures (MTBF) was calculated as the sum of measurement times (each up to 10 seconds) divided by the number of detected errors (pulse survived in the loop for less than 10 seconds). The BER was calculated by dividing MTBF by the clock period.

The BER of our circuit in the optimal operating point is too low to be detected. Thus, we estimated it by measuring BER on the edges of the operating region, as in

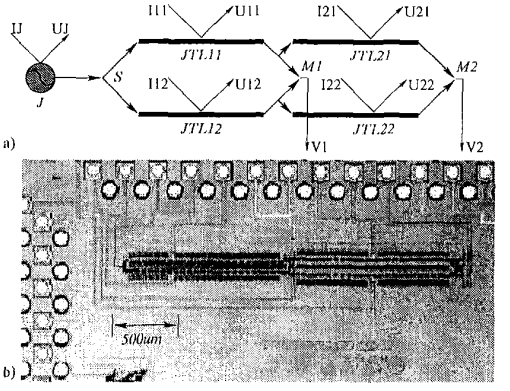


Fig. 3. Test circuit for measuring SFQ pulse jitter: a) schematics and b) microphotograph (courtesy of TRW).

[5]. The results of these measurements are presented in Fig. 1. We have interpolated the boundaries of the operating region with an exponent (straight line in semi-log plot), and the intersection of these lines gave us the estimated BER of $10^{-19}$ in the optimal operating point. We did not have enough data points to apply more correct $e^{-x^2}$ fitting function, which would probably give us better results. The measured BER decrease on the outer side of the high-frequency operating region (but still within the low frequency operating region) apparently due to the switch to another timing mode where overbiased or underbiased circuits satisfy the delay's balance requirement. These regions were not studied in detail.

## III. Measurement of Timing Jitter

The experiment described above does not allow us to measure timing jitter explicitly. Instead, we measure BER which is a complex function of jitter and other parameters.

To estimate timing jitter, we prepared yet another test circuit shown in Fig. 3. The circuit was fabricated in TRW using their $1.5\mu m$ JJ110D technology [1]. The experiment is based on a unique property of an RSFQ merger [6]: if two input SFQ pulses arrive within time $t \leq t_t$ after each other, then only one pulse appears at the output; otherwise, two output pulses are produced. When $t \approx t_t$, the output of the gate is uncertain.

The test circuit consists of pulse source J (an overdamped Josephson junction overbiased by external dc current $I_J$), SFQ pulse splitter S, two long segments of Josephson transmission lines $JTL_{11}$ and $JTL_{12}$ ($m = 114$ JJs in each branch), two more auxiliary splitters, merger $M_1$, two more JTLs ($m = 114$ junctions in each), and one more buffer $M_2$. Each JTL branch has an independent power supply $I_{xy}$, so that it is possible to vary SFQ pulse propagation speed in a relatively wide range. Two copies of an SFQ pulse originate at splitter S at the same time. (Similar circuit was used in [7] for BER measurements.) If SFQ pulses were reproduced in the JTLs

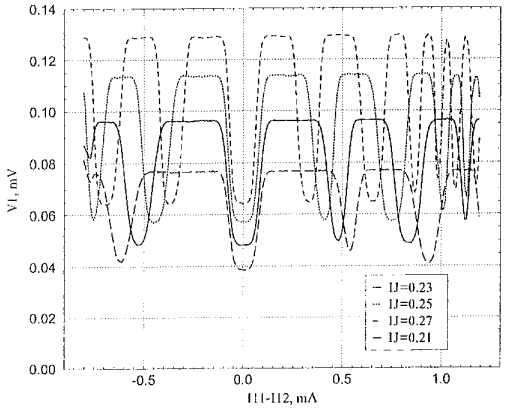


Fig. 4. Experimental behavior of the test circuit.

without any jitter, then the dc voltage $V_1$ at the output of $M_1$ would only depend on the relative delay of the pulses in the two branches of the test circuit: $V_1 = V_J$ if $\delta\tau_1 \equiv |\tau_{11} - \tau_{12}| < t_t$, and $V_1 = 2V_J$ if $\delta\tau_1 > t_t$. More precisely, as we have a continuous train of pulses at frequency $f_J = 2\pi U_J/\Phi_0$ rather than a single pulse,

$$V_1 = V_J \quad \text{if} \quad ||\tau_{11} - \tau_{12}| - n/f_J| < t_t, n \in N. \quad (1)$$

However, because of the timing jitter, the relative delay of the two SFQ pulses becomes uncertain, and the rectangular shape of the function $V_1 = f(V_J, \delta\tau_1)$ is distorted. Experimentally measured dependences of $V_1$ on $\delta I_1 \equiv I_{11} - I_{12}$ for different pulse train frequencies (different values of $I_J$) are shown in Fig. 4.

The accumulated timing jitter in two competing branches of the test circuit $\sqrt{\langle \delta t^2 \rangle}$ can be estimated as the width of the sloppy part of the experimental curve (divided by $\sqrt{2\pi}$ it gives the spread $\sqrt{\sigma^2}$):

$$\sqrt{\langle \delta t^2 \rangle} = f\left(\partial\left[\delta I_1\right]/\partial V_1|_{\max} \cdot \left[V_{1,\max} - V_{1,\min}\right]\right). \quad (2)$$

It is possible to establish the relationship between timing jitter values measured in current and in time units: minimums of $V_1$ in Fig. 4 appear when condition (1) is satisfied, so the distance between two neighboring minimums measured in current units, corresponds to $1/f_J$.

We assume that timing jitter in each junction $\sqrt{\langle \delta t_0^2 \rangle}$ is independent of jitter in any other junction [3]. Therefore, in a chain of $2m$ JJs, $\sqrt{\sigma^2} = \sqrt{\langle \delta t^2 \rangle}/\left(2\sqrt{\pi m}\right)$.

We have tested both short chains ($m = 114$, output voltage measured at $M_1$, data in Fig. 4) and long chains ($m = 214$, output voltage measured at $M_2$). Extracted timing jitter per JJ is $\sqrt{\sigma^2_{\text{exp}}} \approx (0.20 \pm 0.04)$ ps (namely, $(0.22 \pm 0.01)$ps for short chains, and $(0.17 \pm 0.02)$ ps for long chains). Simulation carried out in [3] gives slightly lower value: $\sqrt{\sigma^2_{\text{sim}}} \approx 0.08$ ps. The most apparent reason for this disparity is external RF noise penetrating into the testing setup.

## IV. Conclusion

We have experimentally verified the critical path of a 64-bit integer CLA adder and timing jitter in a clock distribution tree branch. To our knowledge, these are the first experiments which measured BER and timing jitter in relatively complex RSFQ circuits. The circuits were assembled from our library cells optimized for interconnectivity, and worked with high dc power supply margins.

The critical path total latency of 860 ps and maximal operating frequency of 17 GHz are in good agreement with our theoretical estimates. Its BER in the optimal operating point is $10^{-19}$ (compared to $10^{-25}$ required for the HTMT petaflop computer). Large global variation of power supply and shunt resistors on that particular wafer and local variations of critical currents as well as inappropriate choice of counterflow clock and problems with finding an optimal clock frequency in this case contribute to this higher BER.

The timing jitter of 200 fs per JJ in a long clock distribution circuit is on the same order of magnitude as theoretically predicted value of 80 fs, though also higher.

In both cases, excessive RF noise penetrating into the insufficiently shielded testing setup may be to blame. We hope that after eliminating the apparent problems we can achieve the required $10^{-25}$ BER and reduce timing jitter.

## Acknowledgment

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