High Performance Analog-to-Digital Converter Technology for Military Avionics Applications

Edgar J. Martinez, Ronald L. Bobb

Aerospace Components Division, Air Force Research Laboratory
AFRL/SNDM 2241 Avionics Circle, WPAFB OH 45433-7321
Tel (937) 255-1874 x3453; e-mail martinej@aa.wpafb.af.mil

Abstract- The signal processing requirements of military avionics systems are constantly increasing to meet the threats of the next century. This is especially true as the digital interface moves closer to the sensor/antenna and the Analog-to-Digital Converter (ADC) performance requirements become a major contributor to spaceborne data and signal/sensor processors and mission management specifications. The benefits of moving the digital interface closer to the sensor/antenna in avionics systems can be classified in four different categories: affordability, reliability and maintainability, physical, and performance. This reduction in RF downconversion stages as the digital interface migrates toward the sensor can result in some difficult ADC requirements that can not currently be met by commercial technologies.

It is the intention of this presentation to expose the aerospace community to these emerging requirements for radar, communication and navigation (CNI), and electronic warfare missions. In addition to these requirements, we are presenting some examples of current state-of-the-art ADCs, their technology limitations, and briefly discuss potential applications in avionics systems. We have also included in this presentation a brief discussion on the fundamental and physical limitations that impair the progress of current and future ADC technologies. This presentation will conclude with a technology forecast, and an estimate on ADC availability for future avionics systems.

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1. Introduction

Analog-to-Digital (A/D) and Digital-to-Analog (D/A) conversions lie at the heart of most modern signal processing systems for military applications in which digital circuitry performs the bulk of the complex signal and data manipulation. These complex circuits are designed to link the domain of discrete numbers to the world of physical quantities, which are known to have finite precision and limited observability. As Complementary Metal-Oxide Semiconductor (CMOS) integrated circuits (ICs) become increasingly sophisticated and inexpensive, more processing functions are performed in the digital domain. Therefore, fewer operations benefit from analog circuitry in which performance tends to drift with time and temperature causing the digital interface to migrate toward the sensor/antenna.

This migration toward the sensor/antenna in military avionics systems has some important ramifications for the role of analog circuitry: As shown in figure 1, only radio frequency (RF) down-conversion circuitry (e.g., anti-aliasing filters) will remain as important niche where analog implementations exhibit clear advantage over the digital approaches. However, the reduction in RF downconversion stages as the digital interface migrates toward the sensor can result in some difficult ADC requirements that can not currently be met by commercial technologies. Second, A/D and D/A converters will continue to play a critical role in advanced electronic
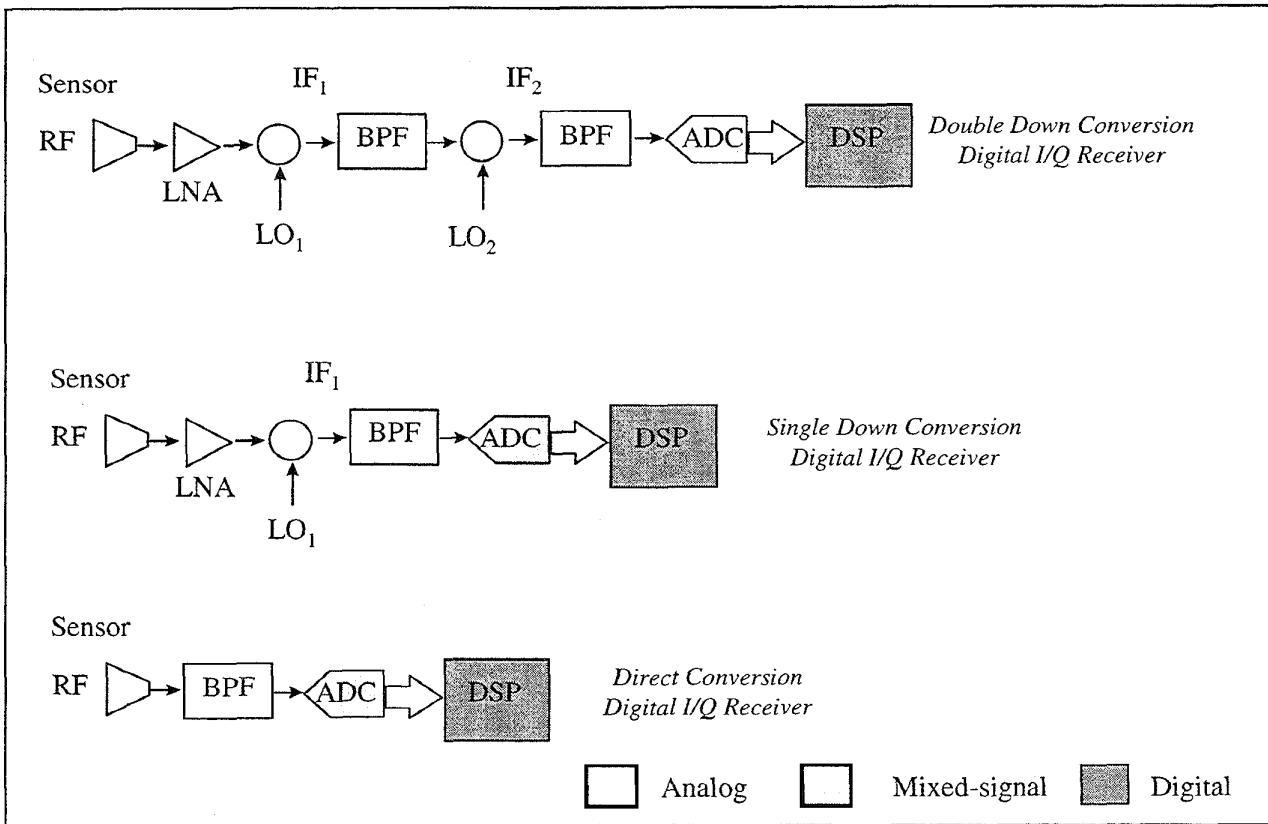
Figure 1. Migration of the digital interface toward the sensor/antenna in military receiver systems.

Table 1: Benefits of Moving the Digital Interface Closer
to the Sensor/Antenna.

CATEGORY	BENEFITS
Affordability	Reduction in Acquisition and Life-cycle Costs
Reliability	Less Component Count Higher Maintanability
Physical	Reduction in Weight, Volume, Power and Cooling Requirements
Performance	Improvement in Spectral Purity, Waveform Flexibility, and Channel Multiplicity

systems operating in the Radio Frequency (RF) and Intermediate Frequency (IF) regimes limiting the overall system performance. Third and finally, the benefits of moving the digital interface closer to the sensor/antenna in avionics systems are classified in four different categories as shown in table 1. It is the intention of this presentation to expose the aerospace community to the emerging requirements for radar, communication/navigation, and electronic warfare missions, and its implications to device technology and ADC architecture. Then, examples of ADC architectures in use today are discussed, followed by some relevant examples of the state-of-the-art in ADC technology and its application to avionics systems. Section 4 is dedicated to describing fundamental and physical limitations to the performance of conversion systems. Finally, we will conclude by presenting future military avionics requirements and forecasting the performance of emerging ADC demonstrations.

2. Analog-to-Digital Converter Architectures

Over more than four decades, many A/D and D/A conversion schemes have been investigated resulting in a great variety of converters with different accuracy and resolution and in many cases closely matched to particular applications. Demonstrations range from discrete components, (monolithic integration of semiconductor or superconductor device technologies), to hybrid combinations in which components are integrated in Multi-Chip Assemblies (MCMs). For commercial applications, the driver has always been healthy competition between performance and cost down, while for military applications performance is always the driver for the demonstration of new components.

According to Gordon [1], an ideal ADC is defined as a device that accepts at its input terminal a voltage potential and which yields at its output a set of electronic signals representing a numerical code whose magnitude is in proportion to an internal and /or external reference signal, and the input voltage potential. Ideally, the input components are isolated with respect to the output signal, the transition from one output state to another will occur with an infinitesimal change in the input signal, and with the change in output state occurring instantaneously upon command. Finally, the transfer characteristics of an ideal ADC would be invariant to changes in time, temperature, and power supply noise. As the reader must realize, in real life none of these conditions prevail. ADCs are very sensitive to noise, and tend to drift with time and temperature. In addition, the time that it takes to convert an analog signal to its equivalent digital code (latency) is directly dependent on the chosen architecture.

Almost every ADC can be classified under two categories: conventional (Nyquist-like) or oversampling. The conventional converter is often more difficult to implement in a monolithic fashion than its oversampling counterpart due to its complexity and the number of analog components, filters, and conversion circuits which can be very sensitive to noise and interference. Oversampling converters, on another hand, have become popular in recent years because they tend to avoid many of the difficulties encountered with conventional methods for A/D and D/A conversion, especially for those applications that call for high resolution of relatively-low frequency signals. It is not our intention to include an exhaustive description of ADC techniques in this section. However, we felt that reviewing some of the most relevant ADC architectures would help the reader to better understand the limitation and challenges inherent to this technology. For a detailed treatment of ADC architectures, the reader is referred to the texts by Razavi [2], Tsui [3], Soclof [4], Norsworthy *et.al.* [5] and the review paper by Gordon [1].

Conventional versus Oversampling Architectures

Most military sensors feature a variety of converters that link the RF domain to the digital signal processors. The majority of these sensors, are of the conventional type. With the migration of the digital interface toward the front end sensor new converter architectures featuring higher sampling rates, smaller size, and lower power are finding their way into military systems.

Under conventional military converters, two categories are worth mentioning: single and multi-stage. Traditionally, high-speed converters have relied upon the parallel or flash architecture (single stage), where the analog signal is simultaneously compared to threshold voltages by a bank of comparator circuits [6, 7]. In this architecture, the threshold levels are usually generated by resistively dividing one or more references into a series of equally-space voltages that are applied to one input of each comparator. In flash ADCs, one comparator is required for each threshold of the converter. Therefore, the total number of comparators required is 2^N-1, where N is the resolution of the ADC. Although the flash topology is very attractive to very high-speed applications, its dynamic range is limited by the device technology. Typical complexity values range around 8-bits for CMOS[1] implementations, and 4 bits for bipolar technologies (e.g., JBTs, HBTs).

In order to improve resolution without paying complexity penalties, A/D and D/A architectures with multiple stages such as subranging, pipelined, and folding have been implemented for high performance applications [8, 9, 10, 11]. Examples of some military-unique converters with multiple stages will be presented in the next section.

The oversampling-type converter has been widely used for many commercial applications such as portable communications and Compact Disk (CD) players. In recent years, advances in device technologies have provided the opportunity to demonstrate the potential of this type of converter topology for military systems. For some applications such as, military communications and radar, in which high dynamic range over a narrow bandwidth is required, oversampling, or delta-sigma ($\Delta-\Sigma$) conversion techniques may provide a unique solution not currently achievable with Nyquist-like converters [3, 5, 12, 13].

As shown in figure 2, oversampling converters can use simple and relatively high-tolerance analog components to achieve high resolution. However, fast and complex

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[1] Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS) technology currently dominates 90% of the market of semiconductor integrated circuits due to its ability to integrate a large number of low power devices at a very low cost.

digital filters[2] are required at the Δ–Σ output loop. In Δ–Σ converters, the analog signal is converted to a simple code, usually single bit words, at a frequency much higher than the Nyquist rate. Therefore, resolution in time can be traded for resolution in amplitude in such a way that variation in analog components can be tolerated. In the Δ–Σ modulator, the input signal is fed to the quantizer via an integrator, and the quantized output feeds back to substract from the input signal. This feedback forces the average value of the quantized signal to track the average input. Any persistent difference between them accumulates in the integrator and eventually corrects itself. Because the number of bits at the output of the modulator circuit is small (usually a single binary bit), the accuracy requirements on the Δ–Σ ADCs are considerably reduced and traded-off for circuit speed. Furthermore, the high degree of oversampling speed of the input signal eliminates the need for complicated analog filters at the front-end of the ADC.
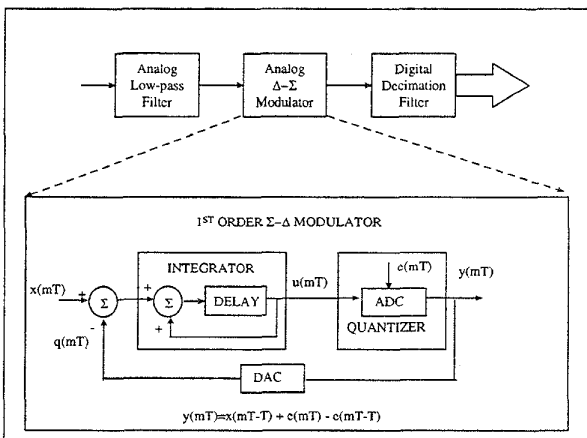

Figure 2. Oversampling A/D Conversion Architecture.

The A/D conversion process is not complete without the output signal to the modulator being digitally converted to the desired sampling rate and resolution through the smoothing and resampling process called decimation, which is usually implemented in a low-power technology. In many military applications where the sampling rate has to be high enough to achieve a wide bandwidth and resolution, the decimation or filtering process needs to be preceded by a demultiplexing stage in order to downconvert the data rate of the Δ–Σ modulator. A more detailed analysis of Δ–Σ conversion techniques is presented in the reference by Norsworthy [5].

As a final note, multibit Δ–Σ ADC approaches offer an alternate solution between the 1-bit Δ–Σ and classical Nyquist ADC-architectures [5]. While continuous-time multibit Δ–Σ ADCs offer most of the same advantages

cited above for 1-bit Δ–Σs, at lower clock frequencies, they do require a highly linear feedback DAC for their implementation. Even though direct fabrication of DACs having the required absolute linearity is difficult to realize in monolithic IC processes, the oversampling involved in a Δ–Σ modulator affords the use of certain "tricks" to improve the effective DAC linearity. Some of these "tricks" are described by Norsworthy, et.al., [5] and need not to be repeated here. For a given F_t IC technology[3], the multibit Δ–Σ ADC architectures offer a potential for signal bandwidth improvement. However, its demonstration in military avionics is still to be seen.

A unique disadvantage of the oversampling architecture is related to bandpass sampling at IF or RF rates. In a Nyquist-like ADC, bandpass sampling is easily accomplished at any IF frequency, provided that the quality of the input sample/hold is adequate, and by simply selecting the ADC clock frequency. While continuous-time Δ–Σ ADCs (either 1-bit or multibit) can also be designed for bandpass sampling applications, the loop filter function in the Δ–Σ modulator must be accomplished by resonator circuits instead of the integrators used in baseband architectures. This means that for each IF or RF frequency in which bandpass sampling is to take place, a unique resonator design for the loop filter function is required. Therefore, the ADC becomes unique to a certain frequency allocation and more likely to the platform that it was designed for.

Now that we have briefly discussed some of the most common ADC architectures used in military systems, it is appropriate to present the reader with some of the state-of-the-art in ADC technology.

3. The State-of-The-Art in High Performance ADCs

As we mentioned before, military requirements for resolution and bandwidth of ADCs substantially exceed the capabilities of currently available commercial devices. The performance limitations of current ADC technology are often illustrated with a chart plotting the resolution of converter parts (prototypes or commercial-of-the-shelf products) versus their sample rate (F_S) [14]. In the case of the oversampling (delta-sigma) converters, the equivalent Nyquist sampling rate derived from the bandwidth is used. From this chart, it has been concluded that an improvement of 1-bit every six years for a given sampling

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[2] In certain cases, a power-penalty is paid at the dig ital filter making this converter architecture impractical for many military platforms. .

[3] The F_t and F_{max} of the device technology will provide the designer with an idea on how fast the input signal can be sampled. As an underwritten rule, the device F_t has to be at least 20 times higher than the oversampling ratio (sampling speed divided by two times the signal bandwidth). This translates into device technologies with F_ts well over 200 GHz in order to achieve bandwidths of at least 60 MHz.

frequency is achieved. Therefore, it takes significant amount of resources in order to accelerate the development of both military and commercial components.
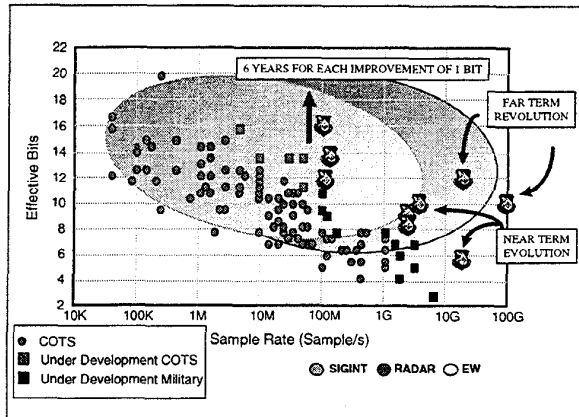

Figure 3. Sampling rate vs. Resolution for Commercial and Military Analog-to-Digital Converters. Figure is Courtesy of Dr. Robert Walden, Hughes Research Laboratories [14].

Flash Analog-to-Digital Converters

As we mentioned in the previous section, flash converters normally utilize a significant number of comparators (2^N-1) where N is the number of output bits. Therefore, circuit complexity increases exponentially with the number of bits while the reference voltages decrease. The consequences are: very large monolithic integrated circuits, high power dissipation, difficulty matching components, and reduction in analog input bandwidth due to large input capacitance. As a result, most flash converters available today feature less than 8-bits of resolution.

We have selected three examples of high-performance flash A/D converters with very wide bandwidth to illustrate the recent trend and advances in device and circuit technologies unique to military applications.

In 1993, Tran *et.al.*, presented for the first time a 4-bit, 2.4 giga samples per second (Gsps) Flash ADC fabricated using InP-based Heterojuction Bipolar Transistor (HBT) technology [6]. For this demonstration, InP-based HBTs were selected over other device technologies due to their high electron mobility in the base region, high saturation drift velocity, high substrate thermal conductivity (0.68 W/cm-°C), and low surface recombination velocity. All these device characteristics make InP HBT technology attractive for high performance ADCs. Reported device parameters include current gain of $25 \leq \beta \leq 30$ at collector current densities of ($J_c = 10$ kA/cm^2 for 1.5 μm emitters), and base-emitter voltage (V_{be}) matching better

than 2 mV in matching pairs 15 μm^2 apart. Reported high-speed measurements included typical current gain cuttoff frequency values ($F_t = 60$ GHz) and maximum frequency of oscillation ($F_{max} = 100$ GHz).

TRW's monolithic 4-bit flash ADC consisted of 15 master-slave current mode logic comparators with differential preamplifiers, encoding logic for a 4-bit binary output, and a fully segmented on-chip DAC. Signal-to-Noise Ratio (SNR) performance of 25 dB was obtained to sample frequencies up to 2.5 GHz and it was reported to be 700 MHz higher than similar flash ADCs fabricated in GaAs HBT technology. It is appropriate to mention that this flash converter was selected to demonstrate the capability of TRW's InP HBT technology at the time. This converter is an important building block circuit for multistage A/D conversion topologies.

In 1996, Baringer *et. al.*, reported the performance of another milestone in A/D conversion technology, a 3- and 4-bit, 8 Gsps flash ADCs [7]. In this report, Nyquist operation up to 8 Gsps was achieved with a potential for quantization between $f_s/2$ up to f_s at a sampling rate of 5 Gsps. These flash converters were also demonstrated using InP-based HBT technology. The reported fabrication process featured the following performance specifications: $\beta = 36$, $F_t = 75$ GHz and $F_{max} = 85$ GHz.

A microphotograph of Hughes' 4-bit flash ADC is shown in figure 4. This particular flash converter was implemented in a fully differential architecture for common mode noise rejection. This circuit contained approximately 1,580 transistors and had a die area of 3.75 x 3.15 mm^2. A fully differential architecture was also used for the implementation of the 3-bit quantizer. For the 3-bit demonstrations, 900 transistors were implemented occupying a die area of 2.2 x 2.7 mm^2.

Nyquist operation was demonstrated in the 3-bit quantizer at sample rates of 8 GHz with a SNR found to be 16.1 dB (approximately 2.4 effective number of bits, ENOB). To demonstrate the ability to convert signals at $f_s/2$ to f_s, the quantizer was tested with an input signal at 4.973 GHz with similar results. Higher SNR values were achieved with these converters when the input signal frequency is significantly low compared to the sampling frequency. Just as the previous demonstration, these converters constitute an important milestone toward achieving direct X-band sampling.
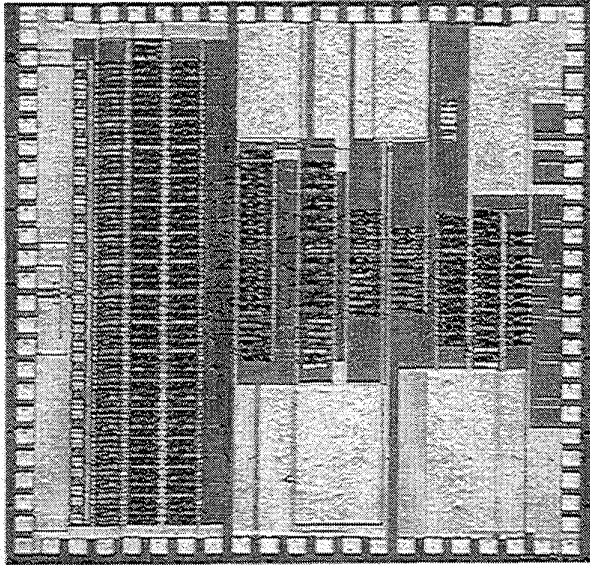
Figure 4. Microphotograph of an InP 4-bit, 8 Gsps Flash ADC Courtesy of Hughes Research Laboratories.

Multi-Stage Converters

In order to improve performance in traditional military systems, pipelined feedforward A/D converters with broad bandwidth have been developed and demonstrated for radar and EW applications [8, 15].

In 1995, Nary *et.al.*, reported the performance demonstration of an 8-bit, 3 Gsps ADC fabricated in an AlGaAs/GaAs HBT process [8]. This particular demonstration utilized a folding and interpolation architecture to provide wide bandwidth with a moderate device count. At 2 Gsps, this particular ADC demonstrated an effective resolution between 6.5 and 7.0 effective number of bits (ENOBs) for analog inputs between DC and 1.5 GHz and single tone spurious free dynamic range (SFDR) of 48 dB at Nyquist.

For the demonstration of this particular converter, Rockwell used their standard GaAs HBT process. This commercial process featured a minimum transistor geometry[4] of 1.4 x 3.0 μm^2. Typical device F_t and F_{max} values of about 55 GHz were used for this design. Figure 5 shows the 8-bit, 3 Gsps ADC described by Nary *et al.*, in reference [8] and table 2 summarizes the design goals for this particular converter.

In 1997, a 10-bit, 1 Gsps ADC was also demonstrated by Rockwell International, and implemented as a two stage

pipelined feedforward converter with a 6-bit coarse quantizer and a 5-bit fine quantizer. Figure 6 shows the topology selected for the demonstration of this particular converter [15, 16]. This particular architecture was selected to minimize the component count while maximizing throughput to attain the 1 Gsps operation. The redundant bit of resolution generated with this topology (6-bits + 5-bits = 11-bits) is used to correct for non-linearities in the coarse quantizer and offsets in the interstage circuitry.
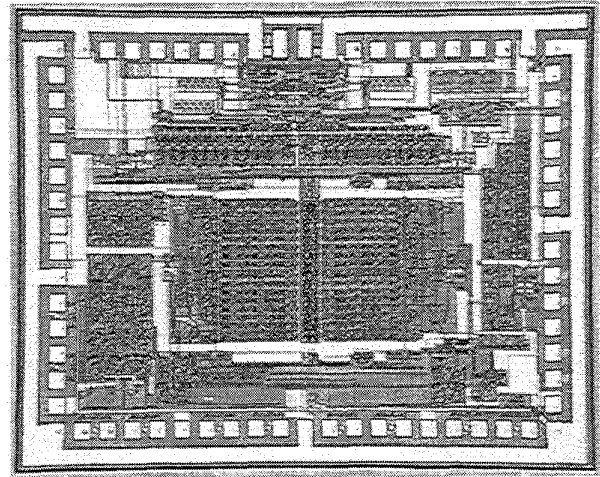

Figure 5. Microphotograph of a GaAs Pipelined Feedforward, 8-bit 3 Gsps A/D Converter. Photograph courtesy of Rockwell Science Center.

Table 2. Relevant Design Goals for Rockwell's 8-bit, 2 Gsps ADC.

Max. Sample Rate	3 Gsps (50% duty cycle clock)
Input Bandwidth	3.0 GHz (flat to ½ LSB)
Full scale Input	640mV$_{pp}$ differential
Input Impedance	50 Ω
Output Levels	CML (0.0 V and -400 mV)
Power Supplies	5.0 V, -5.2 V and ground
Power Dissipation	5.3 Watts
Transistor Count	2511
Die Size	2.8 mm x 3.5 mm

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[4] The minimum transistor geometry reported in reference [8] refers to the current process at the time of publication. Since then, the HBT fabrication process at Rockwell has been refined to accommodate smaller devices with higher performances.
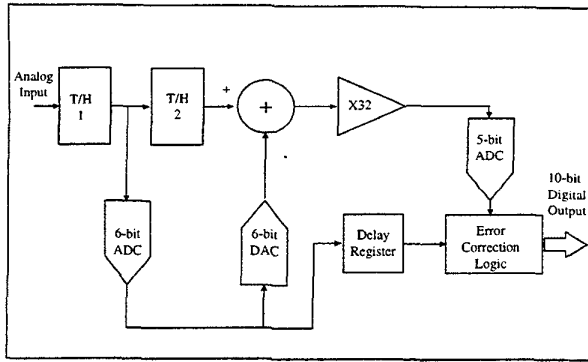
Figure 6. Block Diagram of the Monolithic, Pipelined Feedforward, 10-bit, 1 Gsps ADC Developed by Rockwell International.

Because the front-end T/H would likely limit the dynamic performance of the ADC, significant resources were dedicated to optimize this particular sub-circuit in order to achieve linearity commensurate with 10-bit performance at 1 GHz. Performance data of this converter was not available at the time that this document was generated. These last two converters are currently being used for the demonstration of advanced radar and electronic warfare (EW) receiver concepts for several military applications.

In 1994, the Millennium Advanced Digital Telecommunication program was funded by the Technology Reinvestment Program (TRP) to develop high speed enabling components targeting broadband digital applications, including advanced military digital receivers and commercial satellite digital demodulators. TRW as part of the TRP Millennium Consortium developed and demonstrated two important components critical to broadband EW receivers and military communication systems [9, 11]. The first converter to be described is an 8-bit, 3 Gsps IF sampling ADC fabricated in TRW's Advanced HBT technology. This converter provided 8-bits of resolution up to 3 GHz with a corresponding signal-to-noise ratio (SNR) of -41 dB and with a spur-free dynamic range (SFDR) better than 55 dB in the IF band from 1.55 to 2.95 GHz. As shown in figure 7, this converter has been implemented using two levels of analog sample-and-hold (S/H) circuits followed by two, 8-bit folding-amplifier, interpolate resistor (FAIR) quantizers connected in an interleaved (or "ping-pong") fashion.
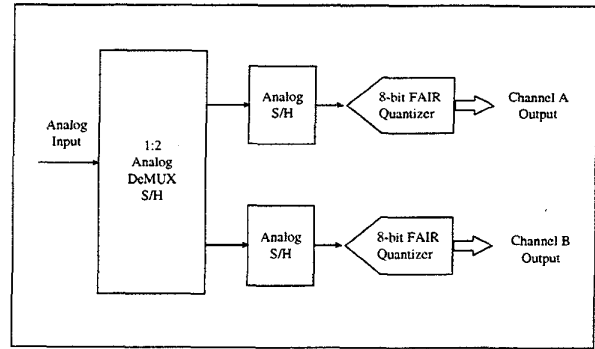

Figure 7, Block Diagram of the Interleaved FAIR Architecture Used for the Demonstration of TRW's 8-bit, 3 Gsps ADC.

To achieve the required performance, the interleaved demultiplexer (DeMUX) sample-and-hold (S/H) circuit samples the analog signal at 3 GHz with a resolution equivalent to 8-bits. This circuit was realized using a single rank of dual master sample and hold front-ends alternately acquiring the input signal in a "ping-pong" arrangement at a clock rate of 1.5 GHz. In this architecture, the two 8-bit FAIR quantizers that convert the analog signal at a rate of 1.5 Gsps, are driven by the analog S/H post amplifiers. Channel synchronization (interleaving) is required to obtain the overall sampling rate of 3.0 Gsps. Table 3 summarizes some of the circuit specifications as reported in [9].

Table 3: Design Specifications for TRW's Interleaved, FAIR 8-bit, 3 Gsps ADC.

1:2 Analog DeMUX S/H Circuit	
Resolution	Equivalent to 8-bits
Sampling Rate	3 Gsps
Analog Input Range	$\pm$ 225 mV
Power Dissipation	5.1 Watts
Dimensions	3.5 x 5.2 mm^2
8-bit FAIR Quantizer	
Resolution	8-bits
Sampling Rate	1.5 Gsps
Analog Input Range	$\pm$ 256 mV
Power Dissipation	6.9 Watts
Dimensions	3.5 x 6.6 mm^2

For this demonstration, all circuits were fabricated using TRW's advanced 1.0 micron, GaAs HBT process. This process features all Npn transistors with a unique combination of very high F_{max} > 60 GHz and high precision V_{be} matching. This circuit is currently being used for the demonstration of advanced ESM digital receivers.
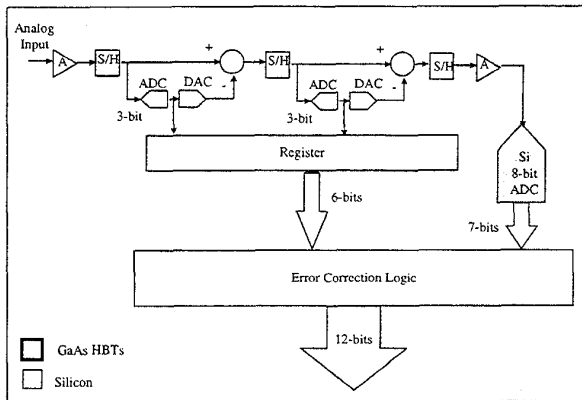
Figure 8. Block Diagram for TRW's 12-bit, 125 Msps Subranging ADC. Diagram Courtesy of TRW.

For narrow-band, high-resolution applications, a 12-bit, 125 Msps ADC represents the state-of-the-art in converter technology. This converter was also developed under the Millennium TRP program for both, military and commercial applications [11]. The performance goals included > 60 dB SNR (> 10.5 ENOB) and 80 dB SFDR for input frequencies up to 150 MHz. As shown in figure 8, this particular converter was implemented with a feedforward subranging (3-3-7) architecture with digital error correction. The coarse quantization or subranger (3+3 bits) was also implemented in TRW's advanced HBT process while the 7-bit fine quantizer was implemented using silicon bipolar technology. The output data from the coarse and fine quantizer are combined and corrected with a GaAs error correction, application-specific integrated circuit (ASIC). The subranger was reported to contain 2,556 transistors and measured 6.95 x 4.2 mm^2 while the error correction ASIC measured 6.95 x 3.8 mm and contained 2,646 transistors. The total power dissipation in the 12-bit, 125 mega-samples per second (Msps) converter has been reported to be approximately 16 watts. This particular converter has many potential applications especially for radar and CNI systems.

State-of-the-Art in A–Σ Converters

Even though oversampling converters are becoming very popular for many military applications, only two demonstrations were selected to represent the state-of-the-art in A–Σ conversion technology.

In recent years, several A–Σ modulators fabricated in InP-based Heterojuction Bipolar Transistors have been reported in the literature [12, 13, 17, 18]. This technology has been selected as the method of choice for many high-resolution A/D conversion schemes. Because integration levels in InP-based HBT technology is still limited to less than several thousand transistors per die, A–Σ implementations have been done in two stages: modulation and filtering.

In 1994, Jensen *et.al.*, reported an InP-based baseband A–Σ modulator with 62.5 MHz input bandwidth [17]. At a sample rate of 4 GHz (oversampling ratio of 32), the first order modulator demonstrated a signal-to-noise (SNR) of 40.3 dB. The reported modulator consisted of a summer, an integrator, and a low-resolution (1-bit) quantizer in the forward path of a feedback circuit and a DAC in the return path (also 1-bit). Figure 9 shows the block diagram of the modulator reported in reference [17]. The reported approach included the implementation of a transconductance cell that converts a differential voltage to a differential current signal, and one-bit DACs as a single current steered differential pair.

For the demonstration of this A–Σ modulator, a double heterojunction bipolar transistor (DHBT) fabrication process was used. Jensen's DHBT process has demonstrated devices with the following characteristics: current-gain (β=55), early voltage (V_a=100 V), collector-to-emitter breakdown voltage (BV_{ceo} = 9 V), F_t=70 GHz, and F_{max} = 60 GHz.

The latest report in A–Σ ADC technology was presented by Jayaraman *et.al.*, at the 1997 GaAs IC Symposium [18]. A fourth order banspass A–Σ modulator with center frequency at 800 MHz was reported. This particular modulator was designed and fabricated in AlGaAs/GaAs HBT technology. This particular modulator was reported to be able to clock at a continuum of frequencies from 2 to 4 GHz achieving a 66 dB (11 ENOBs) and 41 dB (8 ENOBs) SNR over a 100 KHz and 25 MHz bandwidth, respectively. It was implemented using an interpolative loop for better stability at higher IF frequencies (800 MHz). In this topology, two resonators provide the required 4th order loop function resulting in a noise shaping comparable to a 2nd order baseband A–Σ modulator.
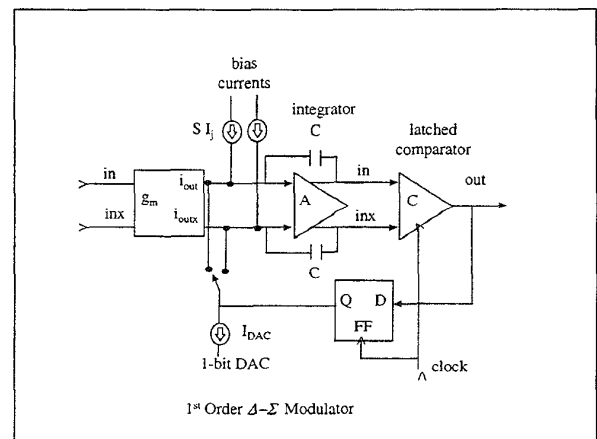

Figure 9. Block Diagram of 1st Order A–Σ Modulator.

The circuit was fabricated in Rockwell AlGaAs/GaAs HBT process with typical F_t and F_{max} values of 40 GHz. The total power dissipation was reported to be approximately 1.8 W with 45 % of it used at the output buffer and clock generation circuits. This monolithic circuit occupies a die area of 1.45 x 1.6 mm^2. No information on device count was provided in this reference.

All these Δ–Σ ADCs show potential for both radar and communication applications.

Now that we have presented the state-of-the-art in ADC technology it is time to list the most relevant military requirements and match them to current technologies.

4. Military Avionics Requirements

Communications Navigation and Identification (CNI)

As digital technology continues to mature and performance improves, an all-digital CNI receiver is envisioned for the next generation of avionics systems [19]. This future receiver should cover the VHF, UHF, and L-band functions concurrently. Table 4 lists specific CNI functions that must be addressed by the next generation of communication receivers:

Table 4 . List of Functions to be Address by Future Communication Receiver Systems.

Radio	UHF,VHF
Data Links:	Link-16, Link-4A, IFDL, IDM, WDL, EPLRS
SATCOM	Secure Voice, TRAP, TIBS, TDDS, TADIXS-B, OCTCIS-II, DAMA
Navigation:	GPS, TACAN, Altimeter, VOR
Landing:	ILS, ACLS, ICLS
ID	Mark 12 IFF

Table 5. Lists of the Quantitative Sensitivity and Bandwidth Requirements for Each CNI Function.

Signal Designator	Frequency Range (MHz)	Sensitivity (dBm)	Band-width (KHz)
SINCGARS	30 - 88	-106	20
VHF FM	30 - 88	-115	19
VHF AM	108 - 174	-103	36
HAVEQUICK	225 - 400	-109	36

UHF TDMA	225 - 400	-120	40
Constant Source	225 - 400	-126	80
EPLRS	424 - 450	-90	3000
Link 16	969 - 1206	-95	3000
TACAN	969 - 1206	-92	6000
IFF	1030 / 1090	-83	8000
GPS	1227 / 1575	-130	20000

The frequency bands of interest for CNI are often lumped into a single band (30 MHz to 2 GHz) referred to as the "Low Band". From a cost, size, weight, and power perspective, it is desirable to develop a common CNI receiver that will cover this entire band. A receiver of this type would require an ADC capable of 14 to 16 bits resolution, 120dBm instantaneous dynamic range, and > 20 MHz bandwidth.

Electronic Warfare (EW)

In general EW receiver functions on both, combat and surveillance aircraft, are being tasked to provide more threat information, more accurately, and on a shorter timeline [20]. Combat aircraft flying air superiority, interdiction, and ground attack/support missions require more capability than just a Radar Warning Receiver (RWR). Accurate RF signal environment data is required to be fused with other sensor data to provide full situation awareness (SA) and passive RF information is used to cue active sensors to maintain stealthiness. In addition, reconnaissance aircraft need to provide fine-grain technical ELINT collection for data base updates. On another hand, UAVs on tactical/operations collection missions are used to penetrate airspace and provide EOB (Electronic Order of Battle) information updates to command authority or directly to the cockpit before and during a battle providing real-time targeting information to the cockpit. To meet these stressing mission requirements, advanced Electronic Support Measure (ESM) receiver capabilities are needed. Some of the characteristics of an ESM receiver are:

- Broad Instantaneous Bandwidth (> 1 GHz)
- Wide Spatial Field-of-View
- High Probability of Intercept
- Simultaneous Signal Processing Capability
- Good Sensitivity and Dynamic Range (SSDR, IDR and TSSFDR)
- Accurate and Fine Resolution Parameter Measurement such as center frequency (CF), angle of arrival (AOA), time of arrival (TOA), pulse amplitude (PA), pulse width (PW), and intentional modulation on pulses (IMOP)
- Rapid and Accurate PDW Processing (SORT & ID

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and Emitter Location)

Current ESM receivers (in operation and development) are analog in nature with multiple downconversion stages and analog processing elements such as mixers, power dividers, lumped element filters, standing acoustic wave (SAW) filters, frequency discriminators, logarithmic amplifiers, etc. Examples of these receivers are listed below in table 6.

Table 6. Operational Examples

System	Function	Implementation
ALR-67 (Hughes)	Acquisition Fine PE/DF	ACR Cued narrowband superhets Amplitude comparison
ADVCAP (TI/Litton)	Acquisition Fine PE/DF	ACR Cued narrowband superhets / Phase comparison

Developmental Examples

JASS Highband Prototype (TRW)	Acquisition Fine PE/DF	ACR Cued narrowband superhets / Phase comparison
WECRS (Northrop Grumman)	Acquisition Fine PE/DF	ACR Cued narrowband superhets / TBD

However, current implementations of ESM receivers are usually plagued by numerous problems, some of which are related to cost, performance, physical dimensions, and other non-desired characteristics. Today's ESM systems tend to be costly due to specialized components frequently produced in low volumes, and procured at premium cost. For many platforms, systems are too large, especially in cases in which size reduction has reached a limit. Similarly, many ESM systems were not designed for small tactical platform integration such as UAVs. With respect to performance, most analog components have nonideal characteristics that tend to drift with time and temperature. This requires frequent system calibration and alignment to maintain performance. Because analog systems have fixed hardware architectures, multiple bandwidths can be supported only by adding or deleting hardware, causing limited and programmable flexibility in deployed systems. In addition, in many cases parameter estimation has reached a performance limit (e.g., estimation is not SNR limited, but bias limited). Finally, analog delay line technology tends to be lossy, and usually requires calibration. Therefore, analog storage for cueing and reprocessing has become a problem in today's ESM systems.

As a result of these limitations/problems, the trend is to push the digital interface as close to the antenna/sensor as possible with emerging ADC capabilities. Some advantages of going to a digital receiver implementation are related to cost, physical properties, performance and maintanability. With respect to cost, systems can be made less costly by lowering the manufacturing, unit integration and maintenance costs. Reductions in system size, weight and ultimately power can be achieved by implementing more functions with advanced silicon technologies (deep-submicron) allowing more functions on a single chip, and by adopting advanced MCM packaging techniques allowing whole system functions to be integrated in a small area. In addition, digital systems provide programmable flexibility for multiple uses including scaling of system bandwidth with sample frequency tuning, programmable filters (bandwidths and shapes), and by implementing dynamically executable algorithms embedded in FPGAs and/or DSP. In addition, digital processing elements feature precise characteristics and tend to be immune to temperature changes, resulting in a reduction of calibration cycles in the field. Due to digital memory technology, signals can be stored digitally in lossless elements with no calibration required. In addtion, simultaneous signal processing can be handled by multiplexing the information stored in the digital memory.

Future ESM receiver systems will require advanced converters with a dynamic range exceeding 60 dB (> 10 bits) will be required over an input signal bandwidths greater than 3 GHz. This translates to converters with spurious free dynamic range (SFDR) >70 dB, and sampling rates ≥ 3 Gsps.

Radar

As component technology evolves, there is a push to do more and more with digital circuits [21]. This is driving the ADC closer to the antenna/sensor in both retrofit and future radar receivers. The advantages of going to digital receivers were addressed above in the EW sub-section and are equally applicable to radar receivers as well. The mission requirements that these future, digital multi-mode radar systems address are given in Table 7.

Table 7

Mission	Requirements
Air to Air	• Search Track and Target small airborne platforms - Look Down - Look Up - ID - LPI/ECCM
Air to Surface	• Search Track and Target fixed and moving ground targets via mapping, ranging, and SGMTI/L - SAR - ID • TF/TA • LPI/ECCM
Reconnaissance	• All weather long range high area mapping to detect, locate, identify, track and classify fixed and moving ground targets - SAR - ID • LPI/ECCM
SOF / Air Mobility	• Search Track and Target fixed and moving ground targets via mapping, ranging, and SGMTI/L - SAR - ID • TF/TA • LPI/ECCM

Table 8

	Present	Near Term	Far Term
Dynamic Range (dBc)	60-80	100	120
Instantaneous Bandwidth (MHz)	60	200	600
Sensitivity (dBc)	65	75	90-95
Interference Cancellation (dB)	20-30	40	70
Phase Noise (dBc/Hz)	-104 @ 10 KHz	-115 @ 10 KHz	-125 @ 10 KHz

Some of the current limitations of radar receivers that are being addressed are: 1) Dynamic Range - need higher resolution ADCs to improve dynamic range to detect and track CLO (counter low observable) targets in clutter; 2) Spectral Purity / Phase Noise - need improved performance to detect and tract CLO targets in noise and need improved waveform stability for higher quality SAR mapping and target ID; and 3) Channel Matching - need improvement to exploit multi-channel space-time adaptive processing (STAP) for interference cancellation. Key performance goals for near, mid and far term are given below in Table 8.

5. A/D Conversion: Fundamental and Physical Limitations

As we mentioned in a previous section, it takes approximately six years to improve the resolution of a given converter by approximately 1-bit. In recent years, many designers have addressed some of the fundamental limitations that impair the continue improvement of commercial and military converters. As shown in figures 3 and 10, commercial and military converters can be plotted in the same graph, when one consider their sampling speed and resolution as stated by the manufacturer. Once we calculate the slope of progress, we found that approximately one bit of resolution is lost for every doubling of the sampling (clock) rate as indicated by the slope in figure 10. As device technologies advance, the line moves slowly upward (approximately one bit of resolution every six years) but the slope remains about the same. The -1bit/octave slope can be explained in terms of three fundamental limitations: aperture and clock jitter, thermal noise, and comparator regeneration time.

In order to explain the slow progress, as shown in Figure 10, we have to consider the fundamental and physical limitations to current ADC technology.

Thermal Noise Limitations

The thermal noise limitation [4] is due to the random Brownian motion of electrons and is related to the absolute temperature through the mean-square noise voltage function (V^2),

$$v^2 = 4K_b TR\Delta f \tag{1}$$

where K_b is the Boltzman constant, T is the absolute temperature, R is the system impedance and Δf is the converter bandwidth. In a true Nyquist converter, the resolution is limited by the thermal noise generated in the signal source impedance (usually 50 Ω). Therefore,

$$N_{eff} = \log_2 \frac{V_{fs}}{\sqrt{12K_b TR\Delta f}} \tag{3}$$

where N_{eff} is the number of effective bits, and V_{fs} is the full scale input voltage
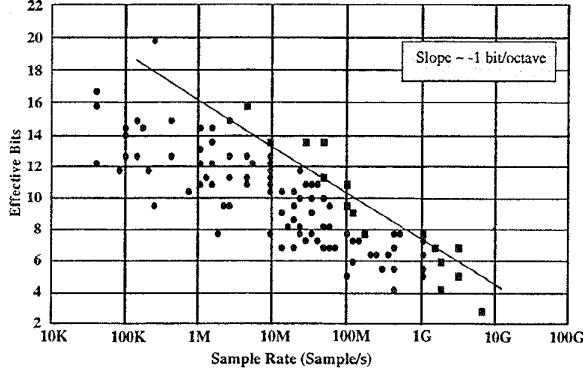
Figure 10. Sampling Rate vs Resolution for Commercial and Military ADCs.

Assuming a source impedance of 50 Ω, a 1V full scale input voltage, and a truly Nyquist converter, the thermal noise contour limits the ADC resolution as shown in figure 11.
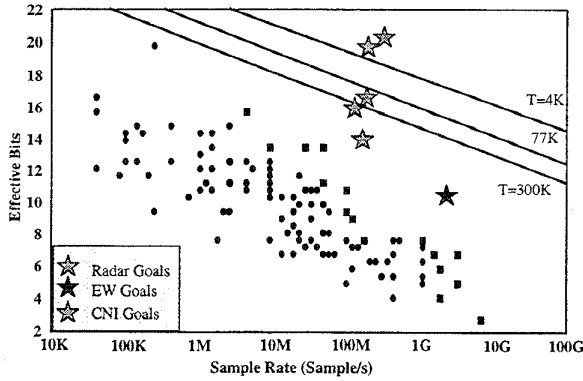

Figure 11. Performance Limitations Due to Thermal Noise in ADCs.

Aperture (Clock) Jitter Limitations

According to the IEEE Standard Dictionary of Electrical and Electronics Terms [22], in data transmission systems, jitter is defined as a small, rapid, and general variation in the size, shape, or position of observable information. More specific, the time related jitter is defined as an abrupt and spurious variation of any specified related interval. The same definition applies to other signal parameters such as, amplitude, frequency, and phase.

The resolution limit imposed by the jitter of clock sources is analyzed by considering the permissible amplitude uncertainty of an n-bit quantizer with a full-scale input amplitude at the Nyquist frequency [23, 24]. This is better known as Aperture Jitter. As shown in figure 12, the maximum slope of such a signal is defined to be

$2\pi V_{fs}(f_s/2)$ where V_{fs} is the full scale amplitude, and $f_s/2$ is the Nyquist frequency $(f_n=f_s/2)$. Therefore, the permissible amplitude uncertainty of an n-bit quantizer cannot be more than one half of the least significant bit (1/2 LSB). Dividing the input amplitude, which causes a 1 LSB change in the quantizer's output, by the maximum slope of the input signal, we obtain the permissible temporal uncertainty (Δt) to be

$$\Delta t = \frac{V_{fs}/2^N}{2\pi V_{fs}f_n} = \frac{1}{2^{N+1}\pi f_n} \qquad (4)$$

where N is the number of bits in the ADC. Solving this equation for N, we obtain the expression that relates the aperture jitter to the effective number of bits (N_{eff}) in ADCs

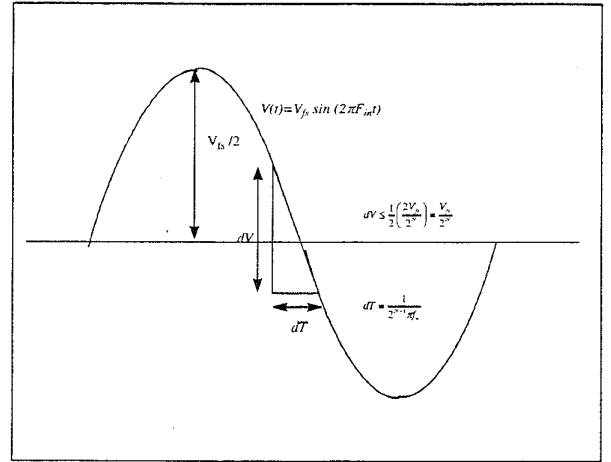$$N_{eff} = \log_2\left[\frac{1}{2\pi f_n \Delta t}\right]. \qquad (5)$$

Figure 12. Aperture Uncertainty Analysis in ADCs.

In ADCs, the aperture jitter is a noise-induced uncertainty in the otherwise periodic sampling interval, and it places a fundamental limit on the achievable converter resolution. Assuming the sinusoidal input signal in figure 12, of amplitude V_{fs} and frequency f_{in}, the number of effective bits as a function of aperture jitter can be plotted as function of the converter sampling frequency and resolution. Figure 13 shows the aperture jitter limitations plotted as function of sampling frequency and effective number of bits for current Analog-to-Digital Converters. Note that many current demonstrations are already limited by the aperture uncertainty and it is likely that this trend will continue unless innovative ways to minimize the clock jitter variations are demonstrated.

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Comparator Regeneration Time Limitations

The finite regeneration times of comparators can result in metastability errors (erroneous code) that contribute to noise power at the output of an ADC [24, 25, 26]. The source of this limitation occurs when a comparator with an analog input makes a decision very close to its threshold. If the change in input voltage is small enough not to be detected and the time that the comparator spends in its regenerated state is only a few RC time constants[5], the output of the comparator may not be large enough to be unambiguosly interpreted by the succeeding encoding logic. It is important to mention that metastability errors depend mainly on the ADC architecture and the output coding used (e.g. binary, gray, etc.) . Therefore, it is hard to predict its effect on the ADC performance charts.
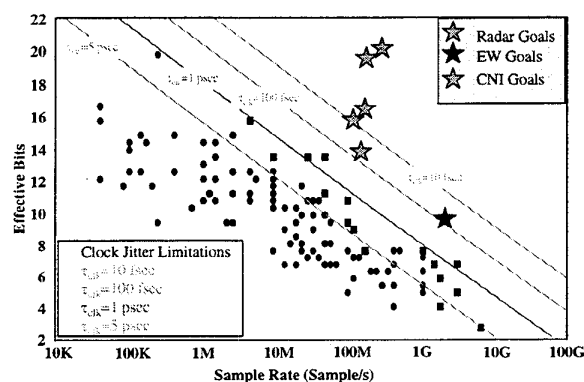

Figure 13. Performance Limitations Due to Clock and Aperture Jitter in ADCs.

Physical Limitations

A recent consensus among ADC designers has demonstrated that not only the fundamental limitations, such as thermal noise, aperture jitter, and regeneration time affect the progress of a given ADC design, but also there are some physical limitations related to device and fabrication technologies that contribute to the slow progress over time [27]. As an example, ADC designers have to trade-off the device and architecture relationship, and its implication to sampling speed and resolution performance. In addition, the characteristics of the active and passive elements in the IC technologies from which they are made, as well as other factors, such as power limitations, and external clock jitter, that strongly influence ADC performance, have to be taken into consideration in each design. This detailed information about how IC/device limitations end up translating into ADC performance limitations is what ADC circuit

designers cope with every day in executing the many tradeoffs involved in the design process. In many cases the actual sample rate and resolution limitations of various ADC architectures do not reflect the speed and linearity characteristics of the IC technologies (e.g., transistor F_t, linearity, V_{be} matching, etc.) with which they are implemented. Unfortunately, designing an ADC is fifty percent art and fifty percent black magic.

There are many other physical limitations that explain the -1 bit/octave slope shown in figure 10. As to date, there is not an available IC technology adequate to achieve "the ideal" ADC performance. In general, ADC designs are characterized by numerous constraints such as, power, bandwidth, linearity, manufacturability, cost/yield and integration densities in which the circuits are to be fabricated. In addition, device parameter values and uniformities such as, current gain (β), V_{be}, early voltage, linearity, F_t, F_{max}, broadband noise figure, 1/f noise, dissipated power, and availability of complementary types determine the realization of reproducible and reliable circuits. No need to mention that the quality of interconnects and passive devices such as, resistors and capacitors available to the designer in the fabrication process, play a very important role in the realization of high performance circuits.

These many constraints in ADC design are compensated by innovative architectures, and by carefully selecting the tradeoffs with the higher payoffs for the desired performance specifications. Therefore, it is unlikely that a single improvement in device characteristics will be reflected automatically in the ADC performance charts (figures 8 and 10). It is an interplay of all these performance parameters that makes the slope of this curve to improve by one bit every six years.

Ultimately, the most serious limitations of any ADC are related to achieving the desired levels of linearity, as indicated by spur-free dynamic range (SFDR), intermodulation distortion (IMD) or total harmonic distortion (THD) specifications.

6. Military Unique Versus COTS

Today's military R&D investments are dedicated to enhance warfighter capabilities and prepare the armed forces for the 21st century threats. In order to enhance these military capabilities, we are required to develop and mature technologies related to the improvement of weapons, communications, and sensors generating and exploiting the information. This can only be accomplished by improving component performance, and reliability while reducing logistic costs. However, there is a clear tradeoff between cost and capability. In many

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[5] The RC or time constant is related to the time response of the S/H circuit. For more information in RC constant, the reader is referred to [24].

military systems, the use of commercial-off-the-shelf (COTS) and best business practices are used to reduce system cost only when performance can be met. In the case of Analog-to-Digital Converters, there is a considerable gap between military requirements and the current state-of-the-shelf technology. For example figure 14 shows the performance, power consumption, and cost of commercial-off-the-shelf ADCs. When one compares future military requirements with the state-of-the-shelf of commercial technology (figure 14), it becomes obvious that for future CNI, radar, and EW missions, COTS CANNOT DO THE JOB!!! Therefore, continue investment in high performance components is required to provide system designers with the demanding ADC performance specification (e.g., dynamic range, bandwidth, power, and reliability, etc.) necessary in future military platforms. This includes investments in key technologies such as, specialized semiconductor materials and packaging technologies. It is possible that in many cases, the military R&D investment could drive and lead to commercial developments or to processes common to both markets. However, because the commercial market is driven by demand, manufacturability, and profit potential, it is becoming harder and harder for the military market to leverage from commercial ventures.
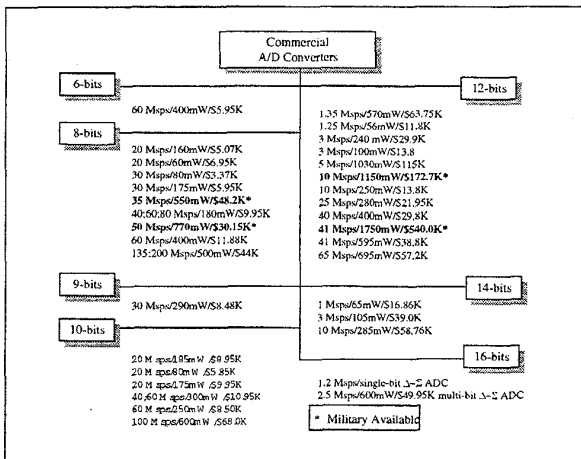

Figure 14. List of Commercial ADC Converters Including Performance, Power Consumption, and Cost. List of COTS Compiled from Analog Devices Catalog.

Finally, table 9 summarizes future ADC requirements for military avionics platforms including development time estimates based on the current state-of-the-art technology. The development time estimates are calculated based on the data presented in figures 8 and 10 from which the 1-bit every six-year progress was assessed.

Table 9. Estimated Availability of Future ADCs for Military Avionics.

| Application	Bandwidth/ Sampling Frequency	Dynamic Range	Estimated Availability
CNI	25 MHz/ (>75 Msps)	100 dB (>16 bits)	12 years
CNI	100 MHz/ (200 Msps)	>125 dB (>20 bits)	> 24 years
radar*	60 MHz/ 4 Gsps	60-80 dB (10-13 bits)	1-5 years
radar*	200 MHz/ 10 Gsps	100 dB (>16 bits)	10-20 years
radar*	600 MHz/ >> 10 Gsps	120 dB (>20 bits)	> 20 years
EW	1 GHz/ 3 Gsps	60 dB (>10 bits)	10 years

* Availability Estimates are Based on the State-of-the-Art of $\Delta-\Sigma$ ADC Technology.

7. Conclusions

In summary, ADCs are critical for the development of current and future generations of military avionics systems. As we approach the next millennium, digital receivers will find more acceptance in many aging and future military platforms such as, the F-22 UAVs, and JSF. However, the realization of digital receivers will only be possible by developing and implementing innovative high performance analog-to-digital converters with revolutionary device technologies and architectures. As the digital domain moves closer to the sensor/antenna, the increasing ADC requirements for military radar, CNI, and EW systems will be hard to meet with existing components including COTS. It is likely that the gap between COTS and military unique components will increase due to diverging interests in the commercial and military sectors. Unfortunately, in today's environment, decreasing funding levels for science and technology have already slowed down the progress of many critical technologies such as ADCs. More leverage from the commercial sector (the dual-use paradox), is being encouraged under today's environment. But before we start leveraging from the commercial sector, we have to keep in mind that in many cases COTS will not do the job. Continue investments in military unique technologies are needed in order to meet future system requirements. Finally, in order to reduce development time, it is recommended that research and development efforts continue focusing toward minimizing the effects of fundamental and physical limitations on high-performance analog-to-digital converters.

References

[1] B. Gordon, "Linear Electronic Analog/Digital Conversion Architectures, Their Origins, Parameters, Limitations, and Applications", IEEE Transactions on Circuits and Systems, Vol. CAS-25, No. 7 (1978)

[2] B. Razavi, Principles of Data Conversion System Design, IEEE Press Marketing 12-27 (1995)

[3] J. Tsui, Digital Techniques for Wideband Receivers, Artech Publishers, 182-189 (1995)

[4] S. Soclof, applications of Analog Integrated Circuits, Prentice Hall 451-453 (1985)

[5] S. Norsworthy, R. Schreier, and G. Temes, Delta-Sigma Converters, Theory, Design, and Simulation, IEEE Press (1996)

[6] L. Tran, S. Southwell, J. Velebir, A. Oki, D. Streit, and B. Oyama, "Fully Functional High Speed 4-bit A.D Converters Using InAlas/InGaAs HBTs", *Proceedings 1993 IEEE GaAs IC Symposium*, **Vol 15**, pp 159-162 (1993)

[7] C. Baringer, J. Jensen, L. Burns, and B. Walden, "3-bit, 8 Gsps Flash ADC", *Proceedings 1996 IEEE Indium Phosphide and Related Materials Conference*, (1996)

[8] K. Nary, R. Nubling, S. Beccue, W. Colleran, J. Penney, K.C. Wang, "An 8-bit, 2 Gsps ADC", *Proceedings 1995 IEEE GaAs IC Symposium*, **Vol. 17**, pp 303-306 (1995)

[9] S. Southwell, J. Zvonik, B. Oyama, and H. Hennecke, "An 8-bit 3 Gsps IF Sampling ADC" , Proceedings of 1996 Government Microelectronics and Advanced Concepts (GOMAC), pp 99-100 (1996)

[10] K. Poulton, K. Knudsen, J. Concoran, K.C. Wang, R. Nubling, E. Pierson, M.C. Chang, P. Asbeck, "A 6-bit 4 Gsps ADC Fabricated in GaAs HBT Process, *Proceedings 1994 IEEE GaAs IC Symposium*, **Vol 16**, pp 240-243 (1994)

[11] TRW Private Communications

[12] G. Raghavan, J. Jensen, R. Walden, W. Posey, "A Bandpass $\Delta-\Sigma$ Modulator with 92 dB SNR and Center Frequency Continuosly Programable from 0 to 70 MHz" *1997 IEEE International Solid-State Circuit Conference Technical Digest*, pp 214-215 (1997)

[13] J. Jensen G. Raghavan, A. Cosand, R. Walden, "A 3.2 GHz, Second Order D-S Modulator Implemented in InP HBT Technology", IEEE Jour. Of Solid-State Circuits, Vol 30, No. 10, pp. 1119-1127 (1995)

[14] R. Walden "Analog-to-Digital Converer Technology Comparison" *Proceedings 1994 IEEE GaAs IC Symposium*, **Vol 16**, pp 217-219 (1994)

[15] Rockwell Science Center Private Communications

[16] R. Yu, N. Sheng, K. Cheng, G. Gutierrez, K.C. Wang, and M. F. Chang, *Proceedings 1997 IEEE GaAs IC Symposium*, **Vol 19**, (1997)

[17] J. Jensen, A. Cosand, W. Stanchina, R. Walden, T. Lui, Y. Brown, M. Montes, K. Elliot, and C. Kirkpatrick, "Double Heterostructure InP HBT Technology for High Resolution A/D Converters", *Proceedings 1994 IEEE GaAs IC Symposium*, **Vol 16**, pp. 224-227 (1994)

[18] A. Jayaraman, P. Asbeck, K. Nary, S. Beccue, K.C. Wang, "Bandpass Delta-Sigma Modulator with 800 MHz Center Frequency", *Proceedings 1997 IEEE GaAs IC Symposium*, **Vol 19**, (1997)

[19] Mr. Mark Minges Private Communications

[20] Mr. David Sharpin and Mr. Scott Rodrigue Private Communications

[21] Mr. Emil Martinsek Private Communications

[22] *IEEE Standard Dictionary of Electrical and Electronics Terms*, 4th Edition, Institute of Electrical and Electronics Engineers, Inc., New York, New York pp 505 (1988)

[23] M. Shinagawa, Y. Akazawa, T. Wakimoto, "Jitter Analysis of High Speed Sampling Systems" , IEEE Jounal of Solid-State Circuits, Vol. 35, No. 1, pp. 220-224 (1990)

[24] W. Colleran, "A 10-bit, 100 Msps Analog-to-Digital Converter Utilizing Folding, Interpolation, and Analog Encoding Techniques", Doctoral Dissertation University of California, Los Angeles (1993)

[25] Dr. Kevin Nary Private Communications

[26] L. Larson, "High Speed Analog-to-Digital Conversion with GaAs Technology: Prospects, Trends and Obstacle", *1988 IEEE International Solid-State Circuit Conference Technical Digest*, pp 2871-2878 (1988)

[27] DARPA Workshop on Sample Timing Jitter and other ADC Performance Limiters, (1997)
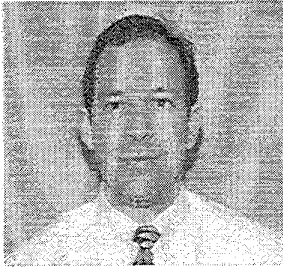
Edgar J. Martinez: received the B.S. degree in electrical engineering from the University of Puerto Rico in 1987, the M.S. degree in electrical engineering from the University of Dayton in 1991, and the PhD. degree in electrical engineering from the University of Virginia, Charlottesville, in 1995.

In 1985, he joined the staff at Intel Corporation, where he worked as reliability engineer of VLSI components. In 1987, he joined the staff at the Air Force Research Laboratory, Wright Patterson AFB, OH where he is currently working in the areas of research and development of high-speed semiconductor device technologies. Since joining the Sensors Directorate at AFRL, his research interests have included processing, modeling, and characterization of compound semiconductor materials and devices, and high performance digital and mixed-signal circuits.

Dr. Martinez is a member of the National Union of Radio Science (URSI) and the Eta Kappa Nu Association.

Ronald L. Bobb: received a B.S. degree in computer engineering from Wright State University 1979, and a M.S. degree in electrical engineering from Wright State in 1994.

In 1980 he joined the staff at the Air Force Research Laboratory, Wright Patterson AFB, OH where he is currently working in the areas of research and development of high-speed semiconductor device technologies. Since joining the Sensors Directorate at AFRL, his research interests have included compound semiconductor materials and devices, device characterization and testing, signal processing, IC design and built-in test, and high performance digital and mixed-signal circuits, in particular, analog-to-digital converters.