Future-Ready Ultrafast 8bit CMOS ADC for System-on-Chip Applications*

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Abstract

Design and performance of an ultrafast 8bit 0.25μm CMOS flash ADC based on the thresholding inverter comparator are presented.

1. Introduction

The semiconductor technology is now approaching 100 nanometer feature size and it is going toward below 100 nanometer. This technology trend presents new challenges in analog-digital mixed signal circuit design. A mixed signal circuit must be integrated on a single chip along with logic and memory circuits to form a system-on-chip. The mixed signal circuit must operate at fast speed along with digital logic and memory circuits; otherwise, it becomes the bottleneck of the system. Thus the authors present in this paper a noble approach to high-speed Analog-to-Digital Converter (ADC) design suitable for the technologies below 100 nanometer and suitable for system-on-chip integration.

Flash ADC architecture is known for its high speed operation. An analog input voltage is simultaneously compared by $2^n - 1$ voltage comparators in an n-bit flash ADC. The comparators are, perhaps, the most critical components in a flash ADC. The high-speed comparators are realized with differential amplifiers using bipolar transistors. The comparator realization in the CMOS flash converters consists of auto-zeroed inverter with switched capacitor input. Yet, another CMOS voltage comparator design is considered.

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2. Threshold Inverter comparator

The authors propose an ultrafast 8bit CMOS flash ADC, shown in Figure 1, featuring the Threshold Inverter (TI) comparators. Circuit wise, the TI comparator is an inverter. Figure 2 shows the TI comparator and the differential amplifier type voltage comparator. The inverter circuit is inherently simpler and faster than the differential amplifier type voltage comparator.

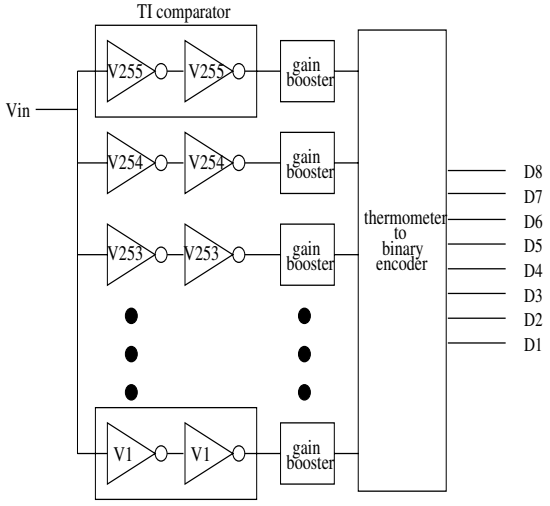


Figure 1. Proposed 8-bit CMOS flash ADC

Highlights of the TI comparators are as follows:

- The comparison voltage V_m of the TI comparator is internal to the inverter, fixed by the transistor sizes. On the other hand, the comparison voltage V_r of the differential comparator is external to the comparator, typically generated by a resistor ladder circuit.

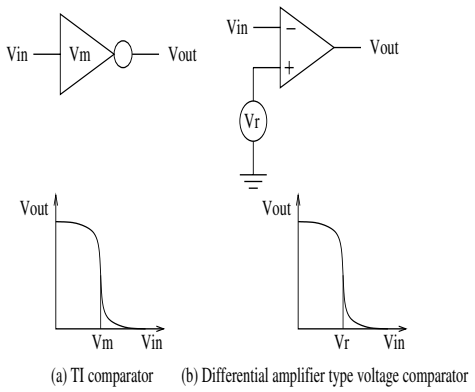


Figure 2. The TI comparator and the differential amplifier type voltage comparator

- The TI comparator does not require switches, clock signal, or coupling capacitors for the voltage comparison. Also, the ADC based on the TI comparators does not require a resistor ladder circuit.

- The TI comparator is suitable for the digital CMOS technology, ideal for the system-on-chip.

- The TI comparator is highly adaptable to future CMOS technology development, going to below 100 nanometer feature size and below 1.0V supply voltage. There is only two transistors connected from the power supply to ground in the TI comparator.

3. Design for TI comparator based ADC

The design method for the ADC based on the TI comparators is not out of ordinary. The ADC requires $2^n - 1$ TI comparators with different V_m. The authors generated the 255 TI comparators for an 8-bit ADC by systematically varying the transistor width of each comparator. Extensive SPICE simulation was the basis of obtaining the 255 uniformly different comparison voltages. The authors were able to design the 255 different TI comparators, and redesign many times without difficulty using the modern VLSI CAD tools.

Figure 3 shows the layout of the 8-bit ADC based on TI comparator. The left half of the layout shows the 255 TI comparators. The right half shows the 255 gain boosters and the thermometer code to binary code encoder. Table 1 shows the summary of the 8-bit TI based ADC design. Currently the chip is being fabricated through MOSIS service, using $0.25\mu m$ digital CMOS process.

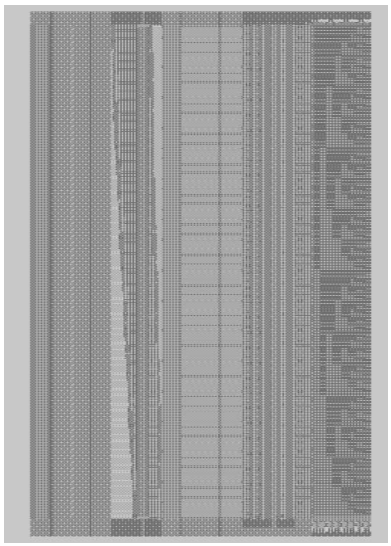


Figure 3. The layout of the 8-bit ADC based on TI comparator

Table 1. Summary of the 8-bit TI based ADC

CMOS technology	0.25 μm
Power supply	2.5 V
Sampling rate	1 GSPS
Area	0.228 mm^2 (0.278 * 0.818)
Power	256.09 mW
V_m range	0.74774 V - 1.64793 V
V_{LSB}	0.00354 V

4. Performance

Figure 4 shows the simulation result of the 8-bit ADC operating at the speed of 1 Gigasamples per second (GSPS), without a missing code. Figure 5 shows the plots of DNL and INL results based on the simulation. Both DNL and INL are well within the 0.1 LSB. These results will be compared with the actual measured results when the chip is returned.

The power consumption of the designed 8-bit ADC is 256mW at 1 GSPS speed. Table 2 shows the power consumption and speed of other ADCs using CMOS technology. The large power consumption of a flash ADC is a inherent problem due to the parallel voltage comparison operation of $2^n - 1$ comparators. Currently, the authors are implementing the circuits which dynamically turn off the TI comparators to significantly reduce the power consumption, at the expense of reduced speed.

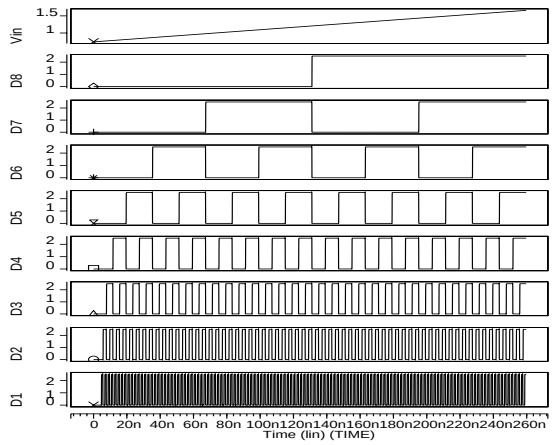
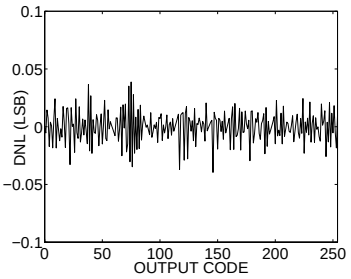
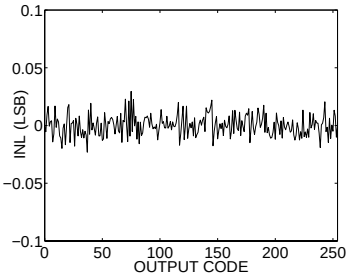


Figure 4. Simulation result of the 8-bit ADC operating at the speed of 1 GSPS



(a) DNL



(b) INL

Figure 5. Plots of DNL and INL results

4.1. Process variation

Perhaps the most critical issue for the TI comparator based ADC is the process variation. The simulation results show that the process variation affects the offset, gain, and linearity of the ADC input voltage range. Table 3 shows the process variation effects of the designed 8-bit ADC using 15 different MOSIS process parameters obtained from the previous wafer tests and design corners. Maximum 18% variation of the offset and the gain variation are observed. The linearity variation is more drastic, numerically. Because the DNL is very consistent (within 0.1 LSB) over all variations, the correction is easier to obtain.

A number of possible solutions exists for the problem of process variation effects on TI comparator based ADC. One solution is to add a programmable pre-amplifier to the analog input of the ADC to dynamically fine-tune the offset, gain, and linearity. Another solution is to performing a digital signal processing on the ADC output to correct the offset, gain, and linearity. This solution is suitable for system-on-chip applications where a processor is already on the same chip with the ADC.

4.2. Other issues on variation problems

Other issues for the TI comparator based ADC are the effects of the: temperature variation, power supply voltage variation, and single ended input noise. Table 4 shows the simulation results of the temperature variation and the power supply voltage variation.

Again, the net effects of the variation are the offset, gain, and linearity changes. The same solution can be applied as the process variation problem. The process variation is a static problem. The temperature and supply voltage variation problems are dynamic problems. Both static and dynamic problems can be solved with the dynamic fine-tuning or the post digital signal processing (with temperature and voltage probes added).

The TI comparator based ADC has a single ended input, more susceptible to noise signal in comparison to the differential input comparator. But it is not completely without a solution. One can add a single differential input amplifier to recondition the ADC input signal.

5. Conclusion

In summary, a new ultrafast 8bit CMOS flash ADC design and simulation results are presented. The TI comparator based ADC is suitable for the system-on-chip applications and it is highly adaptable to the future semiconductor technologies below 100 nanometer.

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Table 2. Specifications of other ADCs

ADCs	Resolution	Gate Length	Type	Speed	Power	Active Area
[8]	8-bit	0.6 μm	Pipeline	150 MSPS	395 mW	1.2 mm^2
[4]	7-bit	0.25 μm	Flash	200 MSPS	187 mW	0.45 mm^2
[3]	8-bit	0.35 μm	Folding and Interpolating	10 MSPS	76 mW	5.01 mm^2
[6]	8-bit	0.35 μm	Unified Subranging	100 MSPS	108.9 mW	0.9 mm^2
[1]	8-bit	0.5 μm	Pipeline	100 MSPS	165 mW	1.68 mm^2
[5]	6-bit	0.35 μm	Current-Interpolation	50 MSPS	10 mW	4.8 mm^2
[7]	6-bit	0.35 μm	Flash	1 GSPS	1155 mW	0.8 mm^2
[2]	6-bit	0.35 μm	Flash Interpolating	1.1 GSPS	300 mW	0.3 mm^2

Table 3. Process variation

Process	Min V_m	Max V_m	V_m range	V_{LSB}	DNL(LSB)	INL(LSB)	Missing Code
T02D	0.76576	1.66084	0.89508	0.00352	0.0623	1.6888	0
T04R	0.70882	1.63864	0.92982	0.00366	0.0747	1.3783	0
T08P-EPI	0.73098	1.60244	0.87146	0.00343	0.1040	2.6049	0
T08P-NON-EPI	0.73114	1.64028	0.90914	0.00358	0.1013	2.4323	0
T09A-EPI	0.75399	1.62559	0.87160	0.00343	0.0728	1.2026	0
T09A-NON-EPI	0.73727	1.59411	0.85684	0.00337	0.1066	2.8842	0
T0BL-EPI	0.76846	1.63072	0.86225	0.00339	0.0570	0.9483	0
T0BL-NON-EPI	0.73436	1.62822	0.89386	0.00352	0.0703	1.4102	0
T0BM	0.74635	1.63290	0.88656	0.00394	0.0556	1.4195	0
T11Y-EPI	0.73449	1.64926	0.91477	0.00360	0.0529	1.4407	0
T11Y-NON-EPI	0.71114	1.63563	0.92449	0.00364	0.0500	0.5552	0
TSMC-FF	0.70803	1.69926	0.99124	0.00390	0.0785	2.3330	0
TSMC-FS	0.69004	1.59432	0.90428	0.00356	0.0393	0.4805	0
TSMC-SS	0.78762	1.60307	0.81545	0.00321	0.0835	1.9656	0
TSMC-SF	0.80580	1.70152	0.89573	0.00353	0.0433	0.5012	0

Table 4. Temperature and Power supply voltage variation

	Min V_m	Max V_m	V_m range	V_{LSB}	DNL(LSB)	INL(LSB)	Missing Code
-40^o C	0.76707	1.60842	0.84135	0.00331	0.0647	1.8118	0
27^o C	0.74719	1.64923	0.90205	0.00355	0.0396	0.0837	0
85^o C	0.73210	1.68785	0.95575	0.00376	0.0593	1.7988	0
2.375V (-5%)	0.72906	1.54588	0.81682	0.00322	0.0455	0.5880	0
2.5 V	0.74774	1.64793	0.90019	0.00354	0.0396	0.0295	0
2.625V (+5%)	0.76598	1.75084	0.98486	0.00388	0.0461	0.6106	0