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Full Length Research Paper

Employing threshold inverter quantization (TIQ) technique in designing 9-Bit folding and interpolation CMOS analog-to-digital converters (ADC)

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This paper presents design and implementation of a 9-bit folding and interpolation ADC using 0.35 µm CMOS C35B4 model under AMS-HIT Kit Library. The complete system consists of two main blocks. One of them is 4-bit flash ADC, which is based on the so-called threshold inverter quantization (TIQ) technique. This part forms the coarse part of the data conversion process. The second one is the 5-bit fine ADC part of the converter. This block includes comparator, analog pre-processing and interpolation units. The designed converter works with 5 V power supply, and has analog input range of 3.4 Vpp. Analog input bandwidth is 1 MHz with clock frequency of 2 GHz for the digital part. The linearity measures of the converter include 2.9 LSB of DNL and 6.3 LSB of INL. The main purpose of this work is to investigate the possibility of employing TIQ technique in designing folding and interpolation type of ADCs. Although, the linearity measures are not satisfying for 9-bit case, the authors believe that this case study will serve as a preferred reference for the researchers who are willing to use TIQ technique in designing fast ADCs other than flash scheme especially.

Key words: Threshold inverter quantization, flash analog-to-digital converter, folding and interpolation analog-to-digital converter.

INTRODUCTION

Analog-to-digital converters (ADCs) work as a bridge between the digital word and the real world. The need for ADCs has been increasing in parallel with the development of applied digital circuits. They have important role in converting analog speech and image signals to digital data especially in digital TVs, cellular phones equipped with cameras, 3G telecommunication systems and wireless wide area networks.

In the literature, there are mainly four different high speed ADC architectures. These are full-flash, semi-flash, pipeline, and folding and interpolation architectures. Full-flash is known as the fastest type of ADC structure. Very high speed ADCs are especially accepted as one of the most important building blocks in the applications requiring magnetic channel reading, optical data storage systems, digital communication systems requiring very high speed of data acquisition, and optical communication systems, (Sheikhaei et al., 2005; Park et al., 2007; Makigawa et al., 2006; Chen and Ren, 2006; Ohhata et al., 2009).

ADCs with high speed and mid-range resolution (8-10bit) are used in high speed image processing applications, digital telecommunication systems, gigabit ethernet, and digital oscilloscopes, (Cheng et al., 2003; Yoon et al., 2000). In system on chip (SoC) applications, using ADCs with low power consumption and high sampling rate are very important to develop new systems.

Due to increase in number of comparators needed, especially in designing high speed fully parallel (flash) ADCs having resolution of 8-bit and above, layout area and power consumption are also increased (Azin et al., 2005). Therefore, in recent years, time-interleaving, interpolating, and folding techniques have been employed in designing high speed ADCs to increase sampling rate

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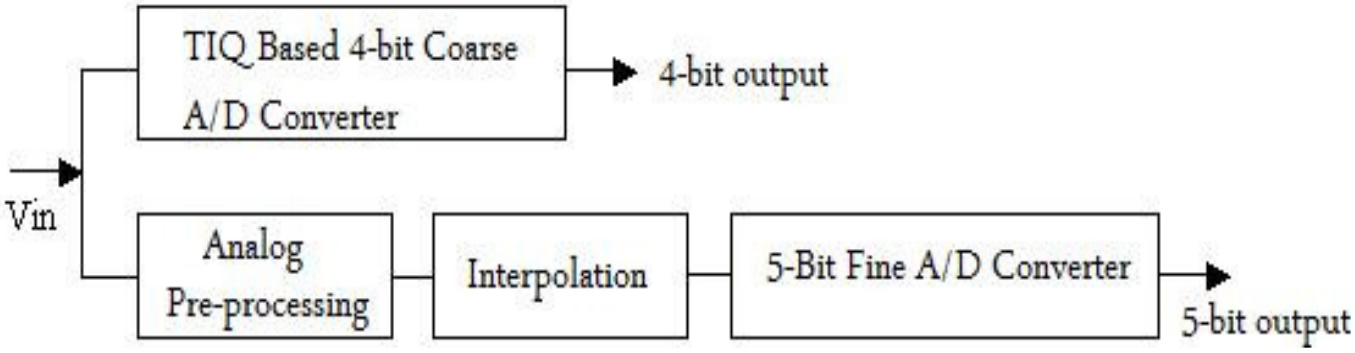

Figure 1. The block diagram of the folding and interpolating ADC.

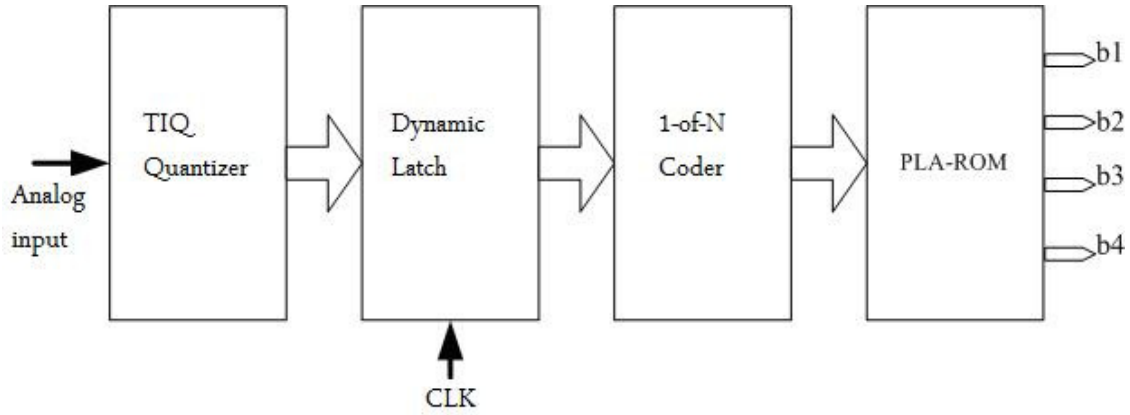

Figure 2. Block diagram of the 4-bit TIQ based coarse ADC.

and resolution. Folding and interpolating type of ADCs have less comparator count and power consumption when compared to full-flash architectures, (Chen and Yuan, 2006; Pereira et al., 2002; Lee et al., 2007; Hsu et al., 2007). Therefore, it is one of the preferred methods for designing high speed, mid-range resolution and low-power ADCs. The reduction of comparator count is obtained by analogue pre-processing circuits. These circuits consist of cross-coupled differential pairs having different DC ofset voltage values applied to one of the inputs of each pair. The result is the folded input signal obtained differentially from the common output nodes of differentail pairs. Here, as the resolution of fine-ADC part is increased, the number of differentail pair needed is also increased accordingly. The interpolation technique is used to solve this problem.

By using interpolation technique, number of folding can further be increased. There are different ways of interpolation (Limotyrakis et al., 2002). The simplest and most commonly used one is using two or more equal value resistors between two folded signal output nodes, which is known as resistor interpolation, (Plassche, 2003). In addition, the number of used resistor is known as the interpolation rate (Valburg and Plassche, 1992). One problem may arise when using resistor interpolation, which is the small amount of nonlinear distortion effects occuring on the interpolated signals. However, as long as the zero crossing points are correct, these distortion effects can be ignored (Grift et al., 1987).

THE DESIGN PROCESS AND SIMULATION RESULTS

The block diagram of the designed 9-bit folding and interpolation ADC is depicted in Figure 1. The system consists of two main block, through which coarse and fine data bits are obtained.

4-Bit TIQ based coarse ADC

Figure 2 shows the block diagram of the 4-bit threshold inveter quantization (TIQ) based coarse ADC. This structure looks like the traditional full-flash ADC scheme except analog input part. It consists of TIQ based voltage comparator array, dynamic latch, 1-of-N encoder, and PLA ROM blocks.

Threshold inverter quantization technique

TIQ technique is based on transistor sizing of two cascaded CMOS inverters as shown in Figure 3, (Tangel, 1999; Aytar et al., 2004;

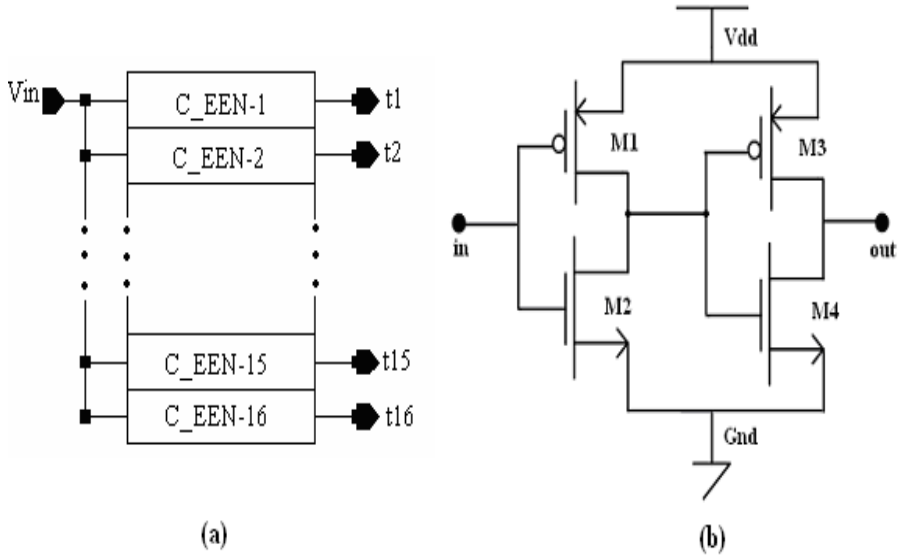

Figure 3. TIQ array and TIQ schematic.

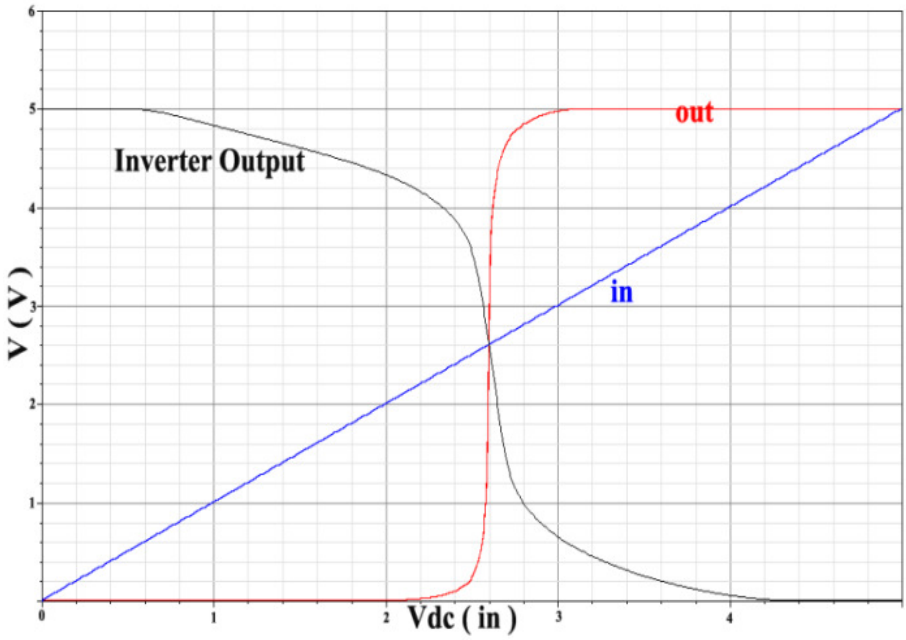

Figure 4. Voltage transfer characteristic of a TIQ quantizer.

Tangel and Choi, 2004; Celebi et al., 2005; Aytar et al., 2008). Therefore, analogue quantization levels of the voltage comparators are obtained inside the comparator without using a traditional resistor array implementation (Yoo et al., 2003). One, perhaps the only important drawback of this technique is that the threshold point of the CMOS inverter is affected by temperature and CMOS process parameter deviations. Therefore it is not practical for high resolution flash ADC designs, Tangel (2004), Tangel and Aytar (2009). Especially, the monotonicity can not be expected for more than 6-bit resolution levels, Tangel and Aytar (2009), Aytar (2009). For that reason, the coarse ADC is chosen to be 4-bit only in this work.

Voltage transfer characteristic (VTC) of a TIQ is shown in Figure 4. Each quantizer must have two identical inverter to obtain the same intersection point with y=x line. Otherwise, there will be a hysteresis problem during AC operation. It is important to produce digital output at the point of VTC' intersection with y=x line as shown in Figure 4.

Dynamic latch unit

Dynamic latch unit transfers its input logic value when the clock signal is logic high. The last value is kept when the clock signal is

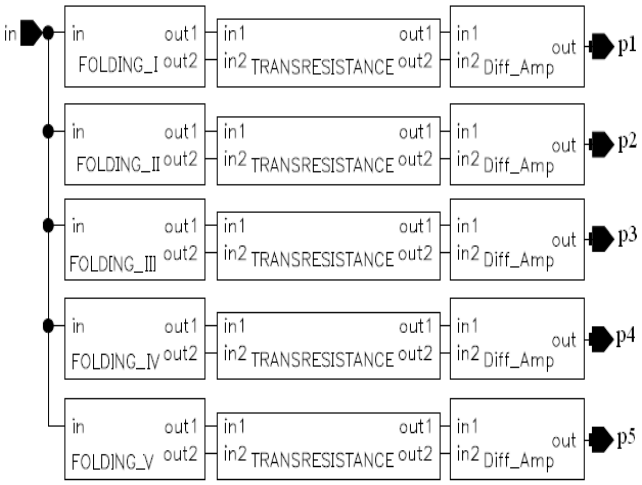

Figure 5. The internal structure of the voltage-mode analog pre-processing block.

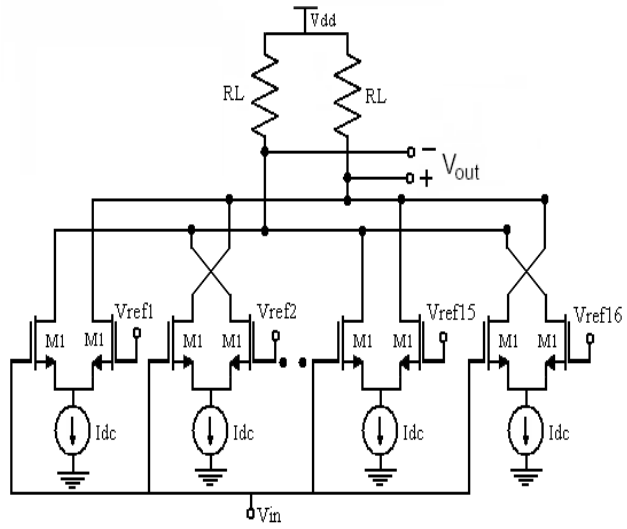

Figure 6. Schematic of the voltage-mode folding circuit.

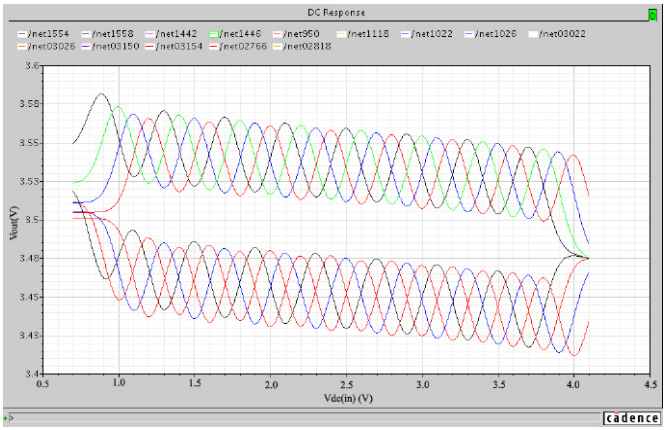

Figure 7. DC analysis results of the folding circuit.

logic zero. During this time digital part of the converter is allowed to finish the conversion process. In other words, the dynamic latch unit works as a sample and hold controller between analog and digital part.

1-of-N coder unit

The 1-of-N coder is used to define the border of “0”s and “1”s array on a thermometer code, which is the form of digital code at the comparator array output. The easiest way to convert the thermometer code to 1-of-N code is to use a logic $\bar{A}B$ circuit, (Yoo et al., 2001; Kulkarmi et al., 2010). Each location of “1” here in this code corresponds to a different binary output value.

The binary encoder unit based on programmable logic array (PLA)

PLA encoder unit converts 1-of-N code to a binary code. This structure consists of n (resolution of the converter) number of PMOS transistors working in linear region, and 2^n-1 number of NMOS line arrays, each of which has a unique transistor number and order depending on its corresponding binary code sequence. The only disadvantage of this structure is not to be in a fully CMOS manner. Therefore, there is a certain amount of static power consumption.

The fine A/D converter block

The fine ADC part consists of an analog pre-processing block, an interpolation block, and a fine flash ADC block as was shown in Figure 1. In this section, some detailed information about these blocks will be given.

Analog pre-processing block

Analog preprocessing unit consists of five folding circuits, which have different offset voltages for each, five transresistance amplifier circuits, and five differential amplifier circuits. These three different circuits are connected to each other in cascaded form as shown in Figure 5.

The folding circuit here is the most important section for the folding and interpolation type of A/D converter designs. The chosen voltage mode folding circuit is shown in Figure 6. A common analog input signal is applied to five folding circuits. Each folding circuit has certain number of differential amplifiers. Everyone of the inputs of these amplfiers are tied to a different but precisely chosen DC offset voltages. The folding circuit reference offset voltages start from 0.8 V. Although ideally only one folding circuit is enough, practically more than two folding circuits are needed to overcome the so called rounding problem on the folded signal. The linearity is lost on the rounding regions of folded signals. Therefore, to produce multiple folded signals and to apply interpolation technique become inevitable for practical designing of folding and interpolation types of ADCs. In this study, five different folded signals (p1 to p5 outputs in Figure 5) are produced to be able to catch the desired linearity.

To be able to increase the resolution of the ADC, 16 pairs of cross-coupled differential amplifiers are preferred for the folding circuit in this work. The required maximum offset voltage range in this case becomes over 3.3 V. Therefore, the power supply voltage of the design had to be increased to 5 V. Fortunately, 5 V power supply option is also available in 0.35 µ AMS design library.

The current contributions from every differential amplifier outputs are collected at the common differential output nodes. The final folded signal is taken differentially between the output resistors as

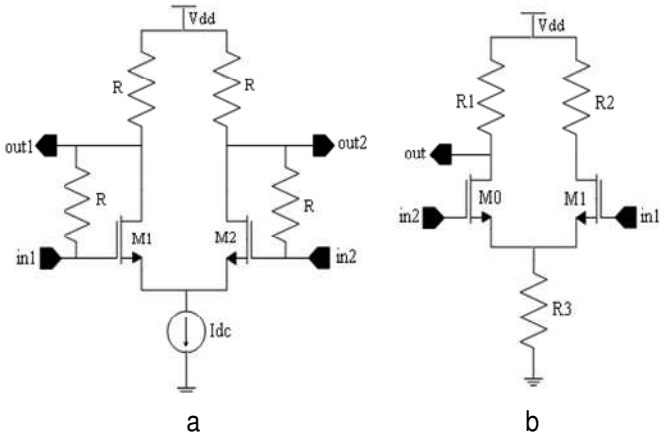

Figure 8. (a) Transresistance amplifier, (b) Differential amplifier.

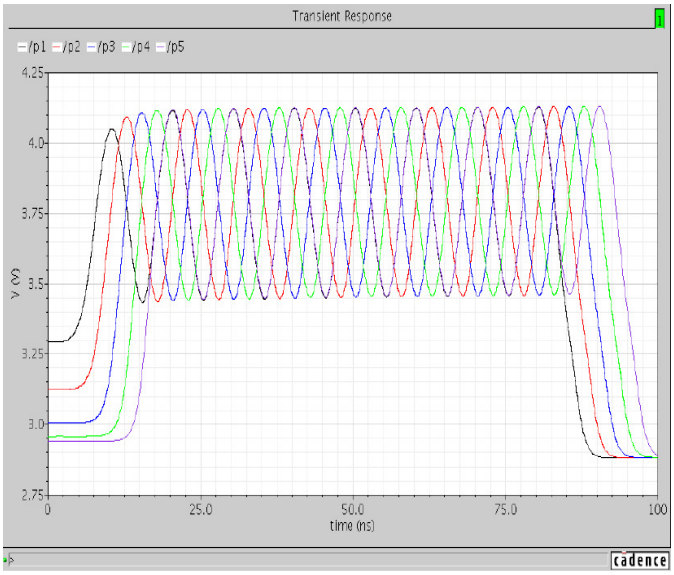

Figure 9. The analog pre-processing block outputs for fin=10 MHz.

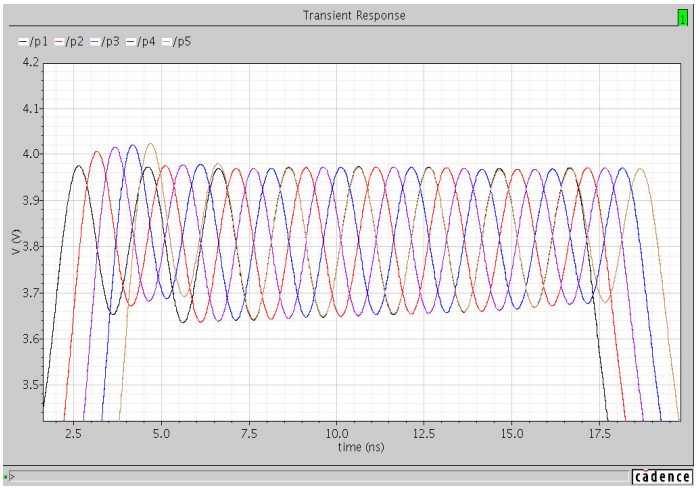

Figure 10. The analog pre-processing block outputs for fin=50 MHz.

shown in Figure 6. Due to nonlinear effects, DC level of the folded signal is shifted as shown in Figure 7. This undesirable effect becomes worse at high frequencies and therefore had to be solved in this work.

To overcome this problem, a transresistance amplifier is followed by the folding circuit as was suggested by Nauta and Venes (1995). A final differentail amplifier circuit is needed for buffering and signal conditioning purposes right after the transresistance amplifier stage as shown in Figure 8. The idea behind these additional circuitry is that the output current from the folding circuit drives the input resistance of the transresistance amplifier. As a result, an output voltage signal, which has a wider dynamic range is obtained. Additionally, the usage of transresistance amplifier increases the analog bandwidth, Nauta and Venes (1995).

Figures 9 and 10 show how these additional circuits work to obtain better folding signals even in AC operation. Please note that the simulation results shown in Figures 9 and 10 are not the differentially taken output signals.

The interpolation unit

If the interpolation technique is preferred to increase the number of folded signals, there will be a decrease in power dissipation, circuit components needed and layout area, (Verbruggen et al., 2009; Semi et al., 2006; Ferragina et al. (2006), Jang (2008), Chang et al. (2008), Deguchi et al., 2008). Therefore, this method is used to reduce the number of folder circuits required in designing folding A/D converters, (Limotyrakis et al., 2002; Martins and Ferreira, 2004; Taft et al., 2004).

There are two ways to accomplish interpolation. These are current-mode and resistive (voltage- mode) interpolation techniques. Although, current mode technique is faster, it has disadvantages of requiring matched current mirror circuits and higher power consumption, |(Seemi et al., 2006). Resistive interpolation technique is much more popular in the literature. It is defined as the easiest method to employ since voltage divider resistors are only connected between two voltage nodes (Martins and Ferreira, 2004; Ahmadi et al., 2003; Uyemura, 2001).

The number of resistors between two voltage nodes for interpolation is called as the interpolation rate, Plassche (2003). If the interpolation rate is more than two, there will be a certain amount of delay on the resulting interpolation signals due to resistive and parasitic capacitance interactions between the related voltage nodes (Limotyrakis et al., 2002). Another issue is the fact that, as long as the zero crossing points occur on the correct order, the distortion on the interpolated signals are not so important (Martins and Ferreira, 1999). Hence, the resistor interpolation technique is chosen in this study. Figure 11 shows the interpolated signal waveforms obtained from the simulation of the interpolation unit.

5-Bit fine A/D converter part

The fine A/D converter part is the section where least significant bits (LSBs) are obtained. It consists of a comparator array block, dynamic latch block, 1-of-N coder, and PLA encoder block. The detailed explanation about these blocks were given in the earlier sections.

As a first attempt, The TIQ comparator block was chosen for this part of the converter. However, the interpolation signals have the zero crossing points at 3.84 V. For a specific TIQ comparator having internal threshold value at this voltage requires large PMOS tansistor, which results in a large input node capacitance. As a result, the delay was more than expected, (Aytar, 2009). Therefore TIQ block was not chosen for the comparator block of the fine A/D converter. Instead, the circuit shown in Figure 12 proposed by Chu

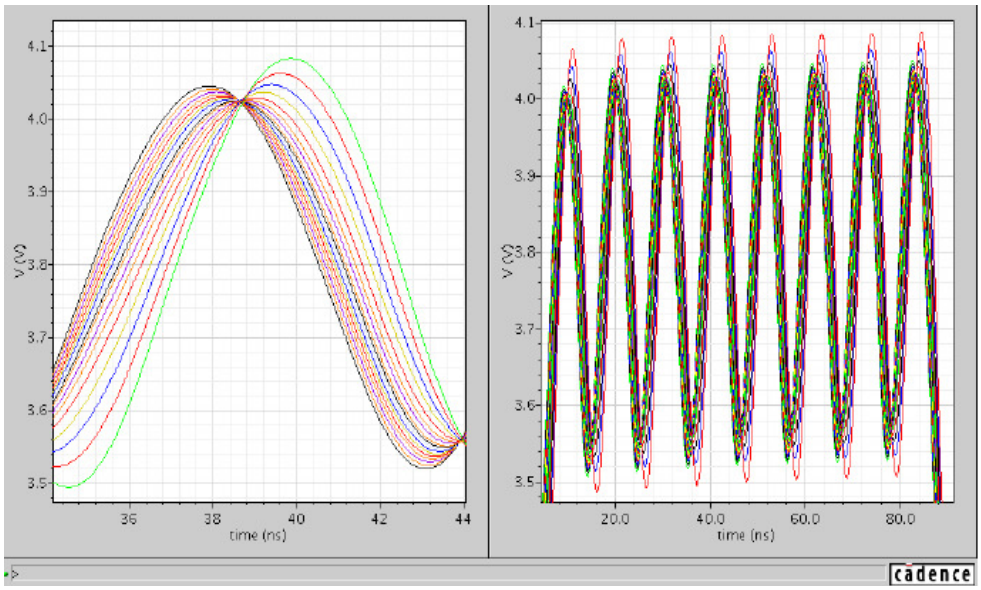

Figure 11. The interpolation unit outputs for fin=10 MHz .

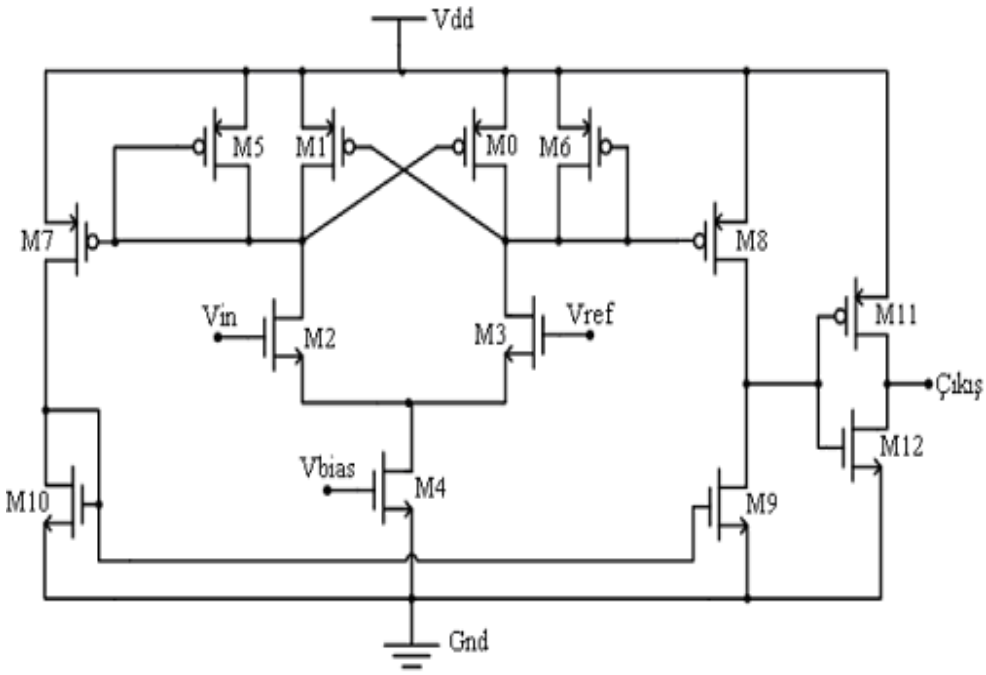

Figure 12. The comparator schematic of the fine ADC part.

and Current (1999) is used as a comparator cell. Figure 13 shows the operation of this comparator cell for 40 MHz input signal.

RESULTS AND DISCUSSION

In this study, a 9-bit folding and interpolation A/D converter including a TIQ based flash ADC core for the coarse bits conversion is designed and implemented. The most important point is the analog input frequency value of the converter. Because, the input frequency and the output frequency of the folding circuit is different. The maximum output frequency that will be observed is defined by Limotyrakis et al. (2002):

$$f_{out} = \sqrt{2}.K_s.f_{in}$$

where f_{in} represents the analog input frequency and Ks

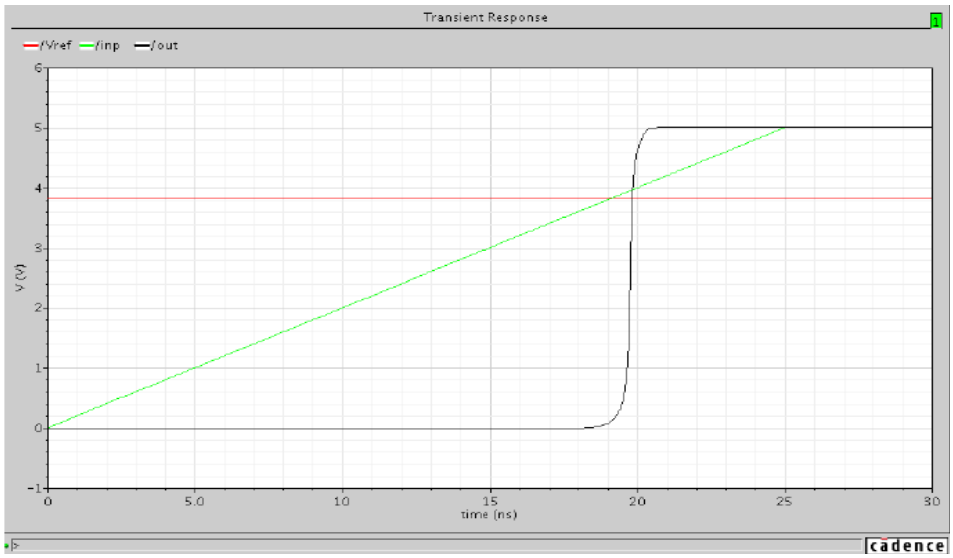

Figure 13. The comparator output at fin=40 MHz.

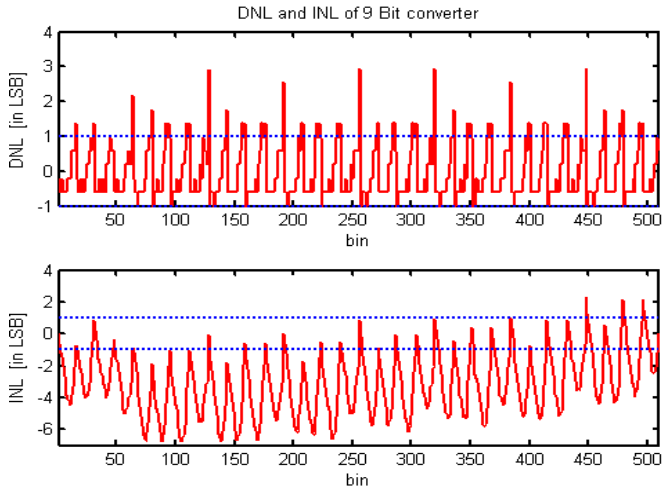

Figure 14. DNL and INL plots.

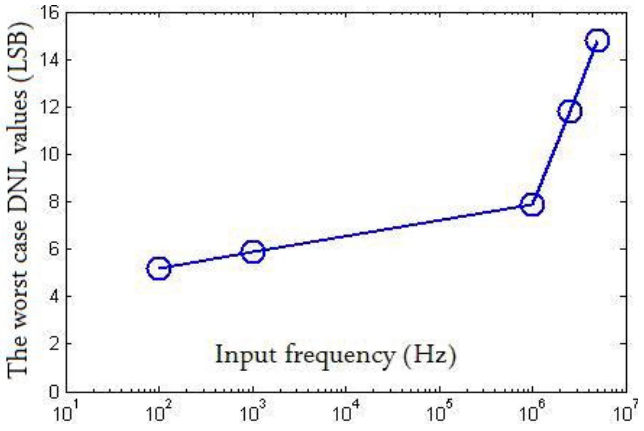

Figure 15. The worst case DNL values with respect to input frequencies.

represents the number of MOS differential pairs (namely the folding rate) used in the folder circuit. As an example, if the input frequency is 10 MHz, then the folded signal frequency is 226 MHz in our case. After these high frequency folded signals are applied to the comparator and dynamic latch blocks, the time difference observed between two digital signal appeared at the inputs of 1-of-N coder becomes less than 100 ps (Aytar, 2009). Therefore there is missing output codes observed for the analog input signals having frequency of more than 10 MHz.

The 9-bit folding and interpolation ADC is designed using 0.35 µm CMOS C35B4 model parameters of AMS-HIT Kit library. DC analysis results and linearity measures are transferred to a MATLAB program referenced from the web site “inst.eecs.berkeley.edu/ (2009). The obtained DNL and INL plots are calculated and depicted in Figure 14.

In addition, when 2 GHz clock frequency is chosen for the digital parts, the worst case DNL and INL measures are plotted for different input frequency values as depicted in Figures 15 and 16.

Figure 17 shows the digital output waveforms for the case fin=10 MHz and clk= 2GHz. The obtained output waveform is applied to an ideal 9 bit D/A converter. The reconstructed ramp-shape analog input signal is shown in Figure 18. The converter for 9-bit case does not work with a satisfying linearity for the given input frequency. The multiplication of the input frequency is the only disadvantages of folding A/D converter designs, which makes the job tedious at the digital part of fine ADC. Hence, the input analog bandwidth becomes inevitably limited although the sampling rate can be very high. The linearity measures becomes better if the two LSB bits are not taken into account (namely 7 bits). Figures 19 and 20 show the layout photo and the die photo of the complete

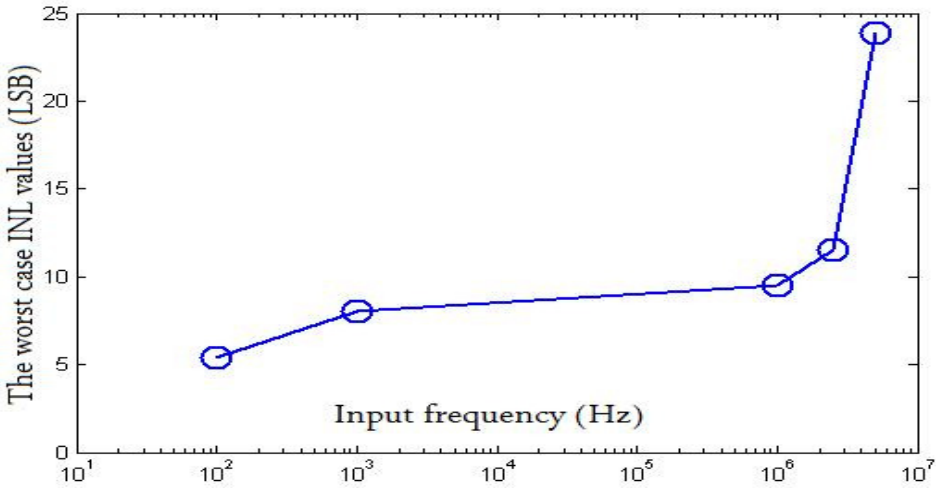

Figure 16. The worst case INL values with respect to input frequencies.

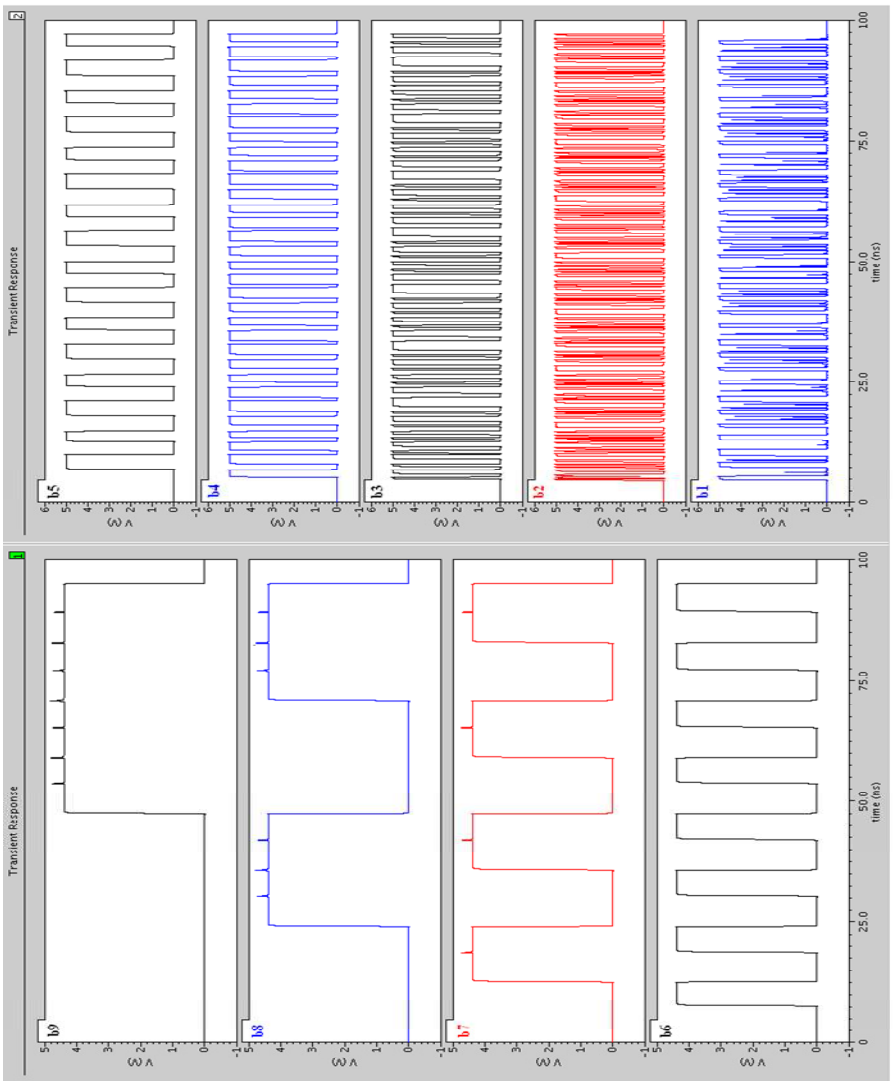

Figure 17. The binary output waveforms for the 9-bit folding and ınterpolation ADC (fin=10 MHz).

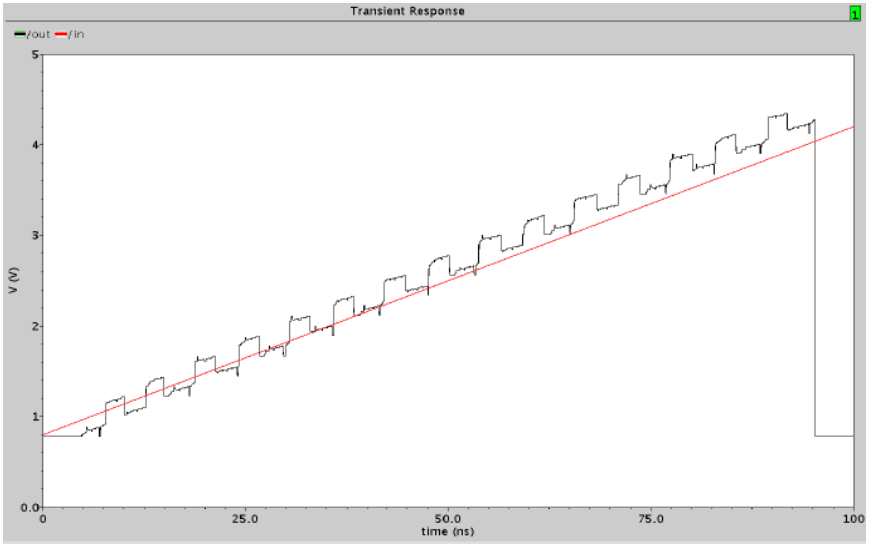

Figure 18. Ideal D/A converter response for fin=10 MHz.

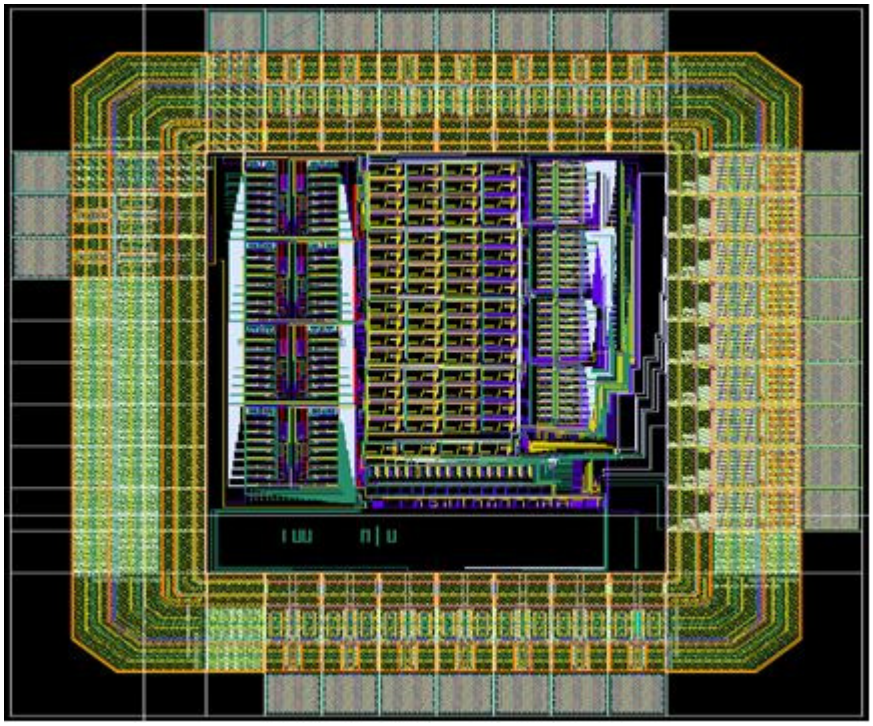

Figure 19. Layout photo of the complete converter.

A/D converter, respectively. The active layout area is only 0.65 mm^2.

Conclusıon

In this research, the TIQ method was employed in designing folding and ınterpolation type of CMOS ADCs. Although 9-bit resolution has not been chosen for this type of ADC architectures in the literature in general, the aim in this work was to succeed the design of a linear 9-bit TIQ based CMOS folding and interpolation ADC. However, the expected linearity measures were reached for the resolution level of 7-bits or below. The ADC performance summary is listed in Table 1. The designed converter was also fabricated through EUROPRACTICE.

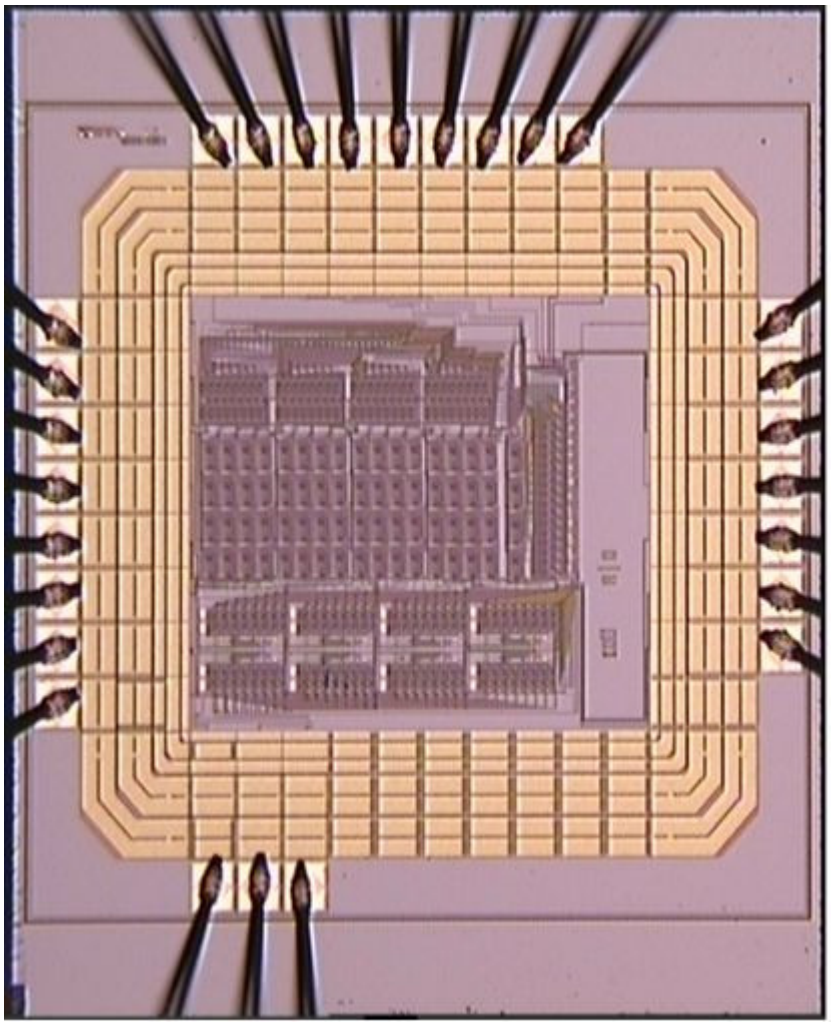

Figure 20. Die photo of the fabricated converter.

Table 1. ADC performance summary.

Technology		0.35 µm CMOS C35 AMS
Active layout area		0.65 mm^2
Resolution		9 bit
Power supply		5 V
Analog input range		3.8 V
Maximum power consumption		4.73 W
Sampling frequency		1GS/s
SFDR		57dB(Fin=1MHz)
SNDR		44.4dB(Fin=1MHz)
Linearity	DNL (LSB) (9bit/8bit/7bit)	2.9/ 1.2/0.9
	INL (LSB) (9bit/8bit/7bit)	6.3/3/0.9

The real test and measurement results have not been completed yet. However, they will be considered in an another publication in comparison with the simulation results. The research results shown that the linearity measures would gradually be lost for over 7-bits of resolution. Moreover, TIQ comparator could not be used

for the fine full-flash ADC core due to large input capacitance effect of the specific TIQ comparator. Therefore, a faster comparator circuit had to be chosen for the fine part design only. However, the TIQ technique can be chosen for the coarse part of the folding and interpolation ADCs up to 4-bits of resolution. Because, a highly linear (less than 0.2 LSB, DNL and INL) flash ADC core was accomplished for the coarse part of the designed ADC. If the resolution for the coarse part is chosen as 5-bits, then the design process of the fine part including analog preprocessing unit as well will become more complex and tedious since more number of folded signals will be needed in this case. Because, multiplication factor for input frequency becomes 32 rather than 16, which yields increased number of required folded analog input signals. Another important result observed here that the increased number of resistive interpolation yields increaed power consumption. That was unfortunately ineviatable in this work.

One final comment should be stated here that although the linearity measures are not satisfying for 9-bit case, the authors believe that this case study will serve as a preferred reference for the researchers who are willing to use TIQ technique in designing fast ADCs such as semi flash, folding and pipeline architectures.

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