

# Small Scale Integrated Technology for HTS RSFQ Circuits

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**Abstract**—A technology for fabrication of YBCO ramp junctions on a superconducting ground plane is developed and evaluated. The technology is based on a two-layer, S-I, structure or on a four-layer, S-I-S-I, structure grown in situ with YBCO superconductor and with multilayer insulator of PBCO/STO/PBCO. Ramps for junctions, via connections and crossovers are formed by Ar ion milling under rotation and the ramp angle is less than 30° for all directions. A 20-25 nm thick Ga-doped PBCO was used as a barrier for Josephson junctions. One additional YBCO layer, for junction top electrodes and wiring, is deposited and patterned. Surface roughness of multilayers is characterized by AFM and is related to the junction parameters. Transport properties of junctions, via connections and crossovers are evaluated.

**Index Terms**—High  $T_c$  superconductors, RSFQ circuits, ramp Josephson junctions, microstructure.

## I. INTRODUCTION

Rapid Single Flux Quantum (RSFQ) circuits implemented in high- $T_c$  superconductors (HTS) have the potential to perform at temperatures 20-40 K, as compared with that of Nb/NbN circuits at 4 K. The main obstacle in realization of such circuits is the lack of reproducible Josephson junctions (JJ) integrated in multilayer structures. Ramp-type Josephson junctions with artificial barrier [1] or with interface-

engineered ramp surface [2] are probably the best choice at present that allow such an integration. Both types of junctions are uniform and stable in time and demonstrate excellent characteristics. The interface-engineered junctions display so far lower spread in junction parameters,  $1\sigma$  less than 8% for 100 junctions at 4.2 K [3]. Their characteristics can be tuned, but not to the level of artificial barrier ramp junctions in which critical current densities of  $10^5$  A/cm<sup>2</sup> can be reached [4]. In addition, properties of ramp junctions are not influenced by the deposition of other layers at high temperatures and by intermediate plasma treatment during processing. The latter considerations motivate the choice of ramp junctions with artificial barrier for our HTS integrated technology. Fabrication ramp junctions and their transport properties are discussed in several articles [5]-[7]. An implementation of HTS RSFQ balanced comparator using directional ramp junctions with buried ground plane was recently reported [8]. The aim of this work is to develop a multilayer technology based on three superconducting layers and with all ramps in the circuit (for Josephson junctions, via connections and crossovers) formed under substrate rotation during the ion milling. This allows for positioning all circuit elements by will at any place on the chip.

Here we report on fabrication and properties of YBa<sub>2</sub>Cu<sub>3</sub>O<sub>7</sub> (YBCO) ramp-type JJ with barriers of PrBa<sub>2</sub>Cu<sub>2.6</sub>Ga<sub>0.4</sub>O<sub>7</sub> (PBCGO). The microstructure of the junctions is correlated with junction properties. The transport properties of vias and crossovers are evaluated.

## II. RAMP JOSEPHSON JUNCTIONS

Junction parameters are determined by the ramp roughness, barrier material and thickness, and by the insulator between the bottom and top electrodes. We have developed a process to produce smooth ramps in multilayers with ramp angles of 25-30°.

### A. Electrodes and insulation

Two-layer, S-I, and four-layer S-I-S-I, structures were grown in situ by pulsed laser deposition, where S is a 150 nm YBCO film and I denotes an insulator. The insulator itself consists of three layers: a 50 nm SrTiO<sub>3</sub> (STO) layer is stacked between two 50 nm PrBa<sub>2</sub>Cu<sub>3</sub>O<sub>x</sub> (PBCO) layers. The STO serves as a high resistive layer. The parasitic capacitance of the overlap area is also lower in comparison to 150 nm STO layer. The PBCO layer separates STO and YBCO layers and prevents oxygen depletion of the latter. All layers were grown at laser energy density of 1.5 J/cm<sup>2</sup> (KrF excimer laser), substrate temperature  $T_s$ =800 °C and at low

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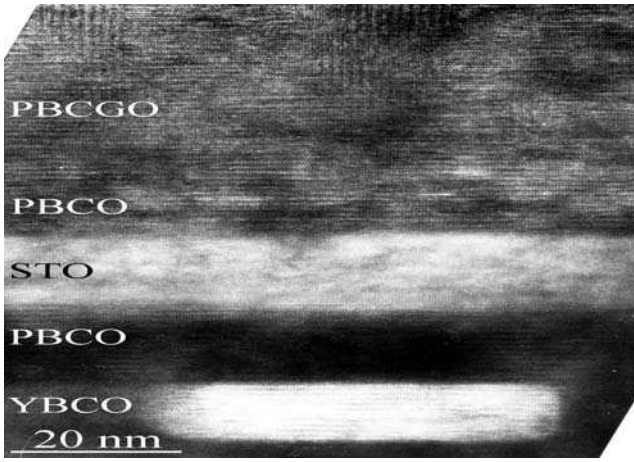


Figure 1. TEM image of a two layer S-I structure: a bottom YBCO electrode and PBCO/STO/PBCO insulator. The PBCGO barrier layer and the top YBCO electrode are grown after formation of the ramp.

oxygen pressure, 0.2 mbar, in order to obtain smooth films with low particle density. The roughness of the first YBCO layer determines the quality of the whole structure and all films were grown at optimal conditions resulting in an average roughness of 1.5 nm and a maximum peak-to-valley distance of 5 nm. To assure a good oxygenation the multilayers were grown by oxygen relaxation technique, after growing the S or I layer it was cooled to 400 °C and heated again to the deposition temperature of the next layer [9]. All materials have a very good match of lattice parameters and the interfaces are atomically smooth (Fig. 1). The multilayer surface was characterized by Atomic Force Microscopy (AFM). Two layer structures, superconducting ground plane and insulator, had an average roughness of 3 nm with maximum peak-to-valley distance of 8 nm. The corresponding numbers for the four layer structures were 4 nm and 15 nm (Fig. 2). The junction's barrier thickness was

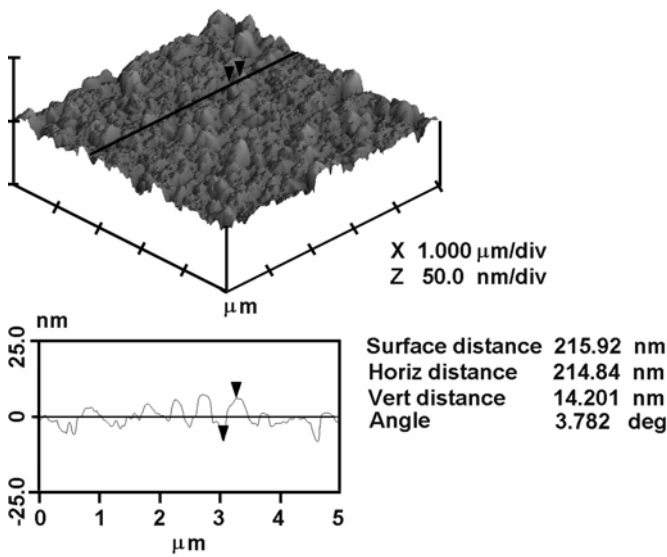


Fig. 2. AFM image and cross-section of a 4-layer S-I-S-I structure with a thickness of 150 nm for each layer. Note that the insulator is a multilayer itself, PBCO/STO/PBCO.

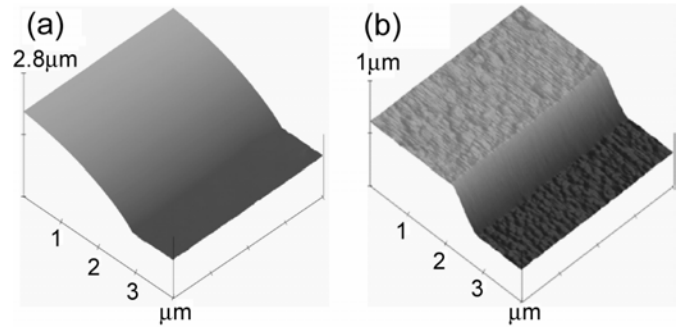


Fig. 3. AFM tapping mode images of the morphology of (a) a photoresist mask after a postbake at 120°C for 30 min, and (b) a uniform ramp after etching and annealing at 780°C and 0.2 mbar O<sub>2</sub> for 30 min.

chosen accordingly 20-25 nm in order to avoid superconducting shorts in it. The particle density was about  $10^5$  per cm<sup>2</sup> in both structures.

### B. Ramp formation

Ramps in YBCO-PBCO/STO/PBCO were formed by Ar ion milling at beam energy of 270 eV and beam current density of 0.2 mA/cm<sup>2</sup>. Smooth ramps with an angle of 25-29° to the substrate were formed only when a hard baked photoresist mask with gentle edges was used in combination with an etch angle of 45° normal to the rotating substrate. An AFM image of a photoresist mask on a multilayer structure is presented in Fig. 3a. The edge slope of the mask was about 40°. Ramp roughness determines the epitaxial growth of the barrier and correspondingly the barrier homogeneity. An AFM image of a ramp is presented in Fig. 3b. The ramp was prepared under the optimized processing conditions, specified above, and the typical ramp roughness after ion beam milling was 5 nm. However, it increased to 8-9 nm after annealing under conditions similar to that for the deposition of the barrier and top electrode.

### C. Microstructure of YBCO ramp Josephson junctions

The surface morphology of as-received film surfaces was studied by scanning electron microscopy in a JEOL JSM-6301F. Transmission electron microscopy (TEM) cross section samples were made by mechanical grinding, polishing and subsequent ion milling down to electron transparency. They were characterized in a Philips CM 200 with a Field Emission Gun and a Gatan Imaging Filter/EELS system.

TEM characterizations of ramp-junctions with low excess current showed a uniform barrier layer in the ramp-edge region. An overview of the ramp-edge region is seen in Fig. 4 and details of the junction area are seen in Fig. 5. The angle of the ion-milled edge was about 30°. The ramp was smooth and this promoted an epitaxial nucleation of PBCGO and a thin film evolution giving a uniform barrier thickness. The subsequent YBCO top layer grew epitaxially on top of the barrier provided that no secondary phases were present. The interface between the YBCO base layer and the barrier was easier to distinguish than the interface between barrier and

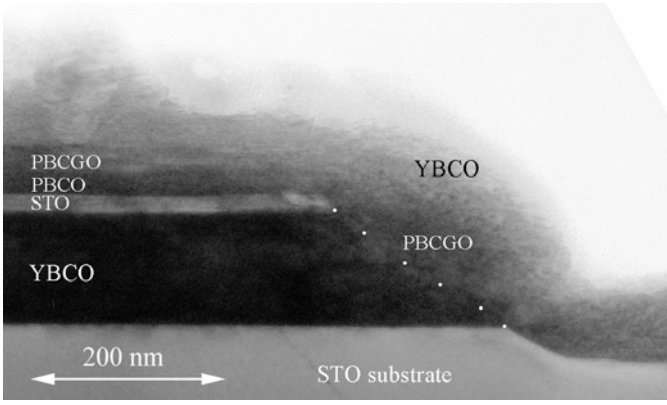


Fig. 4. A TEM micrograph showing an overview of the ramp-edge region. The visible interface between the bottom YBCO layer and the barrier layer is marked with white dots. The interface between the barrier layer and the top YBCO layer is not clearly distinguished due to a relatively large thickness of the TEM specimen. The micrograph was taken with the electron beam incident along the [100]STO.

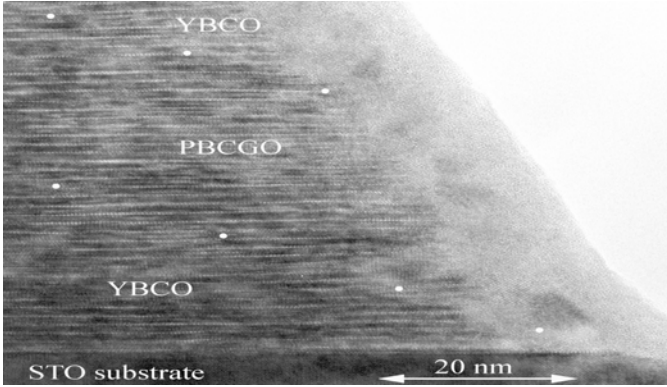


Fig. 5. A high-resolution TEM micrograph of the barrier layer in the junction area. The interfaces between the PBCGO layer and the base and the top layer are marked with white dots. A small particle is seen in the barrier layer close to the substrate surface. The [100]STO is parallel to the electron beam.

the top YBCO electrode. This was probably due to an increased amount of dislocations and stacking faults in the YBCO base layer due to the ion milling.

#### D. Superconducting transport of YBCO ramp Josephson junctions

Junctions with barrier thickness of 7-20 nm had a  $J_c$  of  $10^5$ – $10^4$  A/cm<sup>2</sup> and flux-flow-type  $I$ - $V$  curves. Some of the junctions with 15-20 nm thick barrier showed RSJ-like behavior with large excess current,  $I_{ex} \approx I_c$ . Here we report only on the properties of junctions with 25 nm thick barriers. 27 junctions of 44 in total were investigated. All junctions showed  $I$ - $V$  characteristics with RSJ behavior with negligible excess current, less than 10% of  $I_c$  as shown in Fig. 6a. The  $1\sigma$  spread in critical current density was less than 13 % (Fig. 6b). Such a spread in junction parameters allows for the design of RSFQ circuits with 20-40 junctions.

Keeping in mind that the roughness of the ramps was measured to be about 9 nm, it is clear that the supercurrent transport is determined by microshorts in the junctions with barrier thickness of less than 15 nm.

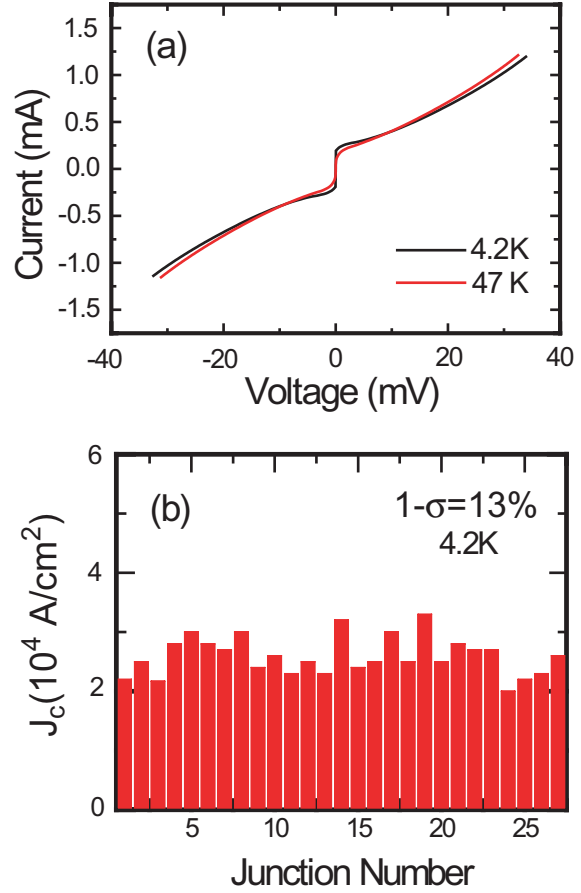


Fig. 6. (a) The  $I$ - $V$  curves of a 4  $\mu$ m wide YBCO ramp junction, (b) critical current density spread of YBCO ramp junctions with 25 nm thick PBCGO barrier.

#### E. Properties of YBCO ramp Josephson junctions

The conductance vs. voltage,  $G$ - $V$ , characteristics were measured for three junctions. A set of  $G$ - $V$  curves measured in the temperature range of 4-71 K is shown in Fig. 7. The shape of the conductance curves can be described by a  $G = AV^{4/3}$  dependence at high bias voltages, with  $A$  as a fitting parameter (Fig. 7). The latter dependence indicates that the normal transport is dominated by resonant tunneling through localized states in the PBCGO barrier. For all three junctions, pronounced peaks were observed in the  $G$ - $V$  dependencies and the positions of the peaks were well correlated in voltage scale. If we assume a superconducting gap of  $31 \pm 1$  meV, peaks can be identified at voltages corresponding to  $2\Delta/n$ , where  $n=1-4$ . Even though the peak near  $2\Delta/8$  was observed, the peaks at  $2\Delta/n$  ( $n=5, 6, 7$ ) were absent. The latter can be explained by the limited sensitivity of the measurement or by the limited resolution in the bias voltage. The results differ from the reported measurements on ramp junctions pointing on the presence of two gaps,  $\Delta_s=25$  meV and  $\Delta_n=16$  meV [10]. The well-pronounced subgap structure indicates that supercurrent transport is dominated by multiple Andreev reflections.

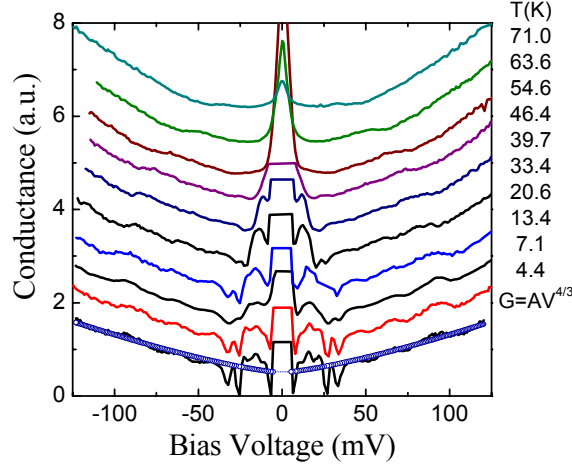


Fig. 7. Differential conductance vs. bias voltage of a 4  $\mu\text{m}$  wide YBCO ramp junction with a 25 nm thick PBCGO barrier at different temperatures. The conductance curve marked by open circles represents a fitted curve with  $G=AV^{4/3}$ . (The central peaks in the curves at temperatures lower than 55K have been removed. All the curves have been offset and rescaled for clarity.)

### III. CROSSOVERS AND VIAS

Crossovers are important elements of RSFQ circuit preparation. The PBCO/STO/PBCO insulator properties are excellent when separating two planar YBCO structures. PBCO/STO/PBCO epitaxial growth on a ramp is very critical to ramp angle and ramp roughness. A test structure with crossovers having the small overlap with the planar insulator, see Fig. 8, was prepared and studied. Transport properties of crossovers with widths ranging from 4 to 20  $\mu\text{m}$  were evaluated. Crossovers with dimensions 4 and 8  $\mu\text{m}$  were highly resistive with resistivities of 2-10  $\Omega\cdot\text{cm}$ . In the case of 12-20  $\mu\text{m}$  wide crossovers a critical current of a few  $\mu\text{A}$  was measured. This result restricts our wiring strips to the size of 8  $\mu\text{m}$ .

A typical size of via connections on the test chip was  $48 \times 62 \mu\text{m}^2$ . Vias were prepared by over etching the insulator assuring an a-b contact between both YBCO layers. AFM inspection of vias confirmed the low angle of the ramp. A high critical current density can be expected because of the transport in a-b plane although the vias were never tested at high current densities. Critical currents of 1-5 mA were measured and such values are enough for most HTS RSFQ circuits with 20-40 junctions.

### IV. SUMMARY

A technology for preparation of YBCO ramp-type JJs with PBCGO barriers has been developed. An optimal thickness of the junction barrier was found to be about 25 nm and  $I_c R_n$ s of the JJs were about 4 mV at 4.2 K and 2 mV at 40 K. The  $I/\sigma$  spread in  $I_c$  was less than 13%. An implementation of a balanced comparator for an RSFQ oversampling Analog-to-digital converter is in progress.

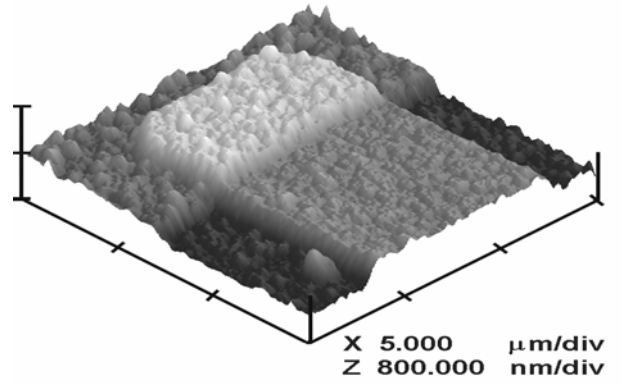


Fig. 8. AFM image of a 8  $\mu\text{m}$  YBCO strip over a 30° ramp in YBCO covered by 150 nm thick PBCO/STO/PBCO insulator.

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