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Overdamped Josephson junctions for digital applications

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ABSTRACT

An interesting feature of Superconductor–Normal metal–Superconductor Josephson junctions for digital applications is due to their non-hysteretic current–voltage characteristics in a broad temperature range below T_c. This allows to design Single-Flux-Quantum (SFQ) cells without the need of external shunts. Two advantages can be drawn from this property: first the SFQ cells can be more compact which leads to a more integrated solution towards nano-devices and more complex circuits; second the absence of electrical parasitic elements associated with the wiring of resistors external to the Josephson junctions increases the performance of SFQ circuits, in particular regarding the ultimate speed of operation. For this purpose Superconductor–Normal metal–Insulator–Superconductor Nb/Al–AlO_x/Nb Josephson junctions have been recently developed at INRiM with aluminum layer thicknesses between 30 and 100 nm. They exhibit non-hysteretic current–voltage characteristics with I_cR_n values higher than 0.5 mV in a broad temperature range and optimal Stewart McCumber parameters at 4.2 K for RSFQ applications. The main features of obtained SNIS junctions regarding digital applications are presented.

1. Introduction

Josephson junctions have been widely used since several decades in different applications whenever ultimate sensitivity or, more generally, performance, is required. This is the case for instance for heterodyne mixers in the millimeter and submillimeter range [1,2] where Josephson junctions act as a non-linear analog device. Josephson junctions are also used in digital mode in the so-called energy-efficient superconductive digital electronics, or Rapid-Single-Flux-Quantum (RSFQ) electronics [3,4], used to process signals at very high clock rates, in the 100 GHz range, with very low power consumption at least 100,000 times lower than its semiconductive counterpart. So far such analog or digital electronics makes use of low-T_c superconductors based more often on Superconductor–Insulator–Superconductor (SIS) Nb/Al–AlO_x/Nb junctions operating at liquid helium temperature, but also sometimes on NbN/MgO/NbN [5–7] or NbN/AlN/NbN [8–10] SIS junctions. This last choice based on the NbN superconductor is motivated by the need to work at slightly higher temperature (around 10 K) to reduce the overall cost associated with cryogenic cooling. For digital applications, where non-hysteretic current–voltage characteristics are necessary for operation [3], a resistive shunt is added in parallel with each SIS Josephson junction. Though this technique is widely used, including for the most complex circuits [4] that can comprise more than 10,000 devices with current densities of around 10 kA/cm^2 [11], it limits the ultimate integration of the technology as the wiring of the parallel resistor occupies typically an area of four times the junction area. It also adds some parasitic inductance that limits the ultimate switching frequency of the shunted device [12]. To bring a solution, self-shunted Josephson junctions, for which the tunnel barrier is resistive, are an attractive alternative, also of interest for future ac voltage standards. Several solutions have been used in the past based on NbN/TiN/NbN, NbN/TiS_2/NbN, NbN/TaN/NbN or NbN/NbN_x/NbN Superconductor–Normal metal–Superconductor (SNS) junctions [13–18]. Some junctions like the ones based on TaN material placed at the limit of the metal–insulator transition, are currently studied to evaluate their reproducibility for complex circuits since they have the advantage to operate in the 10 K temperature range [16]. Another alternative was based on Superconductor–Insulator–Normal metal–Insulator–Superconductor (SINIS) junctions [19,20] that led to circuits with several thousands Josephson junctions. Nevertheless the characteristic voltage of these junctions is not high enough for future digital circuits. Another alternative solution, that has the advantage to operate at and over 10 K, consists of using junctions based on NbN, namely NbN/Nb/AlO_x/(Nb)/NbN Superconductor–Normal metal–Insulator–Normal metal–Superconductor (SNINS) junctions [21–23]. In this case the thickness of the niobium layer is of particular importance and allows to tune

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the properties of the junction by modifying the proximity effect at the NbN/Nb interface. Critical voltages in the 0.5 mV range suitable for SFQ applications have been successfully obtained above 10 K with a reasonable reproducibility [23]. At last, more recently, another approach was proposed, it is based on the replacement on the aluminum oxide insulating barrier of niobium junctions by a poor conductor at the limit of the metal–insulator transition, namely NbSi [24,25], resulting in self-shunted SNS junctions. It led to the successful test of the first digital circuits with such a technology [26]. In this work we propose an alternative process based on Superconductor–Normal metal–Insulator–Superconductor (SNIS) where the normal metal is an aluminum layer with increased thickness compared to the one of SIS and SNINS junctions, and the insulator is the usual aluminum oxide. This process combines the reproducibility of unshunted technological processes with the possibility to operate at temperatures higher than 4.2 K, resulting from the proper engineering of the barrier properties at the desired temperature, located in the 5–8 K range. It is interesting to note that some similar properties can be observed between the presently studied SNIS junctions and the SNINS junctions of [23], while the respective thicknesses of the normal metal layer and of the insulator are different: the SNIS junctions have a thick normal layer and a very thin insulator while the SNINS junctions have a thin normal metal layer and a thicker insulating barrier. Although the junctions are of different nature, it may be representative of a similar universal behavior for tunneling through oxide barrier [27].

2. Technological process for SNIS junctions

The overdamped Nb/Al–AlO_x/Nb SNIS Josephson junctions have been recently developed at INRIM and exhibit high values of critical current density and characteristic voltage, making them appealing both for metrology and digital electronics.

SNIS Josephson junctions are fabricated starting from the well-known SIS trilayer process [28] by oxidizing in situ, without breaking the vacuum, the aluminum barrier in pure oxygen. The thickness of the aluminum metal layer and the oxidation time, properly trimmed, are able to determine the peculiar internal shunt of a SNIS junction and a transition from a hysteretic to a non-hysteretic current–voltage I–V characteristics. This transition has been also observed by increasing the temperature of operation [29,30].

SNIS junctions can be fabricated by varying a wide range of electrical parameters, showing critical current density values J_c from less than 1 kA/cm^2 up to 100 kA/cm^2. The critical voltage $V_c = I_c R_n$, with I_c, the super-current and R_n, the normal-state resistance of the junction, can be easily tuned from 0.1 to 0.7 mV at 4.2 K, for a typical SNIS junction of 5 × 5 μm^2 size realized by optical lithography.

Satisfying the demand of reducing Josephson junction dimensions down to sub-micron scale, necessary for proper operation of superconducting digital devices when current densities are higher, recent results have been obtained concerning the realization of sub-micron SNIS junctions [31], as shown in Fig. 1. The effective area has been defined exploiting a nanolithographic technique based on Electron Beam Lithography (EBL) by using a FEI Quanta 3D ESEM FEG equipped with a J.C. Nabity NPGS pattern generator. A proper scaling of junction current densities has been observed and quantized Shapiro steps have been measured at 4.2 K (left inset in Fig. 1), but also at temperatures of about 7 K, confirming the interest to be employed at temperature above 4.2 K in a cryocooler set up. The left inset of Fig. 1 exhibits also a step around 50 μV, symmetric with respect to zero voltage. It appears in other similar small junctions with radiation at the same microwave frequency. It seems to be a fractional (1/3) step,

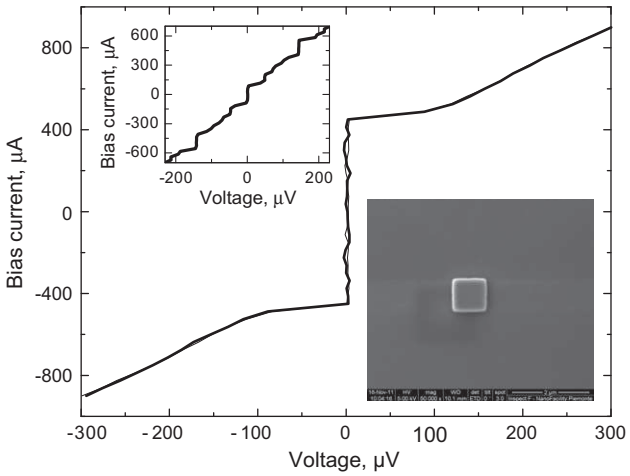

Fig. 1. Representative current–voltage characteristics of a 0.65 μm^2 area Nb/Al–AlO_x/Nb junction measured at 4.2 K (main panel). The effect of a 69 GHz microwave radiation is shown in the left inset. The right inset is a scanning electron micrograph of the device.

likely related to the structure of the junction. It is not unusual in metallic barrier junctions [32]. The critical current vs magnetic field dependence has also been measured and can be totally suppressed for particular values of the magnetic field [31]. The reproducibility of the critical current of 5 × 5 μm^2 SNIS junctions is of the order of 5–10% (see more in Table I of [33]). We are studying how to extend these results for submicron junctions. Applications of such SNIS devices for digital RSFQ circuits require the reduction of sizes of junctions in the 1-μm size range [31] in order to be able to produce junctions with critical currents in the 100–300 μA range. Moreover, it is necessary to develop a multilayer technology with a ground plane in order to guide on the circuit voltage pulses produced by self-shunted Josephson junctions. As a result circuits with self-shunted SNIS junctions can be operated either at 4.2 K with a typical characteristic voltage of 0.55 mV, but also at about 6–7 K with a reduced critical voltage in the 0.3 mV range. The expected performance in this last case is the one of an RSFQ process based on process with current densities of 1 kA/cm^2, with the advantage of a higher temperature that relaxes the cryogenic constraint for specific applications. In all cases the Stewart-McCumber parameter stays in the ideal range, comprised between 1 and 3.

3. Specific capacitance, critical voltage and McCumber parameter of self-shunted Josephson junctions

Digital superconductive electronics circuits are usually designed so the current–voltage characteristics is non-hysteretic while the critical voltage is maximal. This corresponds to a Stewart-McCumber parameter β_c found experimentally in the range of 1–3 [33]; this range is optimum for RSFQ electronics applications. To this regard, the value of the intrinsic capacitance plays a major role, since a too high value reduces the ultimate critical voltage, hence reduces the ultimate speed of the circuit. Several SNIS junctions have been resonated with a parallel inductive stub in order to determine this capacitance, which has been found to be in the range of 180–480 fF/μm^2 [33]. The lowest values have been found for a temperature of 4.2 K and are about a factor of 3 higher than the ones of Nb/Al–AlO_x/Nb SIS junctions. Nevertheless, critical current densities of SNIS junctions can be higher, as mentioned in the former paragraph, than the ones of SIS junctions. This counterbalances the capacitance trend. As a result the critical voltage can reach 0.55–0.7 mV [33] that corresponds to the state-of-the-art

for externally shunted technological processes [11], without the need of external shunts.

4. Influence of temperature

An interesting feature of the SNIS junctions is their ability to still present good performance when temperature is increased up to 7–8 K. Conventional SIS junctions show a sharp decrement of the electrical parameters above 4.2 K, associated to a strong temperature dependence, which comes from a steep behavior of the $I_c(T)$ curve above $0.5T_c$ in the Ambegaokar-Baratoff theory, where T_c is the critical temperature of the superconducting film. The replacement of the bottom superconducting electrode by an S/N bilayer leads to a more gentle curve in this temperature interval [34], as seen in Fig. 2. The origin of such behavior comes from the well-known fact that, if electronic parameters of the two layers are comparable as well as their thicknesses d_N and d_S, at temperatures much lower than T_c the superconducting order parameter in an N layer very rapidly decreases with temperature increase while, at T intermediate between zero and T_c becomes flat up to a nearest vicinity of T_c [35,36]. Variation of the ratio d_N/d_S leads to the possibility of engineering the thermal stability of Josephson SNIS devices.

Let us show it in a more quantified way. In [34] we have applied a general model from Kupriyanov et al. [37] for double-barrier Josephson devices to interpret the data for Nb/Al–AlO_x/Nb junctions. In contrast to the cases discussed in [37], our system is very asymmetric where the resistance of the insulating AlO_x layer strongly exceeds that of the Nb/Al interface $R_{Nb/Al}$. If so, the main equations of the theory [37] can be radically simplified (see in detail [34]) with the only fitting parameter $\gamma_{eff} \approx \gamma_{S/N} d_{Al}/\xi^*_{Al}$, where $\gamma_{S/N} = R_{Nb/Al}/\rho_{Al}\xi^*_{Al}$, $\xi^*_{Al} = \xi_{Al}\sqrt{T_{c,Al}/T_{c,Nb}}$, ρ_{Al} and ξ_{Al} are the normal-state resistivity and the superconducting coherence length of Al, respectively. It is important that in a layer configuration ξ_{Al} differs from the corresponding value in a bulk material ξ^{bulk}_{Al} and is a function of the mean free path l_{Al} in the film. The analytical dependence on l_{Al} is principally different in clean and dirty limits [36]. Whereas in the first case $\xi_{Al} = \xi^{bulk}_{Al} l_{Al}/(\xi^{bulk}_{Al} + l_{Al})$, for another extreme situation, when $l_{Al} \ll \xi_{Al}$, one finds $\xi_{Al} = \sqrt{\xi^{bulk}_{Al} l_{Al}/3}$. Unfortunately, our Al films are in the intermediate state (as it follows, for example, from an empirical formula $l_{Al} = 0.84d_{Al} - 0.00276d^2_{Al}$ obtained in [38] for Al layers similar to ours). What we do expect is that for the thinnest films the dependence of γ_{eff} on l_{Al} should be more similar to the clean case, when it is a linear function $\gamma_{eff} \approx \frac{R_{Nb/Al}}{\rho_{Al}\left(\xi^{bulk}_{Al}\sqrt{T_{c,Al}/T_{c,Nb}}\right)^2} d_{Al}$, whereas for those with d_{Al} above 100 nm it will follow the dirty-limit case $\gamma_{eff} \approx \frac{3R_{Nb/Al}}{(\rho_{Al}l_{Al})\xi^{bulk}_{Al}(T_{c,Al}/T_{c,Nb})} d_{Al}$. Taking into account that the product $\rho_{Al}l_{Al}$ is a material constant, we again obtain a linear dependence but with a larger coefficient (since for Al $\xi^{bulk}_{Al} \gg l_{Al}$). Thus, for the studied range of Al-film thicknesses from 40 to 120 nm we have to observe $\gamma_{eff} \propto d_{Al}$ behavior at lowest and highest values of d_{Al} with a transition from a slow increase in the lowest d_{Al} samples to a relatively steep behavior at $d_{Al} > 100$ nm. And it is just what can be seen from the polynomial fit to the experimental γ_{eff} vs d_{Al} dependence [34, Table 1], shown in the inset in Fig. 2. We notice that this curve can be used to link experimental measurements for a certain Al-film thickness with theoretical calculations using the parameter γ_{eff}.

In Fig. 2 we demonstrate how the shape of the normalized temperature dependence of the critical voltage $V_c = I_cR_n$ is influenced by the Al-film thickness. The $V_c(T)$ values calculated along the lines of [34] are definitely suppressed with increase of d_{Al} but at the same time the $V_c(T)$ curve is flatter above $0.5T_c$. The modification of d_{Al}, resulting in a change of γ_{eff}, provides the possibility to find a compromise between the two factors and optimize the SNIS junction's operation.

5. Sensitivity of a Josephson junction comparator

In order to estimate the performance of this technology for digital operation we estimated the gray zone of a Josephson balanced comparator [39] as a function of the clock frequency. This device is the most crucial one for digitization of analog signals at ultrafast rates. We used two configurations, respectively at the temperature of operation of 4.2 K with an I_cR_n product of 0.7 mV and at a temperature of 7 K with an I_cR_n product of 0.3 mV. In both cases the McCumber parameter was $\beta_c = 2$. For each configuration, the Josephson junction parameters, as well as the inductances, were optimized for the temperature of operation. As a first realistic approach, the resistively-and-capacitively shunted junction (RCSJ) model has been used for considering the dynamics of the comparator. The temperature was taken into account through the shot noise of the shunt resistors. Fig. 3 presents the gray zone width

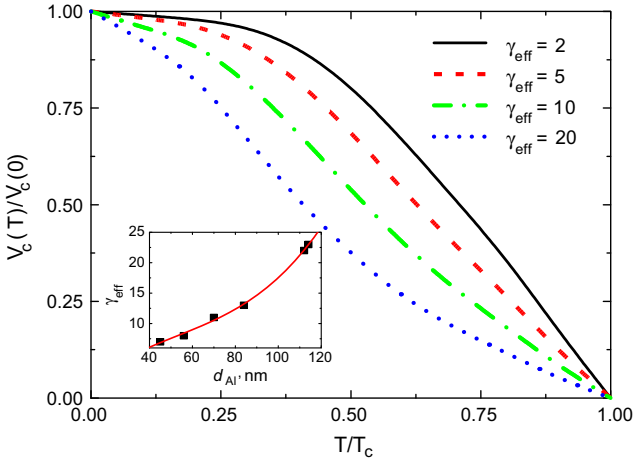

Fig. 2. Theoretical values for the normalized critical voltage vs the normalized temperature in Nb/Al–AlO_x/Nb SNIS junctions. The curves show the influence of the parameter γ_{eff} on the shape of $V_c(T)$ curves. The dependence of the γ_{eff} parameter on the Al-interlayer thickness d_{Al} is shown in the inset, where the solid line is a polynomial fit to the data (symbols) obtained in [34].

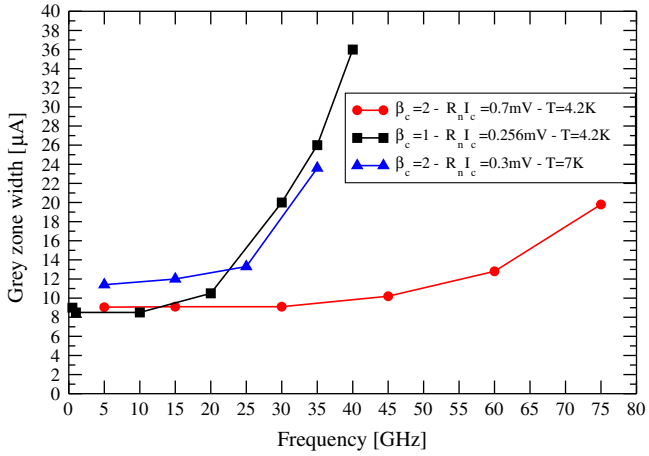

Fig. 3. Sensitivity of a balanced comparator as a function of the clock frequency. Two configurations have been studied with a McCumber parameter of 2: at 4.2 K with a critical voltage $V_c = 0.7$ mV and at 7 K with $V_c = 0.3$ mV. A similar balanced comparator based on the FLUXONICS Foundry technology [40] is presented as a reference.

of the input signal current for the two configurations. Also shown is the performance of a similar comparator based on externally-shunted 1 kA/cm^2 current density Josephson junctions at 4.2 K with an I_cR_n product of 0.26 mV, corresponding to the European FLUXONICS Foundry parameters [40]. As expected the frequency range of operation is higher at 4.2 K due to the higher critical voltage. For such a comparator, the smallest junction has a critical current of 150 μA that can be achieved with a 1 μm^2 Josephson junction with a critical current density of 15 kA/cm^2 that is well inside the accessible range of current density values. More importantly the performances that are expected at 7 K, associated with a relaxed cryogenic environment, are quite acceptable for many applications that do not require to sample above 20 GHz, like digital magnetometry.

6. Conclusion

Sub-micron SNIS junctions have been studied from a theoretical and experimental point of view. It is shown that their properties, in particular the dependence of the parameters as a function of temperature, are adequate and of interest for applications in digital electronics, including voltage standards, with a relaxed cryogenic environment in some cases. A technological process including more layers is under development to address the specific requirements of superconducting digital electronics applications, like magnetometry and fast signal processing.

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