Self-shunted Nb/AlO_x/Nb Josephson junctions

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***Abstract*—We describe the fabrication and properties of high critical current density (J_c) Nb/AlO_x/Nb Josephson junctions with deep-submicron dimensions. The junctions are fabricated using a planarized process in which all levels are patterned using a combination of optical and electron beam lithography. The base and counter electrodes are defined by reactive ion etching using quartz etch masks to give a minimum feature size of 0.2 microns. For J_c = 2.1 mA/μm^2 and junction area less than 0.1 μm^2 the devices are self-shunted and exhibit nonhysteretic *I-V* characteristics. A small hysteresis in the larger junctions is caused by heating in the electrodes.**

I. Introduction

Most of the applications of the Josephson effect in superconducting electronics such as SQUID based magnetic sensors, Josephson integrated circuits (ICs) (e.g., digital devices based on rapid single-flux-quantum (RSFQ) logic [1]), array oscillators [2],[3], and voltage standards [4] require Josephson junctions with nonhysteretic *I-V* characteristics. In present day Nb/AlO_x/Nb technology, the intrinsically hysteretic (underdamped) tunnel junctions are shunted by normal metal resistors (so called resistively shunted junctions, RSJ) to achieve overdamped junctions. From a fabrication point of view, making RSJ has certain drawbacks as it involves additional processing for the resistors, via holes, and wiring. This increases the effective area of the junctions and restricts the level of integration in circuits. For certain high-frequency applications the parasitic inductance of the shunt resistor can cause degradation in performance [3]. The use of intrinsically overdamped or self-shunted junctions would then be desirable for IC applications.

Recently overdamped junctions made from double barriers of the type Nb/AlO_x/Al/AlO_x/Nb were reported [5],[6]. These devices show good Josephson behavior and have larger characteristic voltages $V_c = I_cR_N$ than superconductor-normal metal-superconductor (SNS) type junctions [7] . Here I_c is the critical current and R_N is the normal state resistance of the junction. However, the V_c values obtained (~ 0.24 mV) were still much smaller than the intrinsic value for Nb/AlO_x/Nb junctions (~ 2 mV), which would severely limit the high-frequency performance of the junctions since the response time in the overdamped regime scales inversely as V_c. Also, because of the double barrier, these devices have an inherently low critical current density J_c.

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The J_c of Josephson junctions imposes a restriction on the maximum integration level in ICs , since the I_c of the junctions is usually fixed by design considerations. Therefore, increasing J_c would allow reduction of device size. The maximum speed of devices based on RSFQ logic scales roughly as square-root of J_c [1] and hence, for a fixed I_c, as inverse square-root of device area. Also the white noise limited sensitivity of a SQUID [8] improves with increasing J_c, so does the maximum power generated in array oscillators. The issue of nonhysteretic *I-V* characteristics is also directly related to J_c. Indeed, the McCumber parameter $\beta_c = 2\pi(I_cR_N)^2C_s/(\Phi_0 J_c)$ characterizing the hysteresis decreases with increasing J_c so far as the I_cR_N product remains unaffected. Here C_s is the specific capacitance of the junction and Φ_0 is the flux quantum. Thus junctions with high enough J_c can be intrinsically overdamped ($\beta_c < 1$) and would offer significant improvement in device performance. Nb trilayer based Josephson junctions with J_c as high as 4 mA/μm^2 [9] and with deep-submicron dimensions [10] have been demonstrated. But even at $J_c > 3$ mA/μm^2, these devices showed some residual hysteresis. Two possible reasons for this are heating in the electrodes due to the high currents involved and parasitic capacitance contributing to increase in β_c.

II. Fabrication

In order to increase the flexibility of our implementation [11] of the PARTS process [12] for deep-submicron circuits, we have further developed the process to permit patterning by both electron beam lithography (EBL) and photolithography in all layers. This allows us, for example, to reduce the area of the base electrode (BE) and thus the BE – wiring layer overlap which is the primary cause of parasitic capacitance. In addition to the present work, this EBL PARTS process has also enabled our group to make simple RSFQ circuits that operate to 750 GHz [13] as well as high-quality single electron transistors (SET). The SET results [14],[15], in particular, illustrate the capabilities of the process which has been used to fabricate Nb trilayer transistors having high quality junctions with areas down to 0.01 μm^2. These transistors have modulation amplitudes of up to 60 μV and a noise performance comparable to the standard Al junction transistors.

The fabrication process flow is shown in Fig.1. A Nb/AlO_x/Nb trilayer is deposited on a 50 mm diameter oxidized Si wafer in a cryopumped system with both Nb and Al films DC magnetron sputtered. The base electrode (BE) and counter electrode (CE) are 150 nm thick and the Al interlayer is ~ 8 nm thick. The J_c is controlled by the O_2 exposure (pressure×time) during oxidation of the Al interlayer. For the

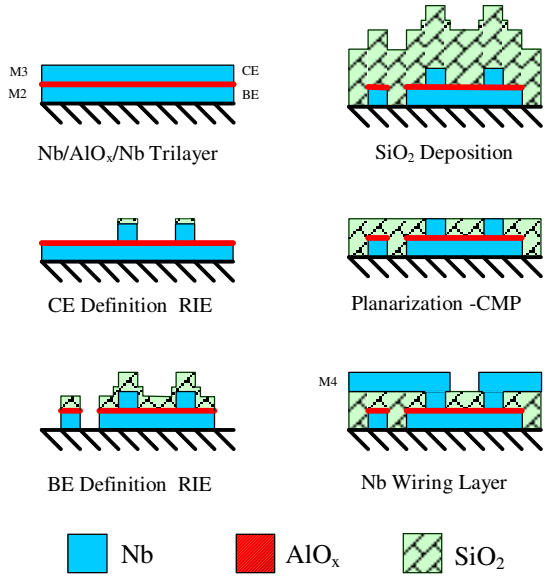

Fig. 1. Process flow for the fabrication of deep-submicron junctions using EBL patterned quartz etch masks and chemical mechanical polishing.

range of high J_c explored (60 μA/μm^2 - 2.5 mA/μm^2) in our experiments, the dependence of J_c on O_2 exposure is in good agreement with [9]. Accordingly, oxidation at 1.0 mTorr of O_2 for 10 min. gave a J_c of 2.1 mA/μm^2. PMMA / P(MMA/MAA) bilayers were used as both EBL resist and DUV resist for contact printing for all layers. A 50 nm thick layer of RF-sputtered SiO_2 (quartz) is lifted off to form an etch mask for the CE. The junction is then defined by a reactive ion etch (RIE) of the Nb CE in SF_6 plasma. Although the Al interlayer acts as a natural etch stop, the precise termination of the etch is critical for obtaining deep-submicron features and is achieved by using an optical end point detector based on measurement of the intensity of certain fluorine lines. A 120 nm quartz etch mask is then lifted off for the BE, which gets defined by a wet etch of the Al interlayer followed by another RIE of the Nb base layer. 550 nm of quartz is then deposited to form the dielectric layer which is planarized using a chemical-mechanical polish (CMP) step [16]. The residual 5-10 nm of quartz remaining after planarization on top of the CE is removed using a CHF_3 + O_2 oxide etch which exposes the top of the junctions. Finally a 200 nm thick Nb wiring layer is lifted off. If required, resistor levels and a contact via level can be added before the wiring layer.

III. Device Characteristics

The results are presented for a J_c = 2.1 mA/μm^2 wafer. The designed junction area ranged from 0.02 μm^2 to 4 μm^2. More than 50 SQUIDs and 200 single junctions have been measured. The yield was greater than 95% for devices 0.04 μm^2 and larger. The *I-V* characteristic of a single junction of 0.04 μm^2 designed area is shown in Fig. 2. The scaling of I_c with designed area for some 40 junctions on one chip at 4.2 K is shown in Fig. 3. The total spread of I_c at 4.2 K across the

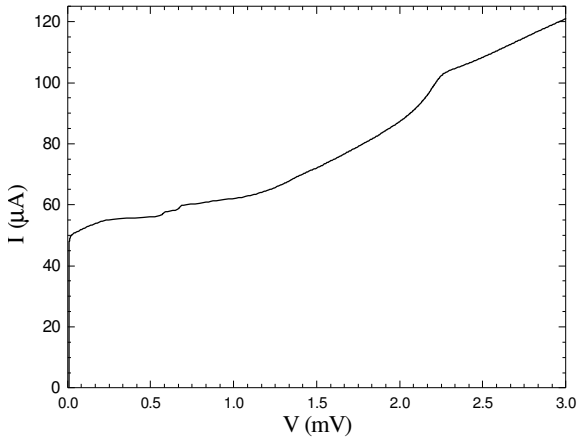

Fig. 2. The *I-V* characteristics of a 0.2 μm × 0.2 μm junction at T = 4.2 K.

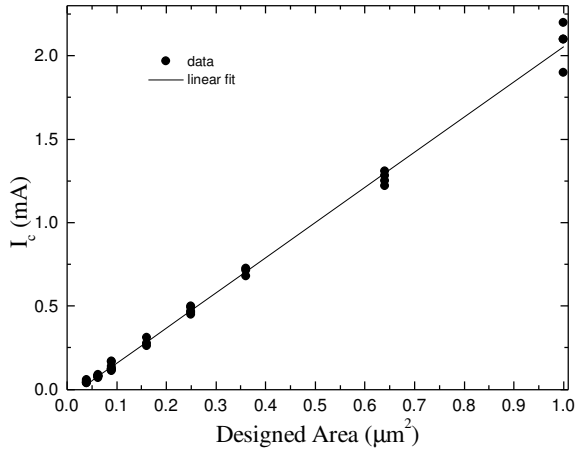

Fig. 3. Critical current scaling for 41 junctions on the same 0.7 mm square chip at T = 4.2 K.

wafer was less than 20% for all areas. R_N was measured at low voltages just below the critical temperature T_c of the electrodes. The measured I_cR_N product was 2.0 mV with less than 20% spread for all areas. C_s was estimated as ~ 90 fF/μm^2 from *LC* resonance in SQUIDs fabricated on the same wafer. The uncertainty in this estimate is no better than 40%, due to the finite width of the resonance steps and uncertainty in the SQUID inductance. The main contribution to the parasitic capacitance (C_p) of the devices is the overlap capacitance between the BE and wiring layer. The ratio C_j/C_p , where C_j is the junction capacitance, is the smallest for the smallest device area since the overlap area is set by fabrication constraints. For 0.04 μm^2 junctions the BE was 0.8 μm wide and the overlap area was 0.6 μm^2. Using a simple parallel plate formula with quartz as the dielectric, gives C_p = 0.16 fF and C_j/C_p = 22. Neglecting parasitic capacitance, we get β_c = 0.6.

All devices smaller than 0.1 μm^2 were found to be self-shunted at 4.2 K and showed no measurable hysteresis. However, larger devices showed a noticeable hysteresis which increased with device area (or I_c). The quantity (I_c I_r)/I_c which serves as a measure of the hysteresis, increases from

2% for 0.25 μm^2 junctions to 22% for 1 μm^2 junctions. Here I_r is the retrapping current. On lowering the temperature, this hysteresis becomes smaller (at 1.8 K , it is 14% for 1 μm^2 junctions), which indicates heating in the electrodes as the likely cause of hysteresis.

The quasiparticle *I-V* characteristic for a 0.5 μm×0.5 μm and 1.0 μm×1.0 μm junctions at 1.8 K are shown in Fig. 4a. A small magnetic field is applied parallel to the plane of the junctions to suppress the Josephson current. The ratio of the subgap resistance to the normal state resistance R_j/R_N is ~ 1. It is known that transport in the subgap region of high J_c junctions is dominated by processes involving multiple Andreev reflections (MAR) [17]. Since at these high J_c's the oxide barrier is only one or two monolayers thick on average, there exists a large number of atomic scale shorts beween the superconducting electrodes. As the dimensions of these shorts are much smaller than the coherence length ξ (~ 38 nm for Nb) and the electron mean free path in the electrodes, each of these "microshorts" or "pinholes" acts as a single ballistic channel for quasiparticle transport [18]. MAR, the mechanism responsible for transport in these microshorts, manifests themselves as peaks in the dynamic conductance at voltages equal to 2Δ/n , where Δ is the temperature dependent superconducting gap in the electrodes and n is an integer. The dynamic conductance ($G_D = dI/dV$) showing the MAR peaks for the two devices is plotted in Fig. 4b. The positions of these MAR peaks are plotted in Fig. 4c. The effect of heating in the electrodes is clearly seen as suppression of Δ at higher voltages. The zero voltage singularity in the dynamic conductance follows a power law $G_D(V) \propto 1/V^{\alpha}$, with the exponent α ranging from 0.6 to 0.8, which differs somewhat from the theoretically predicted value of 0.5 [19]. This deviation and spread in the measured value of α could be due to the Josephson current not being completely suppressed. A detailed analysis will be presented elsewhere.

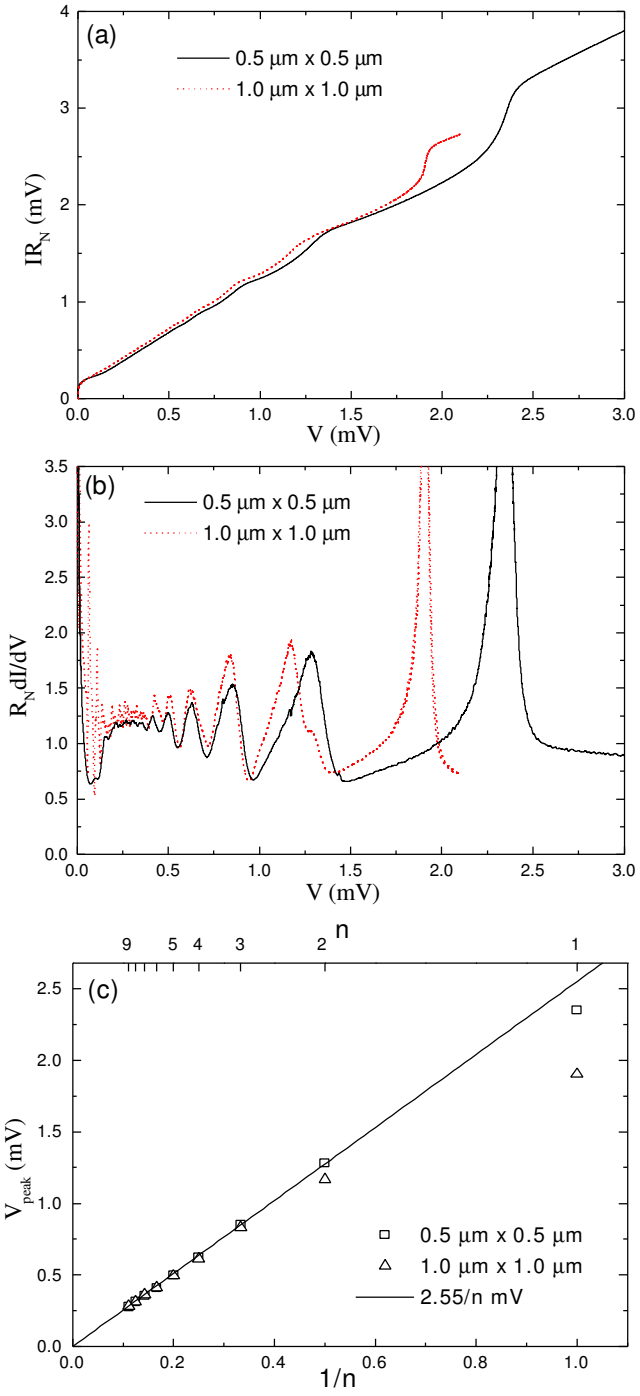

Fig. 4. (a) The quasiparticle *I-V* characteristics of a 0.25 μm^2 (solid line) and 1.0 μm^2 (dashed line) junctions at T = 1.8 K; (b) the dynamic conductances of the same junctions at T = 1.8 K; (c) the locations of the MAR peaks as a function of the reflection order n. The solid line represents the predicted dependence 2Δ/n for 2Δ = 2.55 mV.

IV. Applications

Fig. 5 shows the *I-V* characteristic of a dc SQUID fabricated on the same wafer. Flux is coupled into the SQUID loop by passing a current trough a modulation coil surrounding the SQUID loop. A current of 1.65 mA in the modulation coil injects one flux quantum Φ_0 in the SQUID loop. The inset in Fig. 5 shows the voltage modulation of the SQUID at a bias current I_B of 276 μA. The maximum voltage-to-flux transfer is ~1 mV/Φ_0 . The noise performance of these devices will be presented elsewhere.

Achieving higher operating speeds through better device integration for digital RSFQ circuits was one of the principle motivations for developing high J_c self-shunted junctions. For technology evaluation, superconducting frequency dividers based on the RSFQ T-Flip Flop were designed and fabricated using self-shunted Josephson junctions [13]. These devices, consisted of 8 junctions with a minimum dimension less than 0.1 μm^2 . The operating speed in these TFFs is indicated by the maximum frequency for which accurate frequency division is possible, f_{max}. A f_{max} of 770 GHz was achieved at 4.2 K for a J_c of 2.5 mA/μm^2.

As noted, the parasitic inductance of shunt resistors limits the high frequency and high power performance of Josephson effect array oscillators. The nonhysteretic junctions described

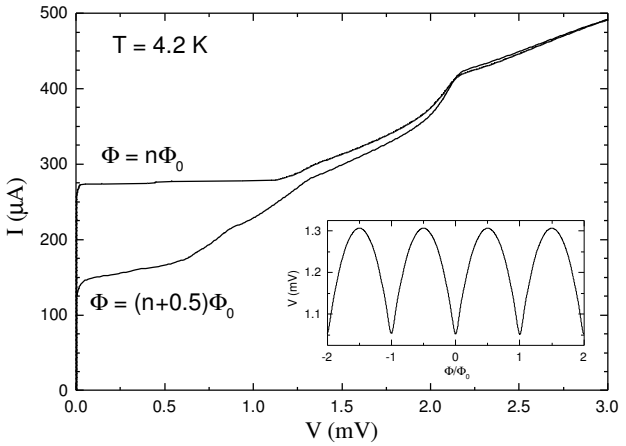

Fig. 5. The *I-V* curve of a dc SQUID with 0.25 μm × 0.25 μm junctions and loop inductance ~ 5 pH. The inset shows the voltage modulation at a bias current of 276 μA.

here have been tested for oscillator applications by studying phase-locking between two 0.25 μm × 20 μm junctions having critical currents of about 10 mA. These two junction cells show good high-frequency locking up to the superconducting gap voltage [20] and so appear promising for oscillator applications.

V. Conclusions

We have fabricated and characterized intrinsically overdamped Josephson junctions using Nb/AlO_x/Nb trilayers with J_c = 2.1 mA/μm^2. Deep-submicron junctions with a small parasitic capacitance due to the overlap between BE and wiring layer are achieved by using a fabrication process in which all levels are patterned by EBL. The junctions with dimensions smaller than 0.1 μm^2 show nonhysteretic *I-V* characteristics while junctions with larger dimensions have a small hysteresis due to heating in the electrodes.

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