Realization of a Square-Wave Voltage With Externally-Shunted SIS Josephson Junction Arrays for a Quantum AC Voltage Standard

Jaani Nissilä, Antti Kemppinen, Kari Ojasalo, Juha Hassel, Antti Manninen, Panu Helistö, and Heikki Seppä

***Abstract*—A quantum-based ac voltage standard operating from about 1 Hz up to 10 kHz at 1 V is being developed. The standard is based on relating the output of a stable sine generator to a square wave obtained by biasing a nonhysteretic Josephson junction array alternately at steps $n = -2$ and $n = +2$. We have constructed a bias current source and a buffer amplifier connected to the array which enable fast switching between steps. In this paper, we describe the system used for generation of the square wave and present experimental results which show that the accuracy of the fundamental frequency component amplitude of the square wave is sufficient for realization of a standard with accuracy better than 1×10^{-6}.**

***Index Terms*—AC, Josephson voltage array (JVA), square wave, voltage standard.**

I. Introduction

PROGRAMMABLE nonhysteretic Josephson voltage arrays (JVAs) exhibit two major advantages over traditional hysteretic SIS arrays: they allow rapid controllable switching between quantized voltage levels and they can better sustain external electromagnetic noise [1]. Their accuracy has recently been verified to be better than 1 nV [2]. Hence, they have a great potential for applications in both dc and ac voltage metrology.

A quantum-based ac voltage standard is being pursued in many laboratories around the world (see reviews [3] and [4] and references therein). Different types of nonhysteretic arrays are used: superconductor–insulator–normal metal–insulator–superconductor (SINIS) arrays, superconductor–normal metal–superconductor (SNS) arrays, and externally-shunted superconductor–insulator–superconductor (es-SIS) arrays. One realization scheme is to drive a binary-divided array with multiple fast bias sources to synthesize a staircase-like approximation of sinusoid. Fundamentally accurate waveforms can also be generated by exciting arrays with short pulses. However, accuracy better than 10^{-6} at 1-V level at around 1 kHz still remains to be demonstrated.

Our goal is to develop an ac voltage standard operating up to 1 V and 10 kHz with an accuracy of better than 0.1×10^{-6} [5]. In this paper, our focus is at $f = 1$ kHz. The idea is to generate a square wave voltage of fundamental accuracy by driving an es-SIS array between -1 V and $+1$ V Shapiro steps with a square-wave bias current. If the transition between the quantized levels is sufficiently fast, the amplitude of the fundamental frequency component is known accurately. The output of a stable sinusoid voltage source is then phase-locked to the square wave, and its amplitude and phase are adjusted to be equal to those of the fundamental frequency component of the JVA-based square wave using a lock-in amplifier as a null detector.

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J. Nissilä, A. Kemppinen, K. Ojasalo, and A. Manninen are with the Center for Metrology and Accreditation (MIKES), Electricity Group, 02150 Espoo, Finland.

J. Hassel, P. Helistö, and H. Seppä are with VTT Information Technology, Microsensing, FIN-02044 VTT, Finland.

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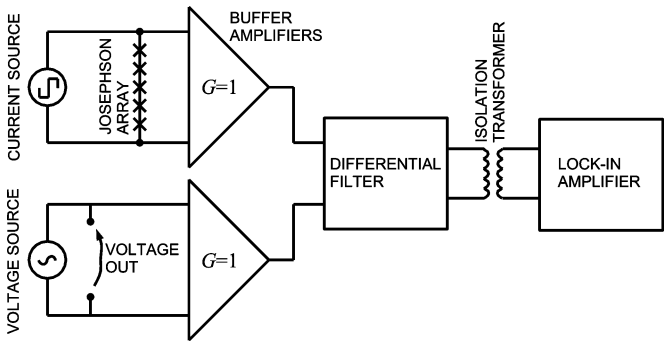

Fig. 1. Simplified diagram of the ac voltage standard.

II. Setup of the AC Voltage Standard

A. Overview of the Setup

We use an externally-shunted SIS array developed by VTT [6]. It has been designed for 70-GHz millimeter wave irradiation. The array with 3488 junctions, divided into 5 bits, provides voltages of 0.5 and 1.0 V at steps $n = 1$ and $n = 2$, respectively. The characteristic *RC* time constant of the array is about 80 ns which corresponds to the time span taken to charge the distributed capacitances in the array [7].

Fig. 1 presents a simplified diagram of the ac voltage standard. The setup consists of three different functional elements: bias source and buffer amplifier directly connected to the JVA, a stable sine generator acting as the output of the standard, and comparison electronics (a differential filter, an isolation transformer, and a lock-in amplifier). The design criteria for attaining 0.1×10^{-6} accuracy have earlier been discussed in [5].

A fast current source drives square-wave current through the JVA resulting in a voltage signal alternating between the Shapiro steps. A lock-in amplifier is used to measure the amplitude difference between the sine output of a stable generator (in our case, Fluke 5700A calibrator) and the fundamental frequency component of the square wave. This information is then used to adjust and stabilize the sine output to the accurate JVA-based

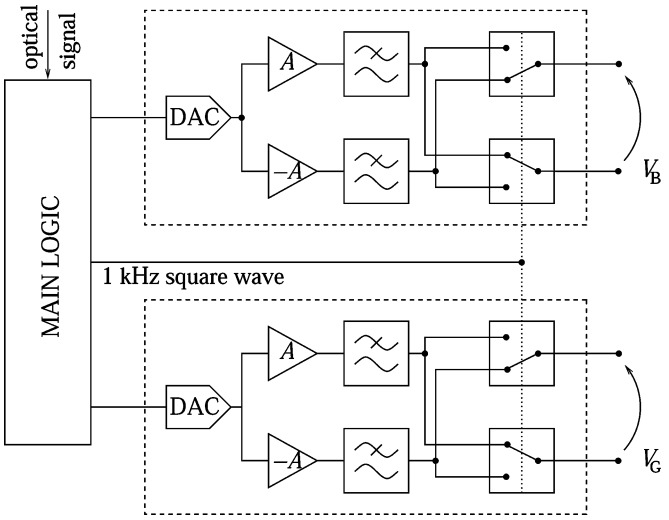

Fig. 2. Schematic diagram of the bias source used to drive square wave current through the Josephson voltage array.

voltage. Due to the finite dynamic range and nonlinearities of the lock-in amplifier, a differential filter is used to attenuate the harmonics in the square wave voltage. Further, an isolation transformer is needed to cancel out the common-mode voltage at the input of the lock-in amplifier. In addition, two accurate unity-gain buffer amplifiers are necessary as explained in the following section.

B. Bias Source, Buffer Amplifiers, and Wiring of the Cryoprobe

One of the challenges in developing an ac voltage standard based on Josephson voltage arrays is to design bias and measurement electronics which is fast but sufficiently noiseless not to deteriorate the flatness of the steps.

The amplitude of the fundamental frequency component in an ideal square wave with amplitude $V_{\rm step}$ is $V_1 = (4/\tau)V_{\rm step}$. In case of linear rising and trailing edges of duration τ, the error is $-(\pi^2/6)(\tau/T)^2$, where T is the period of the square wave. For 0.1×10^{-6} accuracy at 1 kHz, the risetime must be shorter than 250 ns. This corresponds to a bandwidth of some megahertz. Hence, the bias source and the buffer amplifier must be sufficiently noiseless in this band such that the steps are flat [5].

The current bias we have developed is a fiber-optically-controlled floating voltage source in series with two 3.3-kΩ resistors. A schematic diagram of the bias electronics is shown in Fig. 2. Square wave voltage drive $V_{\rm B}$ supplied to the array is generated from positive and negative highly filtered dc voltages which are fed to rapid MOSFET switches used for the current reversals. The switches are controlled with a 1-kHz signal phase-locked to a 10-MHz reference from atomic clocks. The voltage source for guarding the voltage measurement leads (the lower unit in Fig. 2) is identical to the bias voltage source.

The purpose of the buffer amplifier connected to the voltage leads of the JVA is twofold. First, it prevents external noise from disturbing the array, and second, its high input impedance prevents loading of the array and minimizes resistive voltage drops in the voltage leads. A similar buffer is used at the output of the sine source to prevent harmonic components of the square wave from leaking through the filter into the output. We have designed

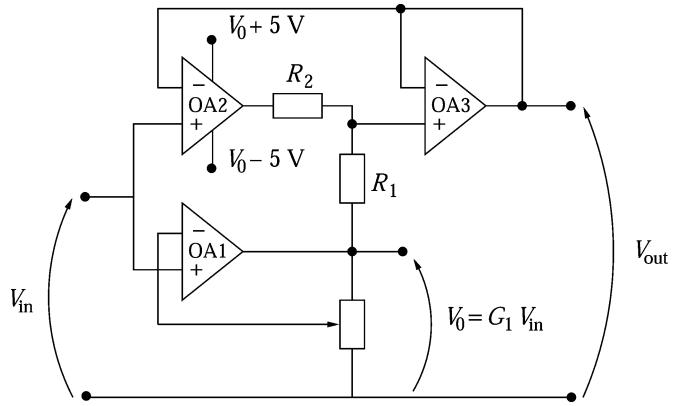

Fig. 3. Schematic diagram of the unity-gain buffer amplifier (the other half). Both of the voltage leads from the JVA are connected to this kind of circuit.

a symmetric amplifier in which both of the voltage leads end at low-noise opamps with high input impedance. Fig. 3 presents a schematic of one of the two identical blocks of the buffer. The signal voltage is connected to two opamps with FET inputs. OA2 is a precision opamp, and OA1 is a fast opamp which follows the input voltage reasonably accurately. The supply voltage of OA2 is produced with a floating 5-V power supply whose center point is driven by OA1 (flying-supply technique). With this technique, the slower opamp OA2 essentially sees a voltage of very low amplitude. The fast opamp OA3 is used to improve the current supply properties of the buffer. The gain of the circuit is

$$G = \frac{\left(\frac{R_1}{(R_1+R_2)}\right) A_2 A_3 + G_1 A_3}{\left(\frac{R_1}{(R_1+R_2)}\right) A_2 A_3 + A_3 + 1} \tag{1}$$

where G_1 is the adjustable gain of amplifier 1, and A_2 and A_3 are the open-loop gains of opamps OA2 and OA3, respectively (see Fig. 3). Based on the specifications of the opamps in our circuit, we have estimated that the gain of the whole buffer can be set to unity with an accuracy better than 0.07 ppm.

The dc input impedance of OA1 is 10^{11} Ω and that of OA2 is 10^{12} Ω. With a voltage lead resistance of 1.3 Ω at 1 kHz, the error due the voltage drop in the leads is, thus, negligible.

The wiring of the array to the bias source and the buffer amplifier is shown in Fig. 4. It is symmetrical with respect to the center of the array. The voltage measurement leads are guarded to prevent capacitive loading effects. For magnetic shielding, the array is enclosed by two superconducting lead shields and a cryoperm shield. The innermost lead shield is connected to the potential of the center of the array and acts as a shield against electric interfering fields as well. All the wiring is surrounded by grounded tubing.

The details of the bias source and the buffer amplifiers will be reported separately.

III. Performance of the Square-Wave Electronics

A. IV-Curves at DC

The noise of the output of the bias source and the input of the buffer amplifier reduces the width of the voltage steps of the JVA. In case of excessive noise, it may destroy the step

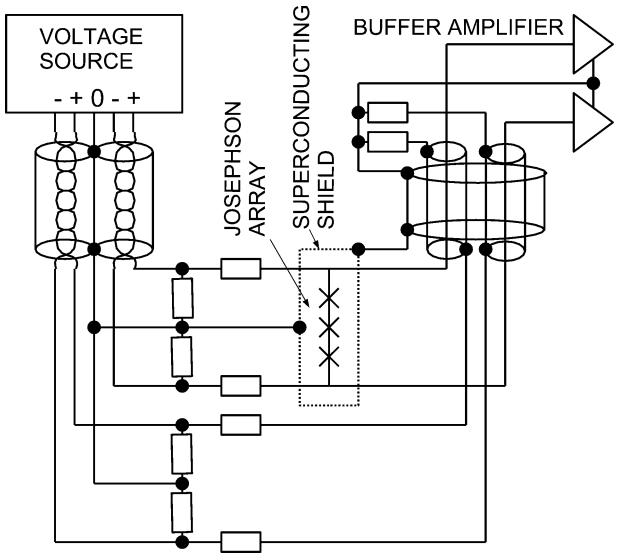

Fig. 4. Wiring of the cryoprobe.

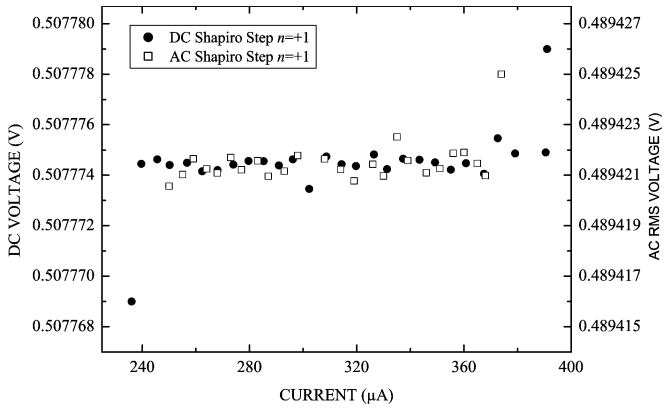

Fig. 5. Current–voltage curve presenting the structure of the first step ($n = 1$) measured at dc (closed circles) and ac (open squares). See text for a more detailed description.

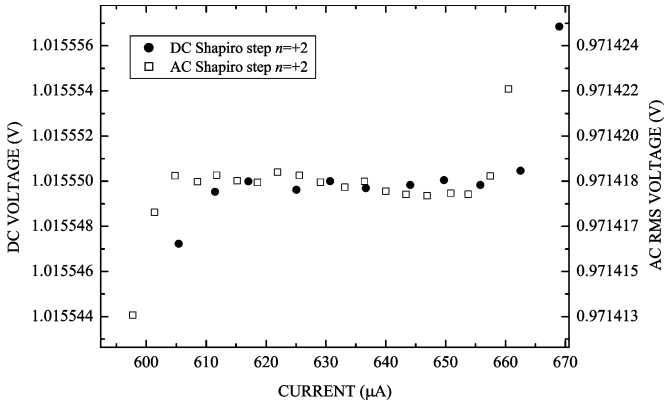

Fig. 6. Current–voltage curve presenting the structure of the second step ($n = 2$) measured at dc (closed circles) and ac (open squares). See text for a more detailed description.

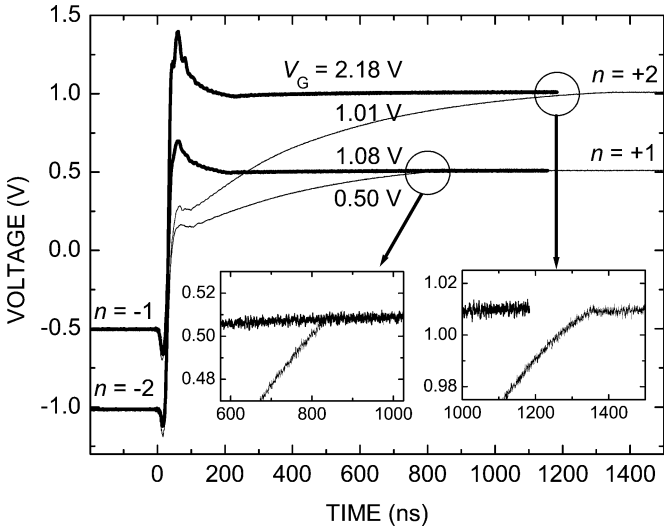

Fig. 7. Oscilloscope traces demonstrating the transition from step $n = -1$ to step $n = +1$ and from step $n = -2$ to step $n = +2$ with different guard voltages V_G indicated in the figure. For the thin traces, the guard voltage has the same magnitude as the JVA output, and for the thick traces, the guard voltage is about two times larger.

flatness totally. To study the performance of our electronics in this sense, we measured IV-characteristics under optimized millimeter wave power at dc bias by deactivating the switching at 1 kHz. The IV-curves for the first and second voltage plateaus are presented with closed circles in Figs. 5 and 6, respectively. The width of the flat region is 140 μA for the first step and 45 μA for the second step. For reference, we also measured the same array with a cryoprobe in which all the leads are strongly low-pass filtered (cut-off frequency=10 kHz). In that case, widths of the first and the second steps were at best 150 and 60 μA, respectively. The similarity of the step widths indicates that the current noise of our fast electronics is much smaller than the step width. The second step is also wide enough such that setting the bias current in the middle of the step is easy.

B. Switching Dynamics

The bias current source consists of a fast voltage source in series with two 3.3-kΩ resistors. The risetime of the voltage source without loading is about 30 ns. When a 1.2-kΩ resistor simulating JVA in normal state was connected as a load into the cryoprobe in place of the array, the risetime increased to 75 ns. With a JVA, dynamics is slower due to charging of the microstrip transition line capacitances. The 6.6-kΩ bias resistance in series with the array increases the time constant well above the intrinsic value of our array (80 ns). This is seen in Fig. 7, in which we present JVA voltage signals measured at the buffer amplifier input during the transition. The thin solid lines represent measurements in which the bias current was set in the middle of the 0.5 and 1.0 V steps and the guard voltages were set at these "correct" values. The time needed for the voltage signal to settle at the final value is 800 ns for the first step and 1300 ns for the second one.

To speed up the transition, extra current is required during the step change. One way to do this is with the help of the guard driver, which can feed the current through the capacitance of the coaxial voltage measurement wires into the array. By adjusting the guard voltage properly, this results in much faster settling time (see Fig. 7). The overshoot is due to the resistive voltage drop in the voltage leads during the transient. The guard voltages

TABLE I
CHARACTERISTICS OF THE SQUARE-WAVE VOLTAGE RELATED TO THE TRANSITIONS BETWEEN NEGATIVE AND POSITIVE STEPS. TRANSITION TIMES WERE MEASURED WITH AN OSCILLOSCOPE (SEE FIGS. 7 AND 8). THE ERROR IS THE DIFFERENCE BETWEEN THE AMPLITUDE OF THE FUNDAMENTAL FREQUENCY COMPONENT OF AN IDEAL SQUARE WAVE AND THAT CALCULATED FROM THE MEASURED WAVEFORMS

Step voltage (V)	Guard voltage (V)	Transition time (ns)	Estimated error at 1 kHz (10^{-6})
0.506	0.50	800	-0.71
0.506	1.08	250	+0.02
1.012	1.01	1360	-2.0
1.012	2.18	350	+0.01

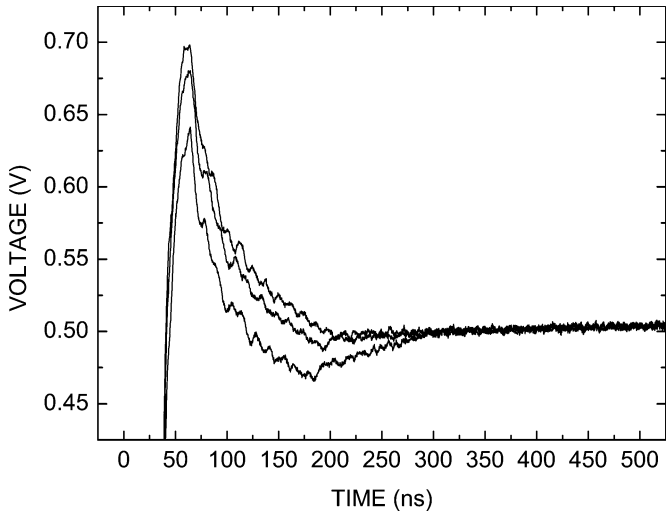

Fig. 8. Closeup of the settling of the JVA at step $n = +1$ at three different guard voltages $V_{\rm G}$. From top to bottom, $V_{\rm G} = 1.08$, 1.06, and 1.01 V, respectively.

in these plots were about two times larger than the "correct" values.

Fig. 8 presents in more detail the transition at the first step with three different guard voltages all of which result in close-to minimum transition times. The minimum time taken before the voltage reaches the asymptotic value is about 200–250 ns with this setup. The intrinsic settling time of the array cannot be decreased by the extra current, although the deviation of the generated square wave from the ideal one can be considerably decreased.

In the next version of the cryoprobe wiring, we will use a third voltage source whose role is just to feed current via capacitors directly to the array during the current reversal transitions. The guard driver will then be used for its original purpose of guarding the measurement wires.

The deviation of the fundamental frequency component amplitude from the ideal value $V_1 = (4/\pi)V_{\rm step}$ was calculated for the waveforms of Fig. 7 by Fourier analysis. The results for 1-kHz signal frequency are shown in Table I. In the calculation, we assumed the voltage to be accurate after the transition time identified from the oscilloscope measurements and given in the table. The calculated deviation is $+0.02 \times 10^{-6}$ for the first step and $+0.01 \times 10^{-6}$ for the second step. The positive sign is due to the overshoot. Considering the goal of 0.1×10^{-6} the error due to the transients is evidently sufficiently small.

C. IV-Curves at AC

Charging the distributed capacitances in the JVA distorts the output signal of the JVA from an ideal square wave. The exact waveform depends on the bias current and guard voltage. However, it is sufficient for the accuracy of our standard that the amplitude of the fundamental frequency sine wave is constant. To investigate ac step flatness, we must filter out higher harmonics. We measured the rms voltage of the 1-kHz square wave from the buffer amplifier ouput via a lowpass filter with cutoff at 10 kHz (6-dB roll-off/octave). The voltages measured as a function of bias current are presented with open squares in Figs. 5 and 6. The low-frequency content of the square wave is not sensitive to the bias current within an accuracy of 1 μV. The sub-μV structure in the data is associated with the output drift of the lowpass filter. The step widths are almost equal to those measured at dc: 125 μA for the first and 50 μA for the second step. These data suggest that the JVA settling at the quantized voltage step is fast enough for the realization of an ac voltage standard with accuracy better than 1×10^{-6}.

IV. CONCLUSION

An ac voltage standard traceable to the fundamentally accurate voltage steps of Josephson junctions is being developed. Electronics capable of driving an externally-shunted Josephson voltage array between negative and positive quantized voltages of 1 V at 1 kHz frequency has been realized. The accuracy of the fundamental frequency component amplitude of the square wave is sufficient for realization of a standard with accuracy better than 1×10^{-6}. The comparison electronics to transfer the voltage value to a stable sinusoid generator is in test phase.

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