AC Voltage Standard Based on a Programmable SIS Array

Panu Helistö, Jaani Nissilä, Kari Ojasalo, Jari S. Penttilä, and Heikki Seppä

***Abstract*—An ac voltage standard is being developed based on phase sensitive detection of the amplitude of the fundamental frequency component of the output of a programmable Josephson voltage array. The setup is described and requirements for relative uncertainties less than 10^{-7} at 1 kHz and 1 V are discussed. According to preliminary experiments, the constructed current bias is able to drive the array from −1 to +1 V within less than 100 ns.**

***Index Terms*—AC voltage, programmable Josephson voltage standard.**

I. Introduction

NONHYSTERETIC programmable Josephson arrays are becoming increasingly popular in electrical metrology [1]–[4]. These arrays are based on SNS junctions [1], intrinsically damped superconductor—insulator—normal metal—insulator—superconductor (SINIS) junctions [2], [3] or externally shunted (es-SIS) junctions [4]. Both SINIS and es-SIS arrays have recently been studied in a Euromet project and found to be as accurate as conventional SIS Josephson arrays at dc [5].

The fast step selection of the binary-divided arrays allows to construct arbitrary waveforms which can be directly used in ac metrology [6], [7].

We have developed an ac voltage standard based on phase locking the output of a sinusoidal signal from a stable signal source to the output of an es-SIS Josephson array. The Josephson array is driven by a square wave bias current. A lock-in amplifier compares the amplitude of the sinusoidal signal with that of the fundamental frequency component of the square wave signal.

II. System Description

In [8], some possible realizations of quantum ac voltages are discussed. They are based on the idea presented in [7]. Our setup is shown in Fig. 1. The Josephson array is biased with square wave current alternately on positive and negative steps. The amplitude and phase of a stable sinusoidal ac source is compared with the amplitude V_1 of the fundamental frequency component of the square-wave output from the Josephson array. By feedback, the difference of these two signals is adjusted to zero. The result is a calculable sinusoidal voltage with amplitude directly traceable to the Josephson array step voltages. Ideally, the amplitude of the first harmonic is $4/\pi$ times the amplitude of the square wave V_0. For example, if $V_0 = 1$ V, the rms value of the fundamental becomes $(4/\pi)/\sqrt{2}$ V $\simeq 0.90$ V.

The Josephson array is grounded at the ac generator ground. This grounding scheme introduces a high common mode voltage in the filtered difference signal between the Josephson array and the ac generator. The common mode signal is eliminated by the isolation transformer at the lock-in amplifier input.

The accuracy of the setup depends critically on the risetime of the square wave signal [7]. Assuming exponential rise and fall with time constant $\tau \ll T = 1/f$, the period of the square wave, the relative error in the amplitude of the first harmonic is $-2\pi^2 (\tau/T)^2$. In order to achieve amplitude errors smaller than 0.1 ppm, the ratio τ/T has to be less than $0.7 \cdot 10^{-4}$, i.e., $\tau < 70$ ns at 1 kHz.

III. Main Components of the System

A. Array

Three major factors influence the speed of step recovery in a programmable Josephson array after bias current changes: the intrinsic dynamics of the Josephson junctions, the RC-time constant of the array, and susceptibility of the steps to disturbances and loading effects due to the bias source, cabling, and external noise. The intrinsic dynamics of shunted Josephson junctions due to Josephson oscillations and plasma frequency allow step changes within 1 ns, whereas the time constant of the array is of the order of 100 ns. The dynamics of step changes under realistic experimental conditions have not been studied much theoretically, but, experimentally, it has been observed that the steps are very sensitive to filtering of the input and output lines [5].

The array used is a 1-V es-SIS array with frequency dependent damping, developed at VTT [4]. This design allows operation at voltage steps $|n| > 1$. Fewer junctions are thus required than in a SINIS array to give the same output voltage. The junctions are arranged in five bits. For proper ac operation, the two most important parameters of the array are its stability, i.e., the width of the steps/noise immunity, and the intrinsic maximum speed. A narrow step has the added complication that the current drive capability at the step is limited [7].

The $n = 1$ step of the VTT arrays is flat approximately from 200 to 400 μA, giving a voltage of 0.5 V at 70 GHz. Typical *I–V* curves are shown in Fig. 2. The 1-V or $n = 2$ step is narrower, a flat step is observed from around 500 to 600 μA. No deviation from the output voltage of a conventional SIS array has been detected at dc [5]. However, the step width is sensitive to filtering

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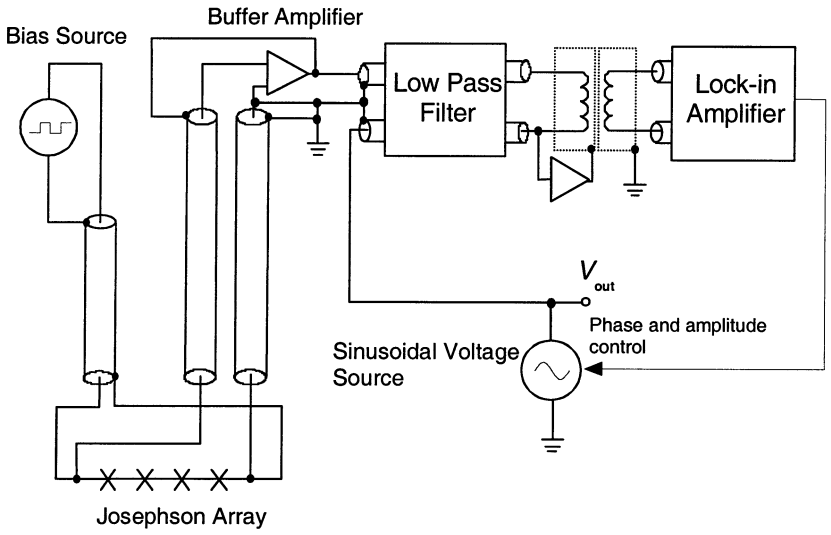

Fig. 1. Setup for ac Josephson voltage generation.

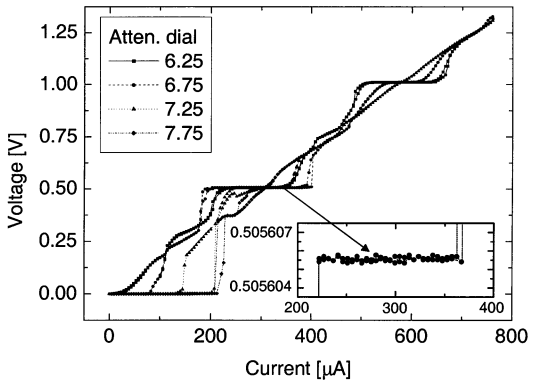

Fig. 2. *I–V* curves of the VTT es-SIS array at 70.10 GHz with different rf attenuator dial readings. Rf power decreases with increasing dial reading. Inset: curve 6.75 at step $n = 1$ in magnified vertical scale.

and noise. For the preliminary ac tests, we operated the array at the 1-V step.

Achieving fundamental accuracy requires the transition between different quantized voltage levels to take place in less than 100 ns. During transients, when the filter and cable capacitances are charging, the array does not produce a stable voltage until the current through all the shunted junctions reaches the step current. An ideal bias source should thus be able to supply additional current for the load capacitances during the transient.

Even without filtering, the intrinsic time constant of an es-SIS array is approximately $\tau_{\rm intr} = N^2RC/\pi^2$, where R is the shunt resistance, C is the stray capacitance per junction, and N is the number of junctions [7]. For the VTT array $\tau_{\rm intr} = 78$ ns. Especially in high output voltage arrays (large N), the rise time increases significantly above 100 ns and dominates the speed of the setup. By biasing the step near the maximum step current, the step change can be accelerated.

B. Current Bias Supply

To avoid operating with voltage bias mode, the bias source impedance should be higher than that of the array. In addition, the current bias should have low noise and risetime adjustable within approximately 10–200 ns.

The bias supply driving the array is a voltage source in series with two 1.5-kΩ resistors. Square wave current at 1 kHz is used in this work. In addition to the bias current, additional guard voltages are supplied to the array output cables to minimize capacitive loading of the array during transients. The bias current is precisely synchronized to the sinusoidal signal from the ac source. The ac source is a Fluke 5700 A calibrator.

C. Isolation Transformer

To reduce the error due to common mode voltage, a triple shielded isolation transformer is used between the filter and the lock-in amplifier. The inner input shield is actively guarded and the outer input and the output shields are grounded. The isolation transformer reduces the common mode error from a low-impedance source to a level below 0.2 ppm.

D. Differential Filter

An ideal square wave signal contains harmonics at frequencies $(2k + 1)f$ with amplitudes decaying slowly with k. This introduces problems due to dynamic range limitations and possible nonlinearity of lock-in detection. To reduce these problems, the difference between the square wave signal and the sinusoid is first filtered with a symmetric differential filter. A differential filter is very useful as it introduces minimal differential amplitude error and is insensitive to variations of component values. The design goal was to reduce the amplitude of the third harmonic by at least a factor of 30 relative to the fundamental frequency component. The maximum output voltage is reduced from >1 V to 1 mV while the 1-kHz difference signal is attenuated only by 70%.

One problem of the filter is common mode signal. Although a symmetrical design was aimed at, there remains a slight asymmetry in the channels relative to the grounded case. Thus, the filter is guarded to the mid voltage of its output. With 2-V peak to peak square wave common mode input voltage at 1 kHz, the

filter gives a common mode rms error of about 2.2 μV, linearly increasing with amplitude.

The input square wave signal leaks to the sinusoidal voltage input through the filter. The amount of the leakage is determined by the ratio between the source impedance of the ac generator and the transfer impedance of the filter between its two input ports at the frequencies in question. Small harmonic components contribute to the rms value in proportion to the square of their amplitudes relative to the fundamental amplitude.

E. Unity-Gain Buffer Amplifier

If the output of the Josephson array is used to drive the filter and the cables directly, the cable capacitances, ohmic losses, and the finite input impedance of the filter deteriorate the accuracy of the array voltage and step stability. Thus, the output leads from the array are actively guarded to compensate for the capacitances and a high impedance unity-gain buffer amplifier is used to avoid ohmic losses in cables due to loading.

The input impedance of the buffer amplifier is >100 GΩ. As the cable resistances are <10 Ω, ohmic losses in cables contribute a negligible error.

The deviation from unity gain is determined by the amplifier open loop gain. At dc, the gain is $A_0 > 126$ dB. Assuming single pole rolloff with corner frequency $f_0 = 10$ Hz, the open loop gain can be described as

$$A = \frac{A_0}{1 + if/f_0}. \tag{1}$$

The dc gain error as a unity gain follower is <0.5 ppm. At 1 kHz, the gain

$$G \simeq \frac{1}{1 + 1/A_0} \frac{1}{1 + if/(A_0 f_0)} \tag{2}$$

is very close to the dc gain. The main contribution of the pole is a phase shift of <0.05 mrad. The gain error should be determined and its stability monitored during the measurement. The slew rate of the amplifier is >150 V/μs.

IV. Influence on Nonlinearities

Nonlinearities can affect the amplitude of the fundamental frequency component and they thus require a careful analysis. We consider two types of nonlinearities: slew rate limited and amplitude dependent.

A. Slew Rate Limited Response

The maximum slew rate $\Delta V/\Delta t$ of the buffer amplifier modifies the square wave signal. For simplicity, we assume that the result is as shown in Fig. 3, an ideal square wave becomes sloped with constant slew rates τ_1 and τ_2 determined by the amplifier. In practical amplifiers, the positive and negative slopes can be different.

The harmonic amplitudes are given by $V_{n,\sin} = (2/T)\int_0^T V(t)\sin(2n\pi ft)dt$ and $V_{n,\cos} = (2/T)\int_0^T V(t)\cos(2n\pi ft)dt$. Summing the squares of the sine and cosine integrals, the amplitude of the fundamental frequency component can be written as

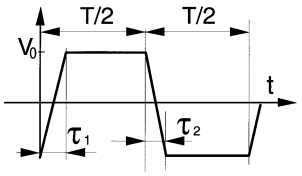

Fig. 3. Ideal square wave distorted by finite slew rates $2V_0/\tau_1$ and $2V_0/\tau_2$.

$$V_1 = \frac{2V_0}{\pi}\left[\left(\operatorname{sinc}\left(\frac{\tau_1}{T}\right) + \operatorname{sinc}\left(\frac{\tau_2}{T}\right)\right)^2 - 4\operatorname{sinc}\left(\frac{\tau_1}{T}\right)\operatorname{sinc}\left(\frac{\tau_2}{T}\right)\sin^2\left(\frac{\pi(\tau_1 - \tau_2)}{T}\right)\right]^{1/2}. \tag{3}$$

If $\tau/T \ll 1$, the relative amplitude error becomes

$$\frac{\Delta V_1}{4V_0/\pi} \simeq -\frac{\pi^2}{24}\left[5\left(\tau_1^2 + \tau_2^2\right) - 6\tau_1\tau_2\right].$$

If both slopes are equal, the deviation reduces to $-\left(\pi^2/6\right)\left(\tau_1/T\right)^2$.

To keep the error below 0.1 ppm when $V_0 = 1$ V, the amplifier slew rates should be higher than 2 V/250 ns = 8 V/μs.

B. Amplitude Nonlinearity

The influence of nonlinear amplitude response can be estimated by assuming that the originally linear amplifier output $V_{\text{lin}} = A(V_+ - V_-)$ from the open loop experiences a nonlinear operation $V_{\text{out}} = V_{\text{lin}} + \alpha V_{\text{lin}}^2 + \beta V_{\text{lin}}^3$, where αV_{lin} and βV_{lin}^2 are small corrections. Substituting into (2) and neglecting higher order terms, we end at a deviation

$$\Delta V_{\text{nonlin}}(f) \simeq \frac{1 + if/f_0}{A_0 + if/f_0}(\alpha V_{in}^2 + \beta V_{in}^3) \tag{4}$$

due to nonlinearity. It is assumed that $f \ll A_0 f_0 \simeq 100$ MHz. The nonlinearity has both an in-phase and off-phase component.

We study next the influence of the nonlinearity on the fundamental frequency component. The nonlinearity influences sinusoidal and square wave excitation slightly differently.

The second (and any even) order nonlinearity does not modify the fundamental frequency component of either sinusoidal or square wave input because of symmetry. This is seen from the trigonometric relation $\sin[(2k+1)\omega t]\sin[(2k'+1)\omega t] = \cos[2(k-k')\omega t]/2 - \cos[2(k+k'+1)\omega t]/2$, i.e., the nonlinearity mixes odd harmonics to even. Only if the input contains even harmonics, the fundamental component becomes modified. When a sinusoidal input includes a second harmonic $V_2\sin(2\omega t)$, the second order nonlinearity generates an in-phase error with amplitude

$$\Delta V_{1,V_2,\sin} = \left(\frac{\alpha}{A_0}\right)\left(\frac{f}{f_0}\right)V_1 V_2. \tag{5}$$

In the case of square wave input, the result is the same as (5) except for a correction factor of 4/3.

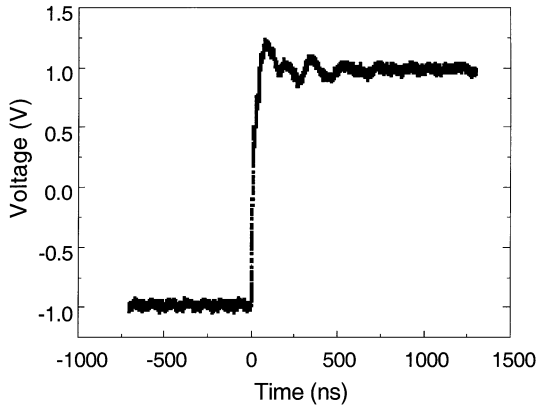

Fig. 4. Response of the VTT 1-V array to a sudden bias current change, measured with the setup shown in Fig. 1.

The third order nonlinearity causes an in-phase change of

$$\Delta V_{1,\beta,\sin} = \left(\frac{3}{4}\right)\left(\frac{\beta}{A_0}\right)V_1^3 \tag{6}$$

to the amplitude of the fundamental in the case of pure sinusoidal input. Assuming square wave input and neglecting the frequency dependence of the amplifier, the coefficient becomes 0.62 instead of 3/4.

To estimate the magnitude of the nonlinearity, let the small signal open loop gain of the amplifier be $A_0 = 10^6$ and let it change by 10% at ± 5 V output due to either second or third order nonlinearity. In the case of second–order nonlinearity $\alpha = 0.02\ \mathrm{V}^{-1}$. If $V_0 = 1\ \mathrm{V}(V_1 = 4/\pi\ \mathrm{V})$ and $V_2 = 1$ mV , the amplitude error according to (5) is $\Delta V_1 \simeq 3 \cdot 10^{-9}$ V. The second order contribution is very small even if the even harmonic amplitudes are considerable.

In the case of third order nonlinearity, $\beta/A_0 = 4 \cdot 10^{-9}\ \mathrm{V}^{-2}$. Then at $V_0 = 1$ V, $\Delta V_1 \simeq 4 \cdot 10^{-9}$ V. In practice, the nonlinearity contribution must be measured and, if needed, compensated for.

V. Experimental Results

The individual components have been constructed and tested, and test measurements with the whole setup have been started at 1-V amplitude and 1-kHz frequency.

The speed of the step changes was studied by switching the bias current between the centres of the steps $n = \pm 2$. By guarding the output cables from the array slightly above the step voltage, the risetime of the voltage from -1 to $+1$ V was well below 100 ns, as shown in the oscilloscope trace of Fig. 4. Some ringing is observed. This speed of the voltage change is well sufficient for an accurate ac standard. The stability of the obtained voltage steps needs still further research before actual ac voltage calibrations can be started.

VI. Conclusion

We have developed an experimental setup for an ac Josephson voltage standard based on the VTT programmable Josephson junction array and analyzed the magnitude of its main error sources. The aim was to verify the functionality of the lock-in detection idea with the prototype at 1 V and 1 kHz and to estimate whether an uncertainty of 0.1 ppm can be reached. According to the first measurements, the array voltage can be changed from ∓ 1 to ± 1 V in <100 ns. Theoretical estimates indicate that the influence of nonlinearities in the unity gain buffer amplifier can be controlled with careful design.

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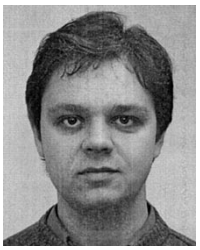

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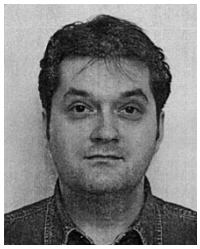

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