Stimulated Power Generation in ES-SIS Junction Arrays

Juha Hassel, Panu Helistö, Leif Grönberg, Heikki Seppä, Jaani Nissilä, and Antti Kemppinen

***Abstract*—We present experimental results on new programmable Josephson voltage standards based on frequency dependently damped superconductor–insulator–superconductor (SIS) junctions. We introduce a design able to generate two independent floating voltages up to 1.5 V using a microwave frequency of 70 GHz. The array is developed for dc and ac voltage and impedance metrology. The design is optimized in terms of speed, power consumption, and stability. Stimulated power generation is shown to affect the performance of long SIS arrays. The collective dynamics of Josephson junctions is analyzed and a boundary condition for the design of long arrays is derived.**

***Index Terms*—Josephson array, Josephson voltage, Josephson voltage standards.**

I. Introduction

JOSEPHSON voltage standards (JVSs) have established their role as the primary realization of the unit of voltage. Under microwave irradiation they produce a quantized voltage $U = nf/K_{\rm J}$, where n is an integer and $K_{\rm J} = 2e/h$ is the Josephson constant. Conventional arrays are based on a series of undamped superconductor–insulator–superconductor (SIS) junctions (see [1] for a recent review). More recently, so called programmable voltage standards have gained interest. They are based on damped Josephson junctions (JJs), the benefit of which is better stability against external fluctuations and the higher speed. Different concepts for damping have been introduced including intrinsically damped junctions (superconductor–normal conductor–superconductor (SNS) [2], or superconductor–normal conductor–insulator–normal conductor–superconductor (SINIS) [3], [4]), and externally-shunted SIS (es-SIS) junctions [5], [6].

In this paper, we concentrate on arrays based on externally damped SIS junctions with frequency-dependent damping. It has already been shown experimentally that with this technology, a dc voltage of 1 V can be generated with metrological accuracy. These arrays are promising candidates for tracing the rms value of an ac voltage back to the Josephson voltage [7], [8]. We present experimental results on a new optimized array, which is able to generate two independent floating voltages. In addition to voltage metrology, the array could be used to compare two complex impedances [9]. The array produces flat voltage steps up to 1.44 V.

Manuscript received July 2, 2004; revised November 5, 2004.

J. Hassel, P. Helistö, L. Grönberg, and H. Seppä are with the VTT Information Technology, 02044 VTT, Finland.

J. Nissilä and A. Kemppinen are with the MIKES (Center for Metrology and Accreditation), Electricity and Time, 02150 Espoo, Finland.

Digital Object Identifier 10.1109/TIM.2004.843119

We study also the possibility to increase the output voltage up to 10 V. This would enable replacing existing undamped dc references with programmable arrays. However, we found that the first version of our 10-V array does not produce sufficiently flat steps. We identify the reason to be the inhomogeneous power distribution due to the stimulated power generated by the junctions. We derive a design criterion to avoid the effect, and show that it will be possible to fabricate a 10-V array using the es-SIS technology.

II. Design and Experiments

The aim is to maximize both the stability of the array against external fluctuations and the speed of the array [6] assuming the standard 70-GHz microwave frequency and the VTT Nb trilayer process. These are quantified by the step width $\Delta I_{\rm n}$, and the time constant $\tau_{\rm RC}$ describing the minimum time needed to switch between different quantized voltage states. At the same time, the microwave power $P_{\rm in}$ should be minimized.

The general layout of the 2×1.5 V chip is presented in [9]. In brief, both subarrays consist of 3315 JJs arranged in a microstripline configuration. The array is designed to produce 1.44 V at step $n = 3$. The microwave power is divided into eight branches per subarray, each with its own microwave input. One branch has 418 or 403 junctions. Junctions are 80×30 μm (width $\times$ length) in size, which leads to a critical current $I_{\rm c}$ of 720 μA (with critical current density of 3×10^5 A/m^2) and a junction capacitance C of 110 pF. The shunt resistance R and inductance L are 0.14 Ω and 3.5 pH, respectively. The dielectric thickness of the microstriplines is 350 nm leading to a transmission line impedance of about 0.6 Ω. Theoretical figures of merit are $\tau_{\rm RC} \approx 100$ ns and $P_{\rm in} \approx 3.4$ mW excluding the effect of the mismatch from the waveguide to the array. These figures should enable ac generation at 1 kHz with an error of the order of 0.1 μV/V [6] and operation with a standard Gunn diode.

The 10-V chip consists of 23 529 JJs divided into 16 branches with 1472 or 1449 junctions in each. It is designed to produce a voltage of 10.23 V at step $n = 3$. Other design parameters (differing from the 2×1.5 V design) are junction size 80×17 μm, $I_{\rm c} \approx 400$ μA, $C \approx 60$ pF, $R \approx 0.2$ Ω, $L \approx 4.9$ pH. The theoretical risetime and input power are $\tau_{\rm RC} \approx 2.5$ μs and $P_{\rm in} \approx 1.6$ mW. Increasing the output voltage tends to slow down the array making it unpractical for ac calibrations [6]. However, a 10-V programmable array is attractive as a stable and fast programmable dc reference.

The fabrication process is the standard trilayer process used for the fabrication of superconducting quantum interference devices (SQUIDs) and JVSs. Junction electrodes and superconductors in the microstriplines are formed by sputtered Nb

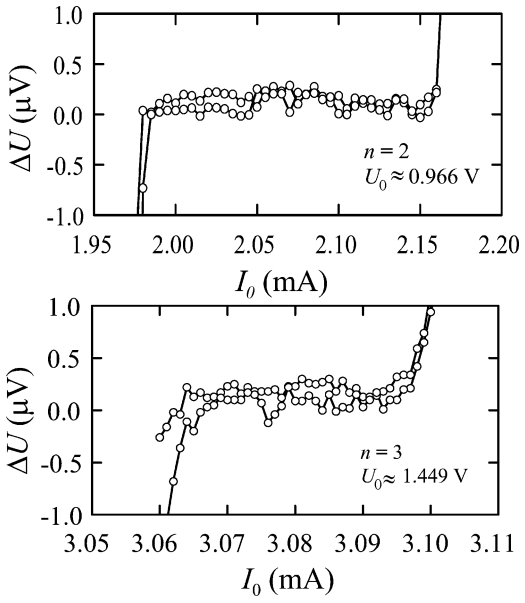

Fig. 1. Steps $n = 2$ and $n = 3$ of a 1.5-V es-SIS subarray. Deviation ΔU from the quantized value U_0 is shown.

patterned by reactive ion etching. The insulating material is SiO_2 grown by plasma enhanced chemical vapor deposition and patterned by wet etching. The JJs are $Nb/Al/AlO_x/Nb$ trilayer junctions bounded by anodizing the Nb around the junction area. The shunt resistors and microwave terminations are fabricated from sputtered molybdenum patterned by wet etching. For a more detailed description see [6].

The step flatness was verified with a high-precision digital voltmeter with a resolution of about 200 nV. The dc wiring was filtered at the room temperature end to avoid interference from the environment and the bias source.

Current-voltage characteristics for one of the sub-arrays of the 2×1.5 V design are shown in Fig. 1. The result for step $n = 2$, giving an output of about 0.97 V, is shown in Fig. 1(a). The step is flat within a current range of $\Delta I_2 \approx 180$ μA using the criterion of the maximum deviation of 1 μV. This is about two times larger than the value obtained for 1-V steps with our earlier nonoptimized arrays [5]. A similar plot for $n = 3$ and an output of about 1.44 V shows that $\Delta I_3 \approx 30$ μA. The decrease in the step amplitude with increasing n is mostly explained by the scattering of the shunt resistances. The experimental results for ΔI_2 and ΔI_3 are justified, if $\Delta R = (R_{\max} - R_{\min})/2R \lesssim 10\%$ [5] for this sample, whose minimum critical current was measured to be about 600 μA. Here, $R_{\max}$ and $R_{\min}$ are the maximum and minimum shunt resistances on the array. The quality of step $n = 1$ was, however, considerably worse than that of $n = 2$. Even the measurement of a single branch of the same array with the whole array biased, gave $\Delta I_1 \approx 130$ μA, i.e., about 30% smaller than ΔI_2. This is unexplained by the parameter scattering.

A result with a 10-V array is shown in Fig. 2. The step structure is clearly visible, but the step amplitude is strongly reduced from the theoretical value. Furthermore, flat steps at a metrological level are not obtained with this array or other similar arrays. The poorer quality of constant voltage steps can, to some extent, be explained by the increasing parameter scattering due to

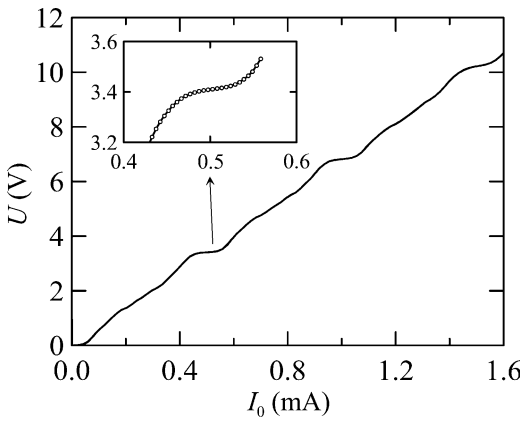

Fig. 2. IV characteristics of a 10-V array. The inset shows a magnification of step $n = 1$ with $V \approx 3.4$ V.

a larger number of junctions. However, for the amplitude of the first step to be completely suppressed, ΔR should be over 30%. Furthermore, the remaining resistance at the optimal point of operation shows that a significant fraction (10%–20%) of junctions are biased off-step. This implies that a corresponding fraction of the shunts should be outside the tolerance. This is not plausible, since a characterization of our resistor process [9] as well as the experience with 1.5-V arrays indicate otherwise.

III. Power Self-Generation

In this section, we develop a model that explains the reduced quality of the constant voltage steps of the 10-V array and the step $n = 1$ of the 2×1.5 V array. The stability analysis of the arrays has so far assumed that single junction dynamics determines the stability and that the passive transmission line properties of the microstripline determine the homogeneity of the microwave power along the junction chain.

Arrays of Josephson junctions are known to act as microwave sources [10]. In overdamped arrays, the radiated power is known to compensate at least partly for the transmission line attenuation [3]. For undamped or frequency dependently damped SIS arrays, the coupling from the junction to the transmission line is smaller, so the effect has been neglected so far. However, we find that for long arrays the effect can become significant even in this case.

We start by studying a single junction embedded in a transmission line as in Fig. 3. The microwave current $I_1 \cos \omega t$ couples through the junction predominantly capacitively, since the capacitive reactance of C is typically much less than the inductive reactances of L or the Josephson inductance $\Phi_0/2\pi I_c$, where Φ_0 is the flux quantum. Therefore, the voltage across the junction is $V_T(t) = (I_1/\omega C)\sin(\omega t) + \langle U \rangle$, where $\langle U \rangle$ is the average voltage. The quantum phase difference is $\phi = (2\pi/\Phi_0) \int V_T dt$, i.e.

$$\phi(I_0, I_1, t) = -\widetilde{i}_1 \cos(\omega t) + \frac{2\pi}{\Phi_0}\langle U \rangle t - \phi_c \qquad (1)$$

where $\widetilde{i}_1 = 2\pi I_1/\Phi_0 \omega^2 C$ is a dimensionless microwave amplitude and ϕ_c is a constant of integration. The dependence on bias parameters I_0 (the dc component) and I_1 is included in $\widetilde{i}_1$

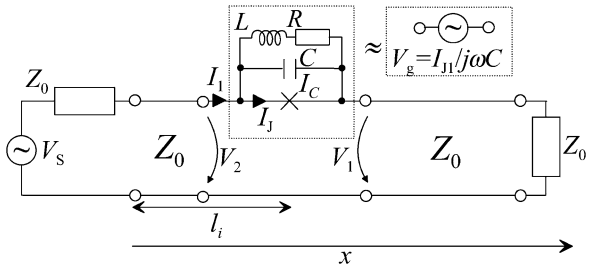

Fig. 3. Model used in the power self-generation calculation. For clarity, only one junction embedded in the transmission line Z_0 is shown. The junction is represented as an equivalent circuit and the simplification to the voltage source model is also shown. The external microwave is represented by source V_S and the transmission line is assumed matched from both ends.

and ϕ_c. The tunneling current is obtained as $I_J = I_c \sin\phi$. Assuming that the junction is biased on a constant voltage step, i.e., $\langle U\rangle = n\Phi_0 f$, we get

$$I_J(I_0, I_1, t) = I_c \sum_{m=-\infty}^{\infty} J_m(\tilde{i}_1)\left[\cos\left((m+n)\omega t - \frac{\pi m}{2} - \phi_c\right)\right] \tag{2}$$

where J_m is the mth Bessel function of the first kind. The dc bias current is $I_0 = \langle I_J\rangle + \langle U\rangle/R$, where $\langle I_J\rangle$ is the average tunneling current. In (2), the dc component is obtained from the term with $m = -n$. This enables us to solve the constant of integration

$$\phi_c = \frac{\pi n}{2} - \arccos\left((-1)^n \left(\frac{\delta I_0}{I_c}\right) J_n^{-1}(\tilde{i}_1)\right) \tag{3}$$

where $\delta I_0 = I_0 - n\Phi_0 f/R$, i.e., the deviation of the bias current from the center of the step.

We consider next the power radiated by the junction into the transmission line at the microwave frequency. We note that since typically $Z_0 \gg 1/\omega C$, the junction acts as a voltage source with amplitude $V_g(I_0, I_1) = I_{J1}(I_0, I_1)/j\omega C$ embedded into the transmission line. Here, I_{J1} is the first harmonic of the tunnel current, i.e., terms with $m + n = \pm 1$ in (2) converted into the frequency plane. The absolute value $|I_{J1}|$ and phase δ of I_{J1} are plotted in Fig. 4(a) and (b) as function of the bias point for step $n = 1$.

We neglect here the effect of higher harmonics for simplicity. This is justified, since their coupling to the transmission line is weaker due to the $1/\omega C$-dependence. We further assume that the transmission line is terminated at both ends, from which it follows that V_g is divided across the transmission line as $V_1 = V_g/2$ and $V_2 = -V_g/2$ (see Fig. 3). Therefore, the propagating waves from a junction to the right and to the left are

$$I(x) = \frac{I_{J1}(I_0, I_1)}{2j\omega C Z_0} \exp\left(-j\beta(x-l)\right) \text{ if } x > l \tag{4}$$

$$I(x) = \frac{I_{J1}(I_0, I_1)}{2j\omega C Z_0} \exp\left(-j\beta(l-x)\right) \text{ if } x < l \tag{5}$$

where l is the position of the junction and $\beta = 2\pi/\lambda$ is the wave number for wavelength λ of the microwave signal.

We sum finally the contribution of all junctions at positions l_i to the microwave current $I_1' \exp(-j\beta x)$ at position x in the transmission line. The resulting total current distribution in the line is then

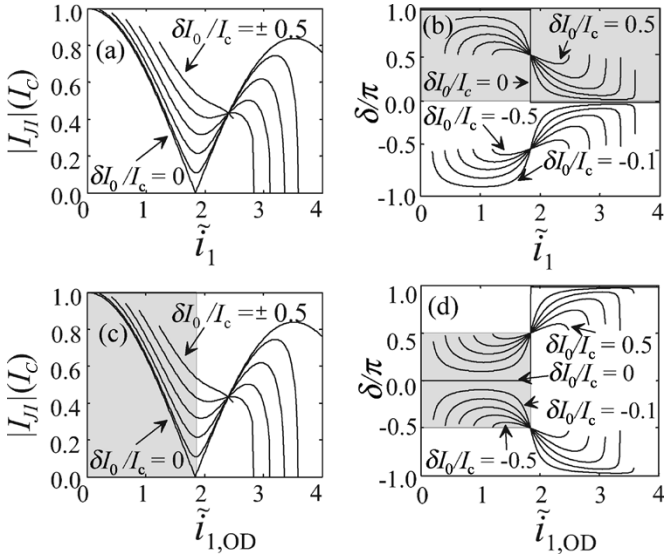

Fig. 4. (a) and (b): Amplitude $|I_{J1}|$ and phase δ for the first harmonic of step $n = 1$ of the tunnel current as a function of normalized microwave current for an underdamped junction. The dc bias point $\delta I_0/I_c$ is varied from -0.5 to 0.5 with step 0.1 as indicated in the legends. The regime where the junction attenuates the signal is shown grey. The signal is amplified elsewhere. (c) and (d): Corresponding plots for the overdamped case.

$$I_1(x) = I_1'(x)\exp(-j\beta x) + \exp(-j\beta x)\sum_{l_i<x} \frac{I_{J1}\left(I_0, I_1(l_i)\right)}{2j\omega C Z_0} \times \exp(j\beta l_i) + \exp(j\beta x)\sum_{l_i>x} \frac{I_{J1}\left(I_0, I_1(l_i)\right)}{2j\omega C Z_0}\exp(-j\beta l_i). \tag{6}$$

Solving this for I_1 is not quite straightforward. However, since we are mainly interested in the onset of the power self-generation, we assume that $I_1(l_i) \approx I_1' \exp(-j\beta l_i)$. This is valid if the self-generated signal is much smaller than the signal from the source. The self-generated signal has, thus, the same position dependence. We may write $I_{J1}(I_0, I_1(l_i)) = I_{J1}(I_0, I_1(0))\exp(-j\beta l_i) = I_{J1}(I_0, I_1')\exp(-j\beta l_i)$. It follows

$$I_1(x) = I_1'\exp(-j\beta x) + \frac{I_{J1}\left(I_0, I_1'\right)}{2j\omega C Z_0} \times \left(N(x)\exp(-j\beta x) + \exp(j\beta x)\sum_{l_i>x}\exp(-2j\beta l_i)\right) \tag{7}$$

where $N(x)$ is the index of the junction at position x. The self-generated current has two terms. The first term, a right-propagating wave, increases linearly toward the end of the array. The second term, a left-propagating wave, approximately averages to zero for long arrays. The asymmetry stems from the fact that the right-propagating wave propagates to the same direction as the signal from the generator and, thus, the junction currents add constructively. The main source of current inhomogeneity is the first term.

Everywhere else except at point $\tilde{i}_1 \approx 1.85$ and $\delta I_0/I_c = 0$, the generated signal is finite. The zero-generation point corresponds to the middle of the step, with the step amplitude maximized. Due to transmission line attenuation and parameter

scatter it is, however, impossible to bias all junctions at this point. Therefore, the self-generation always either amplifies or attenuates the signal. The signal is amplified, if the phase of I_{J1}/j is between $-\pi/2$ and $\pi/2$ (see (7)). The signal is attenuated otherwise. In Fig. 4(b) the gray-shaded area shows the range of bias parameters, where the signal is amplified. We see that the signal is amplified if the junction is biased above the middle of the step, and attenuated otherwise. The behavior is qualitatively similar for steps with $n > 1$.

A similar estimation can also be performed for the overdamped arrays by replacing the capacitive reactance $1/j\omega C$ by R in the derivation. The resulting amplitude $|I_{J1}|$ is the same as in the undamped or externally damped case except that $\widetilde{i}_1$ is replaced with $\widetilde{i}_{1,\mathrm{OD}} = 2\pi R I_1/\Phi_0\omega$ [see Fig. 4(c)]. The phases behave now differently [Fig. 4(d)]. The gray-shaded areas in Figs. 4(c) and 4(d) show again the area where the power self-generation amplifies the microwave signal. In this case, the amplification occurs if the microwave current amplitude is below the value maximizing the step width, whereas the microwave signal is attenuated if the amplitude is larger than this optimal value. Therefore, the junctions tend to compensate for the variation of the microwave signal along the transmission line. It compensates also for the attenuation, provided that the effect is strong enough. This has been detected experimentally [3] although not theoretically explained.

The stimulated power tends to cause an inhomogeneous microwave power distribution in case of frequency dependently damped SIS junctions. Therefore, its effect should be minimized. We derive an estimate of its magnitude. We see (Fig. 4), that $I_{J1}(I_0, I_1') \sim I_c$. On the other hand, we know that to maximize the step width, the microwave amplitude should be $I_1' = 2\pi(1+n)\Phi_0 f^2 C$ [6]. The maximum self-generated signal is $MI_{J1}(I_0, I_1')/2\omega C Z_0$ [see (7)], where M is the number of junctions in an array branch. The ratio of the stimulated microwave current to the incident microwave current is described by the gain parameter

$$\eta = \frac{MI_c}{8\pi^2\Phi_0(1+n)f^3C^2Z_0} \times 8.686\ \mathrm{dB}, \qquad (8)$$

which is given in dB for convenience. In the limit of small η, this directly describes the change in microwave power from the first JJ to the last one.

To compare with our experiments, we note that for our 10-V design, $\eta \approx 23$, 16, and 11 dB for steps $n = 1$, 2, and 3, respectively. On the other hand, for the 2×1.5-V design $\eta \approx 3.0$, 2.0, and 1.6 dB for corresponding steps. As a worst case, these add to the attenuation of the shunt resistors and the dielectric. This is estimated to be about 3 dB for both designs, which should be tolerated without a serious degradation of the step quality. Although the simplified calculation based on the linearization is not quantitatively valid for the large generated signals obtained here, one can anticipate problems if η is very large. Thus, the reduced step quality of the 10-V array can be explained by the gain factor. Also the suppression of step $n = 1$ for the 2×1.5-V array can possibly be explained by the same effect. It is also noteworthy that with our earlier designs [5] with $\eta \lesssim 1$ dB, the step amplitudes always decreased with increasing n.

To avoid the inhomogeneity, a safe criterion estimated from the discussion above for the present es-SIS array design is $\eta \lesssim 2$ dB. To design a 10-V array, we should drop η by a factor of 10 as compared to the current design. This can be done, for example, by doubling Z_0, dropping I_c and M into one half (the latter by dividing the signal into more branches). This would decrease the expected step width by one half and increase the required power by a factor of four. This would still be tolerable for stable operation with a realistic bias setup.

IV. Conclusion

We have demonstrated the operation of an optimized 2×1.5 V Josephson voltage standard based on es-SIS junctions. Furthermore, we studied increasing the output voltage up to 10 V. A limitation was found to be the self-generated power, which in case of es-SIS arrays causes an inhomogeneous microwave power distribution. The effect was analyzed and a design criterion to avoid it was derived.

References

[1] J. Kohlmann, R. Behr, and T. Funck, "Josephson voltage standards," *Meas. Sci. Technol.*, vol. 14, pp. 1216–1228, Jul. 2003.

[2] S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E. Harvey, and L. A. Christian, "Stable one volt programmable voltage standard," *Appl. Phys. Lett.*, vol. 71, pp. 1866–1868, Sep. 1997.

[3] H. Schulze, R. Behr, F. Mueller, and J. Niemeyer, "Nb/Al/AlO$_x$/Al/Nb Josephson junctions for programmable voltage standards," *Appl. Phys. Lett.*, vol. 73, pp. 996–998, Aug. 1998.

[4] H. Schulze, R. Behr, J. Kohlmann, F. Müller, and J. Niemeyer, "Design and fabrication of 10-V SINIS Josephson arrays for programmable voltage standards," *Supercond. Sci. Technol.*, vol. 13, pp. 1293–1295, Sep. 2000.

[5] J. Hassel, H. Seppä, L. Grönberg, and I. Suni, "SIS junctions with frequency dependent damping for a programmable Josephson voltage standard," *IEEE Trans. Instrum. Meas*, vol. 50, no. 2, pp. 195–198, Apr. 2001.

[6] ——, "Optimization of a Josephson voltage standard based on frequency dependently damped superconductor-insulator-superconductor junctions," *Rev. Sci. Instrum.*, vol. 74, pp. 3510–3515, Jul. 2003.

[7] P. Helistö, J. Nissilä, K. Ojasalo, J. S. Penttilä, and H. Seppä, "AC voltage standard based on a programmable SIS array," *IEEE Trans. Instrum. Meas.*, vol. 52, no. 2, pp. 533–537, Apr. 2003.

[8] J. Nissilä, A. Kemppinen, K. Ojasalo, J. Hassel, A. Manninen, P. Helistö, and H. Seppä, "Realization of a square-wave voltage with externally shunted SIS Josephson junction arrays for a sub-ppm quantum ac voltage standard," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 2, pp. 636–640, Apr. 2005.

[9] J. Hassel, H. Seppä, P. Helistö, J. Nissilä, and A. Kemppinen, "Fast Josephson arrays for voltage and impedance metrology," in *Proc. CPEM Conf. Dig.*, Jun. 2004, pp. 158–159.

[10] A. B. Cawthorne, P. Barbara, S. V. Shitov, and C. J. Lobb, "Synchronized oscillations in Josephson junction arrays: the role of distributed coupling," *Phys. Rev. B*, vol. 60, pp. 7575–7578, Sep. 1999.

[11] H. Schulze, F. Müller, R. Behr, J. Kohlmann, J. Niemeyer, and D. Balashow, "SINIS Josephson junctions for programmable Josephson voltage standard circuits," *IEEE Trans. Appl. Supercond.*, vol. 9, no. 2, pp. 4241–4244, Jun. 1999.