Programmable Josephson Voltage Standard Circuits Using Arrays of NbN/TiN/NbN/TiN/NbN Double-Junction Stacks Operated at 10 K

Mayumi Ishizaki, Hirotake Yamamori, Akira Shoji, Paul D. Dresselhaus, and Samuel P. Benz, *Senior Member, IEEE*

***Abstract*—Programmable Josephson voltage standard (PJVS) circuits using arrays of NbN/TiN/NbN/TiN/NbN double-junction stacks were fabricated and operated at a temperature of 10 K. Four arrays each with 32 768 junctions produced expected voltage outputs when driven at (10, 15, 17, and 20) GHz with an operating current range of 0.2–1.0 mA. Another circuit showed constant-voltage steps at ± 6 V when driven with an 11 GHz microwave bias, indicating that over 260 000 junctions were operating properly. This circuit did not show constant-voltage steps when driven with a 19 GHz microwave bias, which was the design frequency to achieve ± 10 V output voltage.**

***Index Terms*—Double-junction stack, Josephson junction, microwave, voltage standard.**

I. Introduction

A PROGRAMMABLE Josephson voltage standard (PJVS) was first demonstrated in 1995 [1] and has these attractive features: 1) submillisecond voltage settling time; 2) large operating current range ($>$ 1 mA); and 3) inherent voltage stability against noise. The first 1-V PJVS using junctions with normal-metal barriers was demonstrated in 1995 [2]. A 10-V PJVS chip using insulating-normal-insulating junction barriers was demonstrated in 2000 [3]. We have been developing a PJVS system using NbN/TiN/NbN junction arrays that can be operated with a compact 10-K cryocooler [4]. NbN has a critical temperature of ~ 16 K, and a chip consisting of NbN/TiN/NbN junctions can be operated at a temperature higher than that of liquid helium, which leads to a more compact system requiring lower power than one constructed with Nb junctions [5]. Progress has been made at both AIST [6] and NIST [7]–[10] to increase the output voltages of arrays with normal metal-barrier junctions by developing vertically stacked junctions. We have previously demonstrated operation of a PJVS chip with 1-V output using NbN/TiN/NbN/TiN/NbN double-junction stacks [11]. In this paper, we report additional progress toward the design and fabrication of PJVS chips with double-junction stacks, and present improved electrical characteristics of a number of different series arrays.

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M. Ishizaki, H. Yamamori, and A. Shoji are with the National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki 305-8568, Japan.

P. D. Dresselhaus and S. P. Benz are with the National Institute of Standards and Technology, Boulder, CO 80305 USA.

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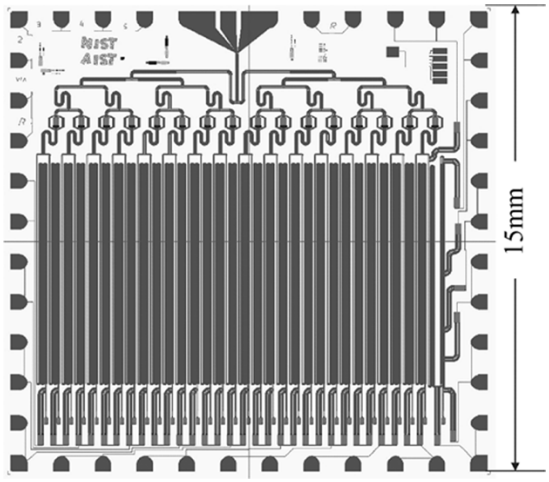

Fig. 1. Layout of metal layers in a PJVS chip.

II. Design

Fig. 1 shows the layout of metal layers in a PJVS chip designed for obtaining constant voltages of 5 or 10 V. The length of each side of the square chip is 15 mm. First, we had fabricated a chip using our single-barrier NbN/TiN/NbN junction technology, which yielded step amplitudes of about 1 mA at the 5-V target voltage. To achieve a 10-V target output voltage in the present study, we doubled the number of junctions using our double-junction stack technology with two TiN barriers in each stack [6]. Fig. 2 illustrates the equivalent circuit of a fabricated chip. There are 262 144 total junctions divided into 32 series-connected arrays of 8192 junctions. Microwaves are fed to the chip at the coplanar waveguide launch at the top and delivered to 32 parallel arrays of double-junction stacks through a 1:32 microwave distributor and 16-dc blocks. Each array has a 50-Ω termination resistor. The microwave distributor consists of coplanar waveguide splitters, while interdigitated capacitors define the dc blocks. Dc bias currents are supplied to the junctions through quarter-wave low-pass filters at the 19 GHz design frequency. One of the 8192-junction arrays is divided in a consecutive binary sequence into six smaller arrays of 256, 256, 512, 1024, 2048, and 4096 junctions which act as the least significant bits for the programmable source. Each of the seven most significant bits is composed of four series-connected 8192-junction arrays. Current bias and output voltage detection can be performed independently for each bit through separate bias taps.

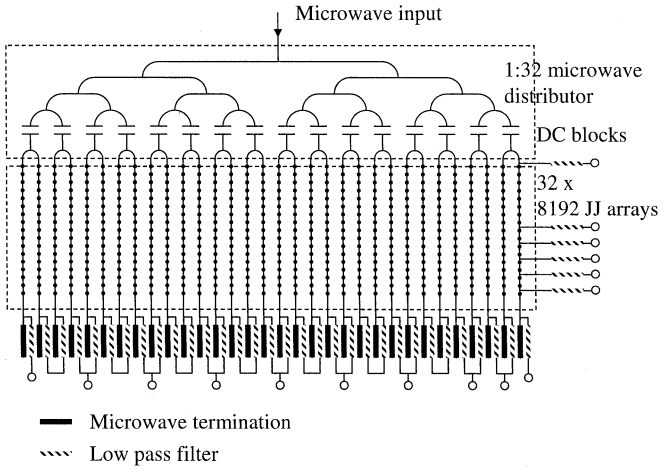

Fig. 2. Equivalent circuit of a PJVS chip.

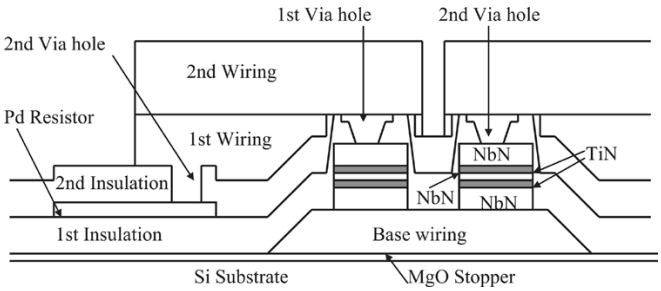

Fig. 3. Cross section showing two double-stacked junctions and the on-chip termination resistor of wafer #2.

III. Fabrication

The circuits were fabricated on a 3-in diameter Si wafer. Fig. 3 shows the cross section of the last two series-connected double-junction stacks in an array and the on-chip termination resistor. The fabrication process includes niobium nitride superconducting electrodes and wiring, silicon dioxide insulating layers, and palladium resistors. The metals and the oxide are rf sputtered, the metal layers are patterned with CF_4 reactive ion etching, and the vias are patterned with a mixture of CF_4 and H_2 reactive ion etching. A more complete description of the fabrication process can be found in [11]. Two wafers with different film thicknesses were fabricated and their properties are summarized in Table I.

IV. Measurement Arrangement

Fig. 4 shows a photograph of a fabricated voltage standard chip that is wire-bonded to a chip carrier. The center tap and the ground of the coplanar waveguide microwave launch are each attached with more than 10 wire bonds. Microwaves are launched to the chip through the carrier using a semirigid coaxial cable that is solder-bonded. The chip carrier is attached to a cryoprobe to which all of the microwave and dc bias leads are connected. The carrier and chip are shielded with a mu-metal box and then cooled to 10 K in the vapor of a liquid-helium dewar. The chips from the first wafer are biased using microwave signal generators and power amplifiers with maximum power output of 30 dBm. The smaller output voltages were measured with a nanovoltmeter. The chip from the second wafer is current-biased by a triangle current wave synthesizer, with a swept-signal generator as the microwave source, and the output voltage is measured using a 12-b digitizer. The microwave power is inferred from the power meter of the signal generator and the nominal gain of the power amplifier.

TABLE I
Fabrication Process

Layer	Deposition / Definition	Wafer #1	Wafer #2
MgO etch stop / NbN base wiring	rf-sputter / dry etch in CF_4+O_2	16/340 nm	16/320 nm
SiO_2 insulation	rf-sputter	400 nm	-
Base planarization	/ chemical mechanical polishing	130 nm	-
NbN/TiN junctions	rf-sputter / dry etch in CF_4	100/35/20/38/100 nm	100/32/20/35/100 nm
SiO_2 insulation	rf-sputter	150 nm	100 + Si50 + 50 nm
Pd resistors	rf-sputter / lift-off	50 nm	50 nm
SiO_2 insulation	rf-sputter	150 nm	100 + Si50 + 50 nm
Via holes	/ dry etch in CF_4+H_2	320 nm	420 nm
NbN wiring	rf-sputter	400 nm	400 nm
Planarization	/ chemical mechanical polishing	50 nm	50 nm
NbN wiring	rf-sputter / dry etch in CF_4	500 nm	500 nm

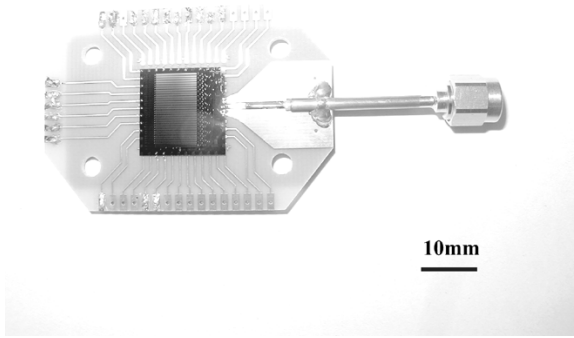

Fig. 4. PJVS chip mounted on a chip carrier showing the dc bias leads and the semirigid coax for microwave bias.

V. Current-Voltage Characteristics

A. Arrays With 32 768 Junctions

First we report the results of nanovoltmeter measurements for three 32 768-junction arrays on three different chips that were fabricated on the same wafer (wafer #1 in Table I). At 10 K and without microwave bias, the critical currents are about 5.0 mA for the four micrometer-square junctions. Fig. 5(a) shows the first constant voltage step for one of these arrays on the first chip driven with 20 dBm microwave bias at 10.69 GHz. The first step voltage is (724.357 ± 0.001) mV which indicates that all of the junctions in the array were on the step over a 0.8-mA operating current margin. This array also has flat constant-voltage steps at 14 GHz with a smaller 0.3-mA operating range.

Fig. 5(b) and (c) shows the first constant-voltage steps for an array on the second chip driven at two different frequencies. The first step voltage when driven at (b) 15.44 GHz and 24 dBm is

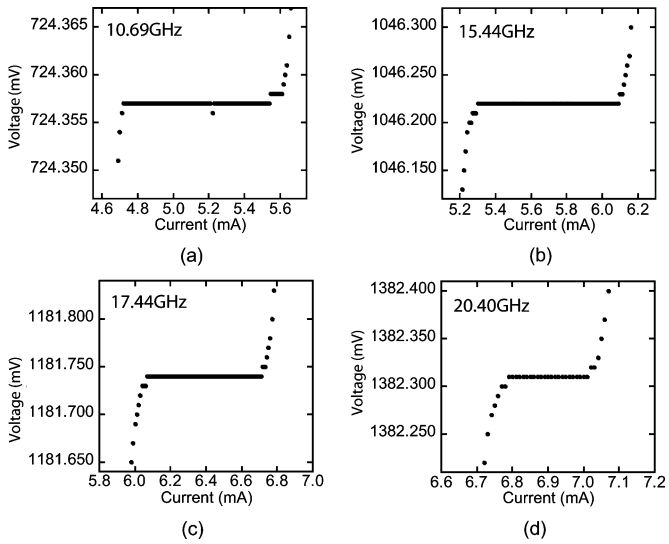

Fig. 5. Current-voltage characteristics of three different 32 768-junction arrays on three different PJVS chips from the same wafer. Microwave drive frequencies are at (a) 10.69 GHz (Array 1), (b) 15.44 GHz (Array 2), (c) 17.44 GHz (Array 2), and (d) 20.40 GHz (Array 3).

(1046.22 ± 0.01) mV. When the same array is driven at (c) 30 dBm at 17.44 GHz, the first step voltage is (1181.74 ± 0.01) mV. The maximum operating-current margin decreases from 0.8–0.6 mA as the frequency increases from 15.44 GHz to 17.44 GHz. This array also produced uniform constant-voltage steps (not shown) at (10 and 12) GHz with 1.0 mA and 0.8 mA current margins.

Fig. 5(d) shows the first constant-voltage step of an array on the third chip driven with 30 dBm microwave bias at 20.40 GHz. The first step voltage is (1382.31 ± 0.01) mV and has 0.2–mA maximum operating current margin. This array also produced constant-voltage steps at 15 GHz with a 0.8-mA current range.

All three arrays had the correct output voltages at the given frequencies indicating that in all cases every one of the 32 768 junctions in each array contributed to the total output voltage. We also conclude, as expected from junction dynamics, that the maximum operating current margin occurred at higher microwave power for higher microwave frequencies, while the current margin decreased. The three different arrays were from three chips taken from the same wafer and consequently they have an identical design and were produced with the same fabrication process. We observed no frequency dependence of the different arrays due to their position on a chip relative to the 32-way divider. However, slight differences in the deposited layer thicknesses due to different chip locations on the wafer could have caused differences in junction, termination resistor, or low-pass filter uniformities, which in turn could have led to the variations from chip to chip in microwave attenuation, microwave reflection or to nonoptimal behavior of the quarter-wavelength low-pass filters.

B. Array With 262 144 Junctions

Fig. 6 shows the current-voltage characteristic of a chip with 262 144 junctions driven with 11 GHz microwave frequency. Constant-voltage steps are observed at ± 5.96 V and appear flat

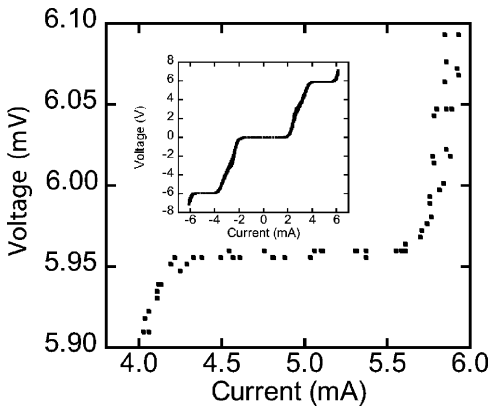

Fig. 6. Current-voltage characteristics of a PJVS circuit with 262 144 junctions biased at 11 GHz.

over a 1.3-mA current range within the 5-mV resolution on the ± 10 V scale of a 12-b digital-analog converter (DAC). A 10-V output voltage is considered large enough for many practical applications. This chip was designed to create 10-V output with 19 GHz microwave frequency, but failed to produce constant-voltage steps at the design frequency. Possible reasons for this are: 1) heating of the chip at high frequencies and the necessarily higher microwave power; 2) junction nonuniformity; and 3) microwave power inhomogeneity to the 32 different subarrays.

VI. Conclusion

With using a double-junction stack technology, three arrays with 32 768 junctions each showed constant-voltage steps at from 0.7–1.3 V with operating current ranges varying from 0.2–1.0 mA when driven with (10, 15, 17, and 20) GHz microwave bias and operated at 10 K. An array of over 260 000 junctions on a chip from another wafer showed constant-voltage steps at approximately ± 6 V over a 1.3-mA current range when driven with 11 GHz microwaves and operated at 10 K. Our goal is to realize 10-V PJVS system which is operated in a compact cryocooler at 10 K. In order to realize 10-V output voltage standard chips, we have been fabricating and testing new designs that are optimized for the higher microwave frequencies and have even more Josephson junctions. We are also trying new fabrication processes to improve the circuit fabrication yield and uniformity.

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