Josephson Voltage Standard - A Review

Clark A. Hamilton, Charles J. Burroughs, and Samuel P. Benz
National Institute of Standards and Technology, Boulder, CO 80303

Abstract — The unique ability of a Josephson junction to convert a microwave frequency f into a voltage $Nhf/2e$ with high accuracy and the adoption of this phenomenon as the basis for the SI Volt Realization have created a market for Josephson voltage standards that is unassailable from any other technology. This paper reviews the development of Josephson voltage standards including the junction and array design, the microwave circuit, and the system integration. With the dc Josephson standard largely transferred to the commercial sector, NIST is developing a new class of devices in which the output voltage can be rapidly programmed either by digitally selecting the quantum number N or by driving the Josephson array with a variable frequency pulse train. These new devices will make possible fast, high-accuracy characterizations of A/D and D/A converters and the synthesis of ac waveforms.

I. INTRODUCTION

The International System of Units, abbreviated SI, has been developed to meet the need for a uniform and consistent set of units [1]. One of the most important and widely used of these units is the volt. The SI definition of the volt is that electromotive force between two points on a conductor carrying a constant current of one ampere when the power dissipated between the two points is one watt. The base SI electrical unit, the ampere, is defined in terms of the force between two current-carrying wires one meter apart. The realization of the SI volt, therefore, depends on experiments that relate the volt and the ampere to mechanical units of length, force, and power. These experiments are exceedingly difficult and lead to an uncertainty in the SI volt of 0.4 parts in 10^6 (0.4 ppm).

Precise modern instrumentation requires voltage measurements with a reproducibility exceeding the accuracy with which the SI volt can be realized. To meet this need, realizations of the volt that are stable and reproducible at a level near 0.01 ppm have been developed even though their value relative to the SI volt is uncertain within 0.4 ppm. Before 1972, realizations of the volt were made by assigning values to carefully stabilized banks of Weston cells. These Weston cells served as a flywheel to maintain the unit of voltage between the comparison experiments with the SI definition of the volt. Drifts and problems with the transportability of Weston cells limited the uniformity of voltage standards around the world to about 1 ppm. The voltage standard clearly needed an intrinsic definition much like the definition of the meter in terms of the speed of light. Fortunately, such an intrinsic standard became feasible with the discovery of the Josephson effect in 1962 [2]. Brian Josephson derived an equation for the current that would flow through a tunnel junction formed by a thin insulating barrier separating two superconductors:

$$I = I_o \sin\left[\frac{4\pi e}{h}\int V dt\right] \tag{1}$$

In this equation, I is the junction current, I_0 is the critical current (a constant of the junction), V is the junction voltage, and e/h is the ratio of the elementary charge to Planck's constant. When a dc voltage is applied across the junction, Eq. (1) shows that the current will oscillate at a frequency $f = 2eV/h$, where $2e/h \approx 484$ GHz/mV. The very high frequency and low level of this oscillation make it difficult to observe directly. However, if an ac current at frequency f is applied to the junction, the junction oscillation tends to phase-lock to the applied frequency. During this phase lock, the average junction voltage must equal $hf/2e$. This effect, known as the ac Josephson effect, is observed as a constant-voltage step at $V = hf/2e$ in the current–voltage (I–V) curve of the junction. It is also possible for the junction to phase-lock to harmonics of f. This results in a series of steps at $V = nhf/2e$, where n is an integer, as shown in Fig. 1a.

The ac Josephson effect was initially used to improve the measurement of the constant $2e/h$. These measurements were limited by the accuracy of the voltage standard available at the experiment. Thus, in the early 1970s many nationl standards laboratories assigned a value to the Josephson constant $K_J = 2e/h$ and began using the ac Josephson effect as the practical standard of voltage [3]. Since there were small differences in national standards, several different values of K_J were in use around the word. By international agreement, effective January 1, 1990, K_J has now been assigned the value 483 597.9 GHz/V. Although the Josephson voltage standard (JVS) does not realize the SI definition of the volt, it provides a very stable reference voltage that can be reproduced anywhere without the need to transfer artifact standards such as Weston cells.

The accuracy of the Josephson voltage-frequency relation, $V=nf/K_J$, and its independence from experimental conditions, such as bias current and junction materials, have been subjected to many tests. No significant deviations from this relation have ever been found. In the most precise of these experiments, the voltage difference between two Josephson devices operating at the same frequency is less than 3 parts in 10^{19} [4].

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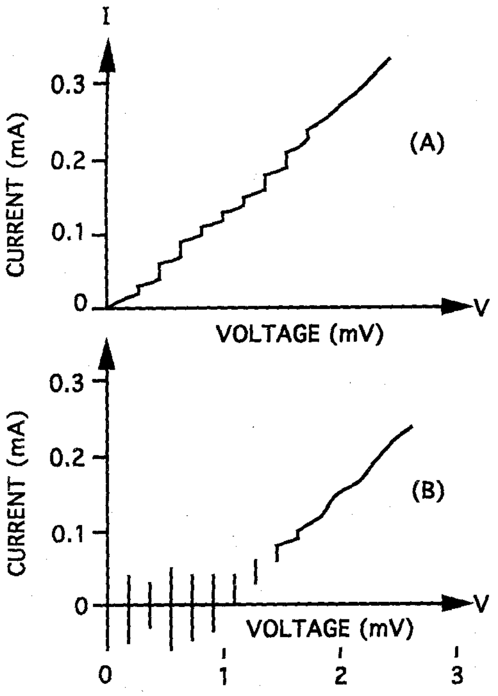

Fig. 1 Constant voltage steps for a junction driven with microwave current for (A) a low capacitance junction and (B) a high capacitance junction.

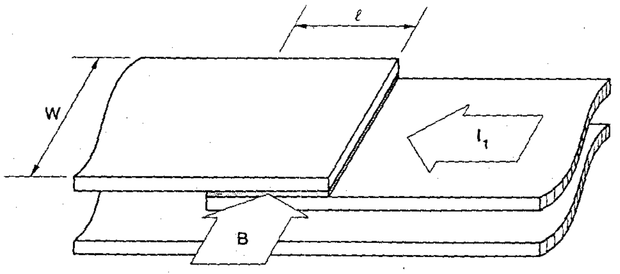

Fig. 2 The important parameters of a Josephson junction lying above a ground plane are the length ℓ, the width W, and the critical current density J.

Although the ac Josephson effect provides a much better voltage reference than standard cells, the first single-junction Josephson standards were difficult to use because they generated very small voltages (1-10 mV). Early attempts to add the voltages across many junctions were limited by the independent bias-current adjustment needed for each junction [5]. In 1984 a joint effort between the National Bureau of Standards and the Physicalishe Techniche Bundesanstalt in Germany resulted in a new design in which the multiple-bias problem was avoided by using constant-voltage steps that cross the zero-current axis of the junction [6]. These zero-crossing steps occur when junctions with a large capacitance, C, are driven by microwave current at a frequency well above the junction's plasma frequency, $f_p=(I_0 e/\pi h C)^{0.5}$. The plasma frequency is a natural junction resonance defined by the capacitance and inductance of the junction.

An I-V curve with zero-crossing steps is shown in Fig. 1b. The lack of stable regions between the first few steps means that for small dc bias currents, the junction voltage must be quantized. With a common bias current at or near zero, the voltage across a large array of these junctions must also be quantized. The first chips to implement this new design used about 2400 junctions to achieve voltages of 1 V. In 1987 the design was extended to a chip with 14 484 junctions that generated about 150 000 quantized voltages spanning the range from -10 to +10 V [7]. By 1989 all of the hardware and software required for a complete voltage metrology system was commercially available. Today there are Josephson voltage standards in more than 45 national, industrial, and military standards laboratories around the world.

II. JUNCTION PROPERTIES

The important parameters for the Josephson junction shown in Fig. 2 are its length, ℓ, width, W, critical current density, J, and the rf-drive frequency, f, The practical realization of an array voltage standard requires a thorough understanding of how these parameters affect the stability of the quantized voltage levels shown in Fig. 1b [8]. Stable operation requires that four conditions be satisfied: (1) ℓ must be small enough that the flux induced through the junction area by the ac magnetic field is much less than $h/2e$, (2) both W and ℓ must be small enough that the lowest resonant cavity mode of the junction is greater than f, (3) the junction plasma frequency, f_p, which is proportional to $J^{0.5}$, must be about one-third f, and (4) the junction's critical current, $I_0=W\ell J$, should be as large as possible to prevent quantum-step transitions due to noise. If any of these conditions is violated the junction voltage is likely to switch randomly among several steps and make measurements impossible. Table 1 lists a suitable set of design parameters.

Table 1. Junction design parameters.

Junction materials	$Nb/Al_2O_3/Nb$
Critical current density J	20 A/cm^2
Junction length ℓ	18 μm
Junction width W	30 μm
Critical current I_0	110 μA
Plasma frequency	20 GHz
Lowest resonant mode	175 GHz
rf drive frequency	75 GHz

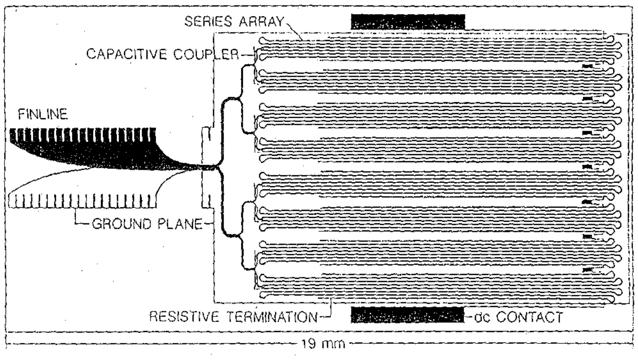

Fig. 3 The layout of a 20 208 junction array.

III. ARRAY DESIGN

A Josephson series-array voltage standard requires a circuit design that can deliver nearly uniform microwave power to many thousands of junctions, all of which are connected in series. A typical integrated-circuit layout for a 20-208-junction array is shown in Fig. 3. The rf-drive power is collected from a waveguide by a finline antenna, split 16 ways, and injected into 16 linear series-connected arrays of 1263 junctions each. The arrays are separated from a superconducting ground plane by SiO_2 dielectric and operate as microstriplines. Each stripline is terminated by a matched load. Addition of the dc voltages across the 16 arrays produces the reference-voltage output. Capacitors prevent the dc voltage from shorting through the rf-distribution network. The rf power is applied by inserting the finline end of the chip into a slot parallel to the E-field in a WR-12 waveguide. The dc output appears across superconducting pads on the edge of the chip. The number of junctions in each stripline section is limited by the attenuation in the stripline, which is estimated to be 0.004 dB per junction. After passing through about 1200 junctions the microwave power is significantly below the optimum value for step generation. At 72 GHz, each junction generates about eight quantum voltage levels separated by $f/K_J \approx 150\ \mu V$. The array shown in Fig. 3 can generate about 150 000 levels spanning the range from -10 to +10 V.

Voltage standard chips are fabricated on silicon or glass substrates. The integrated circuit has eight levels: (1) a 300-nm niobium ground plane that shields the circuit from outside interference and defines the impedance of the microstriplines, (2) a 1000-nm layer of SiO_2 that forms the microstripline dielectric, (3) a 200-nm niobium film that forms the lower electrode of the Josephson junctions, (4) a 3-nm metal oxide layer that forms the Josephson tunneling barrier, (5) a 100 nm niobium counter electrode, (6) windows in a 300-nm SiO_2 film that define the contact to the counter electrode, (7) a 400-nm film of niobium that connects the junction counter electrodes, and (8) a 100-nm resistive film that forms the stripline terminations.

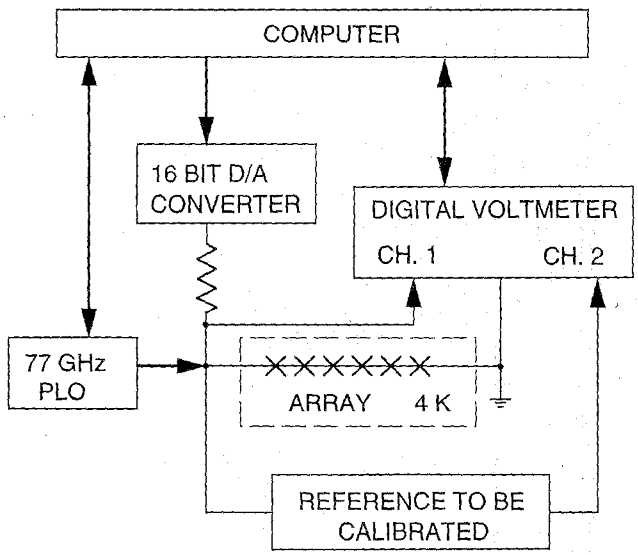

Fig. 4 A simplified block diagram of an automated Josephson voltage standard.

IV. VOLTAGE STANDARD SYSTEMS

The block diagram of a modern Josephson voltage-standard system is shown in Fig. 4. The Josephson array chip is mounted in a magnetic shield and immersed in liquid helium or cooled with a closed cycle cryocooler. A phase-locked oscillator (PLO) operating at a fixed frequency near 75 GHz provides the microwave power to the chip. Bias current for the array is supplied by a 16-bit digital-to-analog converter (DAC). One channel of a two-channel voltmeter monitors the array voltage and other diagnostic system parameters. The second channel is a high sensitivity null meter that is used to measure the difference voltage between the Josephson array and an external device to be calibrated. All system adjustments and data collection are controlled by a computer that can perform calibration, record-keeping, and diagnostic functions. Several software packages have been developed to automate all of the system functions. The PLO, array bias circuit, 2-channel DVM, and diagnostic electronics have recently been integrated into a single 13 cm-high rack-width box [9].

Systems like that shown in Fig. 4 are used to calibrate secondary standards, such as Weston cells, Zener references, and precise digital voltmeters. These calibrations are greatly simplified by the fact that the Josephson array voltage can be set to any value $V = nf/K_J$ where the integer n can have any value in the range of about -75 000 to + 75 000. In a typical dc reference standard measurement, the reference and Josephson array are connected in series opposition across the null meter. The automatic bias circuit then selects a value of n such that the array voltage is within a few millivolts of the reference voltage. The reference voltage is then given by $nf/K_J + V_{null}$. The effects of noise and thermal voltages are

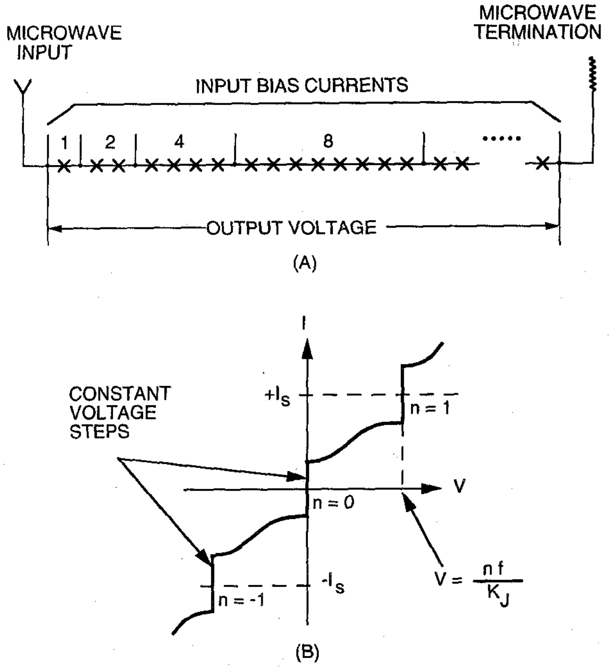

Fig.5 (A) A programmable Josephson array consisting of a set of binary array segments and (B) the junction *I-V* curve that is required for a programmable voltage standard.

greatly reduced by reversing the reference voltage and time averaging null measurements over several minutes. The typical uncertainty in these measurements is limited by noise in the reference to about 0.01 ppm. An international program of direct comparisons between Josephson standards at national standards laboratories and the travelling Josephson standard of the Bureau International des Poids et Mesures (BIPM) has found no significant differences at an uncertainty level below 0.001 ppm. The ability to set the Josephson array to a wide range of discrete voltages also makes it the most accurate tool for measuring the linearity of high accuracy digital voltmeters.

V. PROGRAMMABLE VOLTAGE STANDARDS

Two disadvantages of Josphson voltage standards based on the zero-crossing steps of series arrays of hysteretic junctions are that the step number n cannot be quickly set to a desired value and noise may cause spontaneous transitions between steps. In the case of classical dc measurements, this is a minor inconvenience that can be easily dealt with in software. However, the step stability and selection problem precludes measurements such as the fast analysis of A/D and D/A converters and the synthesis of ac waveforms with a computable RMS value.

A new type of Josephson voltage standard is under development in which the output voltage $V = nf/K_J$ is defined by digitally programming the step number n. In this circuit, an array of nonhysteretic junctions is divided into a binary sequence of array segments, as shown in Fig. 5a. The microwave excitation for each junction is set to equalize the amplitude of the n=0 and n=1 steps, as shown in Fig. 5b. Each segment of the array can be set to the n=-1, 0, or +1 step by applying a bias current ($-I_s$, 0, $+I_s$) at the appropriate nodes. The combined step number N for the whole array can thus be set to any integer value between $-M$ and $+M$, where M is the total number of junctions in the array [10].

The rapid settling time and inherent step stability of the JVS in Fig. 5 make it potentially superior to a conventional JVS for dc measurements. (We define a dc measurement to be one in which the transient associated with changing N can be excluded from the measurement.) Such measurements include calibration of dc reference standards and digital voltmeters, and the characterization of A/D and D/A converters.

The circuit of Fig. 5 can also generate a staircase approximation to a sine wave by selecting appropriate step numbers in rapid succession. In theory, the resulting waveform has a computable rms value and might be used to confirm the ac-dc difference of a thermal voltage converter and for other ac measurements. In the case of ac measurements, however, the transient waveform during step transitions is included in the rms value and may lead to an unacceptably large uncertainty.

Practical measurements may also require an output current of several milliamperes – well beyond the current sourcing capability of a typical Josephson array. These problems are resolved by adding a semiconductor D/A converter that supplies the predicted load current through a small resistor[10]. The array then acts as a fine trimmer by sinking or sourcing just enough current to bring the output voltage to the correct value. This addition to the bias circuit amplifies the available output current and minimizes transients at the step transitions.

VI. SIS VS. SNS JUNCTIONS

Experimental realization of the programmable JVS has been pursued with both superconductor-insulator-superconductor (SIS) and superconductor-normal-metal-superconductor (SNS) junctions. In the case of SIS junctions, the required nonhysteretic *I-V* curve is achieved by adding a shunt resistor in parallel with each junction. Theoretical analyses [11]-[13] have shown that the best combination of bias margin, stability, and microwave drive power is achieved when the step voltage f/K_J is approximately equal to $I_c R$, where I_c is the junction critical current and R is the shunt resistor. In practice, the shunt resistor has an unavoidable parasitic inductance on the order of 1 pH. The resistor is effective only if its inductive reactance at the drive frequency f is small compared to its resistance. Thus for practical frequencies, $f < 100$ GHz, the maximum critical current is about 300 μA. The shunt resistor for SNS junctions is inherent to the metallic barrier, and its inductance

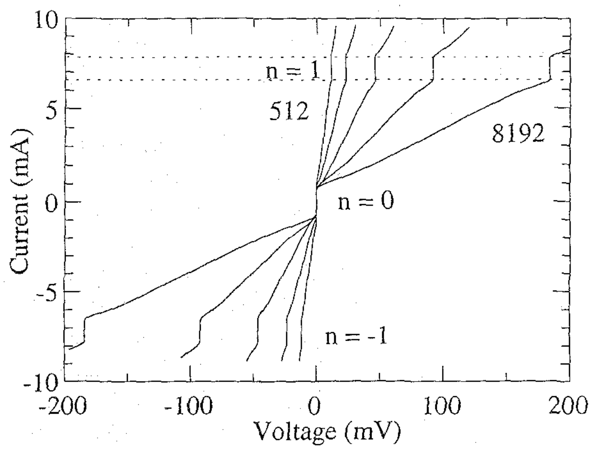

Fig. 6 *I-V* curves for five segments of a programmable SNS junction aray. The applied microwave power at 11 GHz is the same for all five curves.

is negligible. In this case, I_c is only limited by the available microwave power and/or heating effects, and step amplitudes of several milliamperes are easily achieved. Large critical currents are essential to achieve the noise immunity that high speed operation demands. For this reason, the SNS junction geometry is now the preferred design for programmable voltage standards.

SNS junctions are intrinsically shunted by the conductivity of the metallic barrier. The junctions that we are using have a palladium-gold barrier for which the I_cR_N product is typically 5-20 μV [14]. Using the condition that $f \approx I_c R_N K_J$ as described above leads to an optimum drive frequency near 8 GHz. The arrays work nearly as well at frequencies up to 15 GHz so we use this higher frequency to increase the output voltage range. Since the resolution of this type of Josephson standard is given by the step separation, the lower frequency relative to the SIS design results in higher resolution at the expense of requiring more junctions per volt of output range. (At 15 GHz, 32 240 junctions are required for 1 V.) Fortunately the SNS junction process is able to generate large arrays of highly uniform 2.5 μm diameter junctions with critical currents near 5 mA [14]. With such high critical current density (100 000 A/cm^2) and the corresponding high bias currents, we have encountered difficulty with breakdown of wiring contacts in the circuit. Also, for $I_c > 5$ mA, the rf power dissipated in each junction ($P \approx I_c f / K_J$) leads to excessive chip heating for very large arrays [15]. Figure 6 shows *I-V* curves of the segments 512, 1024, 2048, 4096, and all 8192 junctions of an 8-segment SNS junction array operated at 11 GHz. (The maximum voltage is 186 mV.) The n=-1, 0, and +1 steps are all larger than 1 mA and occur over identical bias current ranges for every segment. This precise matching of the *I-V* curves of thousands of junctions is one of the critical requirements of a programmable array.

The junctions are arranged in series along the center conductor of a 50 Ω coplanar waveguide. In contrast to the 3 Ω striplines used in the SIS design, the 50 Ω coplanar design eliminates two fabrication levels. Also, because of the larger ratio of line impedance to junction resistance, it is possible to maintain the required rf power uniformity through a larger number of junctions. The lower frequency used in the SNS design makes the rf dividing network too large to fit on the chip, so most of the divider network is on the finger contact board to which the chip mounts. Typically 4096 junctions are used in each branch of the rf distribution network. A 32 768 junction SNS array designed to reach 1 V is under development [15]. An important goal of this circuit is the direct measurement of the ac/dc difference of a thermal voltage converter (TVC). Since the array can be programmed to generate either ac or dc, this measurement can be made without switching between sources. A variety of difficulties including junction yield, flux trapping, and circuit contact breakdown has limited these measurements to an array of 4096 junctions operating at 13.2 GHz to generate a maximum voltage near 0.1 V. In the best result to date, an ac/dc difference of $\delta = 4 \pm 7$ ppm has been measured [15]. The uncertainty in this measurement needs to be improved by about an order of magnitude to match the state-of-the-art for other indirect methods of measuring δ. This can easily be achieved with larger programmable arrays that can generate voltages above 1 V.

VII. PULSE DRIVEN VOLTAGE STANDARDS

Thus far, we have discussed ways to program the voltage of a Josephson array by changing the step number N in the equation $V = Nf/K_J$. It is also clear that the same result might be achieved by changing f. Unfortunately, in the case of a sine wave excitation the step amplitudes collapse rapidly to zero as the frequency decreases. This means that it is practical to control the voltage via the frequency only over a range of frequency within about a factor of 2 of the optimum frequency $f_c = I_cRK_J$. Recently Benz et al. have shown that if the sine wave excitation is replaced with a pulse excitation, then the step amplitude is independent of the pulse repetition frequency for all frequencies below f_c [16]-[17]. The optimum pulse width is $\tau = 1/(2\pi f_c.)$. Figure 7 is a calculation of the n=1 step boundaries for a junction driven with a sine wave (shaded area) and a pulse train (black area) Note that the pulse driven step amplitude is large, symmetric around zero, and independent of frequency all the way to zero frequency. In fact, if the pulse polarity is reversed at zero then the array can generate both positive and negative voltages.

A programmable voltage source based on this idea would consist of a single large array of N junctions distributed along a wide bandwidth transmission line. A pulse train at frequency f propagating down the line would generate an average voltage Nf/K_J across the ends of the array. A complex output waveform can be generated by modulating the pulse train with a long-digital-word generator.

For example, using a clock frequency of $f_c = I_cRK_J = 10$ GHz, the pulse sequence 11111000001111100000.... would create an output square wave of amplitude of Nf_c/K_J and frequency of 1 GHz.

In order for this circuit to work properly it is essential that the pulses remain undistorted as they pass through the series array of junctions and by the output voltage taps. This means that the filters need to look like an open circuit over a bandwidth of at least $f_c/10 < f < f_c$. The filter must not generate reflections that distort the pulses in the line. Achieving this filter characteristic in a thin film design that can be implemented on chip is a significant microwave design challenge.

CONCLUSION

The accuracy and stability of voltage standards based on the Josephson effect far surpass those of all other voltage standard devices. The voltage generated is independent of environmental and material characteristics because it is based on a fundamental constant, the ratio of the elementary charge to Planck's constant. International agreement on a defined value, K_J = 483597.9 GHz/V of this constant ensures uniformity and reproducibility throughout the world. Commercialization has made this technology widely available.

The feasibility of programmable Josephson voltage standards for fast dc measurements and waveform synthesis has been demonstrated. A new SNS junction technology is being developed to make high critical current, self-shunted junctions, that have the noise immunity, I_cR_N product, and output drive capability that are required to achieve practical waveform synthesis. Present devices are limited by fabrication technology to a maximum output voltage of about 300 mV and are susceptable to transient induced magnetic flux trapping. The flux trapping problem is likely to be solved by improving the critical currents of wiring films and contacts within the circuit. As the fabrication yield improves, output voltages of 1-10 V should be possible. Sine waves synthesized from a programmable Josephson array will bypass the usual thermal methods and provide an ac standard that is derived directly from the international realization of the volt. In the near term, it is likely that programmable Josephson voltage standards will find their greatest use in fast automated dc measurements and in ac measurements at low voltages or frequencies. Success of the pulse-driven programmable voltage standard will substantially extend the output bandwidth of Josephson waveform synthesizers.

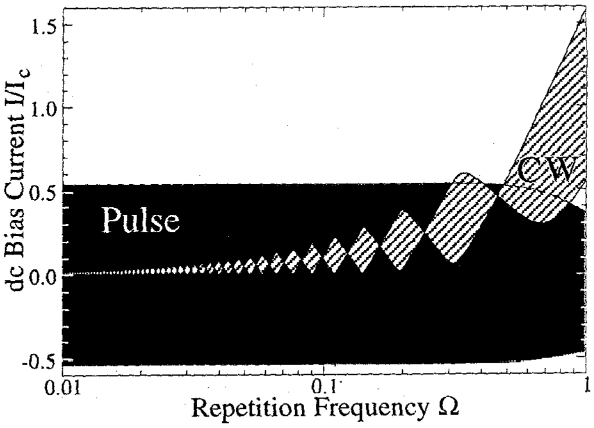

Fig. 7 Comparison of the normalized n=1 step boundaries for a junction driven with a pulse train (black) and a continuous sinewave (shaded) as a function of normalized frequency $\Omega = f/f_c$.

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