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Josephson voltage standards

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Abstract
This paper reviews the present state of modern Josephson voltage standards. The presentation focuses on conventional dc standards based on underdamped superconductor–insulator–superconductor junctions and programmable standards based on overdamped superconductor–insulator–normal conductor–insulator–superconductor junctions. The current developments of ac standards on the basis of pulse-driven arrays and single flux quantum-based voltage multipliers are briefly summarized.

Keywords: conventional and programmable Josephson voltage standards, SIS Josephson series arrays, SINIS Josephson series arrays, quantum voltmeter

(Some figures in this article are in colour only in the electronic version)

1. Introduction

In metrology, macroscopic quantum phenomena have increasingly gained in importance in recent years. Reference of the units to artifacts has been replaced by reference to physical constants. Nowadays, the unit of voltage, the volt, which is one of the most important electrical units, is reproduced by a quantum standard based on the ac Josephson effect. Fundamentally, the Josephson effect is due to the tunnelling of Cooper pairs formed by bound pairs of electrons occupying states with equal and opposite momentum and spin. As an illustration, a voltage is generated by the specific transfer of flux quanta $\Phi_0 = h/2e$ through Josephson junctions consisting of two weakly coupled superconductors (h denotes Planck's constant and e the elementary charge). The irradiation of the Josephson junctions with microwaves of frequency f (usually in the range from 70 to 100 GHz) effects this specific transfer and produces steps of constant voltage V_n (n denotes the integer step number, i.e. the number of flux quanta which are transferred by each period of the microwave):

$$V_n = n\Phi_0 f$$

as had been predicted by Josephson (1962) and was first observed by Shapiro (1963). The Josephson effect thus reduces the reproduction of voltages to the determination of a frequency and this can be finely controlled with high precision and accurately referenced to caesium atomic clocks. To take full advantage of the high-precision voltages reproduced by Josephson voltage standards, which are by orders of magnitude more precise than the SI realization of the unit volt, for applications such as calibrations, a conventional value for the Josephson constant $K_J = 1/\Phi_0$ has been assigned by international agreement. The agreement of the value $K_{J-90} = 483\,597.9$ GHz V^{-1} took effect on 01 January 1990 (Quinn 1989).

A single Josephson junction generates voltages of a few millivolt at most. Today highly integrated series arrays are used to achieve output voltages of 1 or 10 V. These modern Josephson array voltage standards (JAVS) consisting of up to about 20 000 Josephson junctions are typically fabricated on silicon wafers using industrial deposition and structuring procedures, including patterning by photolithography. The superconducting layers are typically fabricated from durable materials such as niobium. The weak coupling of the superconductors is ensured by an insulator based on thermally grown Al_2O_3 or a normal conductor (e.g. AuPd or HfTi), resulting in underdamped SIS (superconductor–insulator–superconductor) junctions or overdamped SNS (superconductor-normal conductor-superconductor) junctions, respectively. The use of an $Al_2O_3/Al/Al_2O_3$ multilayer is another possibility for realizing overdamped SINIS (superconductor–insulator–normal conductor–insulator–superconductor) junctions.

Several papers have reviewed the development and use of the JAVS (Niemeyer 1998, Hamilton 2000, Yoshida 2000, Behr *et al* 2002) as well as the fundamentals, including simulations

(Kautz 1996). The early state of this development is described by Niemeyer (1989), Kautz (1992) and Pöpel (1992). The present paper summarizes the current state of modern Josephson voltage standards. The presentation focuses on standards based on conventional SIS and novel SINIS junctions. Section 2 briefly discusses some fundamentals of the physics and design rules. The conventional SIS Josephson voltage standard is presented in section 3. The new programmable voltage standards are described in section 4, including first applications. Section 5 gives a summary.

2. Fundamentals

The main characteristics of Josephson junctions and the requirements for their stable operation in the Josephson voltage standard are briefly summarized in this section. Detailed descriptions have been given in several reviews (e.g Josephson 1964, Kautz 1992, Rogalla 1998) and textbooks (e.g. Barone and Paternò 1982, Likharev 1986, Kadin 1999).

2.1. Josephson effects

A Josephson junction consists of two weakly coupled superconductors. Besides a dc supercurrent $I = I_c \sin\varphi$ (I_c denotes the critical current and φ the difference in phase between the macroscopic wavefunctions of the two superconductors), the main feature of a Josephson junction is an ac supercurrent of frequency $f_J = (2e/h)V$ if the junction is operated at a non-zero voltage V, i.e. the Josephson junction is an oscillator. Irradiation of the junction with microwaves of frequency f vice versa produces steps of constant voltage due to the phase locking of the Josephson oscillator by the external oscillator:

$$V_n = n(h/2e)f$$

($n = 1, 2, 3, \ldots$ denotes the integer step number). A Josephson junction thus is a strongly non-linear system. To assure stable operation of this non-linear system which can show chaotic behaviour, several parameters must be suitably adjusted.

The dynamics of Josephson junctions is often investigated using the resistively-capacitively-shunted-junction (RCSJ) model (Stewart 1968, McCumber 1968). Within this model, the physical Josephson junction is described as a parallel shunting of an ohmic resistance R, a capacitance C and an ideal Josephson element. In the linear approximation, the resonance frequency is given by the plasma frequency $f_p = (ej_c/\pi hC_s)^{1/2}$ (j_c denotes the critical current density, $C_s = C/A$ the specific junction capacitance and A the junction area). Details of the behaviour depend on the kind of the junction and this can be characterized by the dimensionless McCumber parameter $\beta_c = Q^2$ being equal the square of the quality factor $Q = 2\pi f_p RC$ of the junction: underdamped junctions with $\beta_c > 1$ show a hysteretic I–V characteristic, overdamped junctions with $\beta_c \leqslant 1$ a non-hysteretic one.

2.1.1. Underdamped Josephson junctions. Underdamped junctions are realized using SIS junctions which today usually consist of an Nb/Al_2O_3/Nb trilayer. When the microwave frequency and the junction materials are chosen, only three parameters must be adjusted to maximize the stability of the phase lock and to assure the generation of stable steps of constant voltage. These parameters are the critical current density j_c, the length l, and the width w of the junction, as was shown by investigations of Kautz *et al* (1987) and Kautz (1992) on the basis of the RCSJ model.

The critical current density follows from the requirement that the microwave frequency f must be higher than the plasma frequency f_p. Simulations by Kautz *et al* (1987) have shown that the ratio should be at least $f/f_p \approx 3$. They regarded the average time between phase slips induced by Johnson noise as a measure of stability. The phase slips by 2π with respect to the external frequency resulting in a short break of the phase lock between Josephson oscillator and external frequency. The phase slip often causes a switch from one step to another and therefore determines the stability. The maximum value of the critical current density is given by

$$j_{c,max} = (f/3)^2 \pi hC_s/e.$$

The limitations of the length l and the width w of the junction follows from the requirement of spatial uniformity of the phase between the superconductors. The optimum length effects maximization of the phase lock stability. Kautz *et al* (1987) calculated this length to be

$$l = \lambda_J (3j_c/\pi f C_s V_n)^{1/2}.$$

($\lambda_J = \{h/[4\pi e\mu_0 j_c(d+\lambda_{L1}+\lambda_{L2})]\}^{1/2}$ denotes the Josephson penetration depth, μ_0 the magnetic permeability of the vacuum, d the barrier thickness, λ_{L1} and λ_{L2} the London penetration depth of the junction electrodes.)

The width of the junction is limited to avoid excitation of Fiske resonances (geometric resonances). This leads to an upper limit of the width (Kautz *et al* 1987):

$$w = (1/2f)[\mu_0 C_s(d + \lambda_{L1} + \lambda_{L2})]^{1/2}.$$

Following the calculations of Kautz *et al* (1987) who performed an estimation of the critical current density and further calculations of the activation energy for loss of the phase lock, a high frequency of irradiation should be chosen. An additional advantage of a high frequency is a high output voltage. At present, most JAVS are therefore operated at frequencies between 70 and 100 GHz, a range where oscillators (Gunn oscillators in most cases) are available with an output power of up to about 100 mW.

2.1.2. Overdamped Josephson junctions. The behaviour of overdamped Josephson junctions differs from that of underdamped ones. Damping of the junctions can suppress the chaotic behaviour. Overdamped junctions can be realized by shunting junctions intrinsically or externally. Intrinsically shunted junctions have the advantage that the fabrication process is easier and less space is required. Overdamped, intrinsically shunted junctions have been realized using SNS junctions (consisting, for example, of AuPd (Benz 1995), Ti (Schubert *et al* 2001a), or HfTi (Hagedorn *et al* 2001) as normal conductor) or SINIS junctions consisting of an Nb/Al_2O_3/Al/Al_2O_3/Nb multilayer (Schulze *et al* 1998).

Kautz (1995) performed simulation calculations of Shapiro steps in SNS Josephson junctions. He found that an optimal formation of Shapiro steps could be defined when the zero step and the first step are of the same size. The microwave power required to generate these steps scales with the critical current. The homogeneous distribution of the microwave power is an important requirement for large series arrays. To assure large step width at moderate microwave power, the junction area should not exceed $2\lambda_J$ for configurations with a ground plane and $4\lambda_J$ for those without a ground plane. The microwave frequency f should be about the characteristic frequency $f_c = 2eI_cR_n/h$, i.e. $f/f_c \approx 1$. Enhanced stability against external noise is reached for slightly higher frequencies using $f/f_c = 2, \ldots, 3$. The value $f \approx f_c$ yields the greatest tolerance of the step position with respect to a distribution of critical currents among the junctions. The chosen operating frequency is, therefore, a compromise between the different criteria.

Although the simulations were performed for SNS junctions, similar restrictions apply for SINIS junctions as well.

3. Conventional SIS Josephson voltage standards

The realization of modern conventional Josephson voltage standards takes advantage of two important ideas. First, highly underdamped junctions with hysteretic I–V characteristics produce constant voltage steps whose current ranges overlap one another for small bias currents. This idea was suggested by Levinson *et al* (1977). This means that a single bias current source can be used to bias all junctions of a series array on quantized steps of constant voltage. Underdamped junctions take the form of SIS junctions. Secondly, the Josephson junctions are integrated into a microwave transmission line (cf figure 1(a)) which was first realized by Niemeyer *et al* (1984). Because of this arrangement, the Josephson junction series array is connected in series for the dc bias and acts as a microstripline at rf frequencies. As the microwave power is mainly capacitively coupled to the junctions, the rf attenuation of the series array is very low, therefore enabling uniform rf bias of all junctions.

3.1. Fabrication process

Modern Josephson voltage standard arrays are typically fabricated using the reliable Nb/Al_2O_3 technology developed by Gurvitch *et al* (1983). Many improvements of the fabrication process and the intensified use of technological procedures of semiconductor industry made possible the fabrication of voltage standard arrays consisting of Nb/Al_2O_3/Nb Josephson junctions (Niemeyer *et al* 1986). In the course of time, this technology was adopted by all institutes fabricating 10 V series arrays (Pöpel *et al* 1990, Hamilton and Burroughs 1995, Endo *et al* 1995, Radparvar 1995, Schubert *et al* 2001b) and 1 V series arrays (Park *et al* 1995).

Figure 1(a) schematically shows the integration of the Josephson junctions into the microstripline. The fabrication process of PTB yields the highest quality junctions when the Nb/Al–Al_2O_3/Nb sandwich is directly deposited onto the wafer (Müller *et al* 1995, 1997a). The thick SiO_2 dielectric and the groundplane of the microstripline are then arranged above the patterned array. The quality was further improved by use of a modified anodization process for the insulation of the junction edges (Müller *et al* 1997b).

The main steps of the PTB fabrication process are briefly summarized below. First, as an etch stop layer, a 30 nm thick Al_2O_3 layer is sputtered onto the thermally grown SiO_2 of the 3 inch Si wafer. The Nb/Al_2O_3/Nb trilayer deposited by dc magnetron sputtering consists of a 170 nm thick base electrode, a 10 nm thick Al layer, and a 85 nm thick top electrode. The Al layer is oxidized for 18 h in O_2 at 200 mbar and 30 °C, which results in a critical current density j_c of about 10 A cm^{-2}. The trilayer is patterned by reactive ion etching (RIE) in CF_4 (Nb top electrode) and by a combination of physical sputter etching in Ar and wet etching (Al–Al_2O_3). Using the photoresist pattern for the anodization process which covers the entire wafer, the Nb base is removed between neighbouring base areas by RIE in CF_4. The edges of the trilayer are subsequently insulated by anodization in ethylene glycol with ammonium pentaborate in aqueous solution up to a voltage of about 35 V (Kroger *et al* 1981). An additional SiO_2 layer 250 nm in thickness is sputter-deposited and patterned by RIE ($CHF_3 + O_2$) to improve the insulation. After careful cleaning of the Nb top electrode by rf-sputtering, the wafer is covered by the Nb wiring layer 450 nm in thickness. The Josephson junction area is defined by etching the wiring layer and the top electrode in a single RIE step. The junction area is determined by the overlap of wiring and base electrode. The dielectric for the stripline is produced by a sputtered SiO_2 layer about 2 μm in thickness. The load resistance of the stripline is made of a 350 nm thick AuPd layer that is formed by dc magnetron-sputtering and patterned by a lift-off process. Finally, the Nb groundplane 250 nm thick, which covers the Josephson junction series array, is dc-sputtered and patterned by RIE.

3.2. Design

The uniform microwave power distribution over all junctions is an important requirement for the formation of stable and wide steps. To achieve this, most present designs integrate the Josephson junctions into a low-impedance microstripline taking into consideration the conditions discussed in section 2.1.1 (Kohlmann *et al* 1997b, Hamilton and Burroughs 1995, Radparvar 1995, Endo *et al* 1995, Park *et al* 1995, Meyer *et al* 1999). Recently, Schubert *et al* (2001b) realized first 10 V arrays using a coplanar stripline (figure 1(b)). First measurement results were very promising; these new arrays work as well as microstripline arrays. This new concept simplifies the fabrication process by eliminating the need for several layers, including the thick dielectric, the ground plane and the load.

At present, all of the series array Josephson voltage standards operated throughout the world are based on microstripline designs. The most recent PTB design for 10 V arrays is shown in figure 2 (Kohlmann *et al* 1997b). An antipodal fin-line taper serves as an antenna to connect the microstripline, consisting of the series array of Josephson junctions, to the E-band rectangular waveguide while at the same time matching the impedance of the waveguide (about

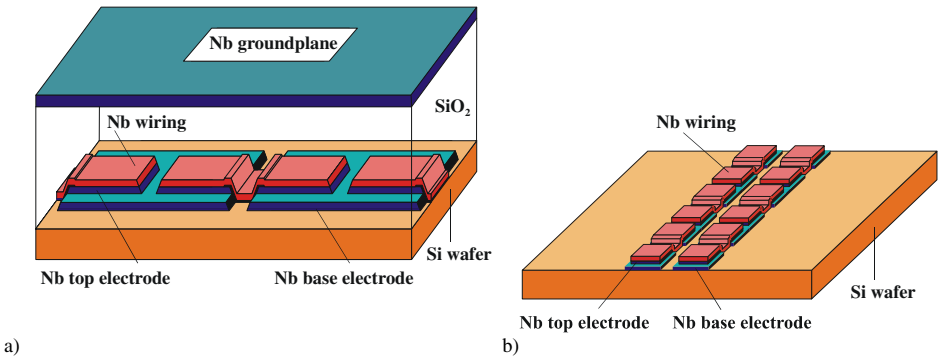

Figure 1. (a) Cross section of the microwave stripline. (b) Cross section of the coplanar stripline: the Josephson junctions are integrated into the two strips of the coplanar stripline.

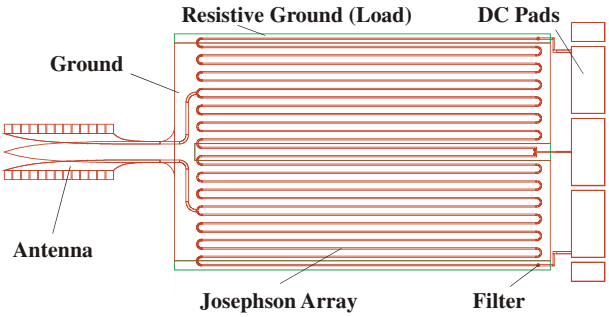

Figure 2. Design of a 10 V Josephson voltage standard array consisting of 13 924 Josephson junctions. The length and the width of the junctions is 18 μm × 50 μm. The length of the chip is 24 mm.

520 Ω) to that of the microstripline (about 5 Ω) (Hinken 1983, Hinken *et al* 1986). The microstripline is split in two stages forming four parallel branches altogether. Each branch contains about 3500 Josephson junctions. The maximum attenuation of these branches ranges from 4 to 8 dB, which assures a sufficiently uniform distribution of the microwave power to all junctions. Using the double fin-line taper shown in figure 2, all Josephson junctions are connected in series at dc without requiring additional blocking capacitors for dc separation of the segments of the array (cf section 4.2 for a design with 64 parallel branches). Each branch is terminated by a matched lossy stripline that serves as a load while suppressing microwave reflections from the end.

The design of 1 V arrays is very similar; the stripline is split into two parallel rf branches, each containing 1000 Josephson junctions (Müller *et al* 1997a).

3.3. Characteristics and metrological applications

The I–V characteristic for a 10 V SIS array is shown in figure 3(a) and, under microwave irradiation, in figure 3(b). Typical critical currents range from 80 to 200 μA, corresponding to a current density between 8 and 20 A cm^{-2} (i.e. a ratio of f/f_p of about 6). Due to the series connection of the 14 000 junctions, any technological fault (for some typical faults see Pöpel (1992) or Behr *et al* (2002)) can destroy the well-formed I–V characteristic and render the array unusable as a voltage standard. Under microwave irradiation, overlapping voltage steps are formed with a current width of about 20–50 μA. These quantized voltage steps are called zero-crossing steps, because they cross the zero current axis of the I–V characteristic. If the optimum microwave power is applied, about 170 000 quantized voltage steps can be observed in the range from −12 to +12 V (cf figure 3(b)).

The measurement set-up of the Josephson voltage standard consists of the following components (cf figure 4): the array is mounted in a sample holder, which allows the array to be cooled in a simple helium storage dewar. The sample holder also contains a waveguide for the microwave supply and cables for the bias supply and the voltage measurement. The microwave power is transmitted to the array by a microwave waveguide, e.g. an oversized circular waveguide having an attenuation of only about 1 dB m^{-1} (Kohlmann *et al* 1997a). The microwave system typically consists of a Gunn diode oscillator and a combined frequency stabilizing and measuring system, which in most cases is a source locking counter. A directional coupler diverts a small part of the microwave power to a harmonic mixer in the frequency stabilizer where it is compared with the desired frequency. The resulting error signal is converted to a dc voltage applied to the Gunn diode, completing the frequency stabilization loop. To adjust the optimum microwave power for the Josephson array, an attenuator is fitted between oscillator and sample holder.

A bias current supply is needed to select and stabilize the desired voltage step of the array. It typically consists of a voltage source connected to the array via a resistor in such a way that the load line of the combination of voltage source and resistor crosses only a few (1–10) steps of the array. Most bias sources also contain a simple curve tracer to view the I–V characteristic and the voltage steps of the array on an oscilloscope.

Calibrations of voltage sources such as electronic voltage standards based on Zener diodes are the most important application of Josephson voltage standards based on SIS arrays. The difference between the voltage to be calibrated and the output voltage of the Josephson standard is measured using a sensitive electronic voltmeter. Digital nanovoltmeters provide resolutions in the order of a few nanovolts, while analogue meters are able to resolve sub-nanovolt differences. The highest calibration accuracy is obtained when using a null detector set to the most sensitive range possible. The output voltage of the Josephson standard must therefore be selected correspondingly by adjusting the microwave frequency and the step number. In order to make this selection of a specific step

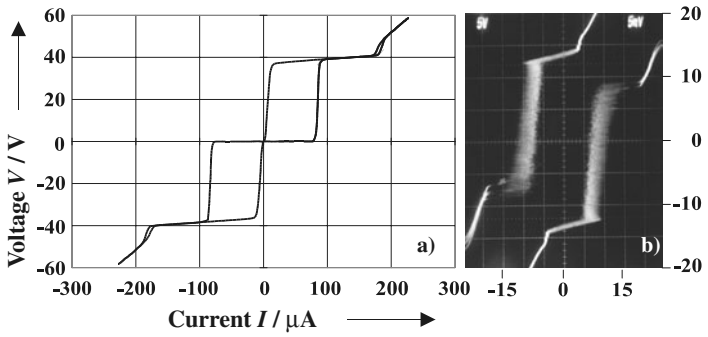

Figure 3. *I–V* characteristic of a 10 V array shown in figure 2: (a) without microwaves, (b) with 70 GHz microwave irradiation.

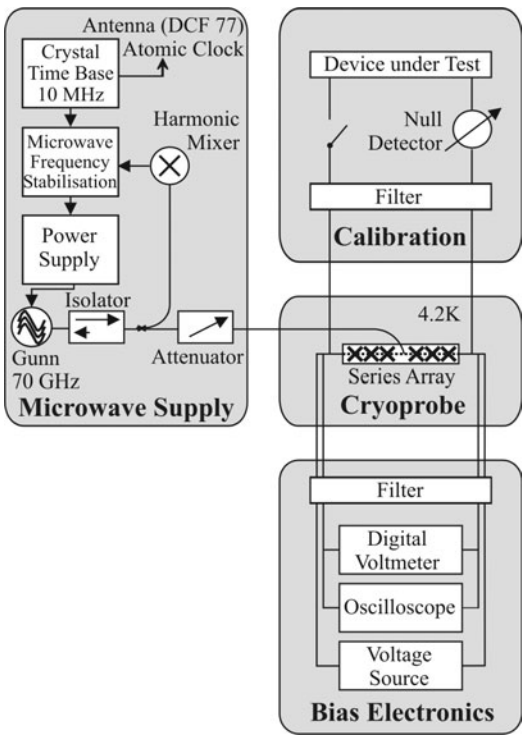

Figure 4. Set-up of a Josephson voltage standard for the calibration of electronic voltage standards.

of constant voltage possible in spite of the large number of overlapping steps, the specially designed bias current supply is used. The voltage across the load resistor shunting the array reduces the number of possible voltage steps to only a few and the desired step can then be selected by changing the bias current. In order to eliminate the effect of thermoelectric voltages generated by temperature differences along the cables, both the voltage of the Josephson standard and the voltage to be calibrated are reversed. While this is easily possible for the Josephson standard by reversing the bias, other voltage sources need an external switch for reversal. This switch must be designed for low thermal voltages in order to minimize errors. Uncertainties of the voltage measurement of the order of a few tens of nanovolts are possible, which corresponds to some parts in 10^9 of 10 V or some parts in 10^8 of 1 V. The uncertainty of the calibration of electronic voltage standards is limited by their noise and drift (cf Reymann *et al* 1999 or Hamilton and Tang 1999). In these calibrations, the uncertainties associated with thermal voltage drifts and the Josephson voltage are commonly negligible.

A proof of the capability of Josephson voltage standards at the highest level of precision can be achieved only when directly comparing two of them. At least one set-up must be operated electrically floating, in order to avoid ground loops that result in impairments of these high-precision measurements. When using good arrays and set-ups, it is possible to directly compare 10 V Josephson standards with uncertainties of the order of a few parts in 10^{11} (cf Reymann *et al* 1999).

3.4. Characteristics of SIS arrays limit applications

Stable steps are an important prerequisite for calibrations, that is to say, the steps must be stable for the typical measurement time, usually 1–2 min. As discussed in section 2.1.1, the stability of the steps is related to the ratio of the external frequency to the plasma frequency, i.e. the critical current density. Investigations of different arrays have shown that this ratio f/f_p should be increased to about 4–6, corresponding to critical current densities of about 20–10 A cm^{-2}. The stability of the steps is thus increased while maintaining sufficient widths of the steps. In addition to the intrinsic instability, external noise can disturb the proper operation of the voltage steps and must, therefore, be carefully filtered. The choice of the critical current density therefore represents a compromise between intrinsic instability and noise immunity.

Adjustment of the microwave power is the most complicated process for SIS arrays. At a certain voltage level, e.g. 10 V, a minimum power is needed to create steps. Due to the Bessel-function-like dependence of the step width on power, the step width is largest at the lowest power and decreases with increasing power. The latter description applies only to ideal arrays. In most real arrays variations in junction parameters and flaws become prominent at particular power levels, superposing one or more relative minima on the otherwise monotonic decrease of step width with increasing power (Müller *et al* 1997b). Measurements show that the stability of steps initially increases with increasing power. Therefore, the microwave power has to be larger than the minimal value required to get stable steps, but not too large, because small steps lose stability by the noise of the device under test. To check the calibration capability of SIS arrays, a test procedure is used at PTB (Behr *et al* 1999). After testing the array for trapped flux, the step width and stability is

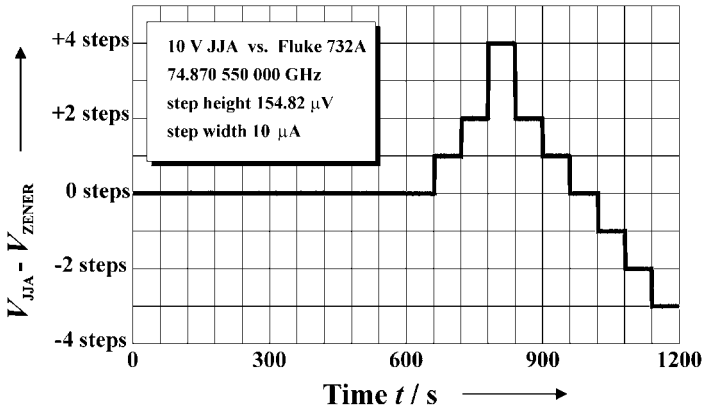

Figure 5. Characterization of a SIS voltage standard array by investigation of the stability and the adjustability of a step at 10 V.

measured as a function of microwave power. While the array is then connected in series opposition to a Zener reference, the step stability is tested for 10 min (figure 5, first 600 s), which is a long time compared with the time for calibrations. After 10 min, the bias current is changed every 60 s to test the feature of directly adjusting neighbouring steps (figure 5, 600–1200 s).

To avoid calibration errors from a small series resistance in the array—a fault that sometimes arises in large arrays—it is sensible to operate arrays on zero current steps. Disconnecting the bias current source ensures that no current flows through the array and, therefore, eliminates the possibility of these errors (Hamilton and Burroughs 1995).

The conventional SIS Josephson voltage standard has been very successful in dc calibrations and instruments have been commercially available since 1989. Technology has been successfully transferred from national metrology institutes to firms such as (Hypres[1]) and (PREMA[2]). The hysteretic I–V characteristic with overlapping steps has the advantage that the formation of steps is not very sensitive to variations in parameters of the junctions. However, SIS junctions have two important disadvantages due to the ambiguity of the steps:

(1) it is not possible to rapidly select a particular voltage step;
(2) the steps are only weakly stable so that electromagnetic interference can cause spontaneous switching between steps.

These disadvantages have been overcome by programmable voltage standards based on overdamped Josephson junctions showing non-hysteretic I–V characteristics. These new developments are described in section 4.

4. Programmable voltage standards

In spite of the successful operation of the conventional Josephson voltage standard, possibilities have recently been investigated of overcoming the disadvantages of SIS junctions and making possible new and broader applications of the Josephson voltage standard. As the disadvantages are due to the overlapping steps of underdamped junctions, overdamped junctions having non-hysteretic I–V characteristics have been studied. The I–V characteristic remains single-valued under microwave irradiation (cf figure 6) so that the steps of constant voltage are inherently stable and can rapidly be selected by external biasing of the junctions. As all junctions are operated at the same step (typically the first one), the number of junctions necessary to attain a given voltage must be increased by a factor of five compared with SIS arrays (SIS junctions are typically operated on the fifth step). Additionally, the series arrays must be divided into segments containing numbers of junctions belonging e.g. to a binary sequence so that the array can generate any integral number of voltage steps permitted by that sequence. Such arrays can therefore be operated as a D/A converter, too. These new kinds of Josephson junction series arrays are called programmable voltage standards.

Hamilton *et al* (1995) demonstrated these new ideas for the first time using externally shunted SIS junctions. The arrays operate at 75 GHz and consist of 8192 junctions divided into a binary sequence. The step width of these first arrays is limited to a few hundred microamperes because of design restrictions. The step width could be significantly increased up to more than 2 mA by using intrinsically shunted SNS junctions (Benz 1995, Burroughs *et al* 1999a). The N layer of these junctions consists of AuPd. The junctions are integrated into a coplanar waveguide of 50 Ω impedance; this simplifies the fabrication process. Compared with SIS arrays, SNS junctions have a low characteristic voltage, $V_c = I_c R_n \approx 20\ \mu$V so they are operated at about 16 GHz. For the same reason, a 1 V array requires 32 768 SNS junctions. The series array is divided into segments such that it functions as a 9-bit D/A converter. The least significant bit consists of 128 junctions. Each dc connection includes a bandstop filter in order to provide a uniform microwave power distribution along the coplanar waveguide. As the size of these filters is rather large, they prevent further division of the series array. The dimension of the SNS junctions is 2.5 μm × 2.5 μm; the critical current density is more than 200 kA cm^{-2} which involves several technological challenges. Pöpel *et al* (2000) developed a fabrication process for sub-micrometre SNS ramp type junctions (Nb/AuPd/Nb) in order to reduce the area of the junctions and, therefore, to increase the scale of integration.

Hassel *et al* (2001a) investigated series arrays of externally shunted SIS junctions using a scheme in which the attenuation of the applied 70 GHz microwave signal is reduced while

[1] Hypres Inc., 175 Clearbrook Road, Elmsford, NY 10523, USA; www.hypres.com
[2] PREMA Semiconductor GmbH, Robert-Bosch-Straße 6, 55129 Mainz, Germany; www.prema.com

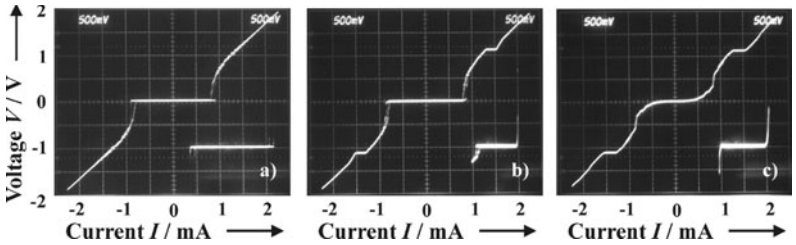

Figure 6. I–V characteristic of a 1 V series array consisting of about 7500 SINIS junctions at 70 GHz microwave irradiation of different power levels: (a) without microwaves, (b) 0.4 mW, (c) 3 mW. The insets show with high resolution: (a) the critical current (I:500 μA/div; V:1 mV/div), (b), (c) the Shapiro step (I:100 μA/div; V:100 μV/div).

the attenuation of signals at lower frequencies is enhanced. Voltages up to 1.4 V have been generated with arrays of about 3200 junctions operated on the third step (Hassel *et al* 2001b). Josephson junctions based on high-temperature superconductors (HTS) also have a non-hysteretic I–V characteristic. Klushin *et al* (2001, 2002) fabricated series arrays of shunted bicrystal YBCO junctions. Voltages of more than 10 mV have been generated with arrays of 136 junctions operated at a temperature of 65 K under microwave irradiation of 36 GHz.

Another promising kind of junctions for programmable Josephson arrays has been investigated at PTB (Schulze *et al* 1998). These junctions consisting of a SINIS multilayer were first proposed by Kupriyanov and Lukichev (1988) and recently studied for electronic applications by Maezawa and Shoji (1997) and Sugiyama *et al* (1997). They, too, are intrinsically shunted Josephson junctions with moderate current density. A main advantage of SINIS junctions is their high characteristic voltage of up to 200 μV (see 2.1.2), which makes the operation at frequencies of around 70 GHz possible. Models of SINIS junctions have been discussed e.g. by Kupriyanov *et al* (1999), Balashov *et al* (2000), Kadin (2001). The use of series arrays of SINIS junctions is discussed in section 4.3.

4.1. Characteristics of SINIS junctions and arrays

Figure 6 shows the I–V characteristic of one of the first 1 V SINIS series arrays consisting of about 7000 junctions. Under microwave irradiation, a step at 1 V is generated (cf figure 6(b)). The formation of steps reveals two unexpected facts: first, only a very low microwave power, about 100 μW or somewhat more, is required to generate a step. By comparison, SIS arrays require at least about 1 mW to generate a 1 V step in an array of 2000 junctions and 10 mW to generate a 10 V step in an array of 14 000 junctions. Secondly, in these SINIS array the step width can be increased only slightly by increasing the microwave power (cf figure 6(c)). This unusual behaviour results from the characteristics of a series array of SINIS junctions integrated into a low-impedance stripline. According to calculations by Kautz (1992) on the basis of the RCSJ model (calculations by Meyer *et al* (1989) on the basis of the RSCJ and the Werthamer model leads to similar results), the attenuation of a SINIS series array can be estimated at about 50 dB/1000 junctions (Schulze *et al* 1999). This large attenuation follows from the fact that the resistive and the capacitive impedances are of the same order of magnitude and a major part of the microwave power is, therefore, dissipated resistively. Nevertheless, the junctions of large series arrays are phase-locked to the external microwave frequency as evidenced by the formation of Shapiro steps. This behaviour can be explained by the active contribution of SINIS series arrays (Schulze *et al* 1999). The SINIS junctions operate as oscillators, compensating the large attenuation in the stripline. The junctions are mutually synchronized by the microwave power which they emit into the stripline by transforming part of the applied dc power of the bias current into ac power.

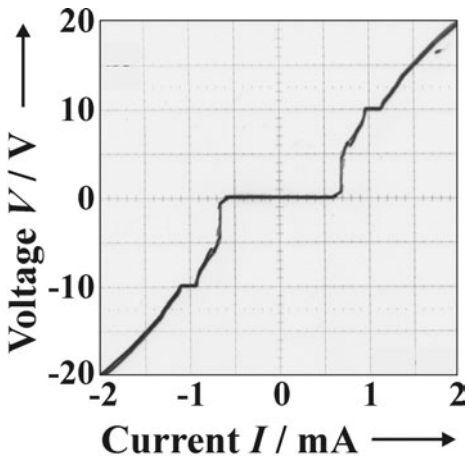

Figure 7. I–V characteristic of a 10 V series array consisting of about 69120 SINIS junctions irradiated with microwaves at 70 GHz. A constant-voltage step at 10 V is generated using only 1 mW of microwave power.

The low microwave power makes possible the operation of very large SINIS series arrays. First SINIS arrays capable of generating output voltages up to 10 V have been designed and fabricated (Schulze *et al* 2000, Kohlmann *et al* 2001). They consist of 69 120 junctions integrated into 64 parallel microwave branches, each containing 1080 junctions. To avoid an increase in chip size because of this large number of junctions, the design has been modified in several respects (smaller junctions, no bends, reduced distance between microwave branches, reduced length of the microwave load). Figure 7 shows the I–V characteristic of a 10 V SINIS series array with a step width of about 200 μA.

4.2. Fabrication process and design

With the exception of the Nb–Al/Al_2O_3/Al/Al_2O_3/Al–Nb multilayer, the process for the fabrication of SINIS arrays is almost the same as for SIS arrays (cf section 3.1 and Müller

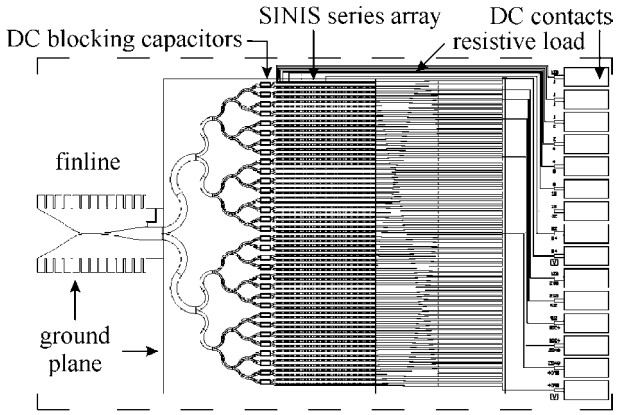

Figure 8. Layout of a SINIS series array. The 8192 junctions (14 bit) divided into binary segments are integrated into 64 parallel branches, each containing 128 junctions.

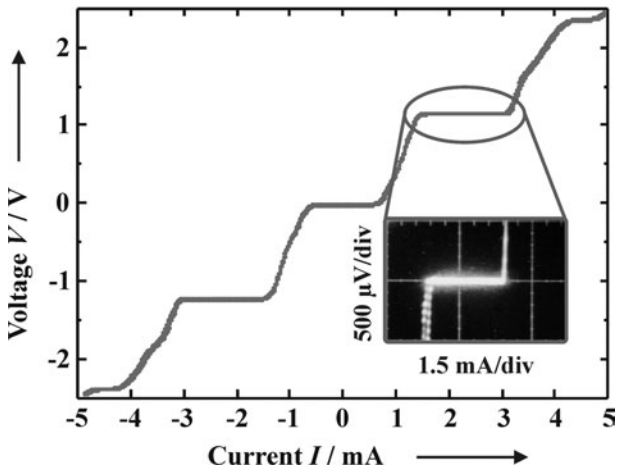

Figure 9. I–V characteristic of the 1 V array shown in figure 8 under 70 GHz microwave irradiation of about 15 mW power. The inset shows the step at high resolution.

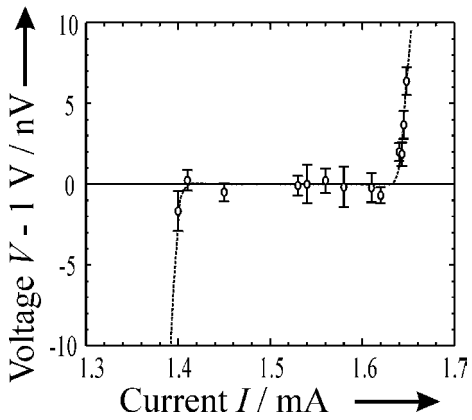

Figure 10. High-resolution representation of the voltage difference between a 1 V SINIS and a 1 V SIS array.

et al 2001). The thickness of each Al layer is 10 nm; for the two Al_2O_3 barriers the first two Al layers are oxidized in 0.4 Pa O_2 at 20 °C for 4 min. This process yields a current density of about 150 A cm^{-2}, a normal state resistance of about 100 mΩ, a characteristic voltage of about 150 μV and a McCumber parameter of about 1. In spite of the slight oxidation of the Al layers, the critical Josephson current density is distributed homogeneously over the whole junction area as demonstrated by the observation of a clear Fraunhofer pattern for the variation of the critical current with an applied magnetic flux density (Schulze *et al* 1998).

As for conventional SIS arrays, a homogeneous distribution of the microwave power among the junctions is essential for programmable arrays, too. Due to the different characteristic voltages of SNS and SINIS junctions, they must be operated at different microwave frequencies. Beyond that, R_n and C (only for SNS junctions) are small in comparison with SIS junctions, resulting in a different matching to the microwave waveguide. Today various methods (transmission lines) are used to distribute the microwave power. They include 50 Ω coplanar waveguides for SNS junctions and low-impedance striplines for SINIS junctions. Recently, Schubert *et al* (2001a, 2001b) proposed a new kind of 50 Ω coplanar stripline which has also been applied to SINIS junctions.

The 50 Ω coplanar waveguide for SNS junctions leads to the same concept as the microstripline for SIS junctions. Attenuation of the microwave is low, because the junctions are loosely linked to the waveguide. In contrast, SINIS junctions in low-impedance striplines attenuate microwave power at the very high rate of about 50 dB/1000 junctions as discussed before in section 4.1. The design of binary-divided series arrays must take this large attenuation into account. Due to the large attenuation, each microwave branch should contain only a small number of junctions, in order to make a homogeneous microwave distribution. Figure 8 shows the layout of a binary-divided array for output voltages up to 1 V taking into account these considerations and consisting of 8192 junctions (14 bit). The junctions are arranged in 64 parallel microwave branches, each containing 128 junctions. These short branches make it possible to attain a large step width of more than 1 mA (about $0.8I_c$) as is shown by the I–V characteristic in figure 9. As the active contribution of the junctions does not play a substantial portion for the generation of large steps, the arrays require more microwave power than those discussed in section 4.1. Operation of the arrays at a microwave power of a few milliwatts is likewise possible and results in a step width of up to 500 μA (i.e. $0.4I_c$)

4.3. Metrological applications of SINIS arrays

For metrological applications of programmable Josephson voltage standards, it is necessary to carefully verify that the steps are flat (i.e. have a constant voltage) and that the output voltage really follows the Josephson equation. This would not be the case if resistive voltage drops are created by the bias current. Behr *et al* (1999) performed direct comparisons of a SINIS and a SIS voltage standard at the 1 V level. The measurements confirm that the steps in SINIS current-biased arrays are really flat with a resolution of better than 1 nV (cf figure 10). Additionally, the voltages of both arrays agree with an uncertainty of 2 parts in 10^{10} ($V_{SIS} - V_{SINIS} = (0.07 \pm 0.16)$ nV; type-A standard uncertainty). These results clearly demonstrate that SINIS series arrays are suitable for metrological applications.

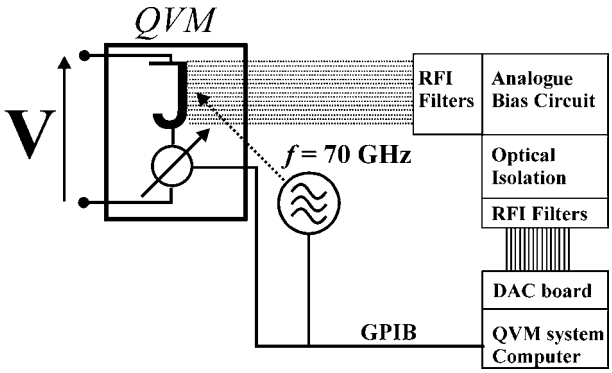

Figure 11. Block diagram of a QVM for dc voltage measurements.

4.3.1. DC calibrations. DC calibrations are a direct application of programmable voltage standards. The *I–V* characteristic is single-valued and the width of the Shapiro steps is much larger than for SIS arrays. The steps are therefore more stable against external noise and disturbances. Nevertheless, external noise must be carefully kept away from the arrays, as it can cause noise-induced phase slipping. This phase slipping can round the steps, and this may result in errors in practical applications (Behr *et al* 1999). Compared with SIS arrays, with programmable arrays the selection of any voltage step is much easier and can be performed very quickly by simply switching the bias source of the corresponding segments. Using binary-divided arrays and multiple bias sources under computer control, a very easy-to-use Josephson voltage standard can be built. Together with a sensitive voltmeter, a quantum-based voltage measuring instrument, the so-called quantum voltmeter (QVM), has been set up (figure 11).

The calibration of electronic voltage standards using SINIS arrays is very similar to that using SIS arrays, except for the shorter period of time needed for polarity reversal. As overdamped Josephson junctions do not show zero current steps (for $n \neq 0$), special care must be taken on to ensure that the array is really operated on a step of constant voltage. A direct comparison of an SIS Josephson voltage standard with a SINIS QVM is easier than a comparison between two SIS standards.

4.3.2. Josephson potentiometer. The ratio of two resistors can be determined using the adjustable and precisely known voltage of a Josephson array. For this purpose the resistors are connected in series to a stable current source. The same current passes through the two resistors so the ratio of the resistances is equal to the ratio of the voltage drops across the resistors. To ensure equal current in both resistors, the leakage current of both voltage measurements must be very low. The voltages across the resistors can be measured in different ways using Josephson voltage standards.

The simplest way is to measure the two voltages one after the other with a conventional SIS voltage standard. This requires a switch to select the potential difference across one of the two resistors and this switch introduces errors due to its thermoelectric voltages. Another source of error is the instability and drift of the current source, as the resistor voltages are measured at different times. The measurement time is twice the time required for a single voltage measurement, which results in larger errors due to drift effects (Warnecke *et al* 1987).

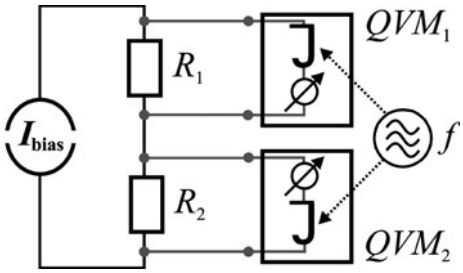

Figure 12. Josephson potentiometer consisting of two QVMs.

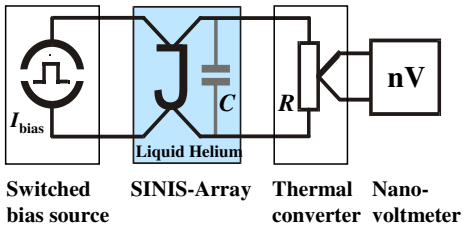

Figure 13. Schematic diagram showing how an SINIS array is used to characterize thermal converters.

Most of the shortcomings described above can be overcome when two Josephson standards are used to measure the potential differences across the two resistor voltages simultaneously (Kohlmann *et al* 1992). Special care must be taken to minimize leakage across the resistors and to ground loops. This makes the set-up more complex. To cancel errors due to thermoelectric voltages, the current source as well as the Josephson voltages must be reversed, which is hard to perform simultaneously with SIS arrays (Thompson *et al* 1999).

Polarity reversal is much faster and easier with SINIS arrays. A fully automated system carries out complete resistance ratio measurements under computer control at a rate of about one per minute and can run overnight without interruption (cf figure 12). The uncertainty is dominated by the smallest voltage to be measured. For precise measurements with relative uncertainties of the order of 10^{-8}–10^{-9}, the smaller voltage must be in the range from about 10 to 100 mV. Since the Josephson voltage is limited to 1 V, the useful range of the measurable resistance ratios extends from 1:1 to 1:100 (Behr *et al* 2001). Optimum performance is, of course, achieved with 1:1 ratios, but little accuracy is sacrificed when measuring the 1:1.29 ratio (10 kΩ:12.9 kΩ) used for measurements of the quantized Hall resistance. The resistance value of a 10 kΩ standard resistor was linked to a quantized Hall resistance (12.9 kΩ) with an uncertainty of a few parts in 10^9 which is comparable to measurements using a cryogenic current comparator (Behr *et al* 2003).

4.3.3. Fast-reversed dc measurements. A first step towards an ac voltage standard based on the Josephson effect was to use an array in the so-called fast-reversed dc (FRDC) method to measure the error introduced by reversible thermoelectric effects (those not due to Joule heating) when using thermal converters to relate ac to dc voltages. This method requires

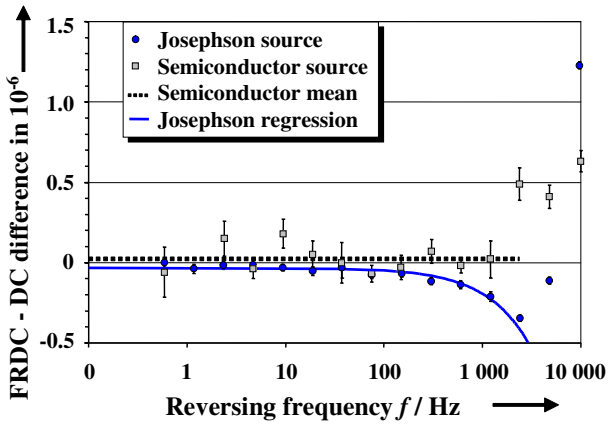

Figure 14. Measurements on a 180 Ω planar multijunction thermal converter (PMJTC) showing the results obtained with the SINIS Josephson standard compared with the results obtained using a semiconductor FRDC source.

three precisely known voltage levels, $-V$, 0, and $+V$, that can be switched quickly to a thermal converter. This task is perfectly easily accomplished using a programmable voltage standard (figure 13). The array output voltages are accurately known, they are of equal magnitude in both polarities and they can be switched and reversed quickly by simply changing the bias current. Such fast reversal is not possible with SIS Josephson arrays. First measurements were made by Burroughs *et al* (1999b). In comparisons carried out at the PTB between an SINIS array and the semiconductor-based FRDC source previously used, differences of less than 0.2 μV V^{-1} were observed for reversing frequencies of up to 200 Hz (figure 14). At frequencies below about 100 Hz, the SINIS source excels due to the lower noise of the quantized voltage (Funck *et al* 2001).

4.4. New principles for the generation of ac voltages

One aim of the early investigations of programmable voltage standards was the use of binary-divided arrays for synthesizing ac waveforms. However, the first precision measurements soon revealed the difficulties in generating ac waveforms with the low uncertainty required for metrological purposes (Hamilton *et al* 1997a). One problem is the transience of the I–V characteristic between quantized steps. As the voltage is not determined during the switching time with fundamental accuracy (i.e. the voltage is not referred to fundamental constants), Hamilton *et al* (1997b) reported that the uncertainty increases to unacceptable values when ac waveforms are generated.

Williams *et al* (2002) started further investigations using a binary-divided 1 V SINIS array and a high-speed bias source with a faster rise time of about 100 ns. The system is operated for synthesizing ac voltages at low frequency (below several 100 Hz or 1 kHz at most), in order to find out accuracy limitations and to check if this system can be used for metrological purposes.

To realize an ac voltage standard with fundamental accuracy, the output voltage must be referred only to the specific transfer of flux quanta, i.e. the transfer of flux quanta must be carefully driven and controlled and other contributions to the output voltage must be completely suppressed. At present, two main suggestions are discussed and investigated: the bipolar voltage source (Benz *et al* 1999) and the SFQ-based voltage multiplier (Semenov 1987).

4.4.1. The bipolar voltage source. One way for the precise control of the transfer of flux quanta is the excitation of Josephson junctions by short pulses generated by a pulse generator instead of excitation by an external sinusoidal microwave. Monaco (1990) has shown that it is possible to drive an overdamped Josephson junction with a pulse train. The formation of the voltage step does not depend on the spacing of the pulses if the rise time is sufficiently short. Researchers of NIST and Northrop Grumman have taken up this idea to develop a Josephson arbitrary waveform generator (Benz *et al* 1998). Detailed investigations have shown that the combination of the digital code with a sine wave to drive the Josephson array makes possible the generation of bipolar voltages and results in a higher output voltage. An instrument based on this scheme uses a small SNS array operated at a microwave frequency of 10 GHz, overlapped by a signal of the binary code generator, that switches the array from the first positive step to first negative step (Benz *et al* 1999). If this switching is phase-locked to the sinusoidal microwave signal and takes place within a small fraction of the period of the sine wave, the output voltage can be controlled in terms of single flux quanta. The difficulties for perfect operation are tremendous, because the signal of the code generator is broadband from DC to 30 GHz. All components used must be broadband and any reflections on the chip including the array must be avoided. The major technological challenge is to achieve a practical output voltage of 1 V by developing the broadband circuits and the small junction. First attempts were made by Liefrink *et al* (1999) to replace the expensive commercial code generator by simplified bias electronics.

Much progress has been made with the Josephson arbitrary waveform synthesizer which is capable of generating ac, dc and arbitrary waveforms with low harmonic distortion and stable, calculable and reproducible amplitude and phase. So far, this device is capable of synthesizing a peak-to-peak (PP) ac output voltage of 127 mV at frequencies from dc to 100 MHz. At a sine wave frequency of 4.8 kHz, the harmonic distortion was measured to be −101 dBc using the ac coupled method (Benz *et al* 2002).

4.4.2. SFQ-based D/A converter. Another way for the precise control of the transfer of flux quanta is a dynamic logic based on the processing of single flux quantum (SFQ) pulses. SFQ pulses are short voltage pulses, the time integral of which yields exactly a flux quantum Φ_0. The SFQ logic allows all logic components to be included that are necessary for digital applications up to a clock frequency that is determined by the characteristic voltage V_c of the junctions. A D/A converter for voltage standard applications was suggested by Semenov (1987, 1993) and in some respects improved by Hamilton (1992). This D/A converter is based on a voltage multiplier, which multiplies SFQ pulses. Due to the quantized SFQ pulses, the voltage multiplier acts as a voltage amplifier with fundamental accurate gain. The SFQ pulses are directly generated on the chip by frequency synthesizers.

The Josephson junctions of the voltage multiplier convert the pulses with a repetition frequency up to several 10 GHz to a voltage given by the Josephson equation. The junctions are connected in series for dc resulting in an output voltage depending on the number of junctions. As the voltage multipliers are likewise connected in series for dc, the output voltage is the sum of the output voltages produced by the voltage multipliers. The SFQ-based D/A converter consequently consists of a frequency multiplier and a frequency divider for providing two local reference frequencies, SFQ-based frequency synthesizers controlled by an external code, and the voltage multipliers amplifying the voltage with integer gain. As the device needs a frequency supply of a few hundred megahertz only, this SFQ-based D/A converter has the advantage of a rather simple experimental arrangement. The inconvenience, however, is that it requires a rather complex circuit that is difficult to design. The fabrication of devices of this type is a real challenge because of the large number of junctions and because any fault in the digital circuits makes the chip unusable. Furthermore, additional junctions are needed for the Josephson transmission lines distributing the SFQ pulses.

Nevertheless, different kinds of devices have been realized and fabricated. Present schemes for reaching higher output voltages are based on hybrid integration of several chips, all fabricated in SFQ logic. The low-frequency input signal is multiplied up to the operating frequency. Signals at this operating frequency are distributed to several voltage multipliers. The output voltage is given by the sum of the voltages from all voltage multipliers. All multipliers are clocked by an extra clock chip that controls the output voltage $V(t)$. Recently, output voltages of about 100 mV have been achieved with a single voltage multiplier (Semenov and Polyakov 2001).

5. Conclusions

Conventional Josephson voltage standards consist of underdamped SIS junctions having hysteretic I–V characteristics. They are very successfully operated in more than 50 national, industrial and military standards laboratories around the world for dc calibrations at the 1 and 10 V levels and are presently commercially available. Programmable voltage standards are based on overdamped SNS or SINIS junctions. Their non-hysteretic I–V characteristics allow fast and easy adjustment of steps of constant voltage by means of the external bias source. The arrays are commonly divided into binary segments and are suitable for metrological applications. A QVM based on these arrays has been used in various applications. The first 10 V SINIS arrays have now been successfully fabricated and operated. However, the fabrication process remains a great challenge because of the large number of junctions required. For synthesizing of ac voltages, new concepts such as the bipolar voltage source or the SFQ-based D/A converter are at present under development. The development of programmable voltage standards makes the exploitation of the Josephson effect for metrological applications ever more easy and will lead to a wider use of this quantum-based voltage standard.

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