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2006 Supercond. Sci. Technol. 19 294

(http://iopscience.iop.org/0953-2048/19/4/009)

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Supercond. Sci. Technol. **19** (2006) 294–298 doi:10.1088/0953-2048/19/4/009

Modified fabrication of planar sub-μm superconductor–normal metal–superconductor Josephson junctions for use in a Josephson arbitrary waveform synthesizer

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Received 9 November 2005
Published 13 February 2006
Online at stacks.iop.org/SUST/19/294

Abstract

A flexible and reliable fabrication technology has been established at PTB for the development of circuits based on superconductor–normal metal–superconductor (SNS) Josephson junctions. Submicrometre junctions are necessary in order to handle the large critical current densities of SNS junctions. In the development of both a new production method and new applications, many changes to the design or fabrication process are inevitable. Electron-beam lithography is suitable for structures down to below 100 nm and offers a high reproducibility. Combining electron-beam lithography with chemical–mechanical polishing (CMP) delivers a powerful tool for both the development of applications and the actual production of experimental circuits. In this paper we describe the design and fabrication of SNS arrays embedded in superconducting high-frequency lines for application in a Josephson arbitrary waveform synthesizer (JAWS), and first measurements are presented. We successfully fabricated junctions from 0.04 to 4 μm^2 in series arrays of up to 512 junctions. Correct function is shown in a frequency range from 5 to 20 GHz.

1. Introduction

Quantum standards are being increasingly used in the field of metrology. While the application of single-electron tunnelling (SET) devices for current standards is still under development [1], Josephson junctions are widely used in voltage standards applications [2, 3]. The interest in improved Josephson voltage standards and AC measurements has led to the development of programmable voltage standards [4, 5] and the Josephson arbitrary waveform synthesizer (see section 3), respectively [6, 7]. Superconductor–normal metal–superconductor (SNS) junctions are a possibility for the realization of overdamped Josephson junctions needed for these applications. They are well suited to low-frequency ($f < 35$ GHz) [8, 9] voltage standards applications, and work is going on to expand this limit up to the typical 70 GHz voltage standard drive frequency [10]. To achieve these goals, numerous test series are necessary. A fabrication method that offers the possibility of making run-to-run changes in both layout and, to a lesser degree, the production process has to be adopted.

Previously, to fabricate sub-μm ramp-type SNS Josephson junctions at PTB a combination of optical and electron-beam lithography was used [11]. Junction areas down to $A = 0.03$ μm^2 were reached. Yet, to obtain knowledge of the actual sizes of the junctions the length of the ramp had to be determined for virtually every chip because it differed from run to run.

This paper describes the development of a new planar fabrication process. As the significant steps of this process are entirely electron-beam-based, the disadvantages of SNS ramp-type technology are overcome. Based upon this, we present the

development of new SNS junction series arrays for application in a Josephson arbitrary waveform synthesizer (JAWS).

2. Technology

The planar fabrication process described in this paper was developed simultaneously with a process for the fabrication of 100 nm Josephson junctions for SET [1]. A thermally oxidized 3 inch (100) Si wafer serves as the substrate for circuit development. In a first step a Al_2O_3 etch stop layer is deposited by RF sputtering. Then, the SNS tri-layer consisting of either Nb/HfTi/Nb or Nb/PdAu/Nb is sputtered in an *in situ* process. The compositions $Hf_{50wt\%}Ti_{50wt\%}$ and $Pd_{68wt\%}Au_{32wt\%}$, respectively, are chosen to maximize the electrical specific resistivity of the N-layer materials. The thicknesses of the Nb base and counter electrode layers are 160 nm (about twice the London penetration depth λ_L), while the thickness of the N layer is set specifically to obtain the required critical current density j_c.

To pattern the Josephson junctions, a two-layered positive polymethylmethacrylate (PMMA) electron-beam resist is used to define an Al etching mask by a lift-off process. In this step the size of the junction can be changed very easily to precisely adjust the required critical currents.

The Nb counter electrode is patterned by reactive ion etching (RIE) using CF_4 at 15 Pa. In this process the Al etching mask is hardly affected. In a second consecutive step the normal conducting layer and the aluminium are etched physically by a (neutralized) Ar ion beam.

To pattern the lower Nb base layer an electron-sensitive negative resist (maN 2405) is used. The precision of alignment of this second electron-beam exposure is 50 nm or better as the electron-beam markers are created alongside the counter electrode structures in the initial exposure. The exposed resist is developed in a metal-ion-free developer (AZ MIF 726). The base structures are etched directly by RIE using SF_6 plasma at a pressure of 1 Pa. The remaining resist is removed in acetone (using ultrasonics) and a REZI 38™ photoresist stripper at 45 °C. REZI 38™ removes Al too, so no Al (which has possibly remained from the counter electrode etching process) remains on top of the Nb counter electrode. Figure 1 shows the structures after the first two fabrication steps.

The SiO_2 insulation between the base electrode and the Nb wiring, to be deposited later on, is established by plasma enhanced chemical vapour deposition (PECVD). In order to guarantee appropriate insulation, 600 nm of SiO_2 are deposited, as the total thickness of the SNS layer system is about 350 nm.

To enable contact between the counter electrode and the Nb wiring the SiO_2 insulation has to be removed from the top of the counter electrodes. This is done by chemical–mechanical polishing (CMP). At a rate of about 120 nm min^{-1} the superfluous SiO_2 is removed, while at the same time the wafer is smoothed. The actual thickness of the PECVD SiO_2 is measured by white light reflection spectroscopy. To be on the safe side, about 50 nm of Nb are removed from the top of the counter electrode. To ensure homogeneous planarization of all circuit elements, dummy structures are placed at the edges and corners of the active circuit structures providing identical surroundings for all active structures. Additionally,

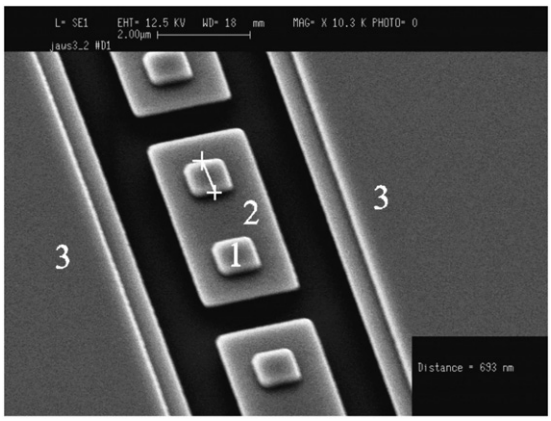

Figure 1. Scanning electron microscope (SEM) photograph of structures fabricated using planar electron-beam technology. Two lithographical steps have already been performed. The bright squares are the Nb counter electrodes (1) with an area of about 0.7 μm × 0.7 μm, the embedding rectangles are the Nb base electrodes (2). Structures to the left and right (3) serve as both waveguide and a support for CMP.

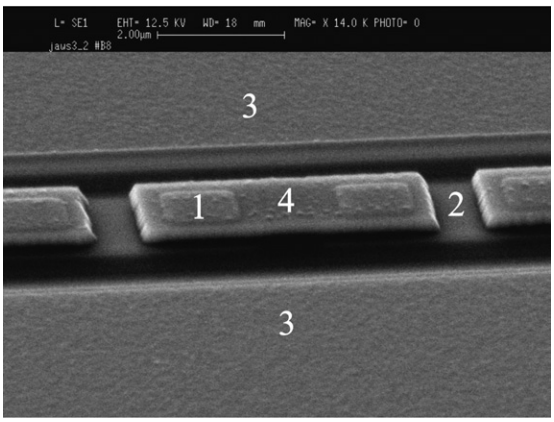

Figure 2. SEM picture of a small part of a series array of planar SNS Josephson junctions (1). After the base structure (2) has been formed (cf figure 1), an SiO_2 insulation layer is deposited by PECVD and polished and smoothed by CMP. As can be seen, the polished Nb counter electrodes are clearly visible as smooth elevations on the Nb wiring (4), while hardly any edges are found where the wiring crosses the gap between two base electrodes (3: waveguide ground).

specially adopted test structures are used to verify the state of the planarization under a microscope. A homogeneous planar surface will provide both a good thermal and a good electrical contact between the top of the Nb and the Nb wiring electrode.

Before the Nb wiring (thickness: 160–200 nm) is deposited, the counter electrode is thoroughly cleaned *in situ* by a RF Ar plasma. Again, to define the wiring structures, electron-beam lithography is applied to create an Al etching mask as described above. The wiring is etched in CF_4 plasma at 15 Pa. Figure 2 shows an SEM photograph of the now completed array. If required, PdAu or HfTi loads are fabricated using PMMA as a lift-off mask.

Finally, by means of optical lithography (for convenience), the remaining SiO_2 is removed from the contact pads in a wet-etching process.

3. Design of arrays for the JAWS

In contrast to the conventional DC 1 V and 10 V Josephson voltage standards driven by sinusoidal microwaves of about 70 GHz, the Josephson arbitrary waveform synthesizer is operated by a 'train' of short pulses as suggested and demonstrated by Benz *et al* [12, 13]. The input pulses cause the transfer of flux quanta $\Phi_0 = h/2e \approx 2.07\ \mu\text{V GHz}^{-1}$ (h being the Planck constant and e the elementary charge). The repetition frequency f of the pulses at any time determines the array voltage $U(t)$:

$$U(t) = n\Phi_0 f \tag{1}$$

where n is the number of flux quanta transferred through the junction by each pulse. The first concept of using unipolar pulses [12] was extended to a combination of positive and negative pulses generated by superposition of a fast digital code and a sine wave with a frequency of about 10 GHz, resulting in bipolar pulses [13]. Another method for pulse-driving the array, demonstrated by Williams *et al* [7], uses photodiodes operated by short optical pulses.

The resistive load at the end of typical Josephson arrays results in problems with common mode voltages for these kinds of applications. Benz *et al* [14] suggested lumped arrays as a simple solution to these problems. In a lumped array common mode voltages are avoided as the array is directly grounded at the end, resulting in standing waves (caused by reflection at the end). Therefore, the array must be short compared with a typical wavelength λ (at the highest frequency) of about $\lambda/8$.

The Josephson junctions are uniformly operated, as the high-frequency components of the pulses do not change significantly over this short distance. The limitation of the length restricts the number of Josephson junctions (lumped array), and thus confines the output voltage.

Recently, SINIS (S, superconductor; I, insulator; N, normal metal) junction series arrays have been developed at PTB as lumped arrays for first investigations [15] within the framework of the EU-funded joint project JAWS [16]. The output voltage is considerably increased if more junctions of a smaller size are integrated in a space of $\lambda/8$. As the critical current density of SNS junctions is much larger than that of SINIS junctions, the size of SNS junctions can be reduced significantly.

Figure 3 displays the layout of one of these circuits as an example. The taper (1) enables the transition between the semirigid cable leading the microwave to the chip and the coplanar waveguide containing the array (2) (close-up in figure 2). The LC filters (3) are specially designed for these applications to minimize the distortion of the input pulses which may be caused by the output cable and the measuring instrument [16].

Up to 512 SNS junctions are embedded in the centre line of a coplanar waveguide matched to the 50 Ω impedance of the RF generator. The impedance of 50 Ω of the coplanar waveguide is realized by a centre line with a width of 2 μm, ground lines with a width of 100 μm and distances of 1.25 μm between the centre and the two ground lines (junction size <2 μm). The length of 1.5 mm adds up to $\lambda/8$ at 10 GHz, corresponding to the pulse repetition frequency of typical high-speed code generators. The junction size is varied from 0.7 μm × 0.7 μm to 2 μm × 2 μm.

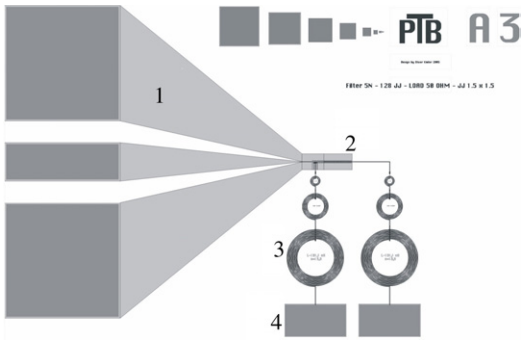

Figure 3. Design of a lumped Josephson junction array using SNS junctions for the JAWS project: 1, microwave antenna; 2, junction array; 3, LC filters; 4, dc contact pads.

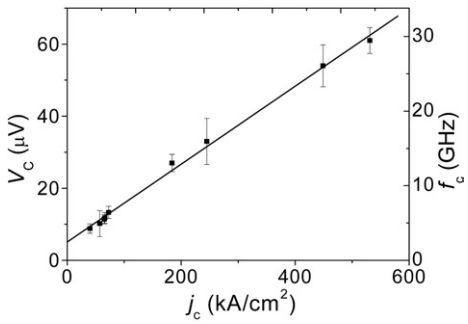

Figure 4. Critical current density versus characteristic voltage for several planar SNS Josephson junction arrays of various wafers with different HfTi barrier thicknesses. The standard deviation is indicated by the error bars.

4. Results and discussion

The data presented in this section were obtained for SNS junction arrays with a Nb/HfTi/Nb tri-layer. The relation between V_c and j_c is presented in figure 4. The results were obtained from several wafers with different HfTi layer thicknesses and junction areas. Generally, the normalized frequency Ω of equation (2) determines the behaviour of a Josephson junction under microwave irradiation:

$$\Omega = \frac{f}{f_c} \tag{2}$$

f being the microwave frequency and f_c being the junction's characteristic frequency.

For use in programmable voltage standards, a normalized frequency of $\Omega \approx 1$ or $\Omega \geqslant 1$ is regarded as optimal for the formation of steps as well as step stability, as discussed by Kautz [17, 18]. Furthermore the microwave power required to produce a large step width is still within a moderate range for $\Omega \leqslant 4$ [17]. Figures 7 and 8 ($f_c = 5$ GHz) present the optimum case between $\lambda = 1$ at 5 GHz and $\lambda = 4$ at 20 GHz.

The Josephson penetration depth λ_J (equation (3)) of a junction compared with its dimensions determines the type of current density distribution over the junction area. A value for λ_J of about 1.4 μm is derived ($d = 30$ nm being the thickness of the normal metal, $\lambda_L = 85$ nm the London penetration depth and $j_c = 65\ \text{kA cm}^{-2}$ the mean value of the critical current density) [17]:

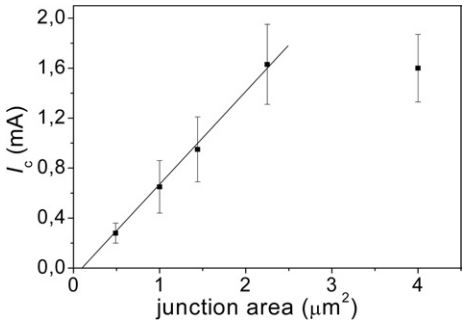

Figure 5. Critical current versus junction area. The deviation from linear behaviour is obvious for a junction area of 2.0 μm × 2.0 μm.

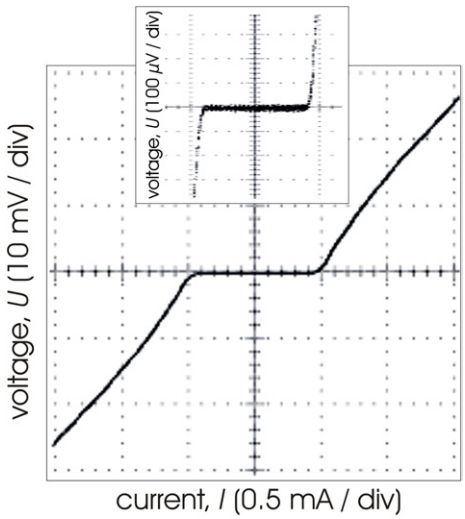

Figure 6. Current–voltage characteristic (IVC) of an array of 512 Josephson junctions (0.7 μm × 0.7 μm). The critical current is $I_c = 0.4$ mA, the normal resistance $R_N = 35$ mΩ and the characteristic voltage $V_c = 14$ μV.

$$\lambda_J = \sqrt{\frac{\hbar}{2e\mu_0 j_c(d + 2\lambda_L)}}. \qquad (3)$$

The investigations presented in this paper were performed with square junctions, i.e. length = width. If the length and the width of the junctions are much smaller than λ_J, Josephson junctions can be well described by the point-junction model. In this case the junction phase Φ is distributed uniformly over the junction area. If length or width exceeds λ_J the phase varies across the junction, hence the simple linear relation scaling between the critical current and the junction area is no longer valid. This behaviour is indeed observed, as shown in figure 5 for junctions with a length and width of 2 μm each. Consequently the junction area should not exceed 2 μm^2.

Figure 6 presents the current–voltage characteristic (IVC) of an array of 512 Josephson junctions (junction area 0.7 μm × 0.7 μm). The diagram shows a hysteresis-free characteristic and a small parameter spread as the shape of the array's characteristic is very similar to the characteristic of a single junction.

By optimizing the fabrication process, a significantly higher yield was achieved (>75%). All Josephson junctions contribute to the Shapiro steps in the functional arrays.

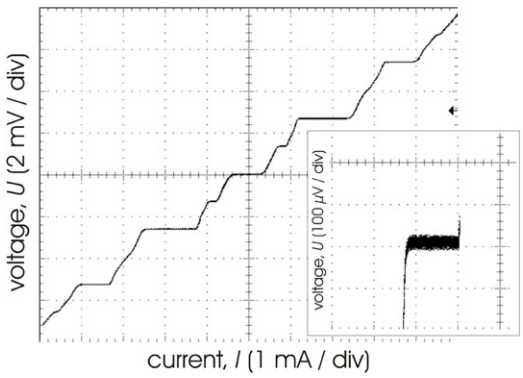

Figure 7. IVC of a 256 Josephson junction array (2.0 μm × 2.0 μm) at a microwave frequency of 5 GHz, power 8.7 dBm, step width 1.1 mA. The inset shows the flat Shapiro step at a higher resolution.

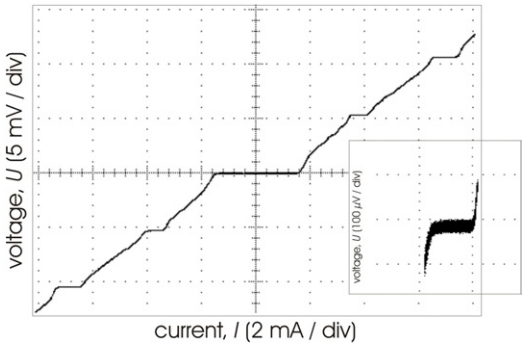

Figure 8. IVC of a 256 Josephson junction array (2.0 μm × 2.0 μm) at a microwave frequency of 20 GHz, power 13.5 dBm, step width 0.7 mA. The inset shows the flat Shapiro step at a higher resolution.

As a first characterization, the arrays were operated under sine wave irradiation before they were investigated under pulse pattern irradiation (results will be published elsewhere). These measurements were performed at different frequencies as pulse operation requires a broadband response of the arrays. As an example, figures 7 and 8 show microwave-induced steps of constant voltage at frequencies of 5 and 20 GHz for an array of 256 Josephson junctions. In both cases the output power level of the microwave source was adjusted for broad and flat Shapiro steps. The critical current for this array is $I_c = 1.5$ mA and the junction area is 2.0 μm × 2.0 μm. The characteristic voltage is about 9 μV. The measured step width of 1.1 mA at 5 GHz and 0.7 mA at 20 GHz is well suited for the array to be driven by short pulses. The maximum step width on average is 75% of the critical current for the tested arrays.

Subharmonic steps are observed for all SNS arrays and all junction sizes, although the reason for this is unclear. Some authors have explained this behaviour with a non-sinusoidal current-phase relation [19] or deviation from the point junction model [17, 18].

To demonstrate that the described technology is suitable for the fabrication of small junctions, the IVC of a single junction (200 nm × 200 nm) under microwave irradiation is presented in figure 9 (critical current I_c = 180 μA, characteristic voltage $V_c = 72$ μV, and critical current density $j_c = 450$ kA cm^{-2}).

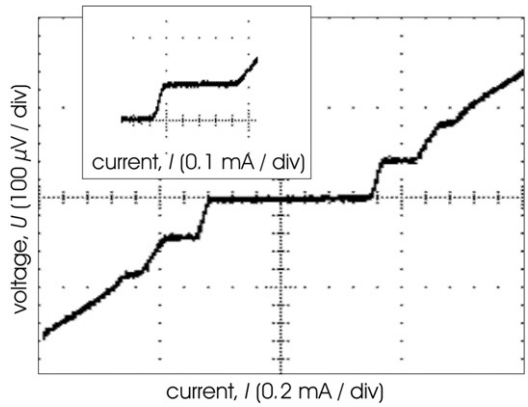

Figure 9. IVC of a Josephson junction (0.2 μm × 0.2 μm) at a microwave frequency of 20 GHz, power 15.5 dBm, step width 90 μA.

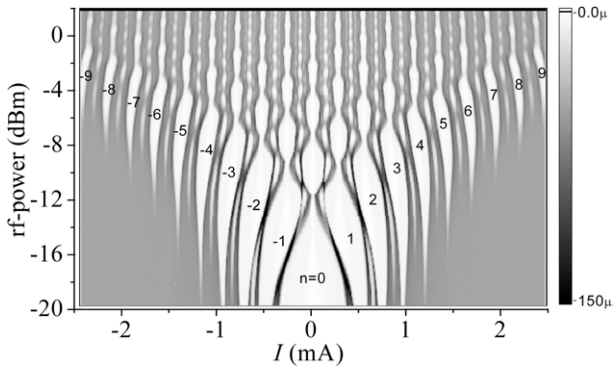

Figure 10. Grey-scaled plot of the current versus dU/dI as a function of RF power at 5 GHz. The grey-scaled values represent absolute values of dU/dI. White regions mark values near zero, i.e. step region (indicated by Shapiro step number n); grey shades denote the transition between steps. The array contained 512 Josephson junctions of 0.7 μm × 0.7 μm.

The relatively high microwave power used is due to the fact that the single junctions were not implemented in a microwave design. Therefore the achieved step width of 90 μA is limited by the maximum output power level of the available microwave source.

Figure 10 shows the IVC as a function of the applied microwave power at a frequency of 5 GHz using an array of 512 junctions (size 0.7 μm × 0.7 μm). The grey-scaled values are the derivatives of dU/dI. White shows a step and the grey shades the transition between steps. The pattern of this figure illustrates that the behaviour of this array is in good agreement with the resistively shunted junction model (cf [18]). The achieved maximum step voltage (first Shapiro step) for this array corresponds to 21 mV at 20 GHz.

5. Conclusion and outlook

A new method of production was developed which allows the fabrication of sub-μm Josephson junctions down to the 200 nm range. This method proved both advantageous and successful for the application and development of small production series which are typical in metrology. Circuits fabricated for JAWS applications show high-quality IVCs and broad voltage steps under RF irradiation.

Investigations in the pulse-driven mode are currently under way. To increase the output voltage, the number of junctions for an array has to be increased. If the array's layout were to be altered by reducing the length of the base structures and the distance between two base structures, the number of junctions fitting into a lumped array would nearly double, leading to a further increase in the output voltage.

Acknowledgments

The authors would like to thank Th Weimann and P Hinze for their help with the electron-beam writer. Also, our thanks go to B Egeling and R Wendisch for their help with the PECVD and CMP processes.

The work was supported within the EU-funded joint project JAWS (G6RD-CT-2001-00599).

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