From Table III,

$$K_1 = 4 \tag{53}$$

$$\alpha = r_0$$

$$= 12/8 = 1.5 \tag{54}$$

from (34). Note that transducer output is zero at T = 278 K (5°C).

From (16) and (53),

$$e_0\Big|_{x=1.108} = 4 \times (1.108 - 1)e_i = 0.432e_i. \tag{55}$$

Consequently, for $|e_0| \doteq 1.0$ V, from (55)

$$|e_i| \doteq 2.3 \text{ V}. \tag{56}$$

Once the circuit impedance level has been decided, thus, along with (52), completely specifying the thermistor required, resistors R_1,R_3,R_4 are also fixed. For a thermistor having $R(25°C) = 5 \times 10^3\ \Omega$ and $b = 2780$, $R(5°C) = 11.2 \times 10^3\ \Omega$; whence, from (9) and (54),

$$R_1 \doteq 7.5 \times 10^3\ \Omega. \tag{57}$$

For $R_3 = 10 \times 10^3\ \Omega$, from (13) and (54),

$$R_4 = 15 \times 10^3\ \Omega. \tag{58}$$

A circuit for this transducer is shown in Fig. 3.

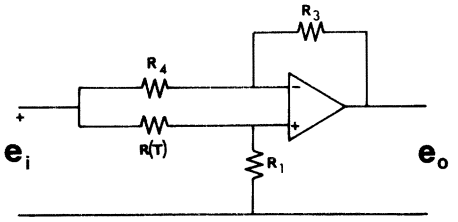

Fig. 3. Active thermistor bridge design example. R_1 = 7.5 K, R_3 = 10.0 K, R_4 = 15.0 K, e_i = 2.3 V. Thermistor: $R(25°C)$ = 5.0 K, b = 2780.

CONCLUSION

A technique for the analysis and design of six one-thermistor temperature transducer circuits has been presented in a way which exploits their basic mathematical similarities. Conditions for maximizing response linearity with respect to the selected operating point have been derived and illustrated. Three circuits containing active elements offer similar gain magnitudes under balance conditions and maximum linearity, being about twice the gain for the simple bridge circuit under similar conditions.

REFERENCES

[1] R. V. Churchill, *Complex Variables and Applications*, 2nd ed. New York: McGraw-Hill, 1960, p. 73.
[2] R. C. Guyton, "Feedback linearizes resistance bridge," *Electronics*, vol. 45, p. 102, Oct. 23, 1972.

Tetrahedral Junction Error Contribution to a Series-Parallel Four-Terminal Resistor

CHESTER H. PAGE, FELLOW, IEEE

***Abstract*—The errors of a series-parallel four-terminal resistor build-up box due to imperfections in the tetrahedral junctions are analyzed. It is shown how these errors can be made negligible by choosing orientations of the junctions.**

THE ADVENT of Josephson-junction voltage standards has increased the importance of highly accurate resistance-ratio devices, such as the series-parallel arrangement of four-terminal resistors originated by Hamon [1], [2]. A string of n resistors permanently connected in series, with additional terminals connected to the junctions

Manuscript received June 14, 1973; revised September 21, 1973.
The author is with the Electricity Division, Institute for Basic Standards, U. S. Bureau of Standards, Washington, D. C. 20234.

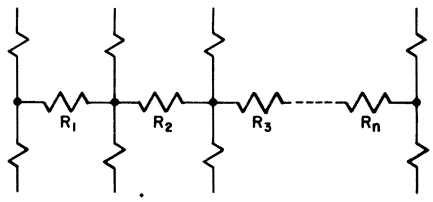

Fig. 1. Resistor string showing lead resistances.

to allow parallel connection of the resistors, offers the possibility of an exact n^2:1 ratio (Fig. 1). Errors are introduced by the resistances of the various leads, and by the fact that the junction of several leads does not form a "point," but a small four-terminal resistor.

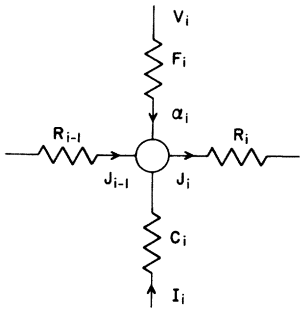

Fig. 2. Unit cell of resistor string.

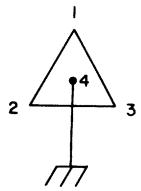

Fig. 3. Triangular slab junction.

The use of both voltage and current fans [3] not only reduces the error due to lead resistance, but makes second-order errors measurable in terms of first-order measurements. This analysis assumed that the tetrahedral junction errors were negligible; current applications require such high accuracy that residual junction errors (after trimming individual junctions) must be considered. Riley [4] gave a formula for the maximum error due to the junctions, without detailed analysis. Gorini [5] gave a set of perturbation formulas for the statistics of various error contributions.

The usual procedure for analyzing the effects of a tetrahedral junction is to derive its equivalent bridge configuration and to analyze the resistor string with these bridges included. In this analysis, there are hidden some operations which essentially "un-derive" the equivalent bridge. The straightforward overall analysis using the nodal properties of the junction, without an equivalent circuit representation, gives a simple and useful result.

The current and voltage fans can readily be adjusted to their ideal values, to the relevant order of magnitude of the resulting errors. We shall therefore assume that these fans are ideal. Much of the complication of analyzing the assembly, and of trimming an actual assembly, can be removed by trimming the series elements to *observational* equality, i.e., not by trimming the main resistors before they are interconnected, but by trimming them *after* assembly in a series string.

The basic cell for analysis of a string of n resistors is given in Fig. 2. In the parallel mode, alternate V_i terminals are connected to two buses, and alternate I_i come from two other buses. Small parasitic currents in the voltage fan are represented by the α_i. The alternate connections to common buses give the relations

$$\sum \alpha_{2i} = 0 \qquad \sum \alpha_{2i+1} = 0 \tag{1}$$

with the consequences

$$\sum_{1}^{n+1} \alpha_i = 0 \qquad \sum_{1}^{n+1} (-)^i \alpha_i = 0. \tag{2}$$

Let the departure of I_i from the nominal distribution be represented by the σ_i:

$$\begin{aligned} I_1 &= I_0 + \sigma_1 \\ I_2 &= -2I_0 + \sigma_2 \\ I_3 &= 2I_0 + \sigma_3 \\ I_i &= -(-)^i 2I_0 + \sigma_i \\ I_{n+1} &= (-)^n I_0 + \sigma_{n+1}. \end{aligned} \tag{3}$$

Then the common-bus conditions give

$$\sum \sigma_{2i} = 0 \qquad \sum \sigma_{2i+1} = 0 \tag{4}$$

$$\sum_{1}^{n+1} \sigma_i = 0 \qquad \sum_{1}^{n+1} (-)^i \sigma_i = 0. \tag{5}$$

JUNCTION PROPERTIES

The properties of a four-terminal junction can be expressed (and measured) conveniently in terms of one grounded terminal, with an input current applied to each of the other three terminals in succession. It is convenient to visualize the junction as an equilateral triangular slab with a center connection (Fig. 3). In practice, junctions are often made in this form, or as disks with central leads.

The voltages on 1, 2, 3, relative to ground 4, are linear combinations of the current inputs:

$$U_i = \sum_{j=1}^{3} \rho_{ij} \hat{I}_j \tag{6}$$

where I_j is the current into the nth terminal of the junction. For convenience, we use an abbreviated notation for particular properties:

$$\begin{aligned} \delta &\overset{d}{=} U_2 - U_1, \qquad \text{for } \hat{I}_1 = 0, \quad \hat{I}_2 = 0, \quad \hat{I}_3 = 1 \\ \hat{\delta} &\equiv \rho_{23} - \rho_{13} \end{aligned} \tag{7}$$

$$\begin{aligned} \epsilon &\overset{d}{=} U_3 - U_1, \qquad \text{for } \hat{I}_1 = 0, \quad \hat{I}_2 = 1, \quad \hat{I}_3 = 0 \\ \epsilon &\equiv \rho_{32} - \rho_{12}. \end{aligned} \tag{8}$$

In operation in the assembly (Fig. 2), the input currents of the ith junction are

$$\begin{aligned} \hat{I}_i &= \alpha_i \\ \hat{I}_2 &= J_{i-1} \\ \hat{I}_3 &= -\alpha_i - J_{i-1} - J_i \end{aligned} \tag{9}$$

and the resulting voltages of interest are $U_{1i} - U_{3i}$ and $U_{2i} - U_{1i}$

$$\begin{aligned} U_{1i} - U_{3i} = {} & \alpha_i(\rho_{11,i} - \rho_{13,i} - \rho_{31,i} + \rho_{33,i}) \\ & + J_{i-1}(\rho_{12,i} - \rho_{13,i} - \rho_{32,i} + \rho_{33,i}) \\ & + I_i(\rho_{33,i} - \rho_{13,i}). \end{aligned} \tag{10}$$

Dropping the second-order terms in $\rho\alpha$, we have

$$U_{1i} - U_{3i} = (\delta_i - \epsilon_i + \rho_{33,i} - \rho_{23,i})J_{i-1} + (\delta_i + \rho_{33,i} - \rho_{23,i})I_i. \quad (11)$$

It will be useful to have this voltage also expressed in terms of J_i:

$$U_{1i} - U_{3i} = (\delta_i - \epsilon_i + \rho_{33,i} - \rho_{23,i})J_i + \epsilon_i I_i \quad (12)$$

where the additional second-order term $\alpha_i(\delta_i - \epsilon_i + \rho_{33,i} - \rho_{23,i})$ has been dropped. Similarly,

$$U_{2i} - U_{1i} = (\rho_{22,i} - \rho_{12,i} - \rho_{23,i} + \rho_{13,i})J_{i-1} - (\rho_{23,i} - \rho_{13,i})I_i \quad (13)$$

with $\rho\alpha$ terms omitted. This can be written

$$U_{2i} - U_{1i} = (\epsilon_i - \delta_i + \rho_{22,i} - \rho_{23,i})J_{i-1} - \delta_i I_i. \quad (14)$$

The successive voltage differences on the voltage terminals along the string are

$$\begin{aligned} V_i - V_{i+1} &= \alpha_i F_i + (U_{1,i} - U_{3,i}) + J_i R_i \\ &\quad + (U_{2,i+1} - U_{1,i+1}) - \alpha_{i+1}F_{i+1} \\ &= J_i(R_i + \delta_i - \delta_{i+1} - \epsilon_i + \epsilon_{i+1} \\ &\quad + \rho_{33,i} + \rho_{22,i+1} - \rho_{23,i} - \rho_{23,i+1}) \\ &\quad + \epsilon_i I_i - \delta_{i+1}I_{i+1} + \alpha_i F_i - \alpha_{i+1}F_{i+1}. \end{aligned} \quad (15)$$

This equation can be simplified by expressing some of its components in terms of series-mode measurements.

SERIES MODE

In series-mode operation, we have the following conditions:

$$\begin{aligned} I_1 &= I \\ I_i &= 0, \qquad i = 2\cdots n \\ I_{n+1} &= -I \\ \alpha_i &= 0 \\ J_i &= I, \qquad i = 1\cdots n. \end{aligned} \quad (16)$$

The observed series element resistances are

$$S_i \overset{d}{=} \frac{V_i - V_{i+1}}{I} \quad (17)$$

so that (15) gives

$$\begin{aligned} S_1 &= R_1 + \rho_{33,1} + \rho_{22,2} - \rho_{23,1} \\ &\quad - \rho_{23,2} + \delta_1 - \delta_2 + \epsilon_2 \\ S_i &= R_i + \rho_{33,i} + \rho_{22,i+1} - \rho_{23,i} - \rho_{23,i+1} \\ &\quad + \delta_i - \delta_{i+1} - \epsilon_i + \epsilon_{i+1}, \qquad i = 2\cdots(n-1) \\ S_n &= R_n + \rho_{33,n} + \rho_{22,n+1} - \rho_{23,n} \\ &\quad - \rho_{23,n+1} + \delta_n - \epsilon_n + \epsilon_{n+1}. \end{aligned} \quad (18)$$

These relations allow (15) to be expressed more simply:

$$\begin{aligned} V_1 - V_2 &= J_1S_1 - \delta_2 I_2 + \alpha_1 F_1 - \alpha_2 F_2, \\ &\qquad \text{with } \alpha_1\epsilon_1 \text{ dropped} \\ V_i - V_{i+1} &= J_iS_i + \epsilon_i I_i - \delta_{i+1}I_{i+1} + \alpha_i F_i - \alpha_{i+1}F_{i+1} \\ V_n - V_{n+1} &= J_nS_n + \epsilon_n I_n + \alpha_n F_n - \alpha_{n+1}F_{n+1}, \\ &\qquad \text{with } \alpha_{n+1}\delta_{n+1} \text{ dropped.} \end{aligned} \quad (19)$$

By virtue of the voltage buses, the box voltage in the parallel mode is

$$V = V_1 - V_2 = -(V_2 - V_3) = -(-)^i(V_i - V_{i+1}). \quad (20)$$

Now

$$\begin{aligned} J_i &= J_{i-1} + I_i + \alpha_i = \sum_1^i (I_j + \alpha_j) \\ &= (-)^{i+1}I_0 + \sum_1^i (\sigma_j + \alpha_j) \end{aligned} \quad (21)$$

and the ideal voltage fan is described by

$$\begin{aligned} F_1 &= 2F \\ F_i &= F, \qquad i = 2\cdots n \\ F_{n+1} &= 2F. \end{aligned} \quad (22)$$

Using (17)–(19) with (16) gives n expressions for V (terms in $\delta\sigma$ and $\epsilon\sigma$ dropped)

$$\begin{aligned} V &= S_1(I_0 + \sigma_1 + \alpha_1) + 2\delta_2 I_0 + F(2\alpha_1 - \alpha_2) \\ V &= S_i[I_0 - (-)^i \sum^i (\sigma_j + \alpha_j)] + 2\epsilon_i I_0 + 2\delta_{i+1}I_0 \\ &\quad - (-)^i F(\alpha_i - \alpha_{i+1}), \qquad i = 2\cdots(n-1) \\ V &= S_n[I_0 - (-)^n \sum^n (\sigma_j + \alpha_j)] + 2\epsilon_n I_0 \\ &\quad - (-)^n F(\alpha_n - 2\alpha_{n+1}). \end{aligned} \quad (23)$$

Adding these n expressions gives

$$nV = I_0[\sum_1^n S_i + \sum_2^n (\delta_i + \epsilon_i)] - \sum_1^n (-)^i S_i \sum_1^i (\sigma_j + \alpha_j) - 2F \sum_1^{n+1} (-)^i \alpha_i. \quad (24)$$

Equation (2) makes the last term vanish. If all the S_i are equal, the second term becomes

$$\begin{aligned} &- S \sum_1^n (-)^i \sum_1^i (\sigma_j + \alpha_j) \\ &= -S(-)^n(\sigma_n + \sigma_{n-2} + \sigma_{n-4} + \cdots \\ &\quad + \alpha_n + \alpha_{n-2} + \alpha_{n-4} + \cdots) \\ &= 0 \end{aligned} \quad (25)$$

by (1) and (4). Then,

$$nV = I_0[nS - 2\sum_{2}^{n}(\delta_i + \epsilon_i)]. \tag{26}$$

The input current is $I = nI_0$, so the parallel-mode resistance is

$$\frac{V}{I} = \frac{1}{n}\left[S - \frac{2}{n}\sum_{2}^{n}(\delta_i + \epsilon_i)\right]$$

$$= \frac{S}{n}\left[1 - \frac{2}{n}\sum_{2}^{n}\frac{\delta_i + \epsilon_i}{S}\right] \tag{27}$$

and the error is essentially twice the *average* of $(\delta + \epsilon)/S$.

APPLICATION TO CONSTRUCTION

The tetrahedral junction (Fig. 3) can be installed in 24 different orientations. These, however, comprise only 3 different values of $\delta + \epsilon$, and these 3 values can be attained by keeping the central lead for the current fan (or voltage fan) connection and rotating the junction about this lead as an axis. All possible values of $\delta + \epsilon$ can be achieved by orientations that look alike, hence the 3 choices are available to the constructor, with no difference in layout or wiring.

From (6)–(8), it is easily shown that if δ_a and ϵ_a are the parameters for a given orientation, the 3 values of $\delta + \epsilon$ are

$$\delta_a + \epsilon_a \qquad \delta_a - 2\epsilon_a \qquad -2\delta_a + \epsilon_a.$$

The sum of these three vanishes identically, so they cannot all be of the same sign. It is, therefore, a simple matter to reduce the average value by the factor n, or better, from the typical value for a single junction.

In a typical construction (copper triangles $\frac{1}{16}$-in thick, with 1-in sides), we found that the largest junction cross resistance was 2×10^{-7} Ω as produced, without any edge filing to reduce this. These junctions were used in a box having ten 100-Ω series elements, hence, the worst set of orientations could introduce an error of 8×10^{-9}. By choosing orientations giving both positive and negative terms, this is easily reduced to below 10^{-9}, which makes this error negligible in comparison with other sources of error in the use of the box.

REFERENCES

[1] B. V. Hamon, *J. Sci. Instrum.*, vol. 31, pp. 450–453, 1954.
[2] F. K. Harris, H. A. Fowler, and P. T. Olsen, *Metrologia*, vol. 6, no. 4, pp. 134–141, 1970.
[3] C. H. Page, *J. Res. Nat. Bur. Stand.*, vol. 69C, p. 181, 1965.
[4] J. C. Riley, "The accuracy of series and parallel connections of four-terminal resistors," *IEEE Trans. Instrum. Meas.*, vol. IM-16, pp. 258–268, Sept. 1967.
[5] I. Gorini, "Errors in the parallel connection of a 100:1 series parallel buildup of four-terminal resistors," *IEEE Trans. Instrum. Meas.*, vol. IM-21, pp. 186–197, Aug. 1972.

Low-Frequency Parametric Amplifier for Small Voltage Measurements

ANTE ŠANTIĆ

***Abstract*—This paper analyzes the low-frequency parametric amplifier, which, in opposition to the parametric amplifiers in the high-frequency range, is wide band and can be realized only simultaneously as an upper and lower sideband up-converter. Three derived basic equations give the possibility of drawing equivalent circuits, in order to calculate gain and stability conditions. The influence of detuning on characteristics of amplifiers is analyzed and investigated experimentally. Cascading more stages of parametric amplifiers is meaningless. The best results can be obtained when the second stage is an upper sideband up-converter. LF parametric amplifiers enable us to achieve a low noise (<0.3 μV for 100-Hz bandwidth), free from flicker noise, a high input resistance and a high common-mode rejection ratio. For this reason, the amplifier can be applied as the measuring preamplifier of brain voltages.**

Manuscript received November 16, 1972.
The author is with the Department of Electrical Engineering, University of Zagreb, Unska 17, Yugoslavia.

I. INTRODUCTION

THE paper presents the theory and application of a low-frequency parametric amplifier. The LF parametric amplifier is distinguished by little noise, low drift, high input resistance, a high rejection ratio, and symmetrical input; an advantage in measuring LF voltages (< 50 μV) such as the voltage of biological activities. The LF parametric amplifier (Figs. 5 and 7) was applied as a preamplifier in more than 300 electroencephalograph channels. Resonant dielectric amplifiers, which have been known for several decades, work on the same principle as the LF parametric amplifiers, but the former have little voltage gain due to their unsuitable capacitive elements (little $\Delta C/\Delta v$ ratio) [1]. These amplifiers, when analyzed