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High-resolution data acquisition technique in broadband seismic observation systems

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The dynamic range of the currently most widely used 24-bit seismic data acquisition devices is 10–20 dB lower than that of broadband seismometers, and this can affect the completeness of seismic waveform recordings under certain conditions. However, this problem is not easy to solve because of the lack of analog to digital converter (ADC) chips with more than 24 bits in the market. In this paper, we propose a method in which an adder, an integrator, a digital to analog converter chip, a field-programmable gate array, and an existing low-resolution ADC chip are used to build a third-order 16-bit oversampling delta-sigma modulator. This modulator is equipped with a digital decimation filter, thus facilitating higher resolution and larger dynamic range seismic data acquisition. Experimental results show that, within the 0.1–40 Hz frequency range, the circuit board's dynamic range reaches 158.2 dB, its resolution reaches 25.99 bits, and its linearity error is below 2.5 ppm, which is better than what is achieved by the commercial 24-bit ADC chips ADS1281 and CS5371. This demonstrates that the proposed method may alleviate or even completely resolve the amplitude-limitation problem that so commonly occurs with broadband observation instruments during strong earthquakes.

seismic data acquisition, analog to digital conversion (ADC), high resolution, dynamic range, delta-sigma modulation

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1 Introduction

Seismic observation has always striven for broadband responses and large dynamic ranges. During the Tenth Five-year Plan, a great number of broadband observation instruments were installed at various seismic stations. However, this still does not satisfy the existing practical needs. During the 2008 Wenchuan earthquake, for example, broadband observation instruments at stations across a large area (including stations more than 1000 km away from the epicenter) encountered a problem of amplitude limitation, which rendered the recorded waveform unusable and caused the loss of valuable data that could otherwise have been used for intensive study of this strong earthquake.

One of the main causes of this amplitude limitation problem is the inadequate dynamic range of broadband observation instruments. A real earthquake dynamic range is very large, from microseisms below Grade 1 to strong earthquakes, which may be above Grade 9 and may result in great damage; measured in decibels, it can exceed 180 dB. In recent years, the study of seismic wave velocity and its underlying structure using background noise data recorded at seismic stations has become a hot topic [1,2]. The earth's ambient background noise has become a very useful form of information, but this requires the self-noise level of seismic instruments to be below that of the earth's ambient background noise.

Broadband observation instruments consist of seismometers and seismic data acquisition devices. The dynamic

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range of the present broadband seismometers existing abroad, such as the STS-1 and STS-2 seismometers, exceeds 150 dB [3]. For domestically produced seismometers, such as the broadband seismometers BBVS-60 and BBVS-120 (www.geodevice.cn), and broadband seismometers JCZ-1 [4] and CTS-1 [5], the dynamic range is also larger than 140 dB. If the self-noise and sensitivity of broadband seismometers are further optimized, their dynamic range and stability may also increase.

The core task of seismic data acquisition devices is to convert analog signals from the seismometers into digital signals suitable for computer (digital) processing. Their performance (resolution, for example) depends largely on the quality of their internal analog to digital converter (ADC) [6]. At present, the best commercial ADC chips available for seismic observation are 24-bit ADCs, such as the ADS1281/ADS1282 from Texas Instruments, AD1555/ AD7765 from Analog Devices, and CS5371/CS5372 from Cirrus Logic. According to the datasheets, their noise spectral density is at the –150 dB level, with full scale at 0 dB. In the current seismic observation networks, the sampling frequency is often set to 100 Hz, for a frequency band of interest below 40 Hz. The dynamic range is defined as the ratio of the root means square (RMS) value of the full scale to the total RMS noise measured with the inputs shorted together. Based on this definition, the dynamic range of these 24 bit ADCs is 131 dB, within the 0.1–40 Hz frequency range.

Many researchers have developed 24-bit seismic data acquisition devices based on these chips [6–16]. However, because of their performance limits, the dynamic range of the resulting data acquisition devices is limited to about 130 dB [6,7], which is 10–20 dB lower than that of the available broadband seismometers. This means that even if the ground movements are within the scope of seismometric monitoring, further amplitude restrictions for proper recording may result from the data acquisition device's shortcomings. If the dynamic range of the data acquisition devices could have been improved to 140–150 dB, broadband observation instruments at the surrounding stations would not have encountered amplitude-limitation problems at the time of the Wenchuan earthquake.

In the U.S., Kinemetrics Corporation developed a commercial device, Q330HR, for high-resolution seismic data acquisition of broadband seismic observations (www.kinemetrics.com). It has three 26-bit acquisition channels, whose dynamic range is 144 dB at a sampling rate of 100 Hz. However, although 26-bit seismic data acquisition has occurred abroad, the corresponding technical details have not been reported. For high resolution (more than 24 bit) and large dynamic range (150 dB, within a 40 Hz bandwidth) seismic data acquisition, independent research must be performed. With ADC chips of more than 24 bits currently absent from the market, it is not possible to simply choose a commercial ADC chip for the analog to digital conversion tasks.

The key problems and difficulties for higher-resolution data acquisition devices lie in achieving more than 24 bit ADC circuits. In this paper, a high-resolution ADC circuit is proposed; it involves a combination of an adder, an integrator, an existing low-resolution ADC chip, a field-programmable gate array (FPGA), and a digital to analog converter (DAC) chip to form a multi-order multi-bit delta-sigma modulator. This modulator is equipped with a digital decimation filter, forming a complete high-resolution analog to digital conversion circuit. Based on this idea, a detailed circuit is designed and a PCB board is produced. Experimental results demonstrate the feasibility and effectiveness of the proposed method. The current objective is to use it to implement a higher-resolution seismic data acquisition device, thereby increasing the observation system's effective dynamic range and its ability to obtain complete seismic waveform information, and thus better support advanced research in tomography, earth free oscillation, and similar fields.

2 High-resolution ADC circuit design

The two techniques that can achieve high-resolution analog to digital conversion are oversampling delta-sigma modulation and multi-slope integration. However, the conversion rate of multi-slope integration ADCs is slow; for example, Agilent's digital multi-meter HP3458A converts only six times per second when working in 8 1/2 digits mode (equivalent to 27–28 bits in binary) [17]. In seismic observations, the seismic wave band of a natural earthquake that needs to be recorded ranges mainly from a 360 s period to 50 Hz. This requires the sampling frequency of the data acquisition device to be above 100 Hz, and this need is not met by multi-slope integration. We therefore take advantage of the oversampling delta-sigma modulation technique [18–20].

2.1 Third-order 16-bit oversampling delta-sigma modulator

Figure 1 shows a schematic diagram of the proposed high-resolution ADC experimental circuit. As shown, an adder, an integrator, a DAC chip, an existing low-resolution ADC chip, and an FPGA are used to build a multi-bit oversampling delta-sigma modulator. The analog signal from the seismometer enters the modulator via the preamplifier. The modulator samples the analog input signal and converts it to a high-rate low-resolution bit data stream. To obtain the desired seismic signal, a digital decimation filter is used to convert the high-rate low-resolution data stream into a low-rate high-resolution digital signal. A digital audio transmitter and a Sony/Phillips digital interface (S/PDIF)

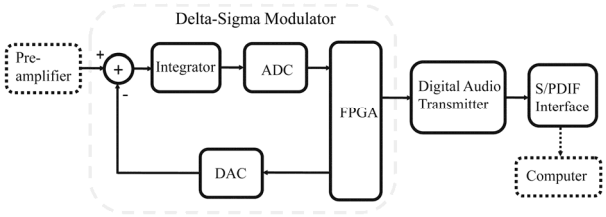

Figure 1 Schematic diagram of the high-resolution analog/digital conversion experimental circuit.

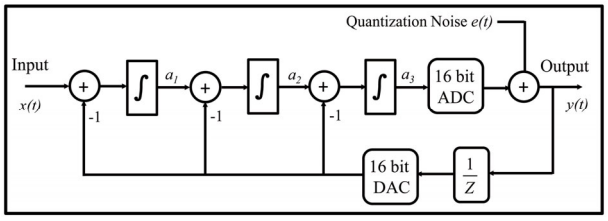

Figure 2 Basic model of the third-order 16-bit delta-sigma modulator.

are then used to send the modulator output to a computer, where further analysis and processing are performed. The FPGA acts as a bridge between the ADC chip, DAC chip, and digital audio transmitter. It is responsible not only for providing the correct timing for these three chips, but also for transferring data among them.

The system dynamic range (DR) that delta-sigma modulation ADCs can achieve depends on the oversampling ratio (R), integrator order (L), and internal number of quantizer bits (N). This relationship can be described as follows [20]:

$$DR = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N - 1)^2 R^{2L+1}.$$

This equation shows that increasing the integrator's order, the number of quantizer bits, and the oversampling ratio can improve the ADC's dynamic range. However, because the delta-sigma modulator is a nonlinear system with negative feedback, the higher the integrator's order, the worse the system's stability. In the actual delta-sigma modulator, the integrator's order seldom exceeds five.

Considering this equation, a third-order integrator and a 16 bit quantizer are selected for the following reasons: 1) To ensure the stability of the delta-sigma modulator; 2) to achieve a higher than 150 dB dynamic range with a relatively low oversampling ratio. A lower oversampling ratio, which translates to a lower sampling rate, facilitates circuit implementation and alleviates the pressure on the digital filter.

To facilitate further analysis, a basic model of the third-order 16-bit modulator is shown in Figure 2. Because the represented 16-bit ADC is an ideal converter, quantization noise is added to model the quantization noise produced during the analog to digital (A/D) conversion.

As shown in Figure 2, after passing through the integration circuit and A/D conversion, quantization noise is added to the input signal to produce an output signal, which is then fed back into the input after delay and digital to analog (D/A) conversion, forming a negative feedback loop. The signal and quantization noise transfer functions of the system are then computed and analyzed in the s domain. The system's input signal $x(t)$ and quantization noise $e(t)$ transfer functions are given by

$$H_x(s) = \frac{a_1 a_2 a_3}{s^3 + a_3 s^2 + a_2 a_3 s + a_1 a_2 a_3}, \quad (1)$$

$$H_e(s) = \frac{s^3}{s^3 + a_3 s^2 + a_2 a_3 s + a_1 a_2 a_3}. \quad (2)$$

Eq. (1) is a typical transfer function of a third-order low-pass filter, and eq. (2) is a typical transfer function of a third-order high-pass filter. The delta-sigma modulation system is therefore showing low-pass filtering characteristics for the input signal, and high-pass filtering characteristics for the quantization noise. Because the target signal is mainly distributed in the low frequency band, it is possible to filter out the quantization noise outside the baseband using a low-pass decimation filter. This method can reduce the circuit board's noise floor, convert the high-rate low-resolution bit data stream of the modulator into the required low-rate high-resolution digital signal and thus give the data acquisition device both a higher signal-to-noise ratio (SNR) and a larger dynamic range.

2.2 Computation of the integrator parameters

In the two transfer functions described above, three unknown parameters (a_1, a_2, and a_3) characterize the modulator feedback loop. Once the values of these three parameters are identified, the overall feedback loop can be determined. We use a Butterworth filter as the delta-sigma modulator's transfer function model. The transfer function of a third-order Butterworth low-pass filter is as follows:

$$H_x(s) = \frac{\omega_0^3}{s^3 + 2\omega_0 s^2 + 2\omega_0^2 s + \omega_0^3}. \quad (3)$$

Comparing eqs. (1)–(3) shows that the transfer function of the delta-sigma modulator matches that of the third-order Butterworth filter. Within the effective passband, the transfer function of the Butterworth filter is very flat and smooth. This characteristic is ideal for the delta-sigma modulator; therefore, the Butterworth filter is used as a reference to determine the modulator feedback loop's parameters.

Specifically, when identifying the three coefficients of the modulator feedback loop, the parameters of the Butterworth filter will be used as references ($a_1 = 0.5\omega_0$, $a_2 = \omega_0$, and $a_3 = 2\omega_0$). The problem of identifying the three parameters of the feedback loop therefore becomes a problem of identifying the single variable (ω_0) of the Butterworth filter. The value of ω_0 can be determined using a third-order But-

terworth low-pass filter simulation in Matlab. The objective is to obtain a value for ω_0 that can not only make the delta-sigma modulator possess a good noise shaping effect, but can also ensure that the system is stable and does not oscillate.

To pursue this objective, a simulation model of the modulator feedback loop must be built, to enable waveform observation, functional simulation, and spectral analysis of the output, and thus determine the best value for ω_0. A simulation model is built in Matlab Simulink (Figure 3). In this model, a_1, a_2, and a_3 are the feedback loop parameters. The inputs are a 2 V (peak-to-peak), 25 Hz sinusoidal waveform, and a 2 V (peak-to-peak), 100 Hz sinusoidal waveform. The number of bits of the uniform decoder and uniform encoder modules is set to 16. Because a sampling frequency of 48 kHz is used in this paper, the sampling time of the unit delay module is set to 1/48000 s.

As shown in eq. (3), a bigger ω_0 implies a wider available signal bandwidth. As shown in eq. (2), a bigger ω_0 also implies a greater attenuation of the quantization noise in the low frequency band. However, larger values of ω_0 may raise stability issues. For this reason, we need to choose a range of values to simulate, analyze the system's stability, and find the maximum usable value of ω_0.

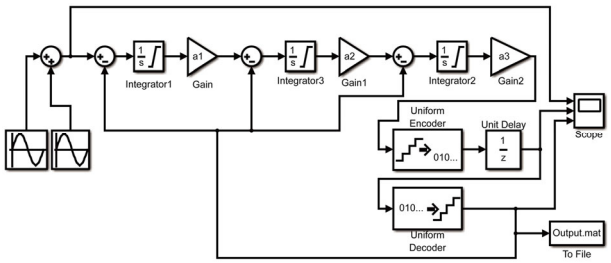

Figure 3 Simulation model of the third-order 16-bit delta-sigma modulator.

After many simulations, we determined that when f_0 ($\omega_0=2\pi f_0$) falls between 2.7 and 2.8 kHz, the system reaches an unstable state. A value of f_0 = 2.7 kHz implies that ω_0 = 16964 rad/s. As previously discussed, $a_1 = 0.5\omega_0$, $a_2 = \omega_0$, and $a_3 = 2\omega_0$; therefore, a_1=8482, a_2= 16964, and a_3 = 33928. The waveforms obtained after this simulation are made visible by the "Scope" module in Figure 4. These waveforms are taken from the input, ADC output, and DAC output. As shown in Figure 4, the first waveform (input) and the third waveform (DAC) have almost precisely identical pattern, which shows that the delta-sigma modulator is working stably with the chosen parameters.

Figure 5 shows the simulation results obtained for f_0 = 2.8 kHz. In this case, ω_0=17592 rad/s, and the parameters become a_1 = 8796, a_2 = 17592, and a_3 = 35184. As shown in Figure 5, the output of the ADC and DAC switches between the positive full scale and negative full scale. This means that the integrating circuit is already saturating, and the delta-sigma modulator has become unstable.

To ensure the system's long-term stability, f_0 = 2.5 kHz is used in the developed circuit board. The corresponding coefficients are a_1 = 7854, a_2 = 15708, and a_3 = 31416. The integrator's specific resistance and capacitance value can be computed using these results.

After the simulation is complete, the "To File" module saves the output data stream as a ".mat" file in the current directory. Reading this file and performing an FFT transformation, the power spectral density of the output data stream can be obtained, as shown in Figure 6. The two spectral peaks correspond to the input signals; the higher frequency noise floor is also visible. Because the model was designed for 10 V at full scale (0 dB), the peaks corresponding to the 2 V (peak-to-peak) sine waves have amplitudes of –20 dB. As shown in Figure 6, a good noise shaping effect was obtained: From DC to 200 Hz the noise floor is at below –200 dB; above 200 Hz the noise floor increases

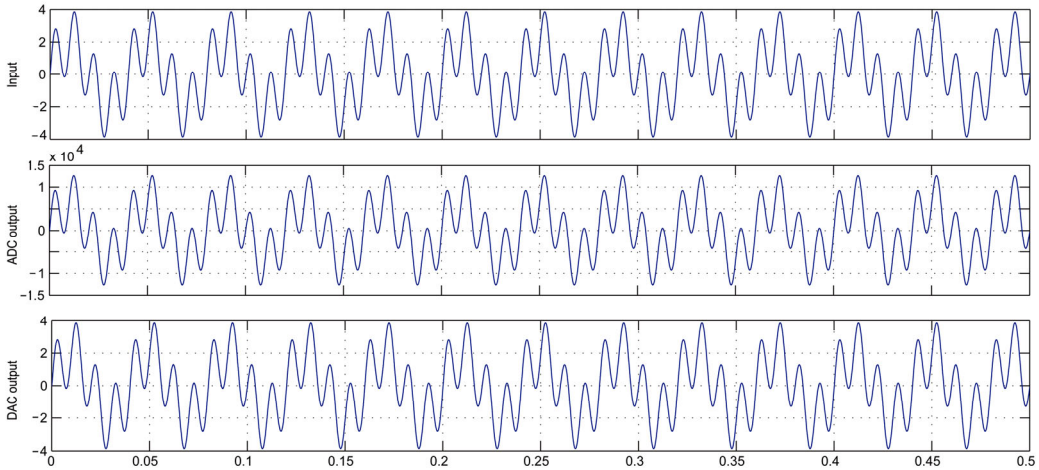

Figure 4 Simulation waveforms of the third-order delta-sigma model for f_0 = 2.7 kHz.

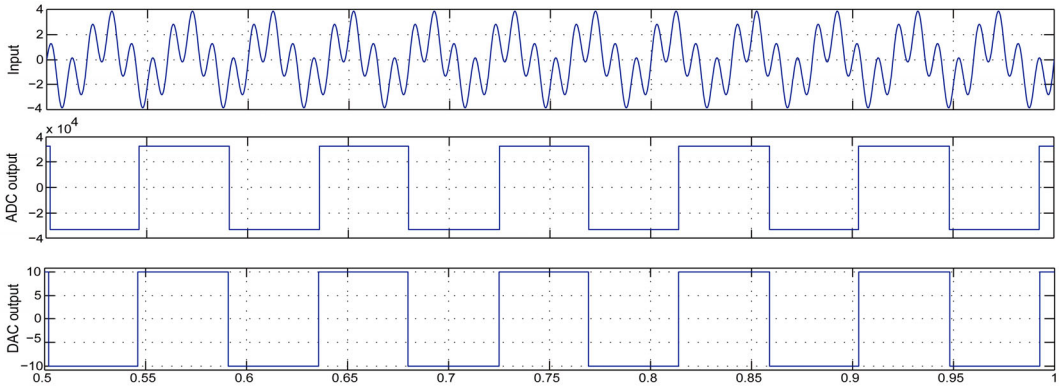

Figure 5 Simulation waveforms of the third-order delta-sigma model for f_0 = 2.8 kHz.

noticeably, as expected.

The dynamic range and effective number of bits (ENOB) achieved by the simulation model up to 80 Hz are computed. From DC to 80 Hz the noise floor is below –200 dB, which indicates that the approximated root means square (RMS) noise value can be upper bounded by $\sqrt{\int_0^{80} 10^{-20}\mathrm{d}f} \times 10$ V = 8.95 nV. The full scale of the sine wave is set to 10 V, for a maximum signal RMS value of 7.07 V. The dynamic range (signal-to-noise ratio) is the ratio of the RMS value of the full scale to the total RMS noise measured with the inputs shorted together. Using this definition, results show that within the band of DC to 80 Hz, the dynamic range of the simulation model is $20\log\frac{7.07}{8.95\times10^{-9}} = 179$ dB. There is a relationship between the signal-to-noise ratio (SNR) and ENOB: SNR=6.02ENOB+1.76. From this equation, we obtain a value for ENOB (the resolution of the simulated model within the band of DC–80 Hz) of 29.4 bits. Therefore, the simulation results show that with the selected parameters desired objective can be achieved. The full chosen set of parameters is as follows. Integrator order, 3; number of internal quantizer bits, 16; a_1, 7854; a_2, 15,708; a_3, 31,416; sampling frequency, 48 kHz.

2.3 Digital decimation filter

The output of the multi-bit delta-sigma modulator is a 48 kHz high-rate low-resolution bit data stream. In this data stream, the signals in question are mainly within the low frequency bands (the seismic wave frequency is usually below 100 Hz). To extract the required information, it is necessary to design a low-pass decimation filter to convert the high-rate low-resolution bit data stream into the required low-rate high-resolution digital signal.

A linear minimum phase FIR filter can be used for low-pass filtering and sampling rate conversion. Considering the large size of the required extraction ratio drop (48000/200=240), a multi-stage FIR decimation filter is designed, as shown in Figure 7, to reduce computational complexity. The first filtering stage is a low-pass FIR filter with an extraction ratio drop of 15. The filter input is the digital signal sampled at 48 kHz coming from the delta-sigma modulator, and its output is a digital signal with a 3.2 kHz sampling frequency. In this filter, the passband cutoff frequency is set to 80 Hz, and the stopband cutoff frequency is set to 3.1 kHz. The second stage is a low-pass FIR filter with an extraction ratio drop of 8. Its input is the digital signal sampled at 3.2 kHz resulting from the first stage and the output is a signal with a 400 Hz sampling rate. In this filter, the passband cutoff frequency is set to 80 Hz and the stopband cutoff frequency is set to 300 Hz. The third, fourth, and fifth stages are low-pass FIR filters with an extraction ratio drop of two; their outputs are digital signals with sampling rates of 200, 100, and 50 Hz, respectively. Because these three stages have the same extraction ratio and the same ratio of transition bands to basebands, identical filter coefficients can be used to design the filter.

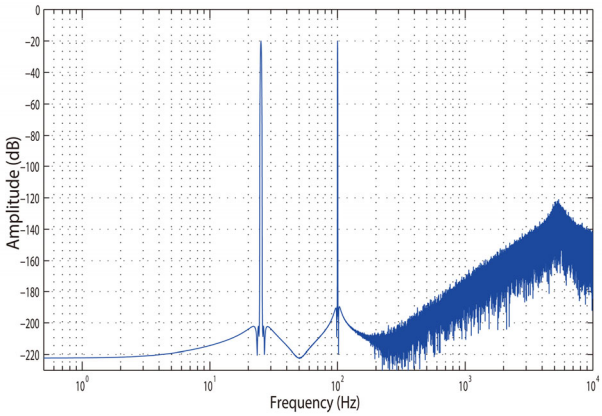

Figure 6 Output power spectral density of the third-order delta-sigma model for f_0 = 2.5 kHz.

3 Results and discussion

To illustrate the method described above, a detailed circuit

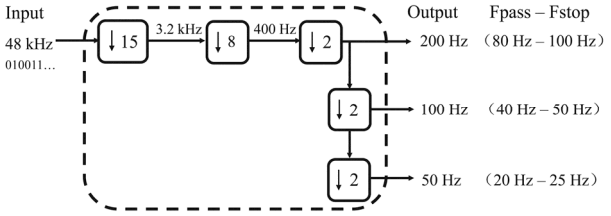

Figure 7 Signal flow graph of the multistage FIR decimation filter.

schematic is drawn and a corresponding printed circuit board fabricated, using the determined parameters and the implied relevant components. The circuit board itself is welded, debugged, and tested.

To build the 16-bit oversampling delta-sigma modulator, precision resistors, precision capacitors, and low-bias/low-noise operational amplifiers are used in the integrator and adder; ADC and DAC chips from Analog Devices with low-noise characteristics and good linearity are also used. To reduce the development time and workload involved in this experiment, the digital filtering and decimating tasks are implemented using the Matlab software package. A Xilinx Corporation's XC2C256 chip is selected as FPGA. It receives clock from a crystal oscillator, generates the correct timing for the ADC, DAC, and digital audio transmitter, receives and processes the ADC data, and sends them to the DAC and the digital audio transmitter.

In this experiment, a relatively high oversampling frequency is used (48 kHz). If the modulator's output was sent to the computer via RS232 or RS485 serial interfaces, data loss might occur. To avoid this and facilitate the circuit's test and evaluation, we implement an S/PDIF audio interface on the board. TI Corporation's DIT4192 is selected for use as a digital audio transmitter; it encodes the digital signal from the FPGA into data matching the audio transmission standards, and sends the data to the computer via an S/PDIF interface.

3.1 Functional test

A functional test to this analog/digital conversion circuit board is performed. In this test, a high-quality signal generator from stanford research system (Model DS360) is used as the signal source.

A 2 V (peak-to-peak), 25 Hz sinusoidal wave is first generated using the DS360 and sent to the circuit board. The computer reads the board's output and plots the time-domain waveform of that output, as shown in Figure 8(a). In this figure, the horizontal coordinates denote the sample sequential number, and the vertical coordinates are the board's output amplitude (in count). For this board's output, assuming a 29 bit resolution and 10 V full scale, one count is equivalent to 0.03725 μV ($10/2^{28}$ V), and the corresponding maximum signal 1 V peak amplitude in counts is 1 V/ 0.03725 μV = 2.684×10^7 counts, which is consistent with the measurements presented in Figure 8(a). This waveform completely represents the conversion code of the 2 V (peak-to-peak) input signal without distortion, which shows that the circuit works correctly. Figure 8(b) shows the power spectral density of the signal in Figure 8(a). The spectral peak corresponds to the input signal; the noise floor is also visible, and includes noise coming from both the circuit board and the signal generator.

A 19 V (peak-to-peak), 10 Hz sinusoidal wave is then generated using the DS360 and sent to the ADC circuit board. The computer reads the board's output and plots the time-domain waveform of that output, as shown in Figure 9(a). In this figure, the horizontal coordinates denote the sample sequential number, and the vertical coordinates are the board's output amplitude (in count). If one count is equivalent to 0.03725 μV, the corresponding theoretical amplitude of the peak value (9.5 V) in count is 9.5 V/ 0.03725 μV = 2.55×10^8, which is consistent with the measurements shown in Figure 9(a). This waveform completely represents the conversion code of the 19 V (peak-to-peak) input signal without distortion, which proves that this circuit has a large signal acquisition ability, as proved by a full-scale value of 20 V (peak-to-peak). Figure 9(b) shows the power spectral density of the signal in Figure 9(a). The visible spectral peak corresponds to the input signal; the noise floor is also seen, and includes noise coming from both the

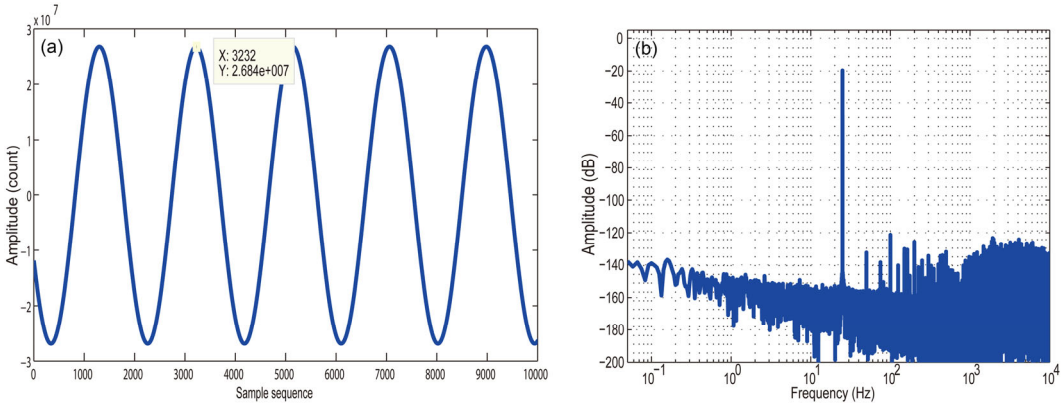

Figure 8 Output for a 2 V (peak-to-peak), 25 Hz sinusoidal input. (a) Time-domain waveform; (b) power spectral density.

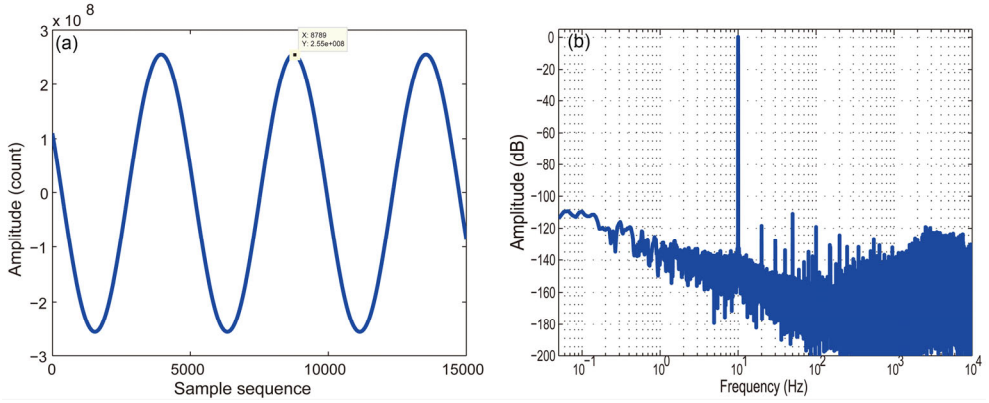

Figure 9 Output for a 19 V (peak-to-peak), 10 Hz sinusoidal input. (a) Time-domain waveform; (b) power spectral density.

circuit board and the signal generator.

Finally, the function of the digital decimation filter is tested. Figure 10 shows the output with a sampling frequency of 100 Hz, after digital decimation filtering, when a 19 V (peak-to-peak), 10 Hz sine wave is input to the circuit board. As shown, due to the reduction in the number of sampling points, although the waveform can approximately reflect the sinusoidal shape, it is not as smooth as that in Figure 9(a).

Figures 8 and 9 show a considerable amount of 1/*f* shaped low frequency noise. It should be noted that a substantial part of this noise comes from the signal generator. As previously stated, a signal generator Model 360 was used as a signal source in this test, to generate 2 V (peak-to-peak), 25 Hz, and 19 V (peak-to-peak), 10 Hz sinusoidal waves. According to the datasheet of this signal generator, its noise reaches up to 150 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ when generating signals with amplitudes in the 1.26–40 V (peak-to-peak) range. Figures 8(b) and 9(b) also show that the low frequency noise decreases if we attenuate the amplitude of the input signal. This proves, from another point of view, that a considerable part of the low frequency noise in Figures 8 and 9 comes from the signal generator.

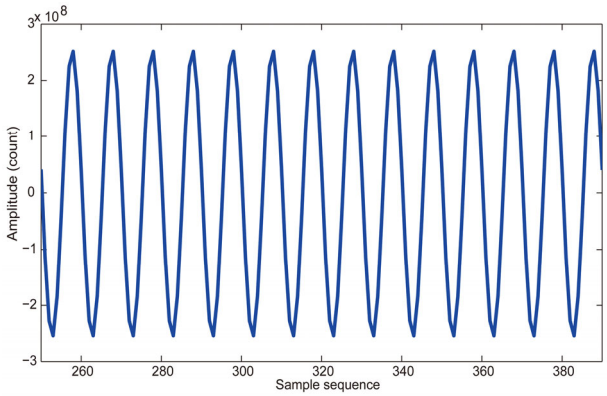

Figure 10 Decimation filter output, with a sampling frequency of 100 Hz and a 19 V (peak-to-peak), 10 Hz sinusoidal input.

3.2 Input shorted noise test

Figure 9(b) is the power spectral density of the signal in Figure 9(a), with full scale at the 0 dB position. It shows that the noise floor of this circuit board is about –140 dB in the 1–40 Hz range. However, the noise observed in this figure is partially caused by the signal generator, as discussed in subsection 3.1.

For this reason, an input shorted noise test is performed to evaluate the circuit board's real noise floor level. Figure 11 shows the power spectral density of the board's output when the inputs are short-circuited. This figure shows that as follows. 1) The usable signal band reaches 800 Hz. Above 800 Hz, the noise level increased markedly. Because the signals in question are distributed in the low frequency bands (from a 360 s period to a 50 Hz frequency), the noise from the high frequency bands is removed using a digital filter. 2) Within the 0.1–10 Hz frequency range, the circuit's noise floor level is below –160 dB. 3) Within the 10–40 Hz frequency range, the circuit's noise floor level is below –180 dB. Such a noise floor is lower than that of the two commercial 24-bit ADC chips ADS1281 and CS5371, whose output power spectral density diagrams are published in their datasheets, and are shown in Figure 12 for comparison. The noise floor of these two chips is of approximately –150 dB. The noise floor of the circuit board designed here is clearly lower than that of those two chips, which proves the effectiveness and feasibility of the proposed method. It should be noted that in Figure 11, a spectral component similar to a small signal can be observed. This is actually 50 Hz interference and its higher harmonics; it is detectable because electromagnetic shielding measures were not used during the experiment.

3.3 Dynamic range and resolution calculation

The dynamic range and resolution are calculated according to the shorted-input noise power spectral density and the design full scale [7]. In Figure 11, full scale is at 10 V and 0 dB. Within the 10–40 Hz band, the circuit's noise floor is at

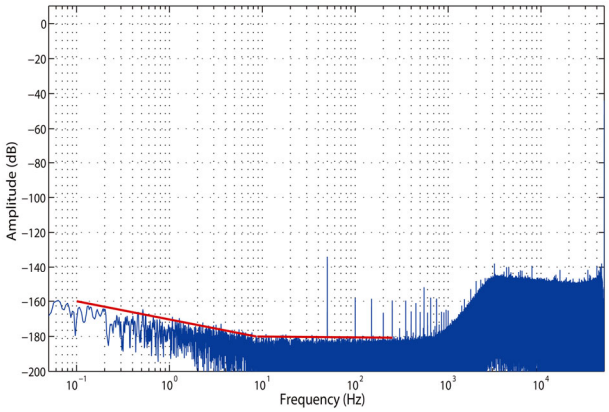

Figure 11 Output power spectral density for a short-circuited input.

–180 dB; within the 0.1–10 Hz band, the circuit's noise floor is below –160 dB. The root mean square (RMS) noise value from 0.1 to 40 Hz can therefore be calculated as follows:

$$\sqrt{\int_{0.1}^{10}\frac{10^{-16}-10^{-18}}{10\times f}\mathrm{d}f+\int_{10}^{40}10^{-18}\mathrm{d}f}\times 10=86.95\ (\mathrm{nV})$$

In this equation, $\frac{10^{-16}-10^{-18}}{10\times f}$ is the estimated noise power spectral density within the 0.1–10 Hz band, 10^{-18} is the noise power spectral density within the 10–40 Hz band, and 10 is the 10 V full scale value, at the 0 dB level.

The signal is a sinusoidal wave using the full 10 V scale range, and therefore with 7.07 V of RMS value. The dynamic range (signal-to-noise ratio) is the ratio of the RMS value of the full scale to the total RMS noise measured with the inputs shorted together, and is expressed in decibels. This definition shows that within the 0.1–40 Hz band (the sampling frequency is 100 Hz), the dynamic range of the circuit board is $20\log\frac{7.07}{86.95\times10^{-9}}=158.2\ (\mathrm{dB})$.

The values of SNR and ENOB are related by: SNR= 6.02ENOB+1.76. According to this equation, the ENOB (the resolution of the data acquisition circuit) within the 0.1–40 Hz band is of (158.2–1.76)/6.02=25.99 bits.

For a fair comparison, the dynamic range and resolution of the two 24-bit chips (ADS1281 and CS5371) are also calculated at the same full-scale condition (10 V). Their noise floors are at approximately –150 dB, and within the 0.1–40 Hz band, their RMS noise value is $\sqrt{\int_{0.1}^{40}10^{-15}\mathrm{d}f}\times10=2\ (\mu\mathrm{V})$. The signal is assumed to be a sinusoidal wave using the full 10 V scale range, and therefore with 7.07 V of RMS value. With these data and the equations given above, the dynamic range and resolution of these chips are 131 dB and 21.5 bits, respectively.

3.4 Linearity test

The circuit board's linearity is also tested. In this test, a high-precision calibrator (Fluke 5720A) is used to generate a DC voltage, as the input signal for the circuit.

Three sets of test are performed. In the first test, the 5720A calibrator is used to generate a sequence of voltages from –9 to 9 V, in 1 V steps, for a total of nineteen DC voltage levels, as input to the circuit board. This voltage sequence is mainly used to assess the overall linearity error of the board. In the second test, the calibrator is used to generate a sequence of voltages from –100 to 100 mV, in 10 mV steps, for a total of 21 DC voltage levels. This sequence set is mainly used to assess the linearity error when the circuit works in small signal mode. In the third test, the calibrator is used to generate a sequence of voltages from 9.01 to 9.09 V and from –9.09 to –9.01 V, in 0.01 V steps. This set is mainly used to assess the linearity error when the circuit works in large signal mode.

The computer reads the circuit board's output corresponding to each DC input, performs digital filtering and decimation on the output, and obtains data at a sampling frequency of 100 Hz. For each value of the DC input, the average value of the output during a period of 20 s is computed and will be called here the "measured value". The first set of tests serves as an example to illustrate the process of calculating the linearity error. Figure 13(a) shows the relation between the measured value and the input DC

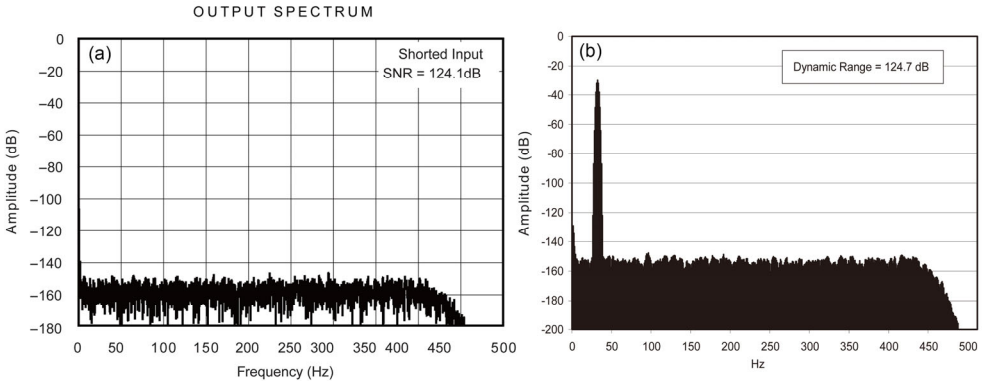

Figure 12 Output power spectral density of 24-bit ADC chips: (a) ADS1281 and (b) CS5371.

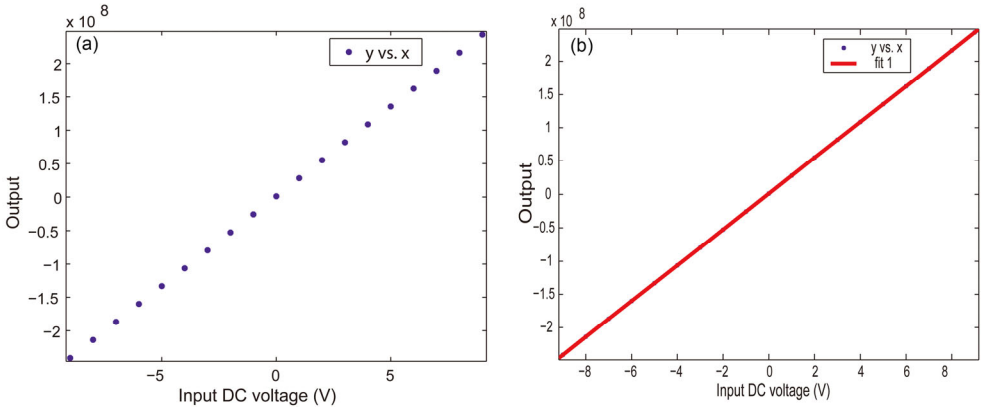

Figure 13 Circuit response for DC inputs in the [–9 V, +9 V] range. (a) Circuit output; (b) linear fit.

voltage during the first set of tests; in this figure, the horizontal coordinates represent the input DC voltages from –9 to +9 V, and the vertical coordinates represent the circuit output (the corresponding sampling frequency is 100 Hz). The MATLAB cftool is used to perform a linear fit on the point diagram of Figure 13(a). The fitted results are shown in Figure 13(b).

To further evaluate linearity, the fitted value and the measured value are subtracted at each measured point. The difference is divided by the digital full scale 2^{28} (As computed in the previous subsection, the circuit board's resolution within the 0.1–40 Hz band is 25.99 bits. Therefore, to express the output data of the board without distortion, 29-bit binary coding is used). Relative output error values are thus obtained for each point (Figure 14(a)). The largest value among them is considered to be the linearity error. As shown in Figure 14(a), with this range of inputs the linearity error of the circuit board is 1.382×10^{-6}.

The linear fit on the measured values and the relative output error computation is performed for the other two sets of tests as well. The results are shown in Figure 14(b)–(d). As shown, the circuit board's linearity error is 1.063×10^{-6} in small signal operation, 2.429×10^{-6} for the [+9.01 V, +9.09 V] inputs, and 2.433×10^{-6} for [–9.01 V, –9.09 V] inputs. These three sets of test results show that the circuit board's linearity error is less than 2.5×10^{-6}, that is, 2.5 ppm.

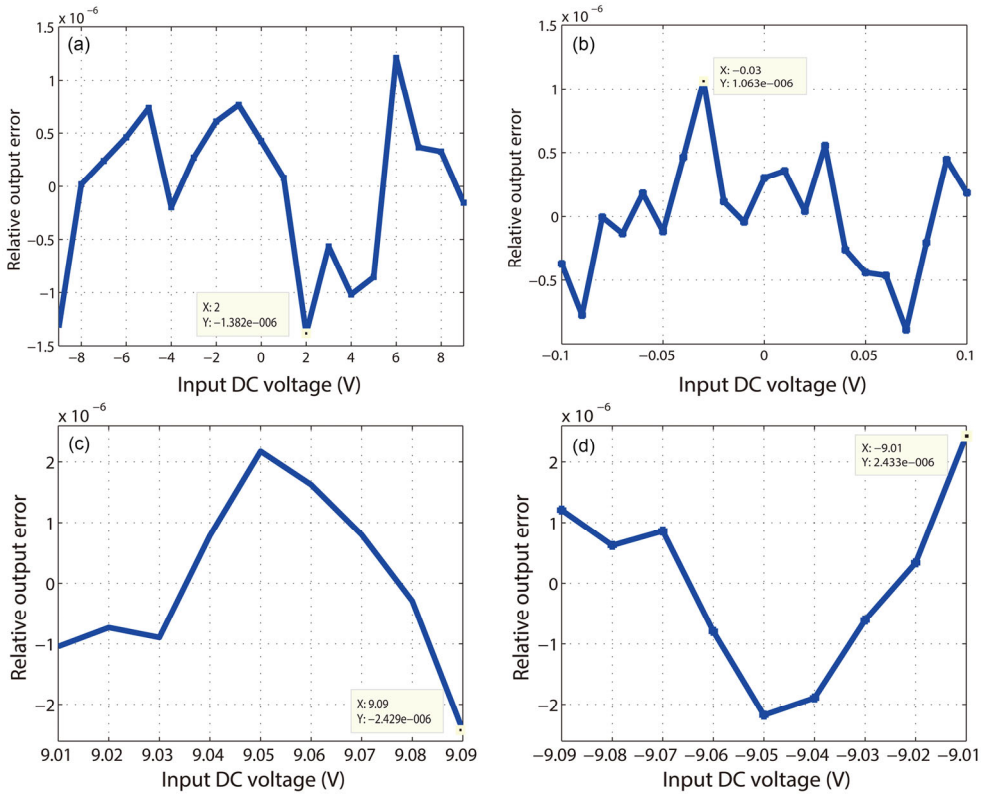

Figure 14 Relative output error for DC inputs of (a) [–9 V, +9 V], (b) [–0.1 V, +0.1 V], (c) [+9.01 V, +9.09 V], and (d) [–9.09 V, –9.01 V].

3.5 Discussion

The main noise contributions for this third-order delta-sigma ADC circuit come from the first stage integrator and the DAC on the feedback loop. Attention should therefore be paid to the design of these two components. We use precision resistors, precision capacitor, and an operational amplifier to build the first stage integrator. Two requirements must be considered when selecting the operational amplifier. 1) The input bias current should be as low as possible, because low input bias current helps to obtain a good integration; 2) under the condition of low input bias current, the amplifier should present low noise. Based on these requirements, we selected the Texas Instruments Corporation's OPA140 as the operational amplifier for this experiment. As desired, it has low input bias current, low noise and very low offset drift. For the DAC on the feedback loop, we use the Analog Devices Corporation's AD5781, which has low noise, good long-term linearity and stability, and low temperature drift. The DAC output is fed back to the input through an AD8675, an operational amplifier with low voltage noise and low input bias current.

Figure 15 illustrates the noise model from the DAC chip on the feedback loop to the first stage integrator. In this model, $V_{N,R1}$ and $V_{N,R2}$ represent the thermal noise of R_1 and R_2, respectively, which are considered here as ideal resistors. $V_{N,AD5781}$ and $V_{N,AD8675}$ represent the noise of the AD5781 and AD8675 chips, and are 7.5 and 2.8 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ respectively. The noise at point A can then be calculated as

$$\sqrt{(V_{N,AD5781}^2 + V_{N,AD8675}^2 + V_{N,R2}^2)\cdot\left(\frac{R_1}{R_1+R_2}\right)^2 + V_{N,R1}^2\left(\frac{R_2}{R_1+R_2}\right)^2}$$
$$= 6.51\ (\mathrm{nV}/\sqrt{\mathrm{Hz}}).$$

The input voltage noise for the OPA140 operational amplifier is 7 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 20 Hz, and 5.8 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 100 Hz. The OPA140 input bias current is very low, typically of only ±0.5 pA, hence, the input current noise is negligible compared with the input voltage noise. The model of the noise injected from the DAC into the first stage integrator is therefore 9.56 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 20 Hz, and 8.72 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 100 Hz. According to the shorted-input noise test result (Figure 11), the noise level of the designed ADC circuit is of approximately 10 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ from 20 to 100 Hz, a slightly higher value than the one resulting from the model in Figure 15.

There is an available commercial device (Q330HR) developed by Kinemetrics Corporation, for high-resolution seismic data acquisition. It has three 26-bit acquisition channels and three 24-bit acquisition channels. According to the progress report on evaluation of the Kinemetrics/Quanterra Q330HR remote seismic system for IRIS/GSN (www.iris.edu), in the 0.1 to 50 Hz range, the RMS noise of the 26-bit acquisition channels is 0.789 μV, the RMS value of full-scale is 14.14 V, and the dynamic range is 145 dB. In the case of our designed circuit board, the RMS noise from 0.1 to 50 Hz is 92.51 nV, the RMS value of full scale is 7.07 V, and the dynamic range is 157.66 dB. Our board is therefore showing better performance values than those of the Q330HR. Hu. et al. [21] studied a 24-bit ADC dynamic range extension method. They used two 24-bit ADCs in one single acquisition unit, with one ADC for small signal acquisition, and the other one for large signal acquisition. Their method is capable of extending the dynamic range, but it carries no improvements to resolution. Our method improves both the dynamic range and the resolution.

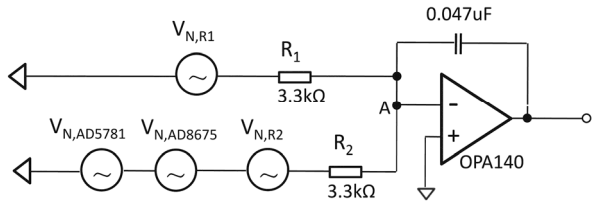

Figure 15 Model of the noise injected from the DAC on the feedback loop into the first integrator.

In Figure 16, the noise power spectral density of our current circuit board is compared with that of the STS-2 seismometer and of two existing data acquisition devices. In this figure, NLNM and NHNM are earth noise models [22]. Curve (a) is the noise power spectral density of a typical 24-bit data acquisition device (EDAS-24GN), with a corresponding full-scale at 10 mm/s of ground velocity. Curve (b) is the noise power spectral density of the 26-bit acquisition channels of the data acquisition device Q330HR, and is plotted using the ISIS evaluation results (www.iris.edu). Curve (c) is the noise power spectral density of the vertical component of the STS-2 seismometer, and is plotted using the USGS test results [3]. Curve (d) is the noise power spectral density of the current analog/digital conversion circuit board, whose corresponding full-scale is at a 10 mm/s ground velocity. As shown in this figure, the noise power spectral density of the designed circuit board is lower than those of both the STS-2 seismometer and the Q330HR, and is much lower than that of EDAS-24GN, a typical 24-bit data acquisition device developed by our team years ago.

Please note that the results in Figure 16 are obtained for a seismometer sensitivity of 1500 V/(m/s) and a corresponding full scale of 10 mm/s, when the gain of the EDAS-24GN preamplifier is set to 1. Usually, the data acquisition device's preamplifier gain has several choices. As shown in Figure 16, the EDAS-24GN makes more self-noise than NLNM at frequencies above 2 Hz. Because the earth's ambient background noise constitutes very important information, the preamplifier's gain is often set to 2 in practice. In this way, the lower measuring limit can be reduced; curve (a) can be moved down by about −6 dB, and the back ground noise can be recorded using a 24-bit data acquisition

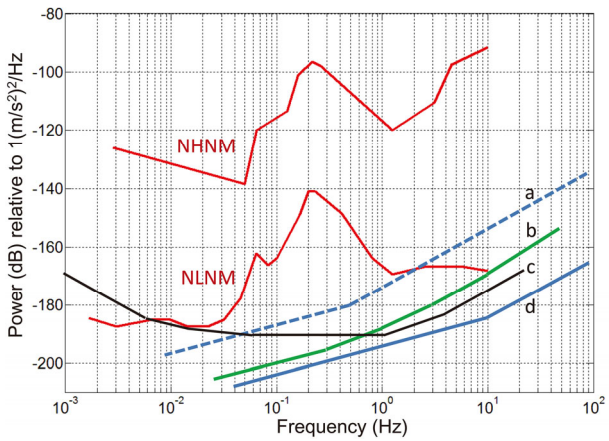

Figure 16 Noise of the developed circuit and those of a seismometer (STS-2) and two data acquisition devices.

device such as EDAS-24GN. However, the upper measurement limit is also reduced by about –6 dB, and the corresponding full scale becomes only 5 mm/s. This is why there were amplitude-limitation problems in so many broadband seismic observation instruments during the Wenchuan earthquake.

If the ADC circuit developed in the study is used, the quality of earthquake-relevant recordings will improve considerably. Because the self-noise of this circuit is well below that of NLNM, the earth's ambient background noise can be recorded, while keeping the upper limit at 10 mm/s.

The seismic data acquisition device is usually installed together with the seismometer, at the caves of seismic stations. Based on the construction specifications of seismograph stations from the China Earthquake Administration, the surroundings around the cave should be very quiet, and both vibration disturbances and electromagnetic interference should be very small. The daily temperature differences in the observation room should be less than 1°C, and the relative humidity should be maintained at 20%–85%. The data acquisition device, which contains the ADC circuit, should be sealed and waterproofed before it leaves the factory, so that humidity has almost no effect on it.

The designed ADC circuit is made using commercially available electronic components and integrated circuit chips. Like seismometers and other electronic products, its working state may be affected by temperature. However, these circuits usually work in the observation room of seismic stations, where the daily temperature difference is very small (below 1°C, as stated above), the influence of such a temperature change on its working performance would be very limited. As an example, let us assume that, while taking measurements at a long-period frequency band (above 100 s), the temperature changes 1°C. According to the datasheet, the offset voltage drift of the OPA140 operational amplifier is typically of ±0.35 μV/°C. The 1°C temperature change would therefore cause an offset voltage of ±0.35 μV. If converted into ground velocity, this 0.35 μV is equivalent to 2.33×10^{-10} m/s, considering a seismometer sensitivity of 1500 V/(m/s). At a long-period frequency band of above 100 s, a velocity of 2.33×10^{-10} m/s is much smaller than the noise of seismometers.

The above analysis shows that our designed ADC circuit performs well and has long-term stability. As a next step, we will research the possibility of using advanced RISC machine (ARM) embedded systems and very low noise preamplifiers, and try to develop a complete network-aware, high-resolution, large dynamic range seismic data acquisition device.

4 Conclusion

The discussed method, in which an adder, an integrator, a DAC chip, an ADC chip, and an FPGA were used to build a third-order 16-bit oversampling delta-sigma modulator, can be used to realize higher-resolution, larger dynamic range seismic data acquisition devices. The modulator presents low-pass filtering characteristics for the input signal, and high-pass filtering characteristics for the quantization noise. By performing digital decimation on the modulator's output, the quantization noise outside the baseband can be filtered out and the effective noise within the baseband can be considerably decreased. In this way, the data acquisition device can achieve both higher signal-to-noise ratios and larger dynamic ranges. The experimental results showed that: 1) The noise floor of the designed ADC circuit board is below –160 dB within the 0.1–10 Hz frequency band, and below –180 dB within the 10–40 Hz band. This noise floor is lower than that of two commercial 24-bit ADC chips, the ADS1281 and CS5371; 2) within the 0.1–40 Hz frequency band, the circuit board's dynamic range reaches 158.2 dB, with a resolution of 25.99 bits and a linearity error that remains below 2.5 ppm; 3) the noise power spectral density of the designed circuit is below that of the STS-2 seismometer. Using a data acquisition device based on the proposed method may alleviate or even solve the amplitude-limitation problem that broadband observation systems so commonly have to face during strong earthquakes.

The proposed method can not only be used in seismic observation, but also in other fields, such as high-resolution measurement. In seismic observation, a data acquisition device based on the proposed method will be adequate to cooperate with current seismometers, because the noise power spectral density of the designed circuit is lower than that of the STS-2 seismometer. To use the proposed method in the field of high-resolution measurement, it may be necessary to further suppress low frequency noise such as the 1/*f* noise, by techniques like digital correlated double sampling [23].

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