Optoelectronic Devices and Packaging for Information Photonics

By

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Abstract

This thesis studies optoelectronic devices and the integration of these components onto optoelectronic multi chip modules (OE-MCMs) using a combination of packaging techniques. For this project, (1×12) array photodetectors were developed using PIN diodes with a GaAs/AlGaAs strained layer structure. The devices had a pitch of 250μm, operated at a wavelength of 850nm. Optical characterisation experiments of two types of detector arrays (shoe and ring) were successfully performed. Overall, the shoe devices achieved more consistent results in comparison with ring diodes, i.e. lower dark current and series resistance values. A decision was made to choose the shoe design for implementation into the high speed systems demonstrator. The (1x12) VCSEL array devices were the optical sources used in my research. This was an identical array at 250μm pitch configuration used in order to match the photodetector array. These devices had a wavelength of 850nm. Optoelectronic testing of the VCSEL was successfully conducted, which provided good beam profile analysis and I-V-P measurements of the VCSEL array. This was then implemented into a simple demonstrator system, where eye diagrams examined the systems performance and characteristics of the full system and showed positive results.

An explanation was given of the following optoelectronic bonding techniques: Wire bonding and flip chip bonding with its associated technologies, i.e. Solder, gold stud bump and ACF. Also, technologies, such as ultrasonic flip chip bonding and gold micro-post technology were looked into and discussed. Experimental work implementing these methods on packaging the optoelectronic devices was successfully conducted and described in detail. Packaging of the optoelectronic devices onto the OE-MCM was successfully performed. Electrical tests were successfully carried out on the flip chip bonded VCSEL and Photodetector arrays. These results verified that the devices attached on the MCM achieved good electrical performance and reliable bonding. Finally, preliminary testing was conducted on the fully assembled OE-MCMs. The aim was to initially power up the mixed signal chip (VCSEL driver), and then observe the VCSEL output.

Dedication

To my parents, wife and son

Declaration Statement

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Table of Contents

Glossary

ACF	Anisotropic Conductive Film
AMOS	Analysis and Modelling of Optoelectronic Systems
ASIC	Application Specific Integrated Circuit
BGA	Ball Grid Array
CCD	Charged Coupled Device
CMOS	Complimentary Metal-Oxide Semiconductor
COTS	Commercial-Off-The-Shelf
CPU	Central Processing Unit
CSP	Chip Scale Packaging
CTE	Coefficient of Thermal Expansion
DBR	Distributed Bragg Reflector
DOE	Diffractive Optical Element
DSP	Digital Signal Processor
EFO	Electronic Flame-Off
EMS	Electronic Manufacturing Services
FPGA	Field Programmable Gate Array
GBP	Gain Bandwidth Product (GBP)
HOLMS	High-Speed Opto-eLectronic Memory System
IOB	Input/Output Block
LIV	Optical Power (L) Current (I) Voltage (V)
LVDS	Low Voltage Differential Signalling
MBE	Molecular Beam Epitaxy
MCM	Multi Chip Module
MCM-D	Multi Chip Module – Deposited
MEM	Memory

MOCVD	Metal-Organic Chemical Vapour Deposition
MPW	Multi Project Wafer
MSC	Mixed Signal Chip
MSM	Metal Semiconductor Metal
NEFO	Negative Electronic Flame-Off
NEP	Noise Equivalent Power
OCC	Optoelectronic Chip Carrier
OE-MCM	Opto-Electronic - Multi Chip Module
PCVD	Plasma-enhanced Chemical Vapour Deposition
PGA	Pin Grid Array
PIFSO	Planar Integrated Free Space Optics
PIN	Detector with an active intrinsic region sandwiched into a PN junction
PLC	Planar Lightwave Circuit
PTFE	PolyTetraFluoroEthylene
RIE	Reactive Ion Etching
SCIOS	Scottish Collaborative Initiative in Optical Sciences
SEM	Scanning Electron Microscope
SIA	Semiconductor Industry Association
SiOB	Silicon Optical Bench
SOI	Silicon On Insulator
SPA	Smart Pixel Array
SPOEC	Smart Pixels for Opto-Electronic Connections (SPOEC)
STAR	System for Transparent Avionics Routing
TIA	Trans-Impedance Amplifier
UBM	Under Bump Metallurgy
VCSEL	Vertical Cavity Surface Emitting Laser

List of Publications

The work in this thesis has been published in the following conference papers and is listed in chronological order.

[1] **S. Kumpatla**, J. J. Casswell and J. F. Snowdon, "Solutions to Optoelectronic Interconnect Problems," *Proceedings. PREP 2005 Conference.*, Lancaster University, UK, pp. 106-107, 2005.

[2] **S. Kumpatla**, J. J. Casswell and J. F. Snowdon, "Solutions to Optoelectronic Interconnect Problems," *Proceedings. IoP Physics 2005 Conference.*, University of Warwick, UK, April 10-14, 2005.

[3] **S. Kumpatla**, J. J. Casswell and J. F. Snowdon, "Solutions to Optoelectronic Interconnect Problems," *Proceedings. Information Photonics 2005 Topical Meeting.*, Charlotte, NC, USA, June 6-9, 2005.

[4] J. J. Casswell, **S. Kumpatla** and J. F. Snowdon, "Board Integrated Micro-Optics for divergence management in Opto-Electronic Interconnect Systems," *Proceedings. Information Photonics 2005 Topical Meeting.*, Charlotte, NC, USA, June 6-9, 2005.

[5] **S. Kumpatla**, J. J. Casswell and J. F. Snowdon, "Solutions to Optoelectronic Packaging Problems," *Proceedings. CLEO/Europe EQEC 2005 Conference.*, Munich, Germany, June 12-17, 2005.

Chapter 1

Background and Thesis Overview

1.1 Background

With increased development of computer technology, the information processing power grows with each generation. Enhancement in design and fabrication of individual computer chips facilitate devices to operate faster, to consume less electrical power and to execute more complex functions. Essentially, this is accomplished by shrinking the size scale of the transistors and applying a lower voltage swing to assign the digital bits. Although this plan of reducing the transistor size is projected to continue to improve the performance of the chips, the Semiconductor Industry Association (SIA) has predicted that the operation of the overall system in the future will be limited by the metallic wires that connect the chips to each other [1.1]. Albeit, processors and memory may get faster and more efficient, but the ability of these chips to communicate with each other will be made worse by the deficiencies of the electrical interconnections.

Studies have been carried out by several researchers on the fundamental limits of electrical interconnects and have proposed various solutions [1.2]-[1.16]. Possibly, advanced electronic architectures will be sufficient to tackle these problems for the future [1.13], [1.14]. In parallel to these all-electrical approaches, numerous research efforts have been concentrating on substituting wires with optical links. For basic physical reasons, optical interconnects offer many advantages over electrical interconnects for high speed links [1.15]. Conversely, practical concerns, such as design complexity, manufacturability, cost and reliability, must also be taken into consideration whether optical interconnects will break in the marketplace [1.16].

1.2 Optics for Communication

Light is electro-magnetic (EM) radiation with wavelengths in the ultra-violet to infra-red range. It's capability to travel at a high speed and long distances with minimal interaction with its surroundings has long been known and utilized.

With the invention of the laser, optical communications came of age. The laser is an application of Einstein's theory in which a photon could stimulate an excited atom to emit another identical photon. Such a device was proposed by Schawlow and Townes [1.17] in 1958, but it was four years before semiconductor based devices were demonstrated by four different research groups roughly simultaneously [1.18]-[1.21].

Modern day versions of these devices have advanced enormously since their early development. This is due to new and more efficient fabrication technologies and also to radical ideas. Long haul fibre optic communications systems have become ubiquitous with almost every call passing through fibre-optic cabling at some point on its route. Optical technologies have begun to invade on areas that were once firmly considered to be the area of electronics.

The advantages of optics are available over increasingly smaller distances and with them the increased bandwidth they offer. Yet, the main recipients of the bandwidth that optical communications can provide, i.e. information systems, computers, home-entertainment, are required to convert this information back into the electrical domain in order to transmit around their internal networks and buses. Therefore, as data rates increase, new bottlenecks occur.

In the microelectronics industry, the mainstream silicon VLSI (Very large scale integration) process used to fabricate the widespread integrated circuit (IC) is a very mature, well developed and high yield process. This is as a result of major investment and research over a number of decades.

In the main, connections between chips, between boards (of chips), and between systems are done electrically. With more and more processing power being compressed into even smaller dimensions, it is the bottleneck of getting data between chips, boards and systems through electrical connections, which is foreseen as the barrier to benefiting from the predicted improvements in VLSI devices. Electrical interconnections do not scale well with diminishing feature sizes. Reduced wire cross-sections and larger die sizes result in increased resistances and consequently larger RC delays. Faster clock rates, increased current-densities and smaller wirer pitches also aggravate crosstalk problems.

The use of "optical interconnects" is seen as an extremely promising option which could provide a viable, cost effective solution to this problem. A large body of research has been carried out over the past 15 years, and is ongoing, into the feasibility of using free-space and guided wave optics for transmitting data over much shorter distances than those in fibre optic telecommunications systems. As a consequence of the advances in technology, the demand for higher data rates increases, and the distance over which optics out-performs electrical transmission gets shorter.

Additionally, there is the fact that demand for bandwidth is predicted to exponentially increase [1.22], and that electronic and memory transistor densities continue to scale according to Moore's Law [1.23], while interconnect technologies do not. At higher speeds, the old limitations of electrical communications previously encountered over long ranges are being experienced at shorter distances. Taking into consideration all these issues, it can be seen that there is clear need for research into ways to counter these electrical bottlenecks and provide an efficient way with which to connect the subsequent systems to the high bandwidth capabilities of long distance optical communications.

1.3 Moore's Law

In 1965, Intel [1.24] co-founder Gordon Moore forecasted the rapid pace of technology innovation. His prediction is known as "Moore's Law" [1.23]. This states that the number of transistors on an integrated circuit roughly doubles every two years. This continued reduction in feature sizes on chips translates to faster devices with increased functionality, at a lower cost per device.

Figure 1 [1.23] shows Moore's estimate of the cost of integrated circuits divided by the number of components in an integrated structure at various times. Further details of Moore's Law can be found in the following references [1.25]–[1.27].

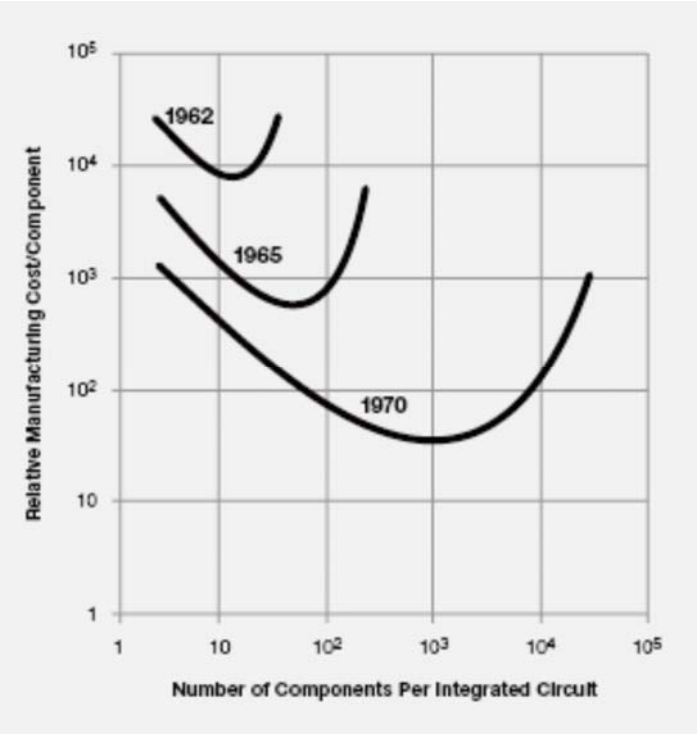

Figure 1) Shows relative manufacturing cost per component versus components in the circuit estimated for various times

1.4 Research Motivation

The motivation for this research comes from limitations of providing, electronically [1.15], [1.16], an interconnection network able to provide the bandwidth required to match the increasing processor performance of commodity processors. Optics is already widespread in the telecommunications industry in high bandwidth applications, but computing applications has different regimes in terms of acceptable latencies than telecommunications.

The following will describe some of the areas where electronic interconnects have known problems, how optics can solve them and why this is a problem for computer systems.

1.4.1 Electronic Limits

Although Moore's Law has held true for the past forty three years, there are fundamental limits to conventional microprocessor scaling, i.e. the quantum limit being the most profound. It is very likely that a technological limit will be reached prior to this, such as the issue of power dissipation or gate insulator breakdown.

Bandwidth:

Preceding the fundamental Shannon limit, Miller and Özaktas show in [1.28] that there is a constraint, to the amount of information that can be transmitted through a simple wire interconnect. This derived from the Physics of electrical signals travelling along wires. The result is independent of the interconnect design and is dependent on the ratio of the length squared to the total cross-sectional area, i.e. the 'aspect ratio' [1.15]. For electronic interconnects there exists the 'aspect ratio' limit [1.15] to bandwidth. This limit, occurring from skin effects is proportional to $f^{1/2}$ above a certain critical frequency. The total capacity of any electronic connection, B_{MAX}, is related to the overall cross-section, A, and the length, L:

$$B_{MAX} = B_0 \frac{A}{L^2} \qquad \textbf{(1.1)}$$

The constant B_0 is related to resistivity of the interconnect and is only weakly dependent on the fabrication technique. For copper, it is about 10^{14} bit/s, for co-axial cable, 10^{15} bit/s, for multi-chip module (MCM) and cross-chip lines it is 10^{16} bit/s. This limit is scale invariant and for a fixed cross-section it is independent of whether interconnect is made of many slow wires or few fast wires until other effects such as dielectric absorption (which is independent of cross-section) dominate.

Due to the dielectric absorption, which increases in proportion to frequency, there is an upper limit on operating speed. For example, standard strip-line on FR4 (this is standard PCB material) is limited to 1m at 1GHz, whereas a good low-loss material such as Polytetrafluoroethylene (PTFE) would reach up to 10m.

There is no equivalent aspect ratio limit for optics. The dispersion of the signal over long distances leads to a fixed bandwidth-distance product for optical transmission lines (1GHz km for typical multimode fibre). For the distances dealt with in this thesis (generally <1m), this is not considered a limiting factor. At the scale in question, the limiting factor for bandwidth will be the speed of the transceiver electronics.

Power:

A key problem with electronic interconnects is the power dissipated in terminating resistors, especially in conventional complementary metal oxide semiconductor (CMOS) signalling. The application of low-voltage differential signalling (LVDS) technologies can be beneficial, but the drawback is that this results in increased circuit complexity and higher susceptibility to noise.

Even with LVDS, electronic interconnects have power dissipation generally an order of magnitude higher than an optical equivalent. This is generally due to the larger parasitic capacitance of electronic interconnects (order of 1pF compared to 100fF for small optoelectronics). For example, a commercially available 2.5Gbit/s bi-directional electronic transceiver core has a power dissipation of 200mW per channel. In contrast, 1Gbit/s optical transceivers have been demonstrated with lower than 10mW power consumption.

Pin Density:

The exponential growth in transistor densities, as predicted by Gordon Moore in 1965 has progressed to smaller and faster chips. This has lead to the input/output (I/O) pins connecting the chips to the outside world being a major problem. To avoid increasing the frequency of the I/O pins operation, more pins are required. At the same time, the chips are reducing in size and because of the planar nature of electronic design; the space available around the chip for connections is shrinking. The size of the I/O pins cannot be decreased much further because of the bandwidth limitation imposed by reducing the cross-sectional area and by the increasing difficulty in working with very fine, i.e. ~ microns, metal wire.

Optics could provide a solution to this problem. It is unproblematic to fabricate arrays of optoelectronic devices with their optical I/Os normal to the chip. Also, it is feasible to have the I/O connected across the whole area of the chip by placing electronic I/O pads across the chip's surface and using a bonding technology such as flip chip bonding to stack the optoelectronic chip on top [1.29]. This has the advantage of allowing the surface area and not the edges of the chip to be used for I/O. In this case, the solder links between the electronic chip and optoelectronic chip would be very short so the bandwidth can remain very high.

Other Factors:

Electronics also suffers from a number of other problems, when high speed interconnects are implemented. These include the cross-talk, caused mainly by the mutual inductance and capacitance of adjacent signal lines, and the finite impedance of a common signal return in a connector or package pin. In addition, interference from other devices can be an issue. Optical signals are immune to electro-magnetic interference from other devices. By providing sufficient spacing between channels, common signal returns and cross-talk from adjacent channels can be prevented.

It is also a major problem to construct electronic transmission lines with uniform characteristic impedance. Discontinuities in the transmission medium caused by package pins, connectors, vias and gaps in the signal return plane lead to unwanted reflections that lead to noise. At high frequencies, this becomes a major issue as even small discontinuities in the impedance can cause large reflections due to the broadband nature of the electronic signal. As optical signals are modulated onto a very high frequency carrier (~10^{14} Hz), they are considered to be narrowband, and the impedances of the transmission line can be matched to the load (i.e. the detector) and by quarter-wavelength sections of transmission medium. This is in the same manner as narrow-bandwidth microwave signals. This is generally achieved with quarter-wavelength dielectric anti-reflection coating.

1.5 Research Work Conducted on Optical Interconnects in Industry

1.5.1 Introduction

A number of companies, such as Intel [1.24], Terahertz Photonics Ltd [1.30] and Luxtera [1.31] have been studying optical interconnects. I will discuss the research conducted by these corporations in the following sections, starting with Intel.

1.5.2 Research by Intel

The Intel Technology Journal (Volume 8, Issue 2, May 2004) [1.32] investigated Intel's work on optical technologies and applications. Optical interconnects were discussed in two papers [1.33], [1.34]. This research was conducted by a team from Intel Components Research Lab. This was led by Intel Senior Fellow, Dr Ian Young.

Also, research on silicon photonics is examined in paper [1.35]. This work was led by Intel Fellow and director of the Photonics Technology Lab, Mario Paniccia. The following sections will discuss these studies.

Optical Interconnects:

The work from [1.33] examined two feasible options for high performance and cost-effective optical interconnect solutions. The first study looked into the silicon optical bench solution (SiOB). The optical design, processing and assembly challenges of this approach were discussed in detail. This method allowed passive alignment of optical components using lithographic definition of fine structures on the silicon substrate and as a result was expected to have a cost reduction. The second study discussed the system architecture and design of (1x12) optical transceiver. This was developed by Intel using a hybrid integration of components on a microprocessor-style package. By using this method, it would have a minimum effect on the existing motherboard technology and so lower costs.

The work from [1.34] examined the capability of on-chip applications of optical interconnects to alleviate the constraints of metal interconnects. Specifically, a comparison of the performance and cost of optical interconnects and copper interconnects for clock distribution and intra-chip global signalling was performed. Their analysis did not show any major benefits for on-die clock distribution using optical interconnects as compared to standard clock distribution. For signalling, it was found that optical interconnects, in combination with wavelength division multiplexing, can possibly offer a low latency-high bandwidth option.

Silicon Photonics:

At Intel, silicon photonics is defined as the use of silicon-based materials for the transmission (electrical-to-optical conversion), guidance, control and detection (optical-to-electrical conversion) of light to communicate information over distance.

The work from [1.35] examined the research on optoelectronic integration using silicon-based optical components, which included a tunable external cavity laser, a 2.5GHz optical modulator and a silicon-germanium waveguide-based photodetector.

Mario Paniccia's team concentrates on developing silicon-based photonic building blocks for future use in enterprise and data centre communications. They have built the first silicon modulator with bandwidth greater than 1GHz in 2004 [1.36]-[1.38].

They also developed the first continuous wave silicon laser in 2005 [1.39], [1.40] using the Raman Effect [1.41], [1.42]. This enabled silicon to amplify light and create continuous beams of laser light for the first time. Intel's existing CMOS manufacturing processes was used to create this. Applications such as optical amplifiers, lasers and wavelength converters could be used for this device.

Also, in collaboration with Professor John Bowers in the Optoelectronics Research Group at University of California, Santa Barbara [1.43], the first electrically pumped hybrid silicon laser was developed in 2006 [1.44], [1.45]. This device integrated the light-emitting potential of Indium Phosphide with the light-routing and low cost benefits of silicon. With this development, silicon photonic chips containing dozens or even hundreds of hybrid silicon lasers could in the future be created using standard high-volume, low-cost silicon manufacturing techniques.

1.5.3 Terahertz Photonics Ltd

Terahertz Photonics Ltd [1.30] was a start-up company based in Livingston. It specialised in the field of photonic integrated circuits, optical waveguide devices and thin-film optical coatings for telecommunications. It was founded in November 1998 by two academics, Dr Frank Tooley and Professor Gerald Buller, from the Department of Physics at Heriot-Watt University.

One of the key technologies of Terahertz was its use of polymers for planar lightwave circuits (PLC). This had advantages of rapid high-yield processing, high thermal stability, low loss and high reproducibility of thickness and refractive index. In

November 2002, due to difficulties in obtaining further funding, it closed its optical device division and sold its specialist coatings division to Helia Photonics [1.46]. Subsequently, in August 2003, Terahertz Photonics Ltd went into liquidation.

1.5.4 Luxtera

Luxtera [1.31] has developed a CMOS Photonics technology platform [1.47]. The technology integrates two lasers and photodetectors, which are mounted on a monolithic CMOS die. It also includes transimpedance amplifiers (TIAs), Mach-Zehnder modulators and receive Clock and Data Recovery (CDR) circuits.

The monolithic recipe of photonics and electronics in a production CMOS process allows a single CMOS Photonics chip to replace tens to hundreds of discrete optical and electronic components. This reduces size, power consumption and cost of the device. This complete single chip solution is fabricated using the 0.13μm silicon on insulator (SOI) CMOS process.

Implementation of 40Gbit/s interconnection between optical fibre to optoelectronic chip in communications is feasible with this device. Other applications this technology can be used in are optical sensors in infrared cameras, interactive gaming, and medical imaging.

1.6 Research Work Conducted on Optical Interconnects in Academia

1.6.1 Introduction

A number of academic organizations, which includes work in my group [Optically Interconnected Computing (OIC) Group] [1.48] at Heriot-Watt University (HWU), have developed optical interconnect systems in the lab [1.49]-[1.53]. The main differences among the various research projects, is they have a tendency to be in two fields: (1) the choice of optoelectronic devices, i.e. lasers or modulators; PIN or metal semiconductor metal (MSM) detectors and (2) the design of the optical system.

I will discuss in the following sections research conducted on optical interconnect systems by academic groups at HWU, Miller Group at Stanford University [1.54], Optoelectronics Research at University of California San Diego [1.55], [1.56], C-LAB [1.57], University of Hagen [1.58] and Vrije Universiteit Brussel (VUB) [1.59].

1.6.2 Optically Interconnected Computing at Heriot-Watt University (HWU)

The Department of Physics at HWU has been working in the fields of optical computing and optical interconnects for the last 27 years. This section will describe projects successfully completed by the Optically Interconnected Computing (OIC) Group. The achievements of the following projects in this order: SCIOS, SPOEC, AMOS, NOSC, STAR, and POCA, are discussed.

The Scottish Collaborative Initiative in Opto-electronic Sciences (SCIOS) project [1.60], [1.61] was a collaborative effort between the universities of Heriot-Watt, Edinburgh, Glasgow and St. Andrews. This project produced the 1K sorter demonstrator, which was an early example of a system demonstrator using smart-pixels. This was designed to sort 1024 data words using a bitonic sort algorithm. Free-space optics were used to route a 32×32 array of diffractively fan-out optical signals between two optoelectronic chips, i.e. from the modulators of one chip to the detectors of the second and then back via a similar process.

The Smart Pixels for Opto-Electronic Connections (SPOEC) project [1.62], [1.63] successfully developed a demonstrator. It was designed as a crossbar switch that would allow the routing of packet data from any of its inputs to any of its outputs. This used optoelectronic technology, which allowed inter-chip communication at the rate of 1 Tbit/s. In order to demonstrate this level of aggregate Input/Output bandwidth to a single silicon CMOS chip, the free-space paradigm was chosen as the main optical technology, as it was well suited to short range, high bandwidth and parallel interconnection purposes. The successful operation of the demonstrator showed that this approach used was feasible.

The Analysis and Modelling of Optoelectronic Systems project (AMOS) project [1.64], [1.65] investigated the use of optics and optoelectronic systems within computer architectures. The project, along with The Informatics Group at University of Leeds whom worked on the high-level algorithmic modelling of the system, continued work previously done in the Department of Physics, Heriot-Watt University, i.e. SCIOS and SPOEC projects.

The aim of the AMOS project was on modelling the close integration of electronic processors, to perform the computation, with free-space optics to provide short range

(~centimetres) communication between the processors. The research conducted concentrated on the optoelectronic interfaces that were required to connect the processors with the optics. Initial studies were performed using computer simulations with later proof-of-concept demonstrators assembled and tested.

The conclusion of the AMOS project was that a completely connected approach provides higher bandwidth per link. This result comes from the high dependence that the performance of the local hop approach has on the electronic, which includes the photocurrent receivers, and optoelectronic components primarily due to power dissipation and yield issues.

In the NOSC (Neural Optoelectronic Switch Controller) project [1.66]-[1.68], HWU developed a demonstrator using optics to perform very high connectivity and off-the-shelf electronics to provide neuron functionality. In the system, arrays of detectors and VCSELs act as neuron inputs and outputs with complex neural interconnection patterns woven through free-space using a single diffractive optical element (DOE). The system constructed consisted of 64 neurons in an 8×8 array. A DSP solution was adopted to provide flexibility. The construction of the optoelectronic neural network demonstrator showed the potential of optical interconnection. This allowed architectures to be developed, which were previously prevented by electronics.

The System for Transparent Avionic Routing (STAR) project [1.69], [1.70] was collaborated between Heriot-Watt University, Imperial College London, BAE Systems and DERA Malvern. The HWU group was responsible for investigating suitable optoelectronic components as well as the packaging and assembly of the switch.

The STAR project investigated the characterisation and integration of suitable devices to form a high-speed optoelectronic crosspoint interconnect demonstrator. The system was based on a novel technique in which an 850nm VCSEL array, GaAs metal-semiconductor-metal (MSM) photodetector array and SiGe crosspoint chip were integrated onto an optoelectronic chip carrier (OCC) substrate using compliant polymer bump flip chip bonding. This used multimode polymer waveguides with total internal reflection, or metallised, 45 degree mirror ends. The waveguides, mirrors and bond bumps were successfully fabricated on glass substrates by direct writing of a custom

polymer material, using a continuous wave (CW) He-Cd laser. 50×50μm multimode waveguide cores were written together with arrays of polymer bumps with diameters and heights of 50 and 100μm respectively.

The Programmable Optoelectronic Computing Architecture (POCA) project [1.71], [1.72] investigated the integration of an optoelectronic communications system with reconfigurable field programmable gate array (FPGA) devices. This was for use in reconfigurable parallel computing architectures based on the analytical results from the previously funded AMOS project, the knowledge of the optoelectronic integration gained through the European Commission funded SPOEC and HOLMS [1.73] projects and digital device characteristics from commercially available FPGAs. The achievements from this project, showed that optoelectronic integration of FPGAs and high bandwidth optical interconnects were feasible.

1.6.3 The Miller Group, Stanford Photonics Research Center, Stanford University

The Miller Group [1.54] led by Professor David Miller have conducted extensive research on optical interconnects, optoelectronic devices and ultrafast all-optical switches. Also, Professor Miller [1.74] and the Miller Group [1.75] have written numerous journal publications and conference proceedings in the field of optoelectronics and photonics.

1.6.4 Optoelectronics Research at University of California San Diego

The OptoElectronic Computing Group (OECG) [1.55] led by Professor Sadik Esener at the University of California San Diego conducts research on parallel optoelectronic computer systems through the optimal utilization of micro-electronic and photonic technologies. The OECG is an integral part of the Optoelectronics Technology Center (OTC) [1.56] at University of California San Diego. This is a centre is funded by DARPA [1.76]. The OTC is led by Professor Larry Coldren and was established to facilitate fundamental advances in photonics and optoelectronics. Specific projects have included work on advanced VCSELs [1.77]-[1.79] and photodetector arrays [1.80] as well as their combination with integrated circuits using new heterogeneous integration technologies [1.81]. This technology should provide new device and material capabilities for the next generation of computer interconnects, communications and optical biosensors.

1.6.5 Optical Interconnection Technology Group (OIT) - C-Lab

The Cooperative Computing & Communication Laboratory (C-LAB) is a joint research and development laboratory managed by Siemens AG [1.82] and the University of Paderborn [1.83] in Germany. It was founded in 1985.

Since 1998, the Optical Interconnection Technology (OIT) Group at C-LAB has conducted extensive research in the field of optical interconnection technology for printed circuit boards. In the project "EOCB" (Electrical-Optical Circuit Board) [1.57], [1.84] basic investigations of optical interconnection technology were performed. The research examined the feasibility of electrical-optical printed circuit boards and assessed their application in areas such as computer technology.

Other projects studied at C-LAB included OptoSys (Optical Interconnections Systems), OptiCon and HOLMS (High Speed Optoelectronic Memory System) [1.57]. The HOLMS project will be discussed in further detail later in this chapter.

1.6.6 Optical Information Technology (ONT) Group - University of Hagen

The Optical Information Technology (ONT) Group led by Professor Jurgen Jahns at the University of Hagen specialises in the area of planar-integrated free-space optics (PIFSO) [1.85]-[1.92].

A system developed using PIFSO technology is composed of diffractive optical elements (DOEs), which are etched into the surface of a glass substrate. The diffractive optical systems are capable of carrying out complex routing functions. Also, optoelectronic devices, for example, vertical cavity surface emitting lasers (VCSELs) and Photodetectors (PDs) are bonded onto the substrate by using hybrid integration techniques such as flip-chip bonding. Light propagation takes place inside the substrate along a crisscross path. The substrate, which is usually several millimetres thick, functions both as a medium for light propagation as well as a board onto which other devices can be mounted.

1.6.7 Optical Interconnects Group - Vrije Universiteit Brussel (VUB)

The Optical Interconnects Group led by Professor Hugo Thienpont at Vrije Universiteit Brussel have investigated using parallel optical fibre connections at the inter-board level where their focus was on the fabrication of 2D fibre array configurations [1.93]-[1.96]. Also, work has been done looking into the integration of optical waveguides into Printed Circuit Boards (PCB). This specifically studied the efficiency of coupling and redistribution of light from optoelectronic devices to layers of optical waveguides [1.97]-[1.100]. Other research has worked on the fabrication of very short-distance free-space micro-optical interconnection modules for intra-chip and intra- multi-chip module (MCM) interconnects. This focussed on the packaging, the scalability and the potential to reconfigure the interconnect topology [1.5], [1.101], [1.102].

1.6.8 Summary

Numerous groups, from industry and academia have been investigating optical interconnects as an alternative for electrical interconnects in the near future. There are many challenges remaining for these systems to achieve the marketplace.

The work conducted so far has highlighted the advantages and disadvantages of different designs from optical system level, to optoelectronic devices and CMOS circuits.

1.7 High Speed Optoelectronic Memory Systems (HOLMS) Project

1.7.1 Introduction

The high speed optoelectronic memory system (HOLMS) project [1.73], [1.103] investigated the potential of optical interconnects to reduce memory latency within multiprocessor computer systems. This was conducted using optoelectronics and associated packaging technologies, which will be discussed in the following sections.

This project was funded by the European Commission Framework 5 IST (Information Society Technologies) programme [1.104]. Table 1 provides details of the project participants in the HOLMS consortium.

Name	Abbreviated Name	Country	Main Role(s)
Heriot-Watt University	HWU	United-Kingdom	Project Coordination, Optoelectronics, Bonding
Swiss Federal Institute of Technology, Zurich	ETHZ	Switzerland	Technical Coordination, Architecture, Memory Protocol, Multi Chip Module (MCM) Layout
University of Hagen	Hagen	Germany	Planar Integrated Free Space Optics (PIFSO)
Siemens Business Services GmbH & Co, OHG	SIEMENS	Germany	Project Coordination, Waveguides
Universitaet Gesamthochschule Paderborn	Uni PB	Germany	Waveguides
ILFA GmbH	ILFA	Germany	PCB design and manufacture
École supérieure d'électricité	Supélec	France	Mixed Signal Chip (MSC)
THALES Communications	TCFR	France	Application, Software

Table 1) HOLMS Project Participants

The theory work was achieved under Engineering and Physical Sciences Research Council (EPSRC) funding through the Analysis and Modelling of Optical Systems (AMOS) [1.64], [1.65] and Scottish Collaborative Initiative in Optical Sciences (SCIOS) projects [1.60]. And, through EC funding with the SPOEC project [1.63]. Within the HOLMS project, this knowledge was consolidated at a time when the technology was developed to a level where commercial use could be predicted.

1.7.2 Overview of Project

The project's aim was to construct a four central processing unit (CPU) shared memory multiprocessor with a low latency, optoelectronic memory interconnection [1.105]. The interconnection was based on a combination of waveguide, fibre and free-space optics, which augmented the electronic memory and processor components. This was integrated with conventional electronic assembly through a novel optoelectronic MCM (OE-MCM) packaging technology. The project started in March 2002 and was successfully completed in December 2005 [1.106].

The three main technologies developed in this project were:

1. The Planar Integrated Free Space Optics (PIFSO) [1.107]-[1.115]. This work was developed by the Optical Information Technology (ONT) Group [1.58] at University of Hagen. An overview of this system was described earlier in this chapter.

2. Optical waveguides integrated in conventional PCBs [1.116]-[1.121]. This work was developed by the Optical Interconnection Technology (OIT) Group [1.57] at C-Lab.

3. Multi-Chip Modules (MCM) [1.122]-[1.127].This was developed by the Computer Architecture Group (CAG) [1.128] at the Swiss Federal Institute of Technology in Zurich (ETHZ).

Figure 2 shows the coupling between the PIFSO, OE-MCM and PCB (optical and electrical layers).

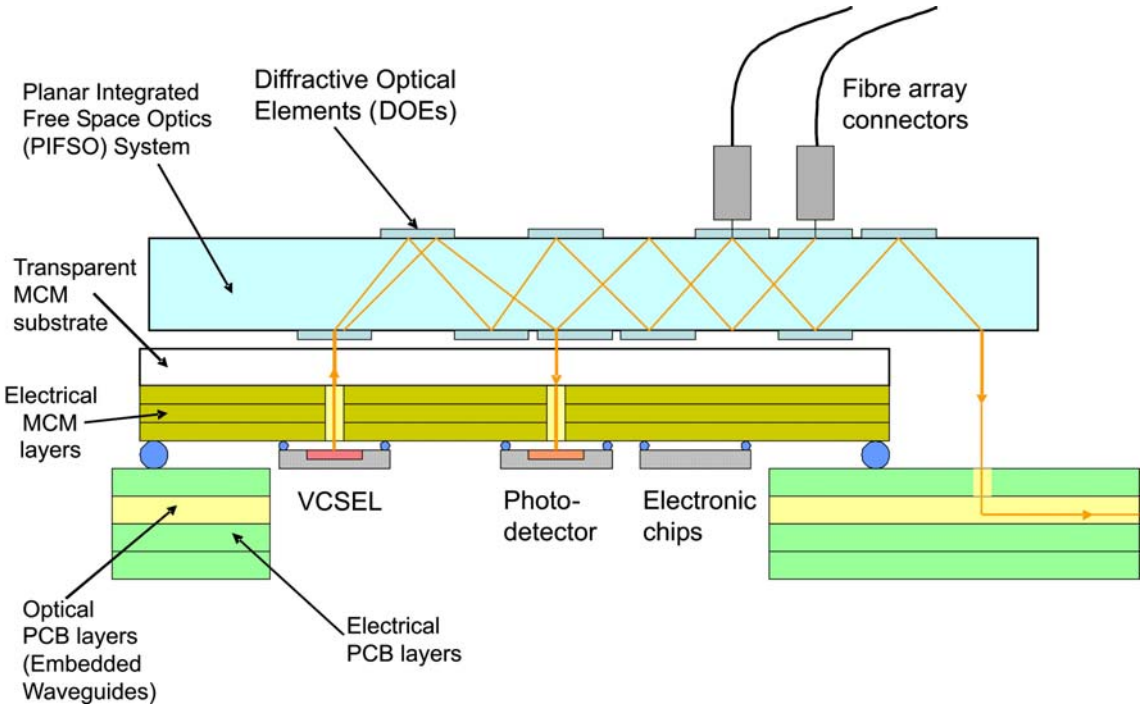

Figure 2) Schematic showing coupling between PIFSO, OE-MCM and PCB

In the HOLMS project, the role of the OIC Group at HWU [1.129]-[1.132] was firstly to design, identify and source suitable optoelectronic devices. And secondly, to integrate these optoelectronic components onto the MCMs using appropriate packaging techniques.

1.8 Thesis Overview

My PhD research involved working on the HOLMS project from October 2003 to its successful completion in December 2005. This thesis studies optoelectronic devices and the integration of these components onto OE-MCMs using a combination of bonding techniques. The thesis layout is described as follows:

1.9 Chapter 2: Receiver Devices – Photodetector (PD) Arrays

This chapter explains details of the background, specifications and design of the receiver devices which were used. Also, characterisation experiments of two types of detectors (Type A and Type B devices) are described.

1.10 Chapter 3: Transmitter Devices and Mixed Signal Chips (MSCs)

This chapter describes details of the background, specifications, and design of the transmitter devices which were used. Characterisation experiments performed on these devices are explained. Also, details of the mixed signal chips (MSCs) used to drive the transmitter devices and amplify the receiver devices are given.

1.11 Chapter 4: Optoelectronic Packaging (I)

This chapter discusses the background of flip chip bonding technologies. Using these techniques, an explanation of the experiments conducted in packaging the components described in chapter 2 and chapter 3 is given.

1.12 Chapter 5: Optoelectronic Packaging (II)

This chapter describes the fully integrated optoelectronic multi-chip module (OE-MCM) developed for my research work. Experimental work conducted on packaging and testing the OE-MCMs is explained.

1.13 Chapter 6: Conclusions

Finally, chapter 6 draws conclusions from the work presented in chapters 2, 3, 4 and 5 and suggests possible future work in the area.

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Chapter 2

Receiver Devices – Photodetector (PD) Arrays

2.1 Introduction

The outline of this chapter is as follows. In section 2.2, background on photodiodes is given. In sections 2.3, 2.4, and 2.5, the photodetector array devices used in my experimental work are described. Finally, in sections 2.6 and 2.7, DC characterisation experiments of Type A and Type B detector arrays are discussed.

2.2 Background on Photodiodes

Photodiodes [2.1]-[2.4] are used in detectors for measuring optical signals and are subject to performance limitations. These limitations are spectral response of the photodiode material, noise generation and photodiode reaction speed, which inevitably limits the detectable signal bandwidth. In general, Photodiodes are the dominant optical detector technology. They can be easily fabricated in large arrays using existing technology and offer fast response times.

2.2.1 PIN Photodiode

This type of diode consists of a p-doped region, intrinsic (depletion) region and n-doped region as shown in Figure 3.

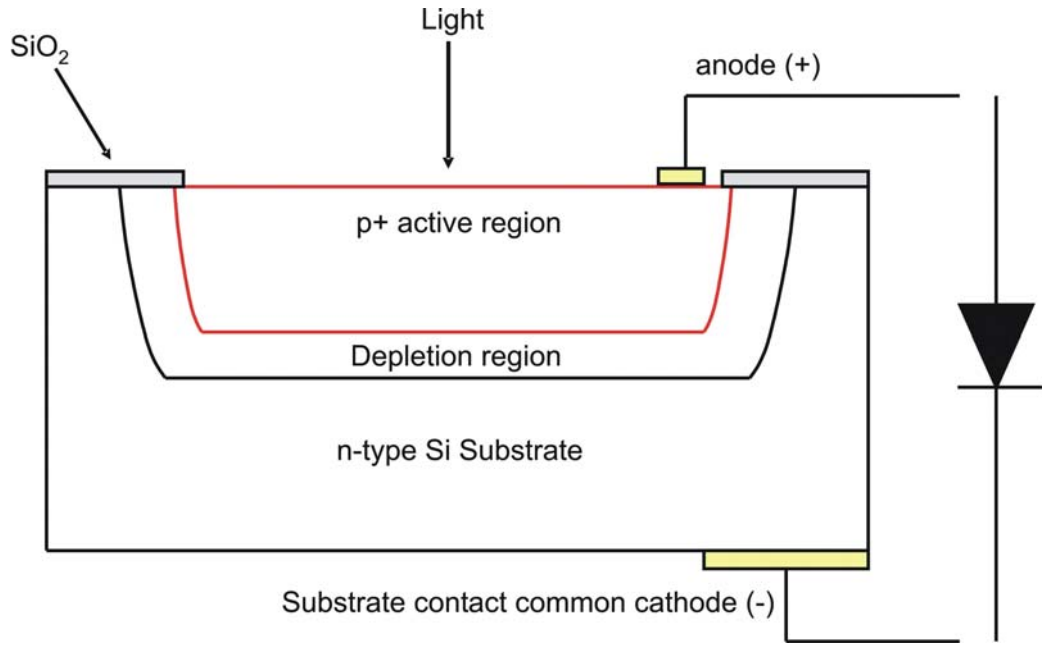

Figure 3) Structure of a PIN photodiode

The PIN photodiode needs only a small bias level to cause the depletion region to extend all the way to the n-region. This provides a large sensitive volume resulting in a good long wavelength response. In an ideal photodiode the generated photocurrent is proportional to the incident power, but in a real photodiode there is a shunt resistance and shunt capacitance. This leads to bandwidth limitations. Also, there is strong wavelength dependency.

Real Photodiodes:

Unfortunately the photodiode in real life can never operate as a perfect component, i.e. conducting perfectly in one direction and blocking all current in the opposite direction. Figure 4 shows an equivalent circuit for a real photodiode.

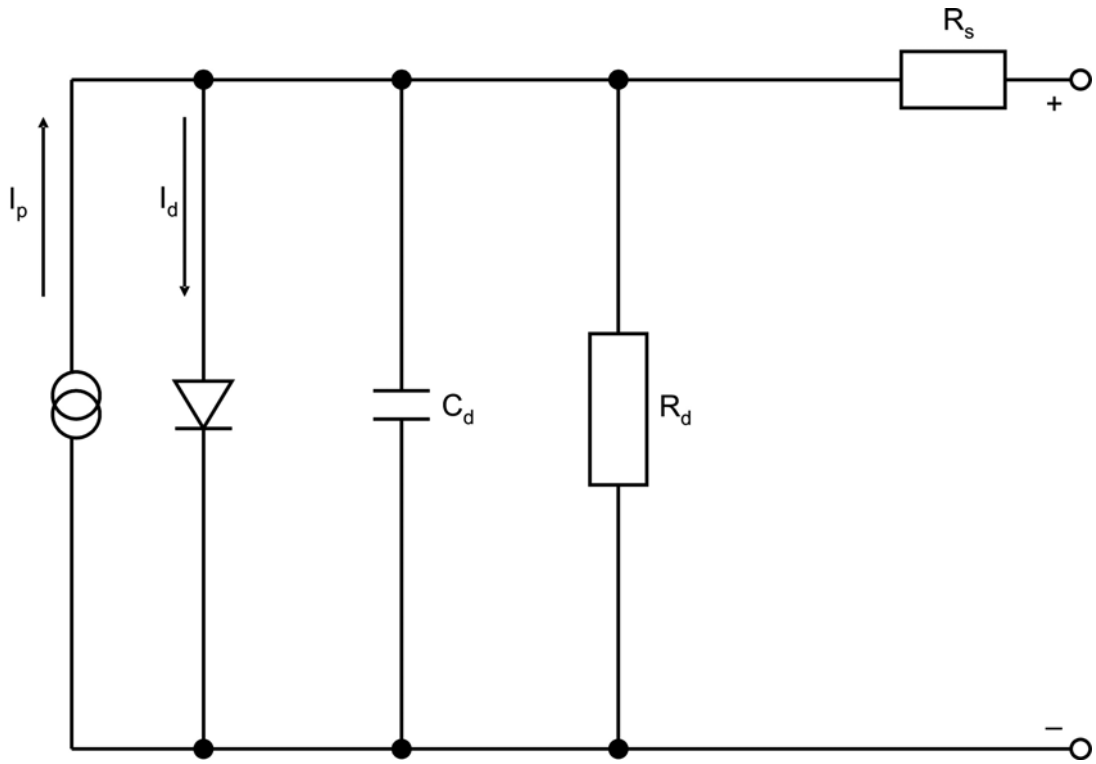

Figure 4) Real photodiode model circuit:
Where, I_p = Current generated by the Incident light, I_d = Dark current generated by photodiode, C_d = Shunt capacitance, R_d = Shunt resistance, R_s = Device's series resistance.

2.2.2 Detector Configurations

A photodiode can be said to be a current source. Its measurements are based upon voltage rather than current measurements. There are two types of current to voltage converters commonly used. They are the passive load detector and transimpedance amplifiers (TIAs).

Passive Load Detector:

The passive load detector relies on passing the photodiode current through a resistor to generate a signal voltage. The unbiased and biased passive load configurations are shown in Figure 5 respectively. Also, comparisons between unbiased and biased passive load detectors are shown in Table 2.

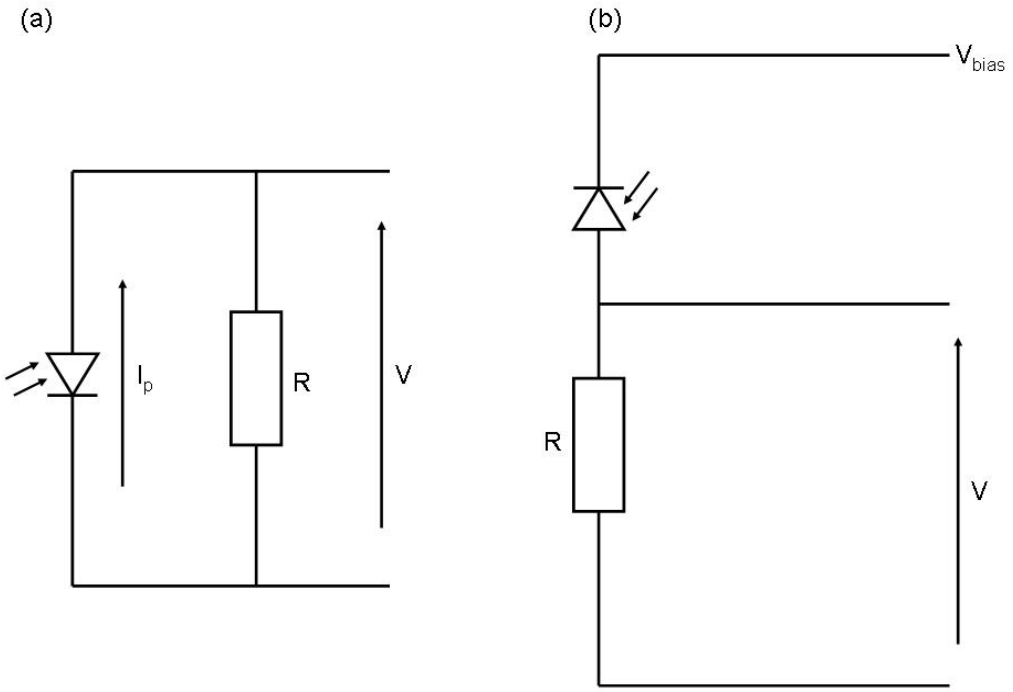

Figure 5) Passive load (a) without bias, (b) with bias

Without bias	With bias
Very temperature dependent	Reduced detector capacitance
Poor linearity	Improved linearity
Easily saturates	Less saturation
	Increased dark current

Table 2) Comparisons between unbiased and biased passive load detectors

Transimpedance Amplifier:

The transimpedance configuration relies on feedback around an operational amplifier. The equivalent circuit is shown in Figure 6. In the unbiased version V_{bias} is zero.

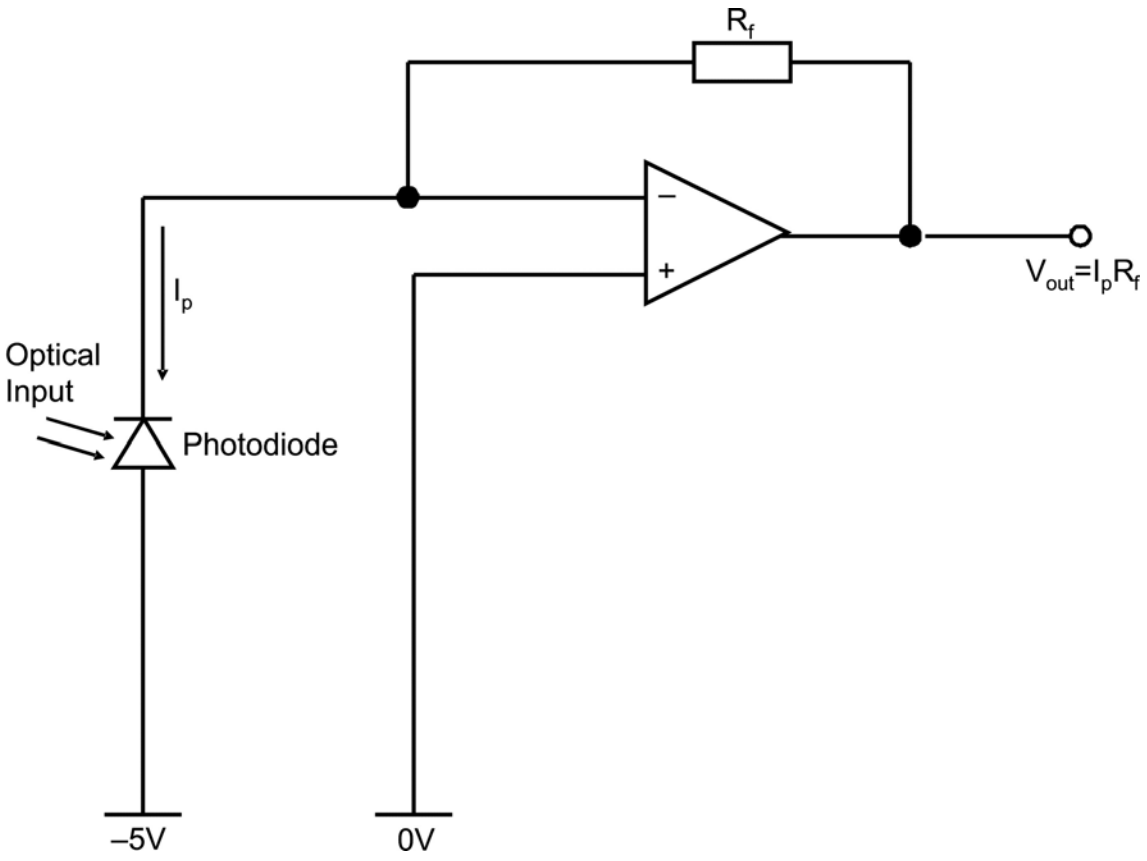

Figure 6) Transimpedance equivalent circuit

2.2.3 Noise in Photodetectors

All photodetectors generate some kind of noise, which limits their sensitivity. Noise can be generated in a number of ways as explained below.

Shot Noise:

This is caused from the fluctuations in electronic charge as current flows through a circuit. It is also known as white noise. The r.m.s current I_s is:

$$I_s = \sqrt{2q\Delta f\left(I_P + I_{dk}\right)} \qquad \textbf{(2.1)}$$

Where, q = electronic charge = 1.60×10^{-19}C, Δf = Bandwidth over which the noise is measured, I_P = Photogenerated current and I_{dk} = Dark current.

Shot noise is the most influencing source when operating in photoconductive (biased) mode.

Dark Current:

An important property for a photodetector, which determines its performance, is dark current (I_{dk}). This is the photocurrent, which we get in the absence of an optical signal. In PIN photodiodes, the dark current can be negligibly small, i.e. pA or nA. This raises the Signal to Noise Ratio (SNR) at the input, which is important, since incoming optical signals are routinely of the order of 1-10 μW.

Johnson Noise:

This is caused by thermal agitation of charge carriers within a conductor, which produces a bandwidth dependent voltage fluctuation. The resulting in r.m.s current I_j is:

$$I_j = \sqrt{\frac{4kT\Delta f}{R_d}} \tag{2.2}$$

Where, k = Boltzmann Constant = 1.38×10^{-23} JK^{-1}, T = Absolute Temperature in Kelvin, R_d = Photodiode shunt resistance, and Δf = Bandwidth over which the noise is measured.

The total r.m.s noise I_n is:

$$I_n = \sqrt{I_S^2 + I_J^2} \tag{2.3}$$

2.2.4 Responsivity

Responsivity is a measure of the sensitivity to light and it is defined to be the amount of photocurrent that is generated per unit amount of incident light power at a given wavelength. See Equation 2.4.

$$R = \frac{I_P}{P_{in}} \tag{2.4}$$

Where, I_P = Photocurrent and P_{in} = Incident light power.

Quantum Efficiency (QE) is defined as the percentage of the incident photons that contribute to photocurrent. It is related to responsivity by:

$$QE = \frac{R_{Observed}}{R_{Ideal}(100\%)} = R\frac{hc}{q} \tag{2.5}$$

Where, $h = 6.63\times10^{-34}$ Js^{-1} (Planck constant), $c = 3.0\times10^{8}$ ms^{-1} (Speed of light), $q = 1.6\times10^{-19}$ C (Charge of electron), R is the responsivity (AW^{-1}).

For detection of the incident light, the photon must have energy greater than the band gap energy (E_g) of the semiconductor. Photons are absorbed as they penetrate the semiconductor with a characteristic absorption length ($1/\alpha$) for the material that depends on the wavelength. A plot of the optical absorption coefficient (α) versus wavelength (λ) is shown in Figure 7.

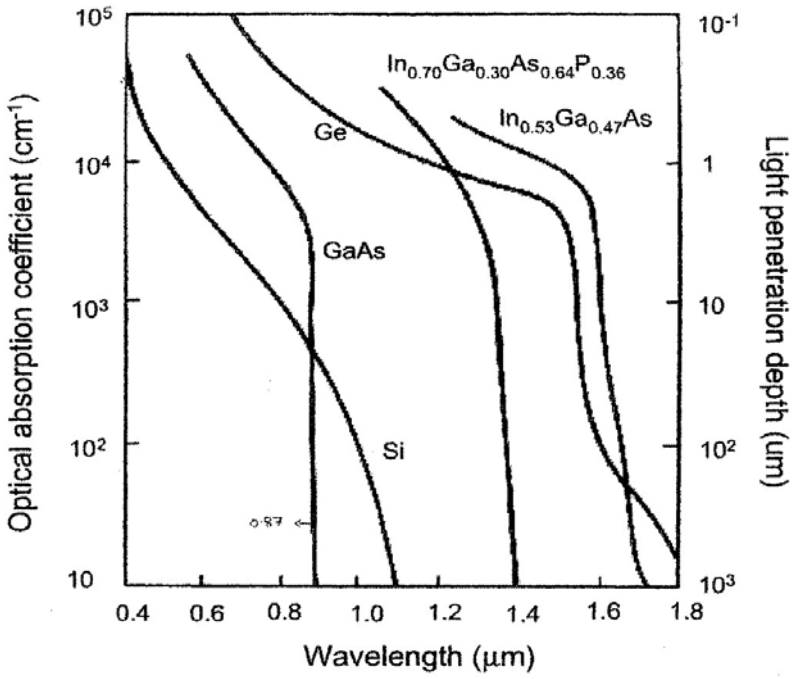

Figure 7) Optical absorption curves for some common semiconductor photodiode materials

Also, the responsivity of photodetectors is dependent on its design and material properties.

2.2.5 Reverse Bias

When biased, the photodiodes must operate in the reverse bias mode, i.e. negative voltage applied to anode and positive voltage to cathode. The application of a reverse bias can greatly enhance the speed of response and linearity of photodetectors. This is due to the width of the depletion region increasing and subsequently this decreases junction capacitance. However, dark and noise currents are greater when applying a reverse bias. Also, there is a greater risk of damaging the device by excessive applied reverse voltage.

2.2.6 Series Resistance (SR)

Series resistance of a photodiode is the resistance of the contacts and the undepleted bulk of the substrate. It is controlled by the thickness, shape and doping of the contact layers. For photodiodes which are fully depleted, the series resistance is just the resistance of the contacts. Series resistance is used to determine the linearity of the photodiode in photovoltaic mode (biased mode). Although an ideal photodiode should have no series resistance, typical values range from 10 to 1000 Ohms.

$$R_S = \left(\frac{W_S - W_d}{A_j} \rho \right) + R_C \qquad \textbf{(2.6)}$$

Where, W_S = Thickness of substrate, W_d = Width of the depleted region, A_j = Diffused area of the junction, ρ = Resistivity of the substrate and R_C is the contact resistance.

SR affects the speed and performance of an overall system, which in turn reduces the system's efficiency.

2.2.7 Bandwidth Calculation

All real photodiodes have a shunt capacitance, which can limit the bandwidth of the overall photoreceiver circuits. The theoretical value of the operating bandwidth of a detector is given in Equation 2.7.

$$f = \frac{1}{2\pi RC} \qquad \textbf{(2.7)}$$

Where, R = Resistance and C = Capacitance

The capacitance and resistance in the detector circuit combine to produce a low pass (RC) filter effect on the frequency response. This limits the speed of response of the detector. The available detector bandwidth can be widened, by reducing the capacitance and resistance in the circuit design. However, the disadvantage in having a wider bandwidth is the increase in noise present in the detector output. So, noise and bandwidth must be balanced (a trade-off), depending on how the detector will be used.

To summarise, the resistance and capacitance (RC) of the detector are important as they set the highest frequency at which the device will operate at. Also, capacitance is an important measure and is dependent on detector active area and the material used to fabricate the device. So, if the active surface area is smaller and the intrinsic region is thinner, the capacitance is less.

2.3 Photodetector (PD) Array Devices

2.3.1 Introduction

For this project, [1×12] array photodetectors were developed using PIN diodes with a GaAs/AlGaAs strained layer structure. The devices had a pitch of 250µm. This matched the corresponding VCSEL array. At this distance, cross-talk could be minimised between adjacent detector diodes.

The detectors operated at a wavelength of 850nm and were required to perform at maximum frequency of 1.2GHz. In addition, the resistance and capacitance were matched to the amplifiers on the analogue section of the mixed signal chip (MSC)

Also, the photodiodes were circular with an optical window of 180µm diameter and an active area of 38×10^{-9} m^2 (220µm diameter). For alignment reasons a large window size was considered and this was traded off with operation speed. The expected receiver sensitivity was between 0.4 to $0.5AW^{-1}$.

The photodetectors (PDs) were designed and modelled by Dr Gordon Russell [2.5] at Heriot-Watt University. This was completed before I started my PhD research, which was pre-October 2003.

Originally "off-the-shelf" photodetectors were considered, however, alignment considerations dictated that a large optical window would be required. Also, commercial photodetectors were not available, when this project started, i.e. 2002, which could operate at a frequency of 1.2GHz and which gave a Responsivity of $0.5AW^{-1}$. Therefore, HWU initially engaged with Kelvin Nanotechnology Ltd (KNT) [2.6], Glasgow, UK to produce suitable [1x12] array photodetector devices. These were the Type A devices.

2.4 Type A - Photodetector array devices

2.4.1 Introduction

Type A photodetector devices were fabricated using the Molecular Beam Epitaxy (MBE) [2.7], [2.8] processing method. This was the Type A detector array, which had thickness of 400μm. KNT is a spin-off company from the University of Glasgow, United-Kingdom. The detectors were received by HWU as a quarter wafer form in February 2003. The devices were then diced by Helia Photonics [2.9], a spin-out company from HWU. The design and fabrication of the KNT detectors were already completed before I joined the project.

Since the intrinsic region was 1.5μm thick, a photodiode had a predicted capacitance of 2.69pF. This allowed operation at up to 1.2GHz. Series device resistance was approximately 25Ω, so the load was equivalent. A reverse bias of up to 5V was applied without any problems. Also, since material purity was very high, noise from the device was low. It was decided that to get the specified Responsivity ($0.5\text{-}0.6AW^{-1}$) the intrinsic region of the PIN device would be 1.5μm thick GaAs with 300nm of Be-doped GaAs to form the p-region and 400nm Si-doped GaAs forming the n-region.

2.4.2 Device Specifications

The Specifications of epitaxial layers for the detector wafer are shown in Table 3. Figure 8 shows a schematic of the patterned wafer of the detector. The Substrate thickness is approximately 400µm.

Thickness	Material	Dopant	Doping type	Doping density
100nm	GaAs	Be	p	$1.0x10^{19}cm^{-3}$
200nm	GaAs	Be	p	$3.0x10^{18}cm^{-3}$
1500nm	GaAs			
300nm	GaAs	Si	n	$5.0x10^{17}cm^{-3}$
100nm	GaAs	Si	n	$2.0x10^{18}cm^{-3}$
n + GaAs substrate				

Table 3) Specifications of epitaxial layers for Type A photodetectors

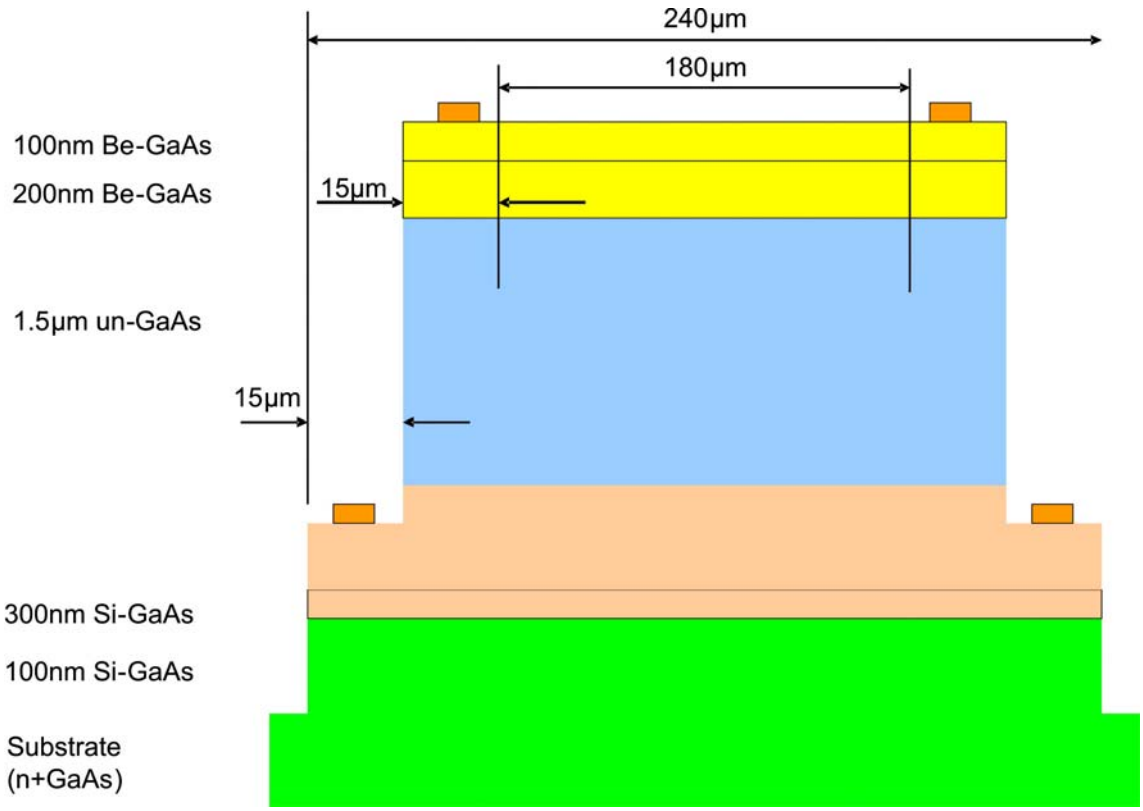

Figure 8) Diagram of patterned wafer

KNT produced a wafer consisting of two [1×12] test array designs: (a) Shoe design, (b) Ring design. A schematic of this arrangement is shown in Figure 9. This was supplied to HWU in February 2003. The metallization of devices was different in both designs. The shoe device has gold tracks only around the appropriate pad side. This means gold was not required down the sides of the optical window, which allowed for slightly larger devices to be manufactured. In comparison, the ring device had a smaller gap (5μm) between adjacent diodes in the array because the gold electrical tracks surround the whole active region.

The disadvantage of shoe design is the electric field through the active region of the device is likely to be far less than the ring diodes. This could result in varying responsivities across the surface of device. The disadvantage of the ring design is increased crosstalk and short-circuit, which would reduce the efficiency of the devices. Characterisation of both layouts enabled me to make a comparison, and choose the ideal array for this project. These experiments are described later in this chapter.

Table 4 shows the specified parameters of the photodetectors.

Property (set by)	Minimum	Typical	Maximum	Unit
Wavelength (VCSEL)	-	850	-	nm
Series Resistance (MSC)	20	25	30	Ω
Capacitance (MSC)	-	3	30	pf
Optical Window (PIFSO)	-	180	-	μm
Bond Pad Size (Packaging)	-	80	-	μm
Pitch (VCSEL)	-	250	-	μm
Responsivity (Material, PD Design)	0.5	0.6	-	AW^{-1}
Passivation Layer Thickness (Wavelength)	191	212	233	nm
Operating Frequency (Memory, Processor, MSC)	1.2	-	-	GHz

Table 4) Photodetector parameters

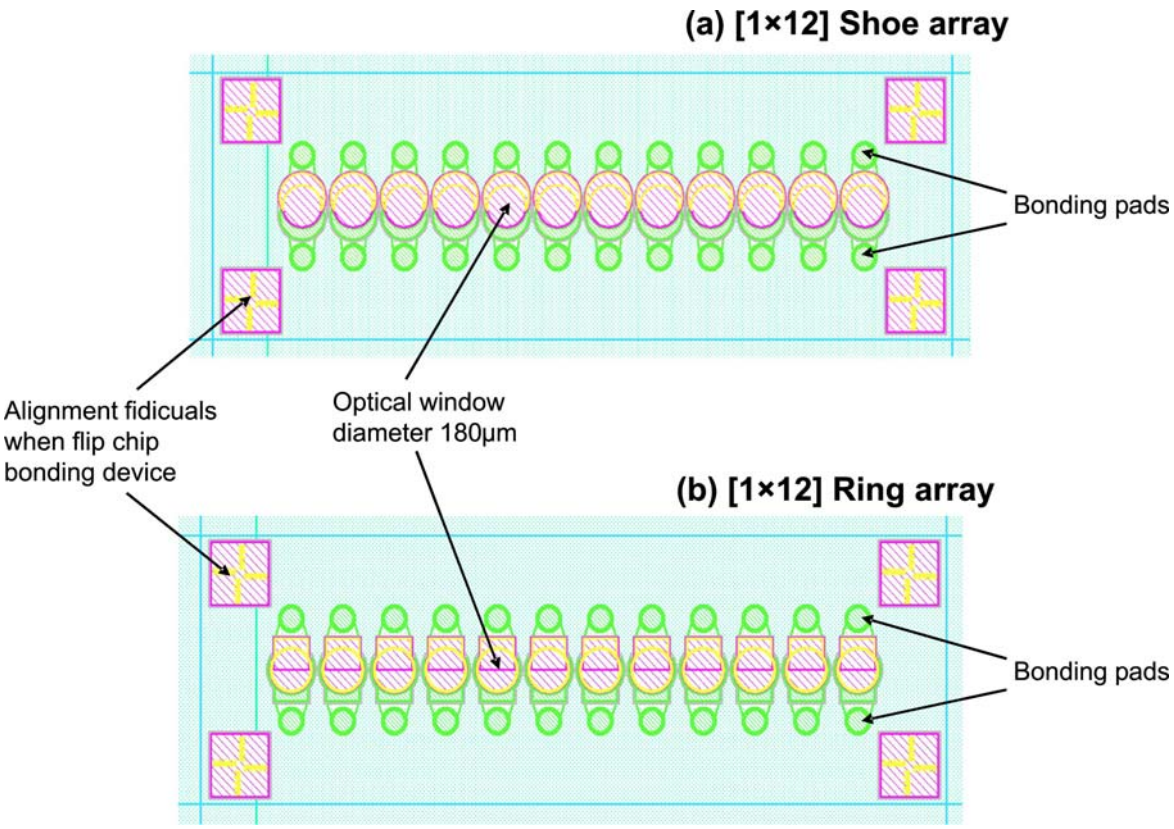

Figure 9) Type A Detector arrays - Schematic and details of [1×12] arrays:
(a) Shoe devices, (b) Ring devices.

Figure 10 shows pictures taken on a Scanning Electron Microscope (SEM) of the shoe and ring diodes.

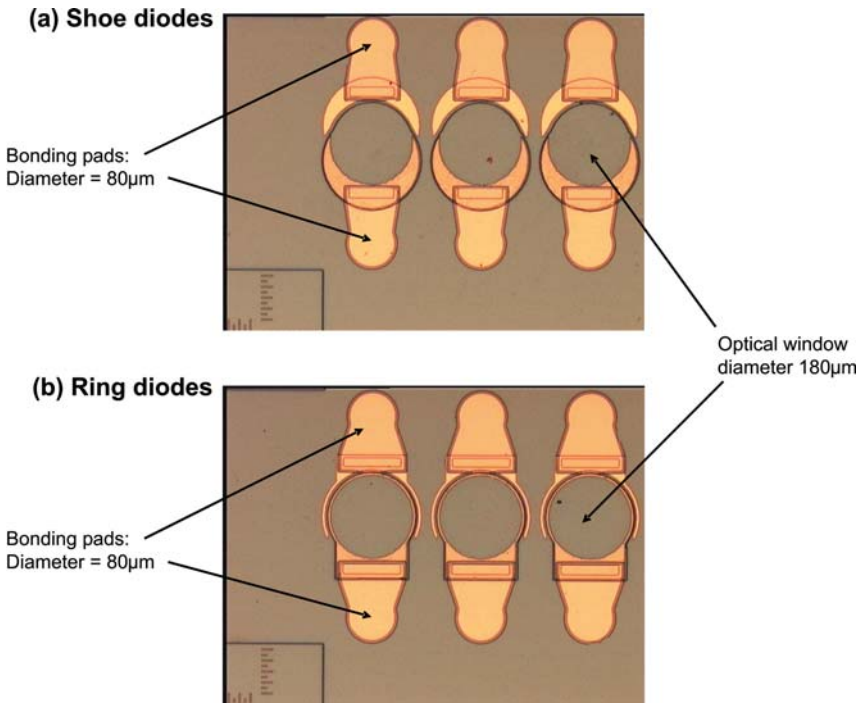

Figure 10) Photos taken using a SEM of Type A Detector arrays: (a) Shoe diodes, (b) Ring diodes.

The optical window of the photodetectors as specified in Table 4 was 180µm, due to the uncertainty in the accuracy of the beam steering capability of the diffractive optics used in the PIFSO for the fan-in elements. However, at 250µm pitch this is impossible to implement as the size of the device is the optical window plus the electrical tracks either side of the diode. These are typically 10µm either side plus another 10Ωm to stop cross-talk between the devices. This would require the devices to be exactly 250µm, which is not possible to manufacture. After further work with the PIFSO, it was decided that the 180µm window was both manufacturable and suitable for use with the PIFSO. For the test wafer, two designs of photodetectors were designed, i.e. shoe and ring. The key dimensions of the photodetectors are shown schematically in Figure 11.

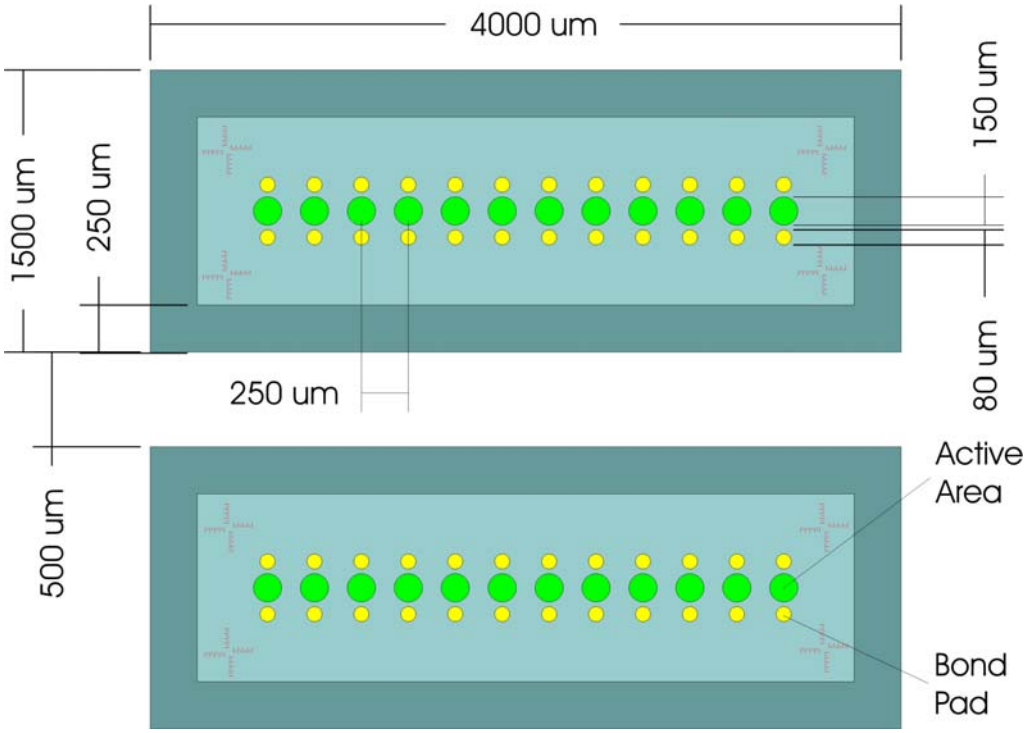

Figure 11) Key dimensions of Photodetectors

With regard to contacts when flip chipping to gold stud bumps Ni contact with Au on top was used. This was because the Au would flow and mix with the contact when heated, which would result in good adhesion. The Ni under-layer was used to prevent the contact from being destroyed.

Photodiode bonding pads were placed as shown in Figure 11. Their pad size was 80µm. The metals used were gold over nickel-chromium (Ni-Cr) tracks and the thicknesses

were Au (300nm) and Ni-Cr (10nm). The preferred passivation layer used was Silicon Nitride (SiN) with a thickness of 212nm. This provided a crude Anti-Reflective (AR) coating. Figure 12 shows a diagram of the photodiode bonding pad detailing its metallisation and respective thicknesses.

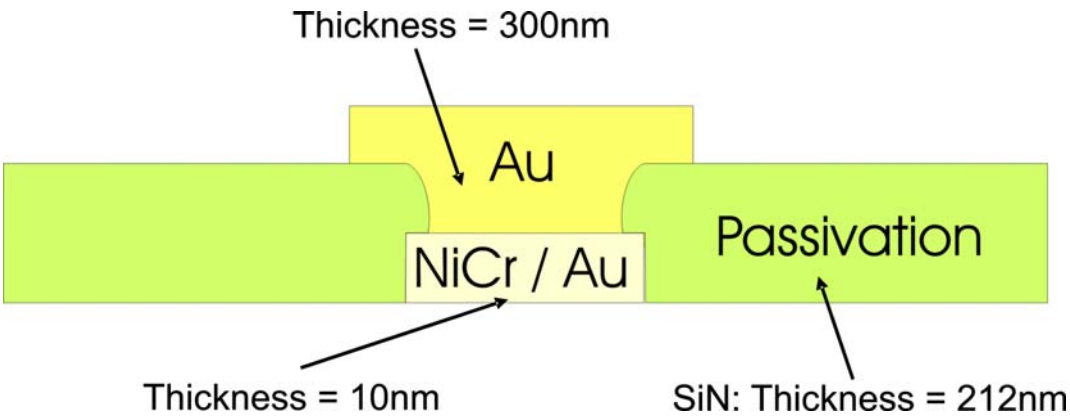

Figure 12) Schematic showing the metallisation and respective thicknesses on the Photodiode bonding pad

As mentioned earlier in this section, the AR coating was a SiN plasma-enhanced chemical vapour deposition (PCVD) material of thickness 212nm (±10%). A 10% change in thickness results in a change of <1% reflectivity. From the system diagrams shown in Figure 13, the angle at which light will enter is straight on. This means that AR coating tolerances imply that a few degrees deviation will not be noticeable.

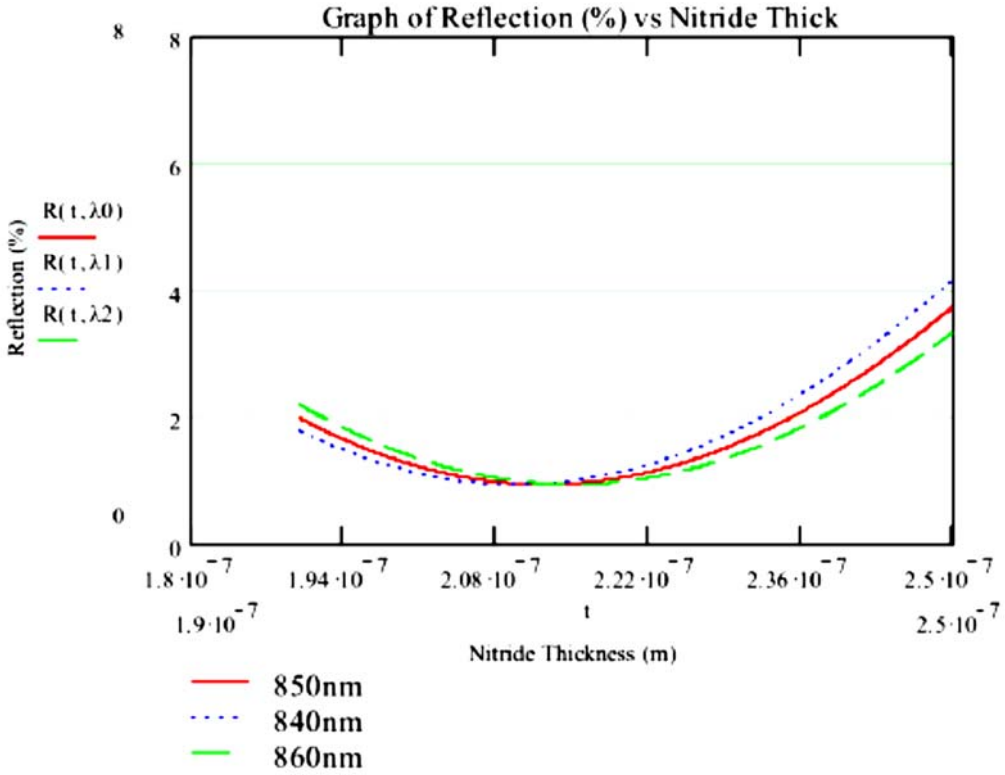

Figure 13) System diagrams of Detector AR coating: Plots of Reflection (%) versus SiN Thickness.

Alignment markers (Fidicuals) for flip-chip bonding were placed at each corner of the device. See Figure 14.

Figure 14) Fidicuals – alignment markers

The design of the Fidicuals was fixed by HWU and the HOLMS consortium before I started the project. So, it was not possible to change the design, as the photomasks were

already completed. To re-design and produce another mask would incur cost, which the project budget would not allow

2.4.3 Results

Several runs were attempted by the initial manufacturer (KNT) but all were flawed. The primary flaws were in variations in resistance from one device to another and in lack of consistency across individual arrays. The designs were retained and a second manufacturer (Sheffield) produced devices of good quality, which were very close to the required specifications. The second manufacturer was selected due to their use of the metal-organic chemical vapour deposition (MOVCD) [2.10], [2.11] process, which promised more than the MBE used by others, i.e. cheaper.

When KNT supplied HWU the wafer in February 2003, they were accompanied by test results and data analysis performed on the detectors. These details can be obtained from reference [2.12]. This data showed that the initial run of photodiodes was not successful, i.e. The I-V characteristics were very poor for the photodiodes. This information showed a variation in the series resistance of detector devices within the same array and no correlation between the performances of the devices with their physical characteristics. This is believed to be because the recipe used for the n-layer metal and the lack of annealing was sub-optimal in this case.

Subsequently, in-house tests on the detectors conducted by myself in October 2003 confirmed this. This work is explained in section 2.6 of this chapter.

To summarise, concerns existed over the electrical characteristics of these components, cost of ordering a full set and production delays. This, coupled with an understanding that KNT did not consider optoelectronics for applications similar to the HOLMS project to be a core market, led us to investigate an alternative supplier. So, to reduce further risk to the project, a further set of detectors was ordered from EPSRC National Centre for III-V Technologies, University of Sheffield.

2.5 Type B - Photodetector array devices

2.5.1 Introduction

A further set of [1×12] array test detectors was ordered from the Engineering and Physical Science Research Council's (EPSRC) National Centre for III-V Technologies based at the University of Sheffield, United-Kingdom [2.3], which is a central facility that specialises in small wafer runs for academic purposes. This array was the Type B detector. The Sheffield detectors were fabricated using the metal-organic chemical vapour deposition (MOVCD) process. These components were substantially cheaper, i.e. Sheffield full set cost £2000; KNT full-set cost £20,000 (Approximately, a factor of 10 more expensive). When I joined the project, the 1st design of the Sheffield detectors was already completed and the chips were in fabrication.

The set of detectors arrived at HWU in September 2003. I started in October 2003 parametric tests to determine specifically the dark current values and series resistance, and optical tests using light source of wavelength 850nm. All tests were completed in March 2004. Experimental set-up and results are explained in section 1.7 of this chapter. A CAD diagram of the Sheffield wafer is shown in Figure 15.

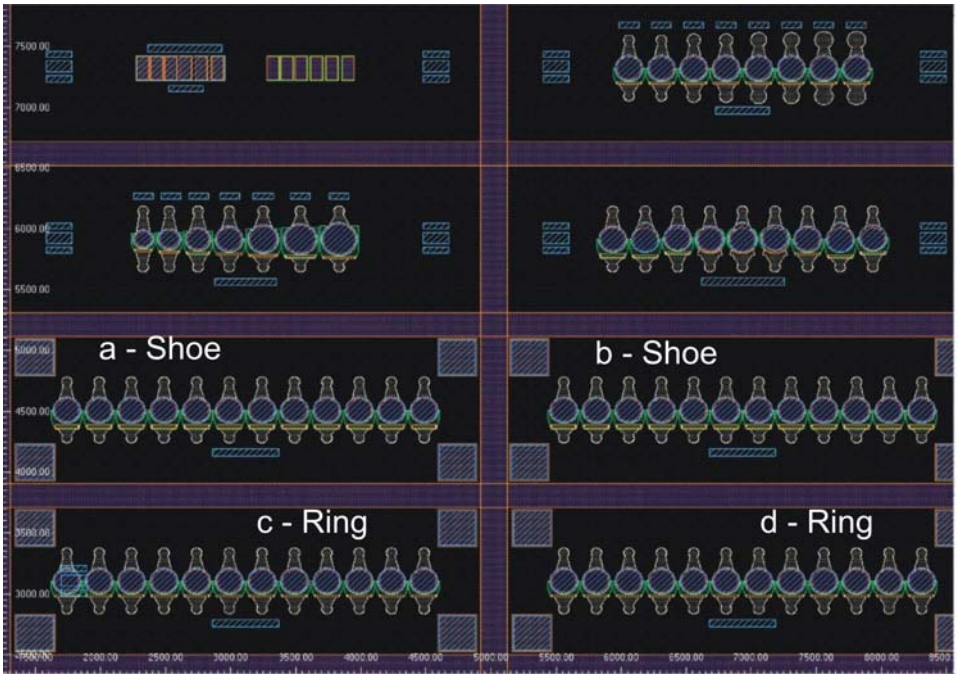

Figure 15) CAD diagram of Type B Detector arrays - quarter wafer showing Diodes:
a – Shoe, b – Shoe, c – Ring and d – Ring.

Similar to the first type of detectors, i.e. Type A – detector arrays, two designs of [1×12] photodetector arrays were fabricated, i.e. shoe and ring designs. Also, the PDs had a thickness of 400um

Figure 16 shows photos taken with an optical microscope of the two layouts.

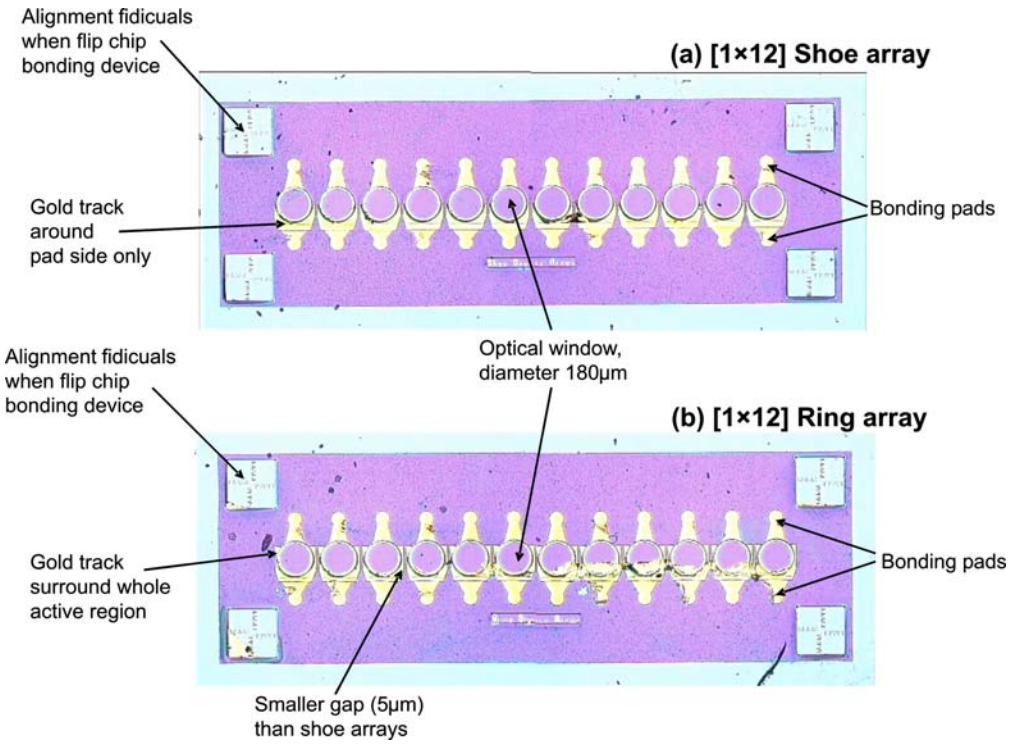

Figure 16) Pictures of Type B Detector [1×12] arrays taken with optical microscope: (a) Shoe design, (b) Ring design.

Also, the same specifications as the Type A detectors were used for the Type B detectors on the test wafer. The only difference was in the two epitaxial layers, where C was used as the dopant instead of Be. See Table 5.

Thickness	Material	Dopant	Doping type	Doping density
100 nm	GaAs	C	p	$9.0x10^{18}cm^{-3}$
200 nm	GaAs	C	p	$2.5x10^{18}cm^{-3}$
1500 nm	GaAs			
300 nm	GaAs	Si	n	$5.0x10^{17}cm^{-3}$
100 nm	GaAs	Si	n	$2.0x10^{18}cm^{-3}$
n + GaAs Substrate				

Table 5) Specifications of epitaxial layers for Type B photodetectors

2.5.2 Cleaving of Type B Detector Wafer

The set of detectors fabricated came in a quarter wafer format from the manufacturer. This wafer needed to be cleaved into individual dies consisting of [1×12] photodiode arrays. The dicing was performed by a spin-out company from Heriot-Watt University, Helia Photonics [2.9].

The wafer was cut into individual devices using a circular diamond saw along the scribing lanes, which are indicated in Figure 17. The scribing lanes are of width 220μm. Outside this region, there was no damage when cleaving the wafer. Figure 17 shows a full schematic of the detector quarter wafer, which was cleaved into individual components of shoe and ring device arrays.

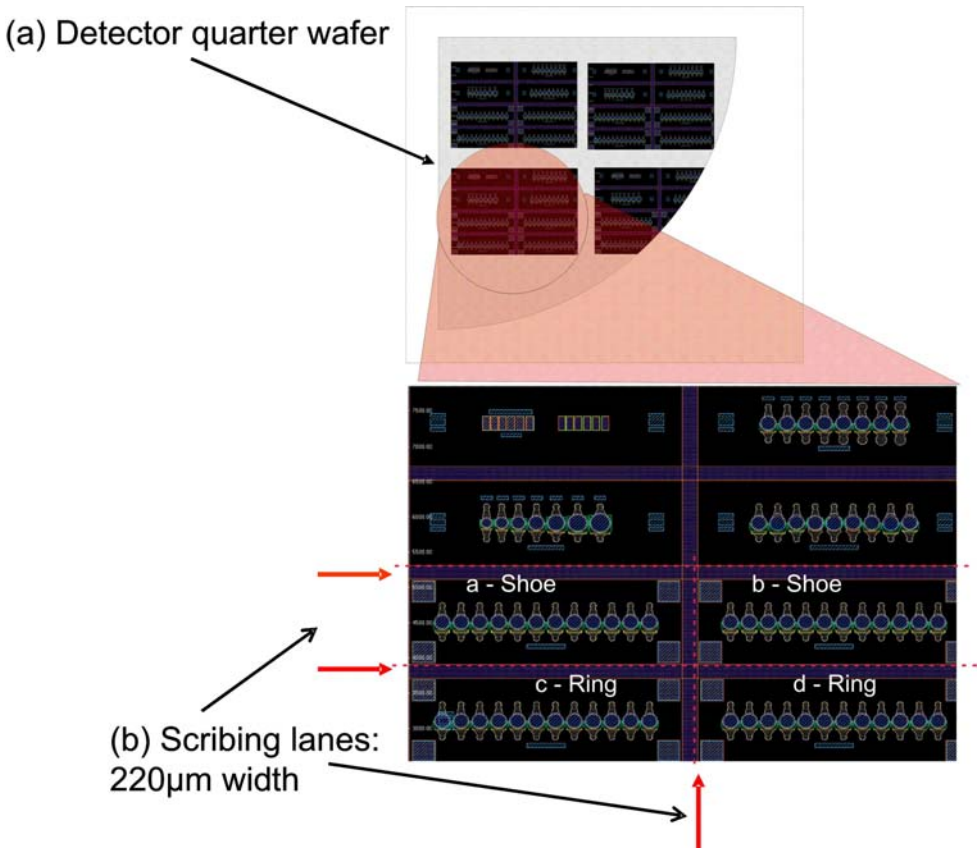

Figure 17) Schematic of Type B Detector quarter wafer, which was diced into individual devices: (a) Detector quarter wafer consisting of (1×12) Shoe and ring arrays, (b) Positioning of Scribing lanes (width 220µm).

2.6 DC Characterisation of Type A Detector Arrays

2.6.1 Introduction

In this section, characterisation experiments of Type A devices are described. Dark current measurements were conducted on the devices. Details of the experimental set-up, procedures used, results and analysis will be described in the following sections.

2.6.2 Layout of Type A Photodetectors

For the purposes of testing, the shoe diodes were labelled x1 to x12 and the ring diodes were labelled y1 to y12. This can be seen in Figure 18.

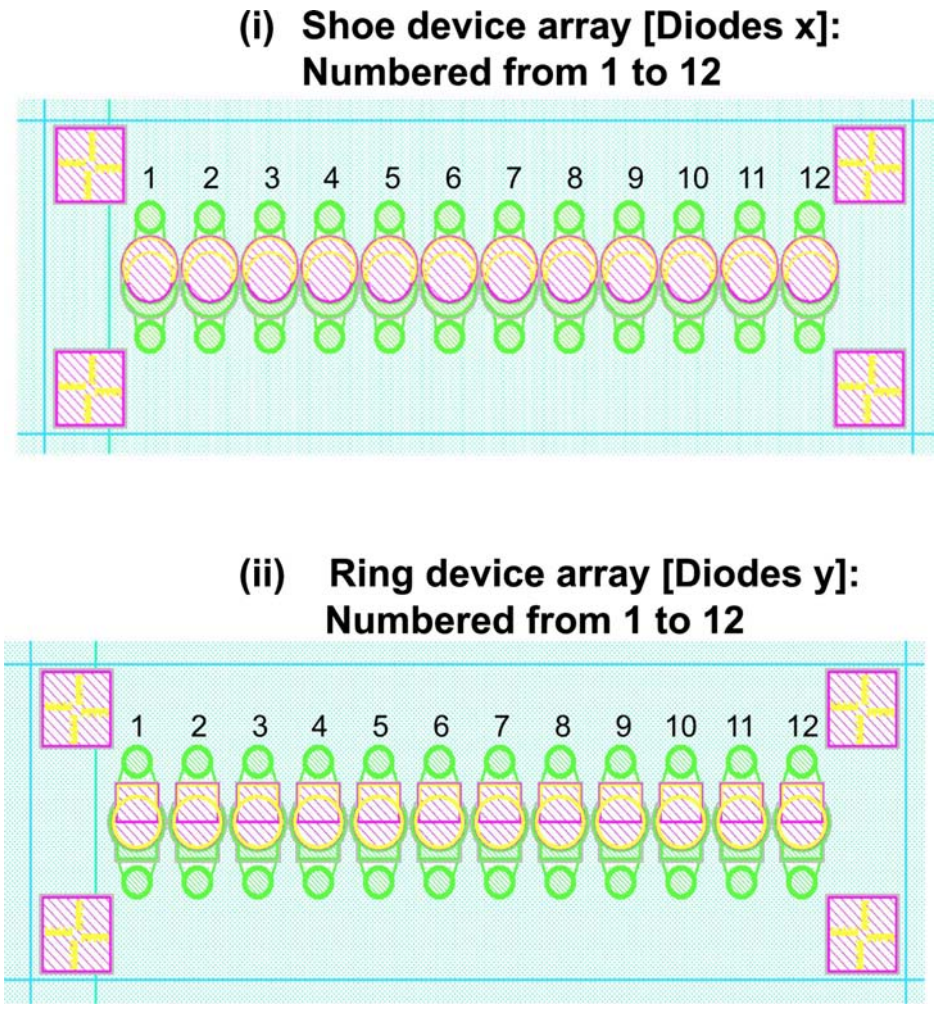

Figure 18) Diagram showing Shoe and Ring layouts of Type A Detector arrays:
(i) Shoe Diodes, x – numbered 1 to 12, (ii) Ring Diodes, y – numbered 1 to 12.

2.6.3 Experimental Set-up and Procedure

Figure 19 shows a diagram of the experimental set-up for conducting dark current measurements. This arrangement consists of a probe station, which included the tungsten probes (Diameter: 25µm) to make electrical contact with detector pads, probe manipulators, x-y translation stage, microscope and HP4145 Parameter Analyzer. The parameter analyzer was used to apply a bias voltage and record the corresponding photocurrent from the diode. Using the probe station, the detector array was fixed and connected with crocodile clips to the HP 4145B Parameter Analyzer.

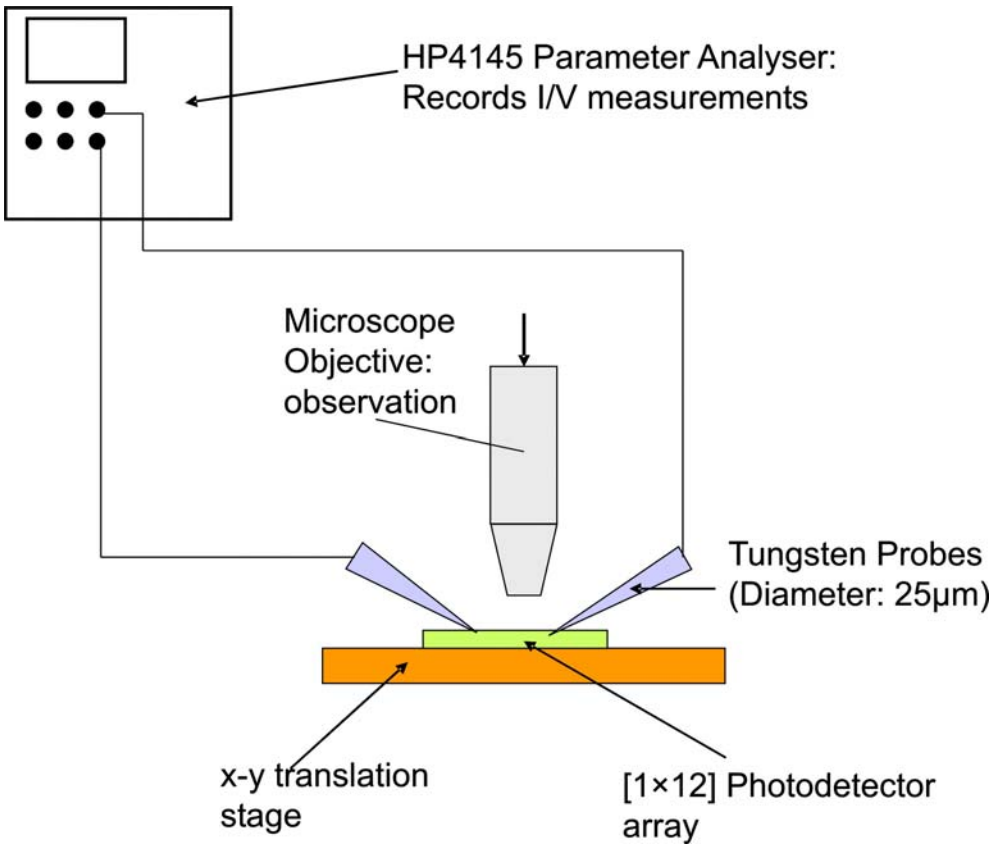

Figure 19) Schematic of experimental layout for conducting Dark current measurements on Type A Detector arrays

Figure 20 shows a photo of the experimental arrangement.

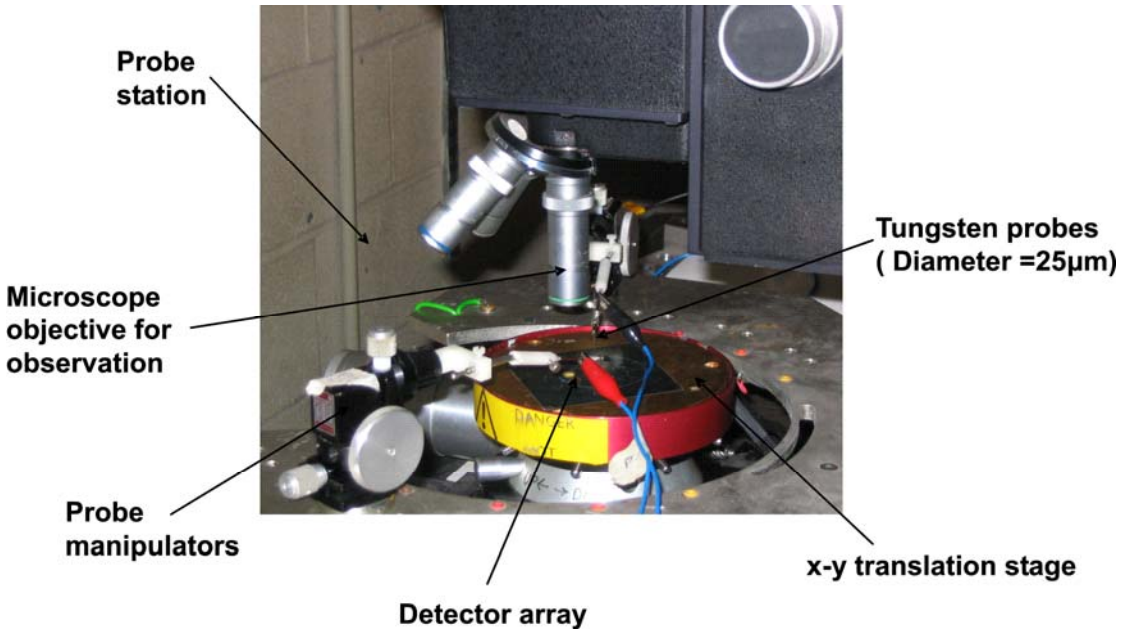

Figure 20) Picture of the probe station used:
Dark current measurements were taken of the Type A Detector arrays.

The following parameters were chosen on the parameter analyzer: range of -10V to +0.3V, a step width of 0.05V and a medium integration time.

The functionality of the detectors was checked under dark conditions. The dark current was recorded and analyzed on the parameter analyser for the following diodes: Shoe diodes - x5, x6 and Ring diodes – y5, y6.

2.6.4 Results

From these results, I-V plots were obtained for all diodes measured. These measurements were then compared with the test results conducted by KNT (See reference [4.1]). Current-Voltage graphs of the dark current data for the tested diodes, i.e. Shoe diodes - x5, x6 and Ring diodes – y5, y6, compared with KNT's data are shown respectively in Figure 21, Figure 22, Figure 23 and Figure 24.

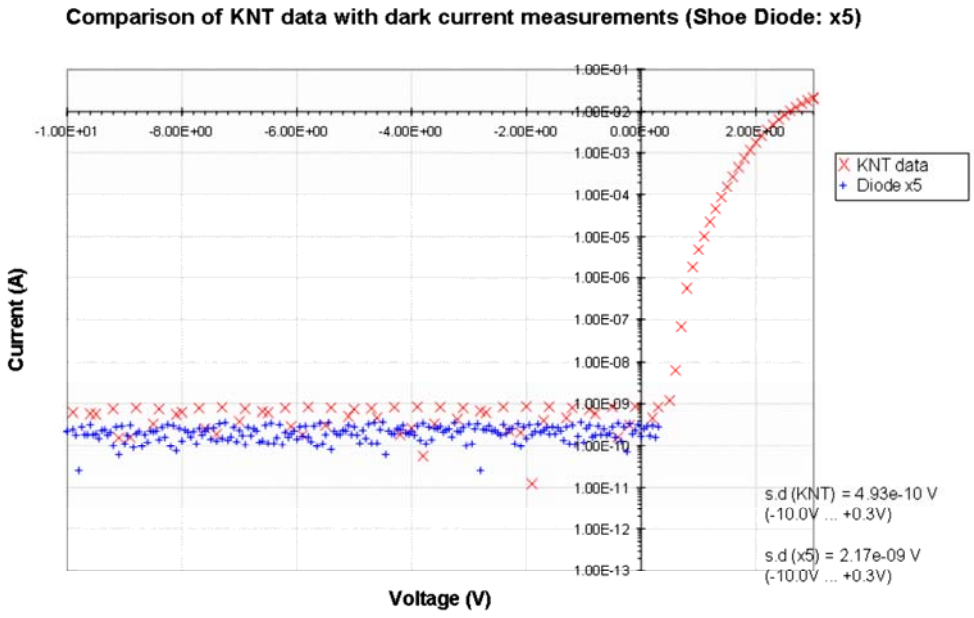

Figure 21) Current/Voltage plots:
Showing comparison of dark current measurements for Shoe Diode-x5 and KNT data.

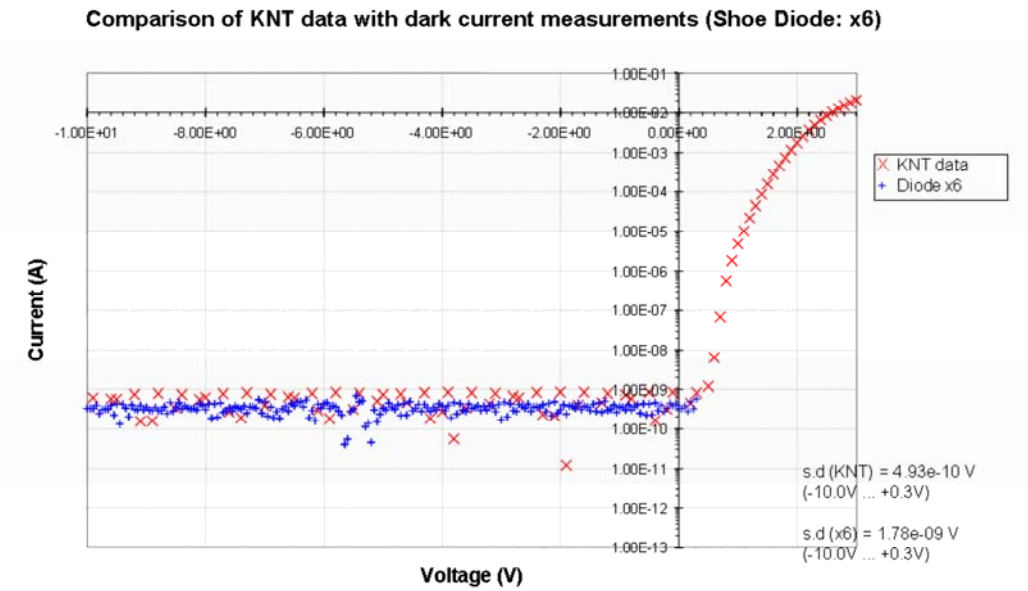

Figure 22) Current/Voltage plots:
Showing comparison of dark current measurements for Shoe Diode-x6 and KNT data.

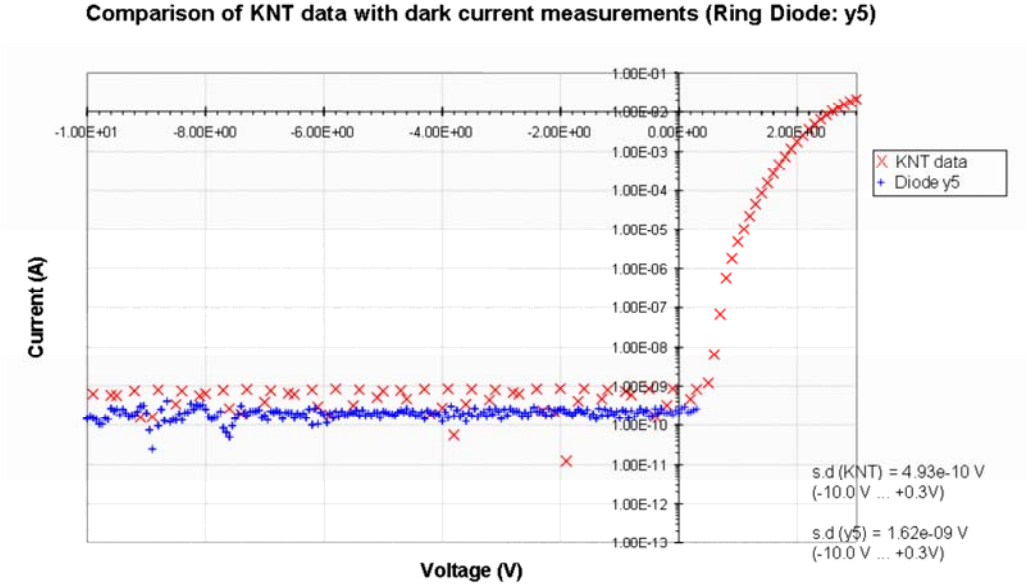

Figure 23) Current/Voltage plots:
Showing comparison of dark current measurements for Shoe Diode-y5 and KNT data.

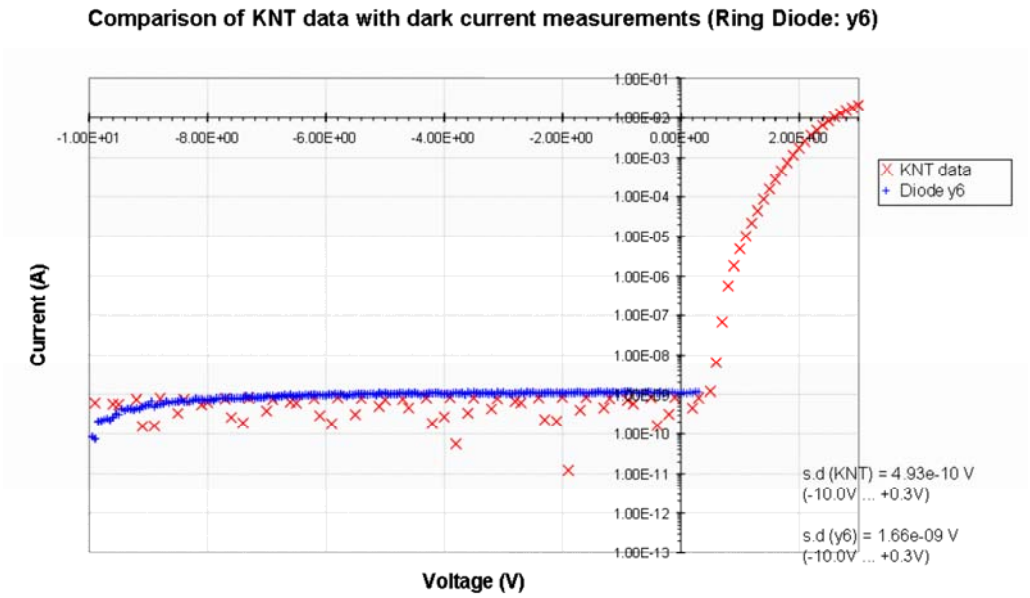

Figure 24) Current/Voltage plots:
Showing comparison of dark current measurements for Shoe Diode-y6 and KNT data.

2.6.5 Summary

The values of the dark current fluctuate around zero in an order of 10^{-9} Amps. To present the dark current values in a visual graphical way, a logarithmic scaling was necessary. The data was processed and shifted to the maximum of the absolute of the measured values ($I_{shift} = \max\{abs(I)\}$).

Table 6 shows the standard deviation (Amps) of dark current measurements for: Shoe diodes - x5, x6 and Ring diodes – y5, y6. All results were in ~10^{-9}A.

Diode tested	Standard deviation [s.d] (Amps)
Shoe diode: x5	2.17×10^{-9}
Shoe diode: x6	1.78×10^{-9}
Ring diode: y5	1.62×10^{-9}
Ring diode: y6	1.66×10^{-9}

Table 6) Standard deviation of dark currents for the test diodes in the Type A Detector array

2.7 DC Characterisation of Type B Detector Arrays

2.7.1 Introduction

In this section, characterisation experiments of Type B devices are described. Dark current measurements were conducted and from these results, the Series Resistances of the devices was computed. Then, optical testing (at λ=850nm) measurements were performed. From this data, the Responsivity of Type B photodiodes was calculated.

Details of the experimental set-up, procedures used, results and analysis will be described in the following sections.

2.7.2 Layout of Type B Photodetectors

As explained in this chapter, the device wafer has two layouts, i.e. shoe and ring designs. For the purposes of testing, the shoe diodes were labelled a1 to a12 & b1 to b12 and the ring diodes were labelled c1 to c12 & d1 to d12. This can be seen on Figure 25.

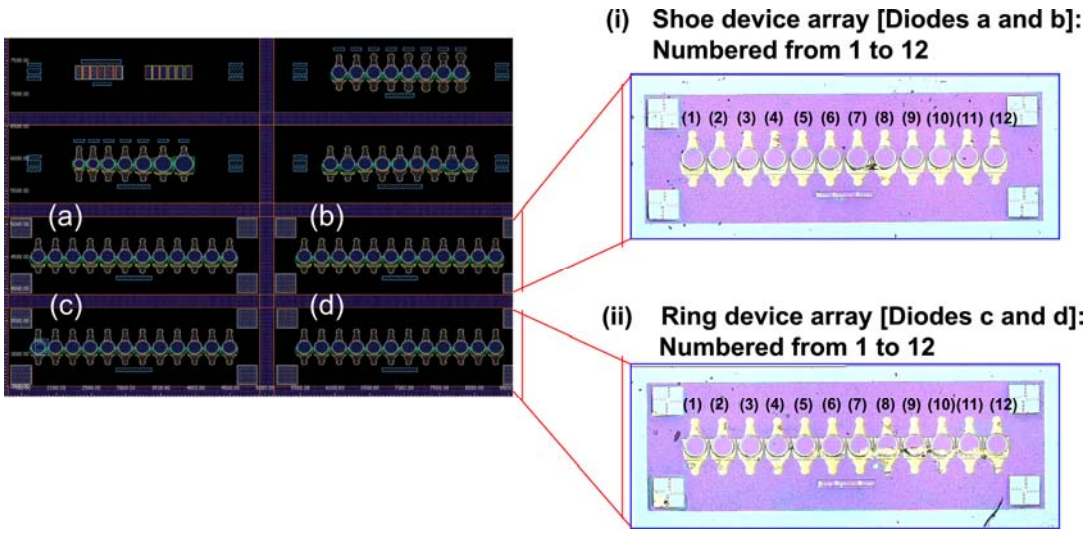

Figure 25) Diagram showing Shoe and Ring layouts of the Type B Detector arrays:
(i) Shoe Diodes a and b – numbered 1 to 12, (ii) Ring Diodes c and d – numbered 1 to 12.

2.7.3 Experimental Set-up

Figure 26 shows the experimental layout used for measurements of the dark current and characterisation of the Type B photodetectors.

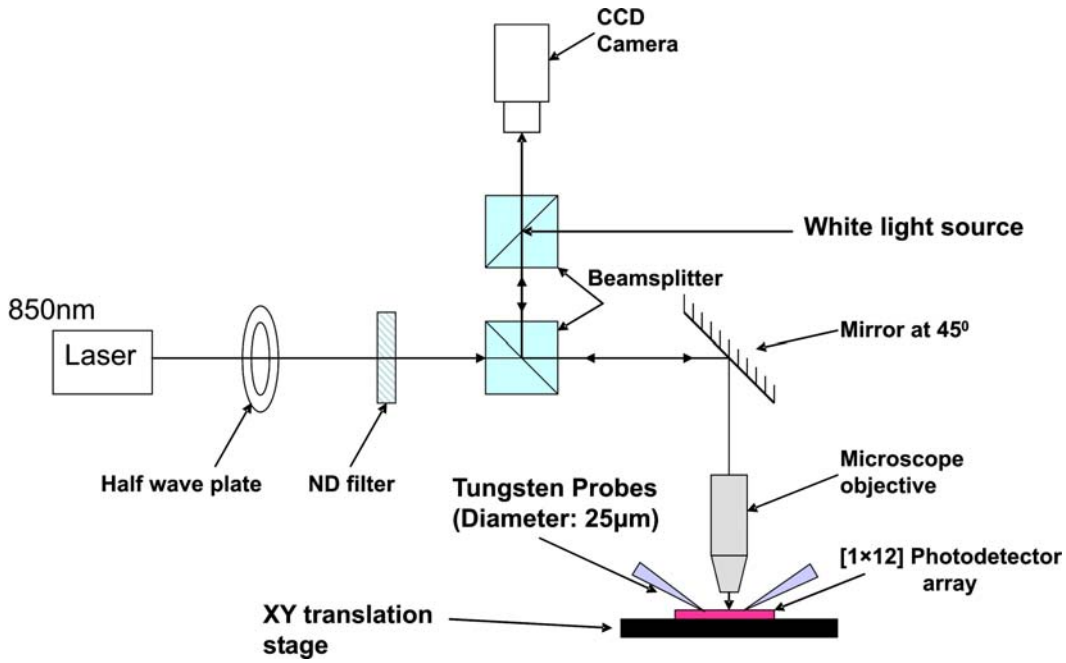

Figure 26) Schematic of experimental layout for optical characterisation of Photodetectors

In this set-up, an 850nm Laser, half wave plate and ND (Neutral Density) filter were used with a polarising beam splitter to equalise the optical power in the device and detector paths. Also, a mirror set at 45^{o} to the plane of the baseplate guided the laser beam on to the device. A microscope objective was used for getting suitable spot size and focusing the beam on to the PIN detector active area.

The sample was mounted on an X-Y translation stage. Due to the small area of the contact pads, very fine tungsten probes (approx. 25µm tips) were used to make electrical contact. White light source with an adjustable lens and beam splitter was used to illuminate the device. A CCD camera, zoom lenses and TV monitor were used in the aligning process. Optical powers were measured using a Newport optical power meter with a silicon detector. A Hewlett Packard Semiconductor parameter analyser (HP 4101 pA meter) was used to apply the bias voltage and record the photocurrent. Figure 27 shows a picture of the experimental set-up.

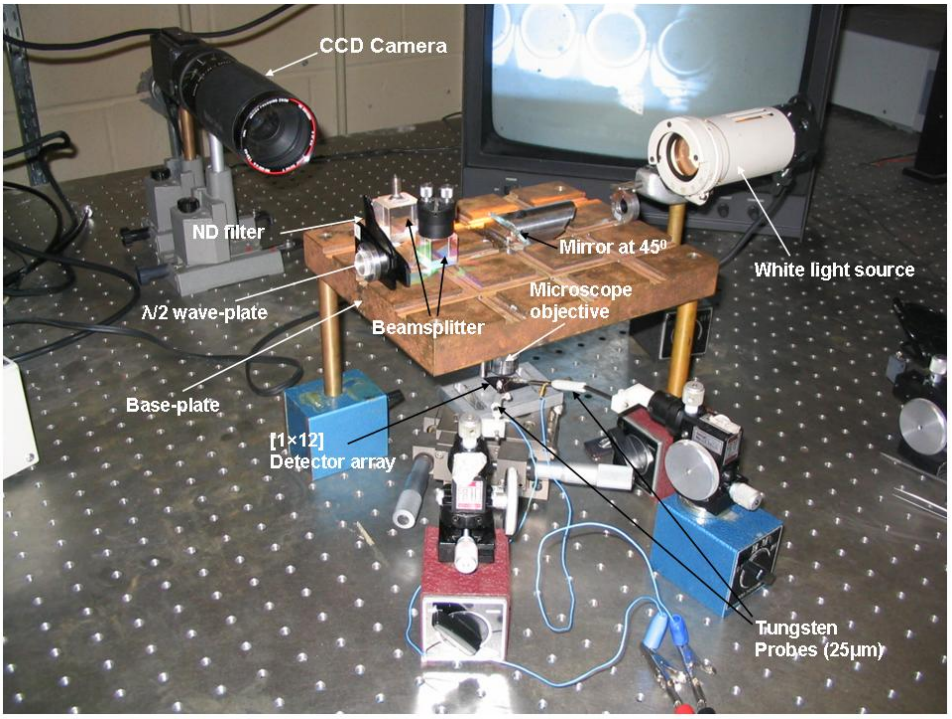

Figure 27) Photograph of experimental layout for optical characterisation of Photodetectors

2.7.4 Experimental Procedure

First of all I fixed the base plate parallel to the optical bench and aligned the laser beam with the help of two pin holes to make sure that the laser beam was aligned to the surface of the baseplate. In this process of alignment, we used the pair of mirrors to have control on the beam. An infrared detector card was used during the process of alignment to "see" the beam.

Once the alignment process was completed, all the optical components as shown in Figure 26 and Figure 27 were assembled. With the help of infrared card and detector we made sure that the laser beam was incident on the translation stage in the correct position and with suitable power. Then we switched on the white light source, which we used for viewing the spot of the laser beam and the device. We aligned the CCD camera on the spot where laser beam is incident. Then we used a spare device for alignment of the spot on the active area of the detector.

As explained earlier, a 3dB beam splitter and half wave plate were used to help monitor the power incident on the device. When all the components were aligned on the baseplate the power levels in the axis were equalised using the half wave plate.

Two fine probes were used for biasing the detector, and monitoring the photocurrent. The HP Semiconductor parameter analyser (HP 4101 pA meter) was used to obtain the corresponding I-V curves by varying the bias voltage from -5 to +2 Volts and monitoring the corresponding photocurrent from the detector. These measurements included one with zero optical power so as obtain the dark current curves for the detector. From the dark current values I calculated the series resistance of the photodetectors.

With the laser fully aligned, optical testing was conducted on the detectors using a source of wavelength 850nm. Analysis of the results is explained in the next section of this chapter.

Photographs were taken from the CCD camera (See Figure 28) showing contact probes in position on the 80µm diameter pads of the devices. The active area of the detector can be seen in between the probes.

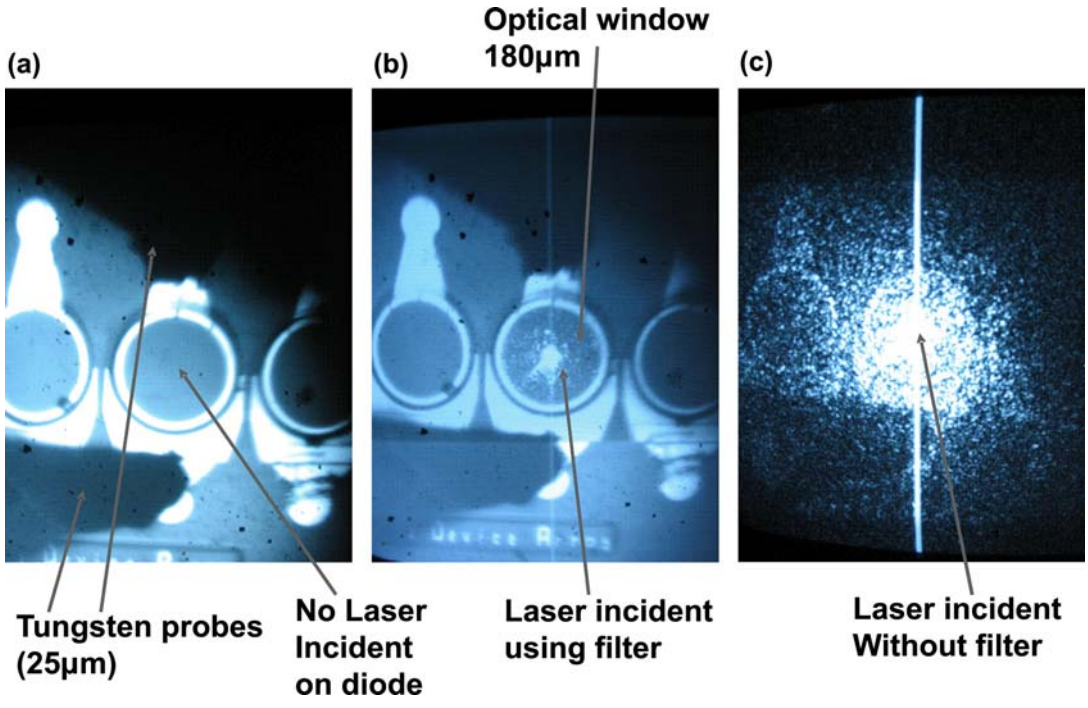

Figure 28) Photos from CCD camera: (a) No Laser, (b) Laser using filter, (c) Laser without filter.

2.7.5 Results

From the dark current measurements, Current/Voltage (I/V) curves were plotted for the following diodes: Shoe – a2, a11, b2, b11 and Ring – c2, c11, d2, d11. This is shown in Figure 29.

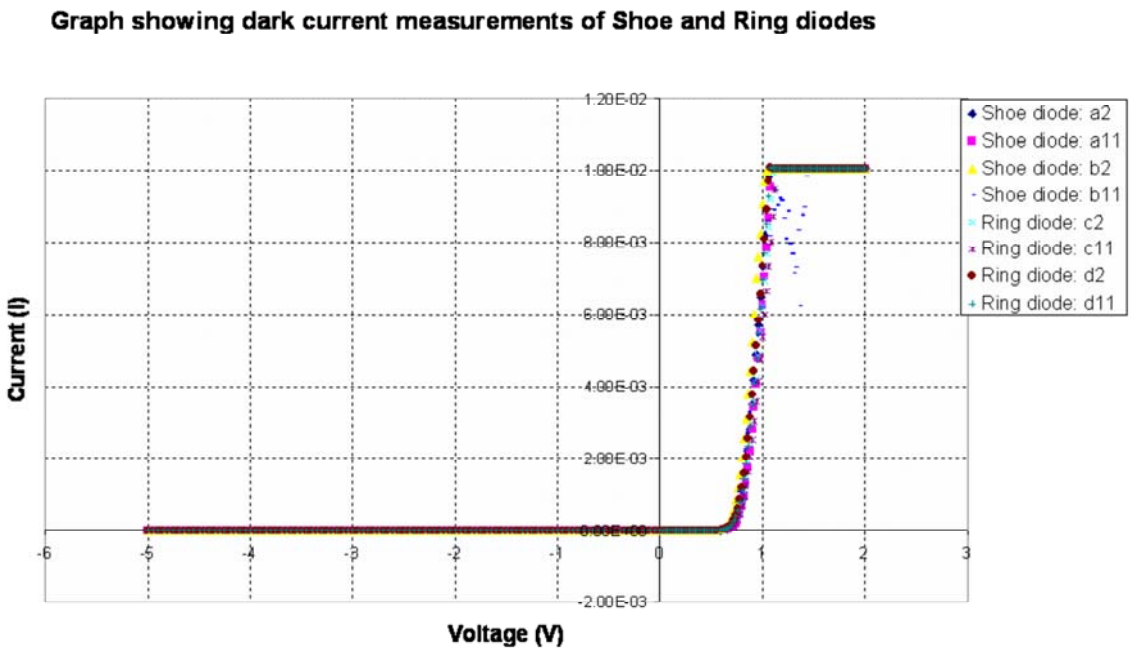

Figure 29) Current/Voltage plots: Showing dark current results for Shoe diodes: a2, a11, b2, b11 and Ring diodes: c2, c11, d2, d11.

The data for the dark current measurements taken for diodes: Shoe – a2, a11, b2, b11 and Ring – c2, c11, d2, d11 are given in Table 7.

Shoe array		**Ring array**	
Diode	Average I [dk] (Amps)	Diode	Average I [dk] (Amps)
a2	8.66×10^{-10}	c2	6.35×10^{-9}
a11	6.08×10^{-10}	c11	4.61×10^{-9}
b2	8.27×10^{-10}	d2	3.95×10^{-9}
b11	4.22×10^{-10}	d11	3.77×10^{-9}

Table 7) Dark current measurements taken for shoe and ring arrays

The results showed that the ring devices had larger dark current values in comparison to the shoe diodes, i.e. ~10^{-10} Amps for the shoe devices and ~10^{-9} for ring devices.

Next, values for the series resistance of each corresponding diode were deduced by calculating the gradient of the linear region of their respective I/V plot, and then taking the inverse of this value. The results are shown in Table 8.

Shoe array		**Ring array**	
Diode	Series Resistance (Ω)	Diode	Series Resistance (Ω)
a2	27.47	c2	31.65
a11	29.76	c11	33.44
b2	26.95	d2	30.67
b11	26.95	d11	28.90

Table 8) Series resistance for shoe and ring arrays

From analysis of the results for series resistance, the values obtained for shoe devices are more consistent with the PD parameters given by the manufacturer. See Table 9.

Minimum	**Typical**	**Maximum**
20	25	30

Table 9) PD parameters (Ohms) given by manufacturer

Using the results obtained for optical testing at λ=850nm, I/V plots were produced for all the following diodes which were measured: Shoe diodes: a4, a8, b4, b8 and Ring diodes: c4, c8, d4, d8. The associated dark current data was also taken for each. This is shown on Figure 30.

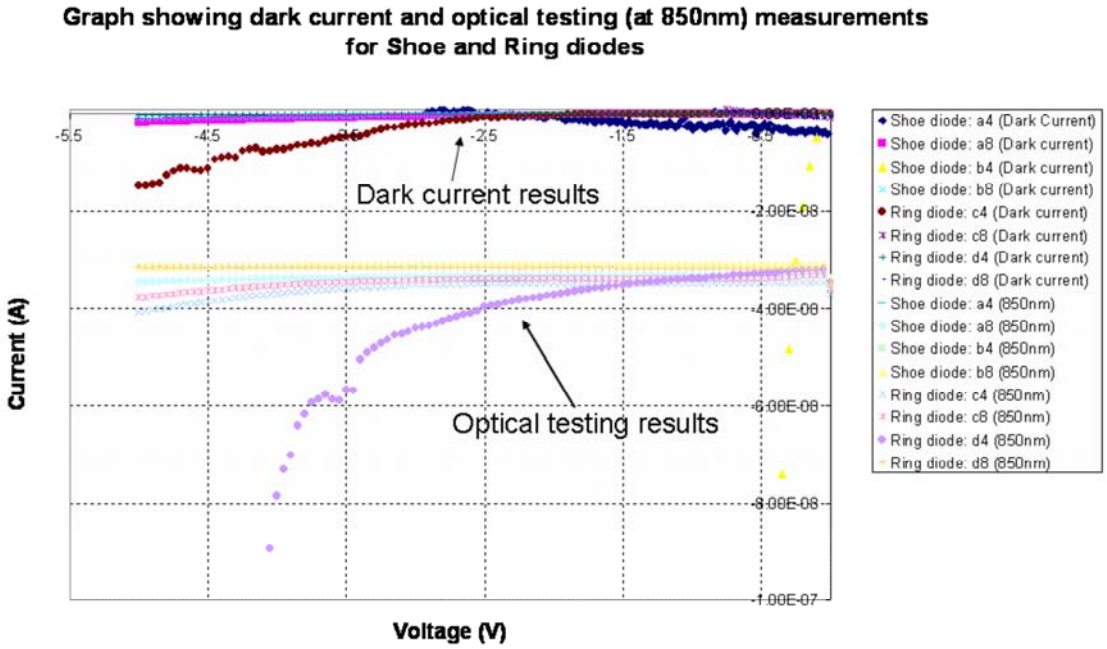

Figure 30) Current/Voltage plots: Showing dark current and optical testing (at λ=850nm) results for Shoe diodes: a4, a8, b4, b8 and Ring diodes: c4, c8, d4, d8.

Table 10 shows data of generated photocurrent (I[ph]) obtained from optical testing at 850nm. These values ranged between -3.16 to -3.58 × 10^{-8} Amps.

Shoe array		**Ring array**	
Diode	I [ph] (Amps)	Diode	I [ph] (Amps)
a4	- 3.16 × 10^{-8}	c4	- 3.58 × 10^{-8}
a8	- 3.35 × 10^{-8}	c8	- 3.45 × 10^{-8}
b4	- 3.18 × 10^{-8}	d4	- 1.59 × 10^{-8}
b8	- 3.32 × 10^{-8}	d8	- 3.17 × 10^{-8}

Table 10) Photocurrent values for shoe and ring devices

Finally, responsivity calculations were made for each diode using the values obtained for photocurrent. The power incident (P_{in}) on each diode was 8.45×10^{-8} W. Equation 2.4 below was computed to determine Responsivity:

$$R = \frac{I_{ph}}{P_{in}} \qquad \textbf{(2.4)}$$

Where, P_{in} = 8.45 × 10^{-8} Watts

Data for Responsivity [R] is shown on Table 11.

Shoe array		Ring array	
Diode	R [AW^{-1}]	Diode	R [AW^{-1}]
a4	0.37	c4	0.42
a8	0.40	c8	0.41
b4	0.38	d4	0.36
b8	0.39	d8	0.37

Table 11) Responsivity data of Photodetectors

The results for responsivity ranged between 0.36 to 0.42AW^{-1}. Shoe and ring devices showed similar values of R, but were lower in comparison to PD specification given by the manufacturer, i.e. 0.5AW^{-1} (Minimum), and 0.6AW^{-1} (Typical).

2.7.6 Summary

Overall, the shoe devices showed more consistency in its results in comparison with the ring diodes, i.e. lower dark current and series resistance values. Measurements showed shoe diodes experienced less cross-talk and short circuiting across the array. A decision was made to choose the shoe design for implementation into the high speed systems demonstrator.

2.8 Conclusion

The main findings from this chapter were that optical characterisation experiments of the two types of detectors (Type A and Type B devices) were successfully performed.

These results determined the most suitable type of detectors to be used for the high-speed demonstrator. This was the shoe design, Type B photodetector arrays, because their performance was more consistent.

In the following chapter, I describe the transmitter devices and mixed signal chips used for my research work.

2.9 References

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[2.13] EPSRC National Centre for III-V Technologies at The University of Sheffield, (http://www.shef.ac.uk/eee/research/nc35t).

Chapter 3

Transmitter Devices and Mixed Signal Chips (MSCs)

3.1 Introduction

The outline of this chapter is as follows. In section 3.2, background on vertical cavity surface emitting lasers (VCSELs) is given. In section 3.3, the VCSEL array devices used in my experimental work are described. In section 3.4, optoelectronic characterisation experiments on these VCSELs are discussed. Finally, in section 3.5, an explanation of the mixed signal chips (MSCs) used is provided.

3.2 Background

VCSELs [3.1], [3.2] are constructed by growing a semiconductor, containing a GaAs active region, between two Distributed Bragg Reflectors (DBRs). In conventional VCSELs the upper and lower mirrors are doped as p-type and n-type materials, forming a diode junction. The planar DBR mirrors, contains layers with alternating high and low refractive indices. Each layer boundary causes a partial reflection of an optical wave. For waves whose wavelength is close to four times the optical thickness of the layers, the many reflections combine with constructive interference, and the layers act as a high-quality reflector. The range of wavelengths that are reflected is called the photonic stop-band. Contacts are placed on top and bottom of the stack to electronically excite the electrons in the active region. Laser emission can be through either the p-type or n-type DBR. Figure 31 shows details of a VCSEL device structure.

VCSELs emit perpendicular to the surface of the chip as shown in Figure 31. This simplifies fabrication and reduces production costs. They were suitable for my research as they could be fabricated with electrical connections for flip chip bonding on the same surfaces as the emission aperture. Unlike stripe laser diodes (LD), there is no longer any need for dicing separate devices from a larger structure. This means smaller structures can be created that consume less power. This is very important as, unlike telecoms applications, computer interconnects may be high density and require many devices in a small area.

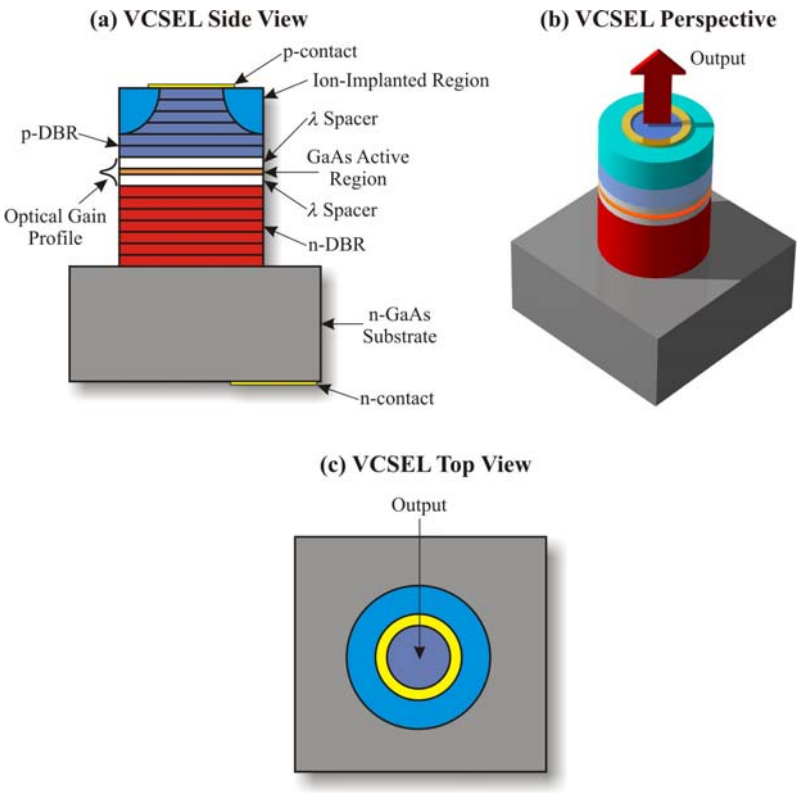

Figure 31) Device structure of a Vertical Cavity Surface Emitting Laser (VCSEL)

Efficiency and high speed at lower powers are of paramount importance for such applications as short-haul data communications. For these applications fibre loss and dispersion are generally not significant factors and so the 830 to 980 nm wavelength is appropriate. Additional attractive characteristics of VCSELs include their circularly shaped, low numerical aperture output beams for easy coupling to fibre or free space optics, their single axial mode spectra (not transverse) for potential wavelength division multiplexing (WDM) schemes, their high power conversion efficiency in the low power range for reduced heating in highly integrated circuits, and their natural vertical emission for array application.

3.3 VCSEL Array

3.3.1 Introduction

These were the optical sources used for the high speed systems demonstrator in my research. The VCSELS were fabricated by ULM Photonics [3.3]. The [1×12] VCSEL array: ULM 850-05TT-A0112B [3.4] was chosen. This was an identical [1×12] array at 250μm pitch configuration, which was used in order to match the photodetector array. These devices were capable of 2.5GHz with a wavelength of 850nm. Due to their

commercial availability, this reduced costs and decreased the likelihood of the project failing due to device problems.

The devices had a threshold current of 1.8mA and work with an operating current of 5mA. Initially, devices with a typical optical output of 1mW at 3mA and thickness 150μm were obtained, but later VCSELs, which had a higher optical power of 2mW at 3mA and thickness 200μm with the same specifications as the earlier version, were also acquired.

HWU received the first set of devices (Power=1mW) from ULM Photonics in March 2004. These included mechanical samples to calibrate the flip chip process. A Second set of higher power VCSELs (Power=2mW) were ordered from the same supplier in April 2004 and they were received in June 2004. These came with the same physical dimensions as the 1mW devices. Also, these components had a higher divergence.

Characteristics:

The VCSEL had the following characteristics as shown in Table 12:

VCSEL array characteristics
Capable of 2.5GHz minimum
1x12 array
1mW/ or 2mW typical optical output at 3mA
850nm emission
AuSn bumping provided
Can survive 330ºC soldering

Table 12) VCSEL array characteristics

Specifications:

The specifications for both the 1mW and 2mW VCSEL arrays are shown in Table 13.

	VCSEL Array (Optical Power = 1mW) at 850nm	**VCSEL Array (Optical Power = 2mW) at 850nm**
Area	3175×475µm	3175×475µm
Thickness	150µm	200µm
Pad diameter	80µm	80µm
AuSn bump height	65µm	65µm
Beam Divergence (Θ)	18^0	28^0
Laser Current	3.0mA	3.0mA
Laser Voltage	2.0V	2.0V
Threshold Current (I_{Th})	1.5mA	1.5mA
Threshold Voltage (V_{Th})	1.8V	1.8V

Table 13) Specifications for 1mW and 2mW [1×12] VCSEL array

Figure 32 shows a schematic diagram of the VCSEL array layout with corresponding key dimensions.

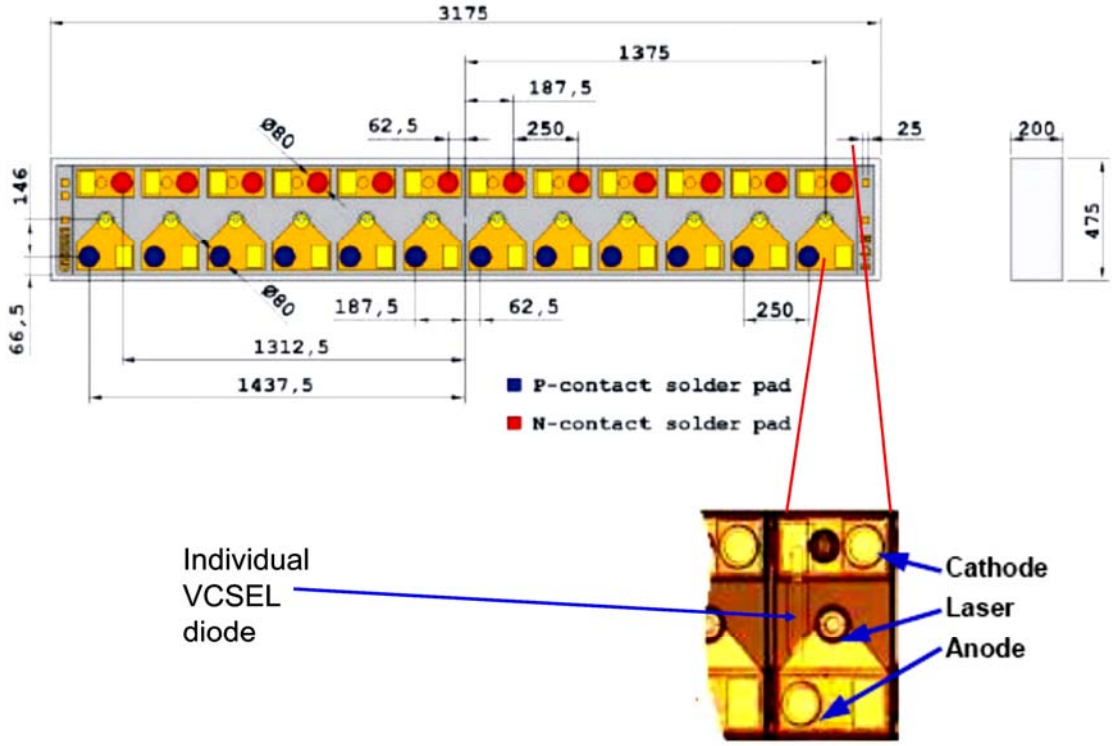

Figure 32) Schematic of [1×12] VCSEL array layout showing key dimensions in microns in microns

Figure 33 shows a SEM picture of the VCSEL array and bumps.

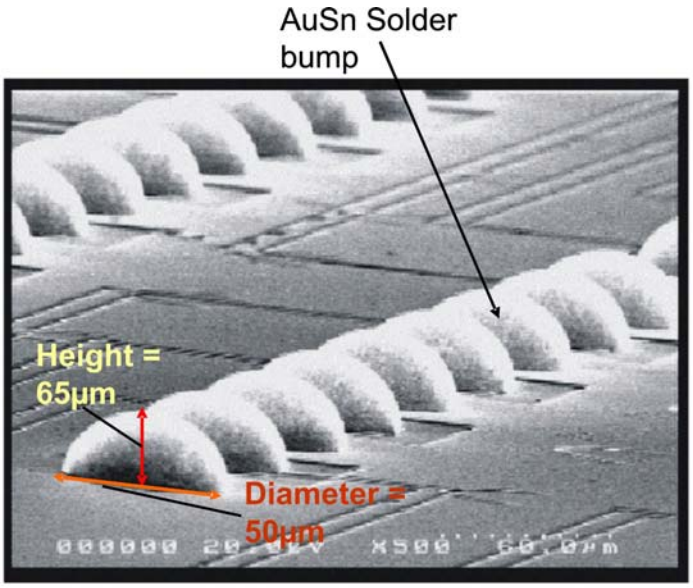

Figure 33) Picture taken from SEM – (1×12) VCSEL array AuSn solder bumps:
Height of solder bump = 65µm, Diameter of solder bump = 50µm.

3.4 Optoelectronic characterisation of VCSELs

3.4.1 Introduction

Firstly, an explanation of how a VCSEL was packaged to enable characterization experiments to be performed is given. Then, Details of the experimental set-up, procedures used, results and analysis will be described.

3.4.2 Wire bonding of VCSEL onto Pin Grid Arrays (PGAs)

There are three types of wire bonding processes: (1) thermocompression, (2) thermosonic and (3) ultrasonic wire bonding. Table 14 illustrates the comparison of the three methods.

Wire bonding method	Type of wire	Force applied to form bond	Type of first bond
Thermocompression	Gold	Heat and Pressure	Ball bond
Thermosonic	Gold	Heat, Pressure and Ultrasonic energy	Ball bond
Ultrasonic	Aluminium Gold	Pressure and Ultrasonic energy	Wedge bond

Table 14) Comparison of three methods of wire bonding

In this method, the thin gold wire is used to make connection between the bonding pads on the chips and the metallization on the substrates. The chip is attached to the substrate face up before the wire bonding process starts. Figure 34 shows the parts of a ball bonding machine that are responsible for leading the wire and executing the bonding process.

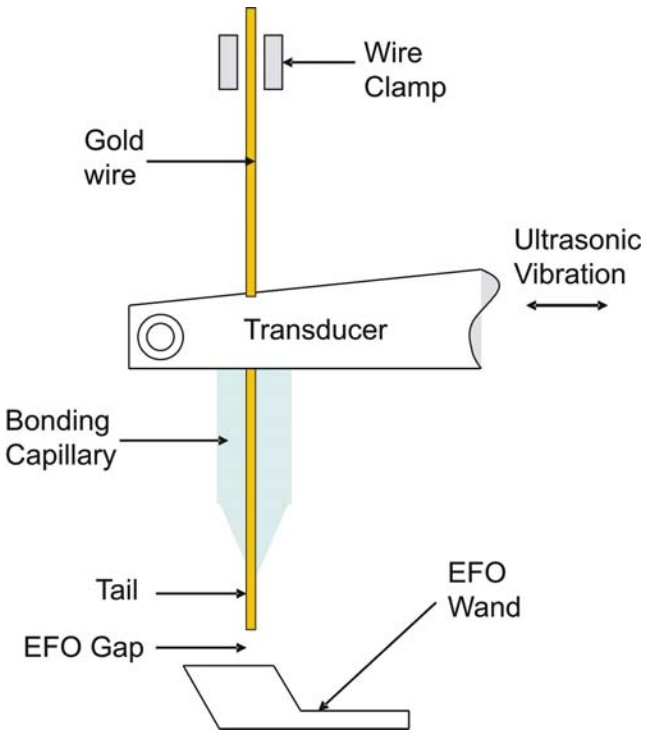

Figure 34) Schematic overview of a bonding head

Wire bonding is a cyclic process. An explanation of the whole bonding cycle can be found in the following references [3.5], [3.6]. The actual bond should look like the one shown in Figure 35. The wire diameter chosen should not exceed one quarter of the pad size and the bond lengths should not be larger than 100 times the wire diameter [3.7] although these values can be exceeded when the bonding parameters are adjusted carefully.

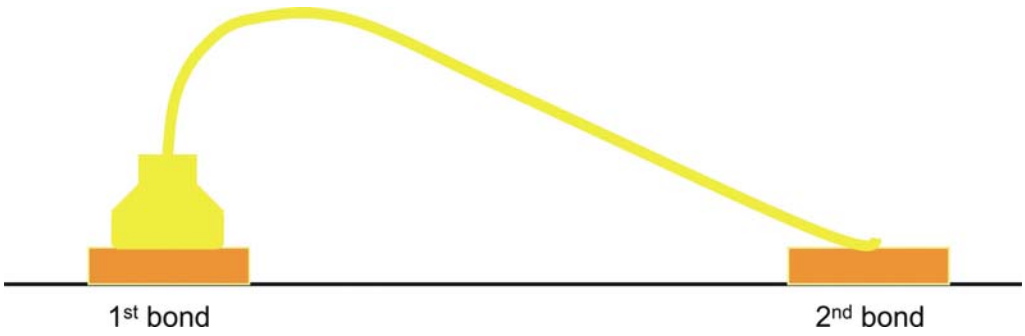

Figure 35) Schematic view of a ball bond

The Kulicke and Soffa (K&S) Model 4124 Thermosonic Ball Bonder [3.8] is a gold wire ball bonder that can be used for bonding services ranging from simple ICs (Integrated Circuits) and discrete devices up to complex hybrids with height variations up to 7500 microns. The K&S bonder was set-up in the MIcroSystems Engineering Centre (MISEC) [3.9] cleanroom at Heriot-Watt University. Figure 36 shows a photograph of the wire bonder.

Figure 36) K&S 4124 Wire Bonder:
This bonder can be adapted for multiple uses, which includes wire bonding, creation of gold studs and coining making it a useful machine for research.

This machine was used for wire bonding and stud bumping work conducted in my research work.

As the cleanliness of the substrate and wire was vital for the whole bonding process, all bonding work took place in the MISEC cleanroom

I did not conduct tests for shear strength and wire pull on the wire bonds. The reason was because none of these testing facilities were available in-house at HWU and project budget constraints did not allow me to perform these tests externally. The gold wire diameters available for my experiments were 25µm and 17.5µm.

Experimental work:

Before the actual bonding could begin, the VCSEL array needed to be attached to the Pin Grid Array (PGA) [3.10]. This was performed using super glue, type 'Loctite Super Glue Precision'. This glue was low cost and readily available in-house, which prevented a delay in the experiments. This was beneficial as the project was on a tight deadline. Unfortunately, at the time I did not consider the potential risk of fumes from cynoacrylates to the optical window on the VCSELs.

The glue was distributed by a very thin needle on the corresponding place of the PGA, and the VCSEL was placed at this position. The results were very good as the array adhered firmly and no deviation from the original position could be observed after leaving for 24 hours.

The area of the PGA was too large to wire bond all the VCSEL diodes. So, the VCSEL needed to be placed on the PGA in a position where most of the VCSEL diodes could be connected. The most optimal arrangement on the PGA for this is shown in Figure 37 being the most promising for the PGA.

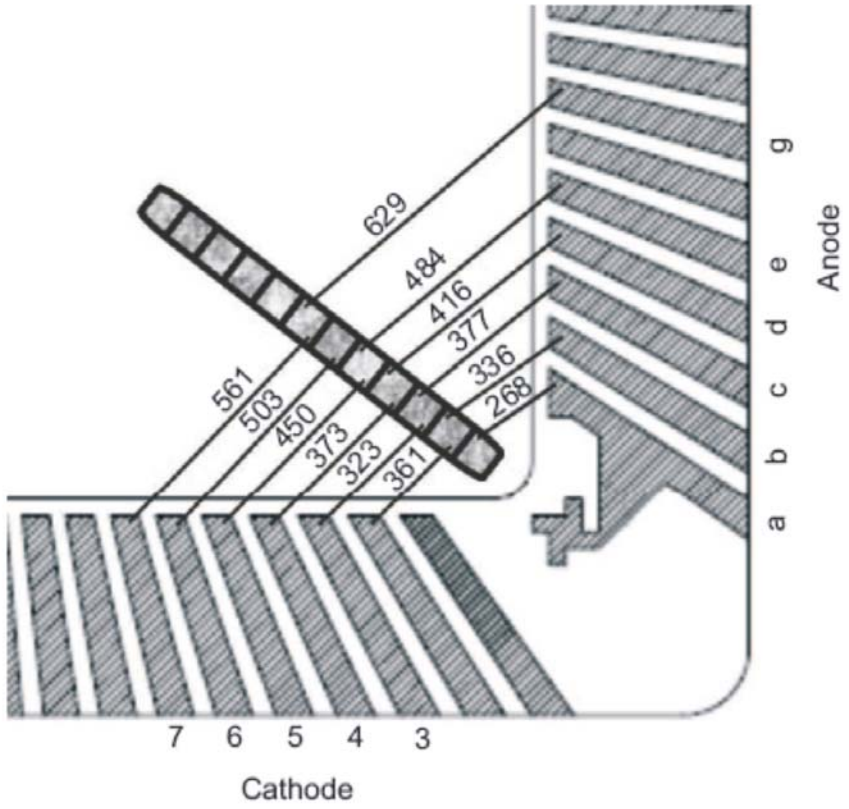

Figure 37) Placement of a VCSEL array onto PGA (Bond lengths in µm)

The array was placed at an approximate angle of 45^0 in the corner section of the PGA and 5 VCSELs diodes were bonded up. Bonds on both sides of the array were of approximately equal length.

A temperature of approximately 150^0C was used to form the bond, so that the force, ultrasonic power and time parameters could be adjusted for optimizing the bond quality.

The machine settings used for the first and second bonds respectively, which produced the most optimum results are shown in Table 15.

	1st Bond	2nd Bond
Force	1.5	3
Time (ms)	5.0	6
Ultrasonic Power (W)	1.5	2

Table 15) Force, time and ultrasonic parameters used for 1st and 2nd bonds

These values are not supposed to be universal values as they are dependent on many other factors within the bonding environment, for example, the material and diameter of the wire used or the quality and state of the capillary. If for instance another wire diameter was used, the bonding parameters will have to be adjusted in order to produce adhering bonds. The parameters may also change depending on the material, thickness and cleanliness of the pad to be bonded.

3.4.3 Characterisation of VCSELs

The following sections of this chapter explains how the packaged VCSEL and a Field Programmable Gate Array (FPGA) was used to develop a demonstrator, which characterised a free space optical interconnect. This system was examined in detail for its characteristics and performance by using eye diagrams.

Field Programmable Gate Array (FPGA) is a microchip that can be reconfigured for many different applications. The FPGA [3.11], [3.12] was first introduced in 1985 by Xilinx [3.13] and since then several other companies have released similar products.

3.4.4 Experimental Work

This experimental work conducted built a system that used an FPGA to drive the Vertical Cavity Surface Emitting Laser (VCSEL). The work also identified and examined the critical phases during assembly.

The first stage was to perform testing on the bonded VCSELs in order to examine their optical and electrical properties. The 1mW VCSEL devices were used for these experiments. For the second stage, an FPGA was used to drive the VCSEL and this demonstrator was tested fully using eye diagrams.

For powering the VCSELs, two different Laser Diode Controllers were used: (1) The Thorlabs ITC502(-IEEE) [3.14], (2) ILX Lightwave LDC-3714B [3.15], [3.16]. Ideally, all measurements taken should have been conducted under constant operating temperature of VCSELs. But, there was no way of controlling the temperature of the Laser diodes because no thermoelectric cooler was available (TEC). To minimise heating effects the VCSELs were switched off and cooled down regularly. For power measurements, a Newport Power Meter Model 1930-C together with a Newport 918-SL silicon detector [3.17] was used with a specification to detect light modulated up to 100kHz. The power output of the VCSELs, which radiated at a wavelength $\lambda = 850nm$, was measured by the power meter and the detector.

Using the equipment, tests were conducted to determine if all VCSELs were bonded up correctly. Results showed that all laser diodes worked fine. Beam profile analysis and measurements of the current-voltage power characteristics, i.e. (I-V-P) were conducted. This will be explained in the next section.

3.4.5 Beam Profile Analysis

In this section, the beam profile analysis of the VCSELs was investigated. This includes measurements of the beam radius, divergence and profile as a whole in order to determine in which region the beam's intensity is at its maximum. By knowing these parameters, it would be possible to build a system with minimum crosstalk between the VCSELs, making it possible to distinguish between the individual data channels.

The Spiricon Beam Analysing Software "LBA-360 PCV.61" [3.18] was used in conjunction with an "AVCAM 405" CCD camera for this Laser beam profile analysis. Also, peripheral component interconnect (PCI) card was used in order to transform the gathered data into a PC readable signal.

For the experimental set-up, an optical bench and components are shown in Figure 38. The white light source, the lens L1 and mirror M1 were solely used to illuminate the laser diode and to assist in focusing of the VCSEL onto the CCD camera. The beam profile was recorded using the CCD camera. The lenses L2 and L3, beam splitter and mirror M2 were aligned while the Laser was turned off, but illuminated by the white light source.

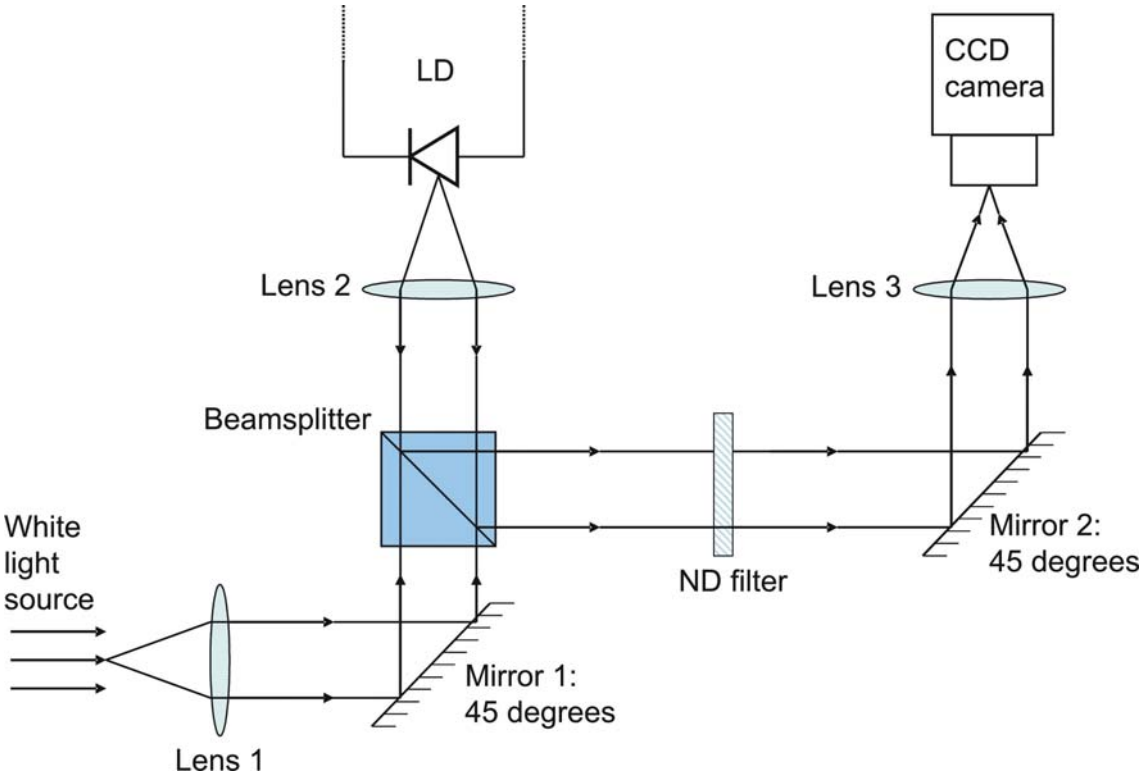

Figure 38) Experimental set-up for the Beam Profile Analysis

The CCD camera was turned on during the alignment process, so that the effects of a change in the experimental set-up could be viewed on the PC. By using this technique, it was possible to achieve a focused image of the VCSEL onto the CCD camera. Once this was completed, the white light source was switched off and the Laser was switched on and a sharp image of the beam profile could be recorded. An ND filter was used to reduce the intensity measured by the camera. Without the filters, the CCD camera became saturated.

One of the main problems during assembly of this set-up was to find a lens L2 with the numerical aperture big enough to record the whole beam profile. Different lenses were tried but in the end one with an NA=0.25 and a magnification of M=10 at 160mm was

found to be the most suitable. Another big problem that could not be solved until the latter part of this project was the issue with the camera saturating too early. As mentioned early, ND filters were used to filter some of the intensity, but this caused a problem. Either the intensity was not filtered enough, which meant the camera was still being saturated, or the intensity was filtered too much, so that only a very small part of the profile could be recorded. In order to solve this issue and finely tune the intensity arriving at the CCD chip, two crossed polarizers were used. Figure 39 shows a typical example of the beam profile recorded by the set-up described.

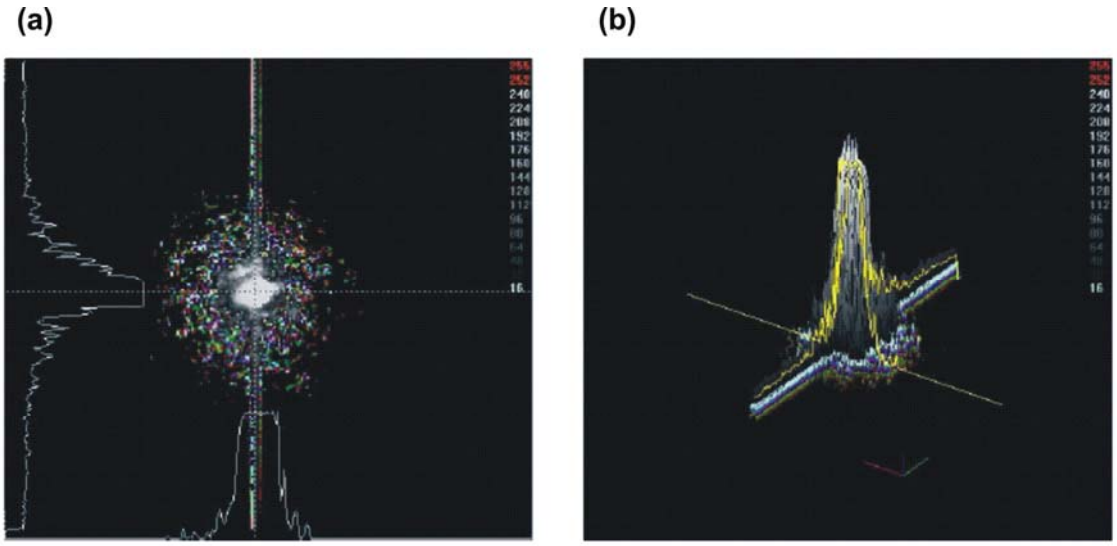

Figure 39) Intensity profile of a VCSEL: (a) 2-dimensional, (b) 3-dimensional

L3 is a photographic lens with an aperture of 5.6, focused at infinity. A ND filter with a transmission coefficient of T≈1.88% has been used to reduce intensity. To further keep the intensity low, a work current of I=1.8mA was chosen, which corresponds to an optical power of P≈0.18mW, as will be shown in the next section.

The saturation of the camera was still clearly recognisable in the left part of Figure 39. The beam profile seems to be Gaussian, although no clear conclusion can be made as the high intensity part of the profile has been cut off, due to saturation.

3.4.6 I-V-P Measurements

The purpose of the I-V-P measurements was to find absolute values for the electrical characteristics given in the VCSEL specifications and to provide the data needed for the construction of the driver. A full measurement of the voltage and optical power between

I=0mA and I=5mA was accomplished, out of which the parameters in question have been computed.

The experimental set-up consisted of the Laser Diode Controller to drive the VCSEL and measure the voltage drop over the VCSEL and the detector connected to the power meter. The detector was placed as close as possible to the Laser diode, leaving a distance $d \approx 2.45 \pm 0.35$cm between the VCSEL and the detector chip. As the transmission coefficient of air is approximately 1 and the distance between the VCSEL and the detector is comparatively small, the absorption of light in air has been neglected. The results of the measurement can be seen on Figure 40.

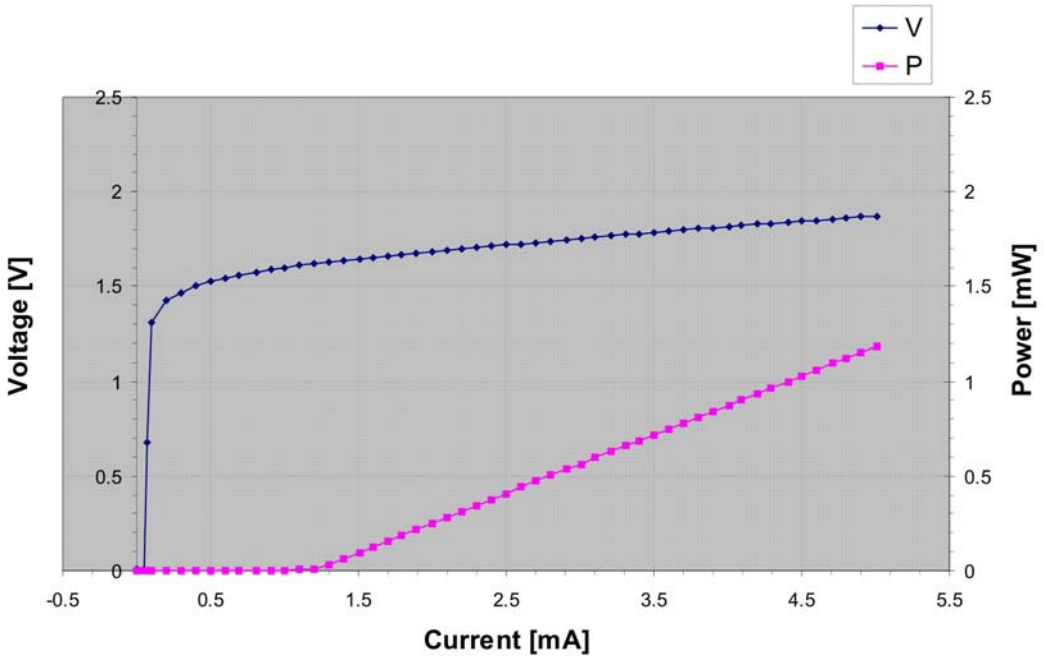

Figure 40) I-V-P characteristics

The electrical characteristics that were computed from Figure 40 are presented in Table 16.

Threshold current	$I_{Th} = 1.189 \pm (6.255 \times 10^{-5})$mA
Threshold voltage	$V_{Th} = 1.628 \pm (2.105 \times 10^{-3})$V
Laser current @ 1mW	$I_{1mW} = 4.408 \pm (6.17 \times 10^{-5})$mA
Laser voltage @ 1mW	$V_{1mW} = 1.84 \pm 3.316 \times 10^{-3}$V
Wallplug efficiency @ 1mW	$\eta w_p = P_{opt}/P_{el} = 12.328 \pm 0.096$ %
Slope efficiency @ 1mW	$\eta s = 0.309 \pm 8.14 \times 10^{-6} WA^{-1}$
Differential series resistance @ 1mW	$R_S = 66.04 \pm 0.602\Omega$

Table 16) Electrical characteristics computed from Figure 40

The error margins are solely due to the statistical variation during the measurement. System errors have not been included, but would surely involve the variation of the values over temperature, a small uncertainty in the measurement of voltage and power appearing as a small uncertainty in providing the exact Laser current. Although the measurements have been conducted in a completely darkened room and the background intensity has been subtracted from the measured signal, some weak variations of the background light may also have affected the results. Of these error sources, the temperature variation surely has the greatest impact on the measurement, but as there was no means to control the Laser temperature, or to specify an absolute value for the variation, this has not been included in the calculations.

A comparison of the computed values with the given specifications for the characteristics show that the calculated values are fully within the specified range so that the measurement was regarded to be correct, i.e. within the limits that were described earlier. The obtained values have been further used during the calculation of the VCSEL driver specifications in section 3.4.8 – Construction of a VCSEL Driver.

3.4.7 Assembly of the System

This section describes how a simple driver was constructed in order to connect the VCSEL to the FPGA. Also, the system was examined for its performance using eye diagrams [3.19].

The FPGA was assembled on a XILINX Spartan-3 board [3.20], supporting speeds up to 333MHz. While the maximum speed of the VCSELs was specified as 5Gbps. The maximum speed theoretically achievable by this system was limited by the detector and amplifier, which were used to pick up the signal.

The software used could drive the VCSELs at various speeds up to 20MHz, which was more than adequate to highlight the limitations of the detector used.

3.4.8 Construction of a VCSEL Driver

In order to drive the Laser with the FPGA without damaging the VCSEL, a driver had to be built that limits the current and voltage drop over the VCSEL. To achieve this, the simple driver layout shown in Figure 41 was soldered up to a breadboard.

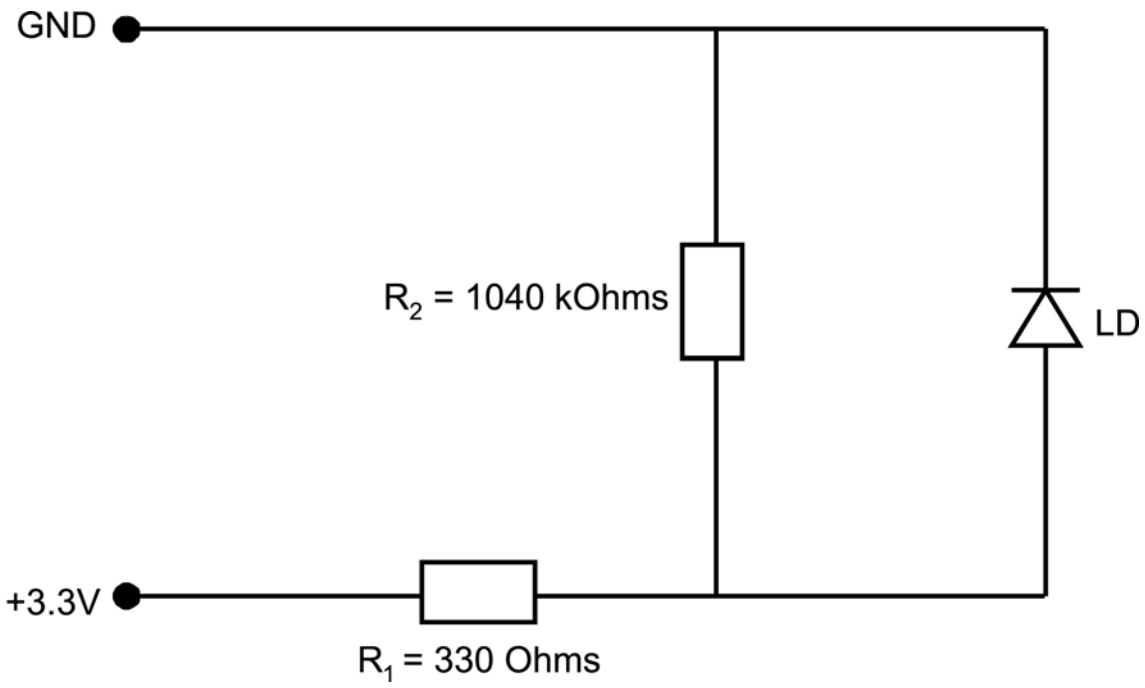

Figure 41) Driver circuit

The resistance R_1 was connected in series with the Laser diode and used to limit the current and voltage drop over the VCSEL. It is mainly responsible for the adjustment of the right working point of the Laser. As there is a current pulse flowing backwards through the system when the power supply (in this case the FPGA) is turned off, the resistance R_2 is connected parallel to the VCSEL. Its purpose was to prevent the current flowing in the reverse direction through the Laser diode, which could seriously damage the diode itself. So, it was chosen to be much smaller than the resistance of diode in the

blocking direction. This was to enable the backward current to flow through the resistor instead of the Laser diode. At the same time, it needed to be far greater than the resistance of the diode in its forward direction. This was so that almost all the current provided by the FPGA flows through the VCSEL instead of the resistor during normal operation.

A resistance of $R_2 \approx 1M\Omega$ was chosen. The voltage supplied by the FPGA is V_{FPGA}=3.3 V at a maximum current of I_{max}=6mA. The working point of the Laser was chosen to be at I_L=4.41mA and V_L=1.838V, which corresponds to a Laser power of P≈1mW. Therefore, because R_2 is far bigger than the ohmic resistance for the VCSEL at the working point:

$$R_L = \frac{V_L}{I_L} \approx 416.78\,\Omega \tag{3.1}$$

We can approximate the current flowing through R_2 to be zero. Using these values and approximations, the value of R_1 leading to the desired working point can be computed as follows. The current flowing through the circuit is:

$$I = \frac{V_{FPGA}}{R_1 + R_{tot}} = I_L \tag{3.2}$$

Where:

$$R_{tot} = \left(\frac{1}{R_L} + \frac{1}{R_2} \right)^{-1} \approx 416.61\,\Omega \tag{3.3}$$

is the resulting ohmic resistance of R_2 and the VCSEL connected in parallel. From Equation 3.18, R_1 is calculated as follows:

$$R_1 = \frac{V_{FPGA} - IR_{tot}}{I} \approx 331.69\Omega \tag{3.4}$$

As there were not any resistances to be found at the exact values calculated from Equations 3.2, 3.3, 3.4, resistances of R_1=330Ω and R_2=1.04MΩ have been used.

3.4.9 Measurements of Eye Diagrams

In this part of the project the VCSEL was connected to the FPGA and the system was examined using eye diagrams. Eye diagrams are a very powerful tool, which examines and characterizes the behaviour of a digital system [3.21]. A properly constructed eye diagram should contain all possible bit sequences from simple 101s and 010s through to long sequences of 1s and 0s. Figure 42 shows how an eye diagram is constructed. The eye diagram will not show problems that arise due to protocol or logic, but will show how the signal becomes distorted through the system. An eye diagram may not show why a channel fails.

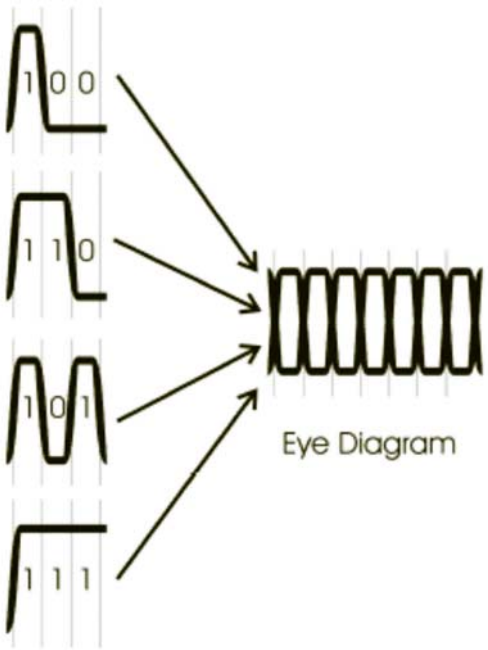

Figure 42) Construction of an eye diagram:
The input signal is triggered to sample at the same rate as the clock and will deliver to the screen a pattern starting at a rising or falling edge. These patterns may consist of any combination of 1s and 0s as supplied by the pseudo random generator. When overlaid in this fashion, they form an eye diagram. The more open the eye is, the better the signal quality is.

To summarise, eye diagrams give an instant insight into how the single bits are transmitted and if they are still recognizable for the receiver or not. A detailed examination of the eye diagram can provide information about further transmission

characteristics, for example; signal-to-noise ratio, jitter, transition times or signal overshoot. See Figure 43.

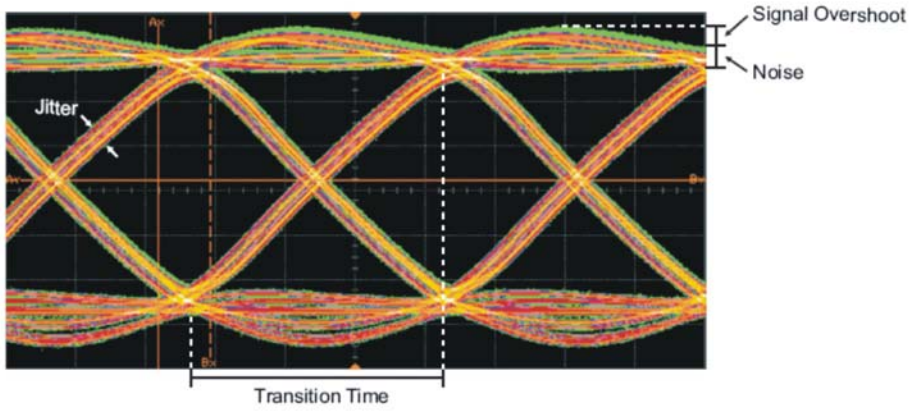

Figure 43) Picture showing an example of an Eye diagram:
Showing jitter, transition time and signal overshoot [3.22], [3.23].

For the measurements of eye diagrams, an Agilent Infinium 2.25GHz 8GSa/s digital oscilloscope was used. The detector used to collect the Laser signal consisted of a photodiode and an amplifier circuit, which will be described in further detail in the next section. The set-up constructed to conduct the following experiments is shown in Figure 44.

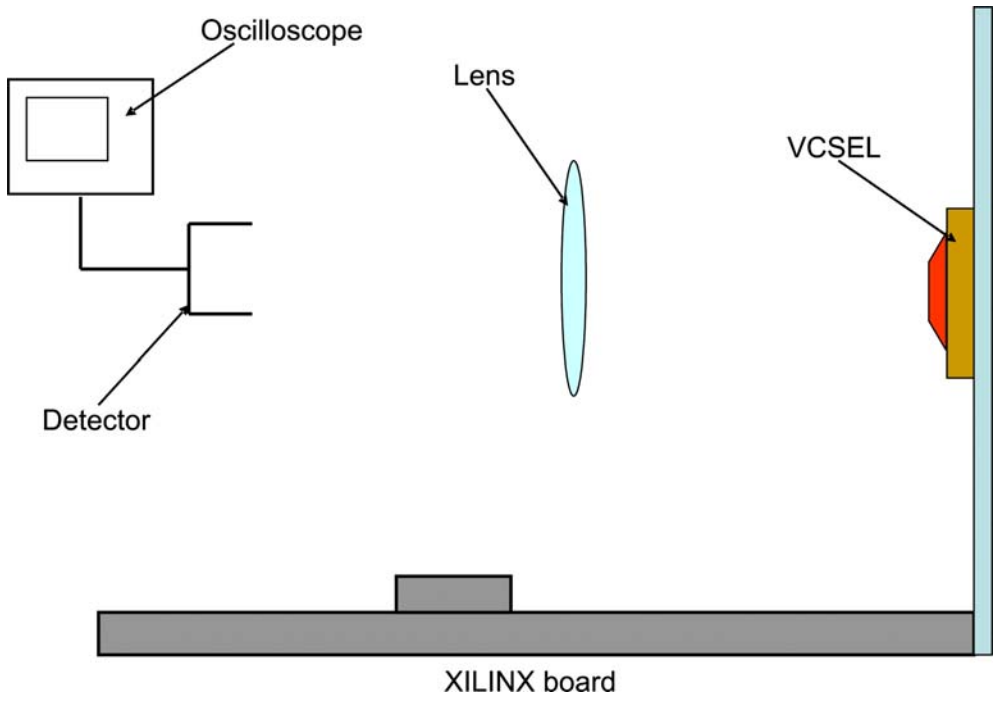

Figure 44) Full system set-up

Since the Laser strongly saturates the receiver, the lens has been positioned in a way so that the beam was slightly out of focus when incident onto the detector. With this arrangement, it was possible to tune the intensity recorded by the photodiode.

In order to distinguish the effects arising from the driver and the results ascribed to the behaviour of the VCSEL, eye diagrams were recorded at two different points of the set-up. They were then compared with the measurements received directly from the board. The first readings were taken directly at the position of the VCSEL within the driver circuit as explained in the next section. From this, it was possible to determine the behaviour of the driver at different speeds. The second readings were taken from the Laser signal recorded by the receiver. If the receiver was fast enough it would have been possible to examine the behaviour of the VCSEL itself at different speeds. However, the receiver was too slow to cope with the speeds that could be achieved by the VCSEL and FPGA itself.

3.4.10 Results for the Driver Circuit

At first, eye diagrams were recorded after the signal passed through the driver circuit, but before it reached the Laser diode. Figure 45 shows the set-up for recording eye diagrams of the driver circuit. This has been done in order to examine the transmission behaviour of the driver circuit. With these measurements it is later possible to distinguish between the effects arising from the driver circuit and the ones arising from the VCSEL or the amplifier.

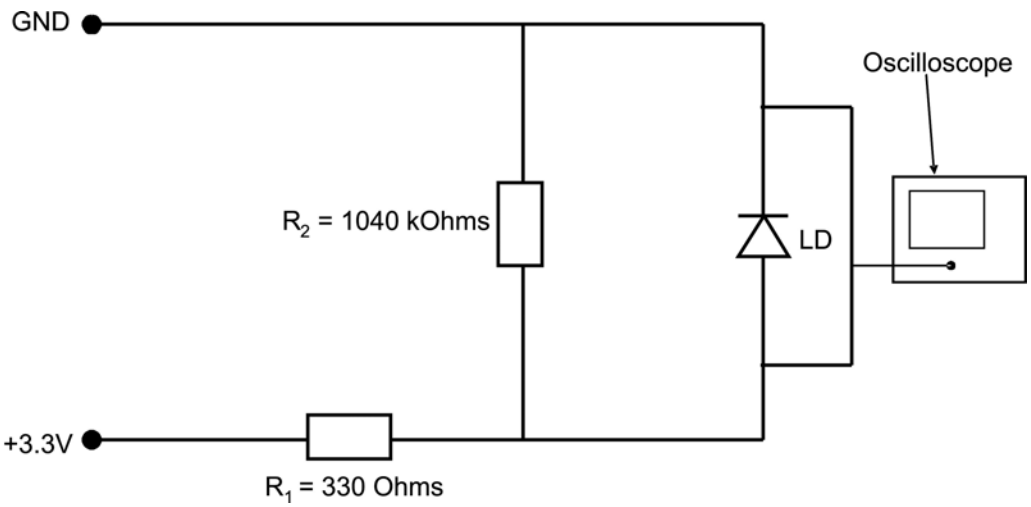

Figure 45) Set-up to record eye diagrams of the driver circuit

Figure 46 shows the results in direct comparison to eye diagrams taken from the board. The upper diagrams in each record show the output of the FPGA, and the lower ones show the signal after it passed through the driver circuit.

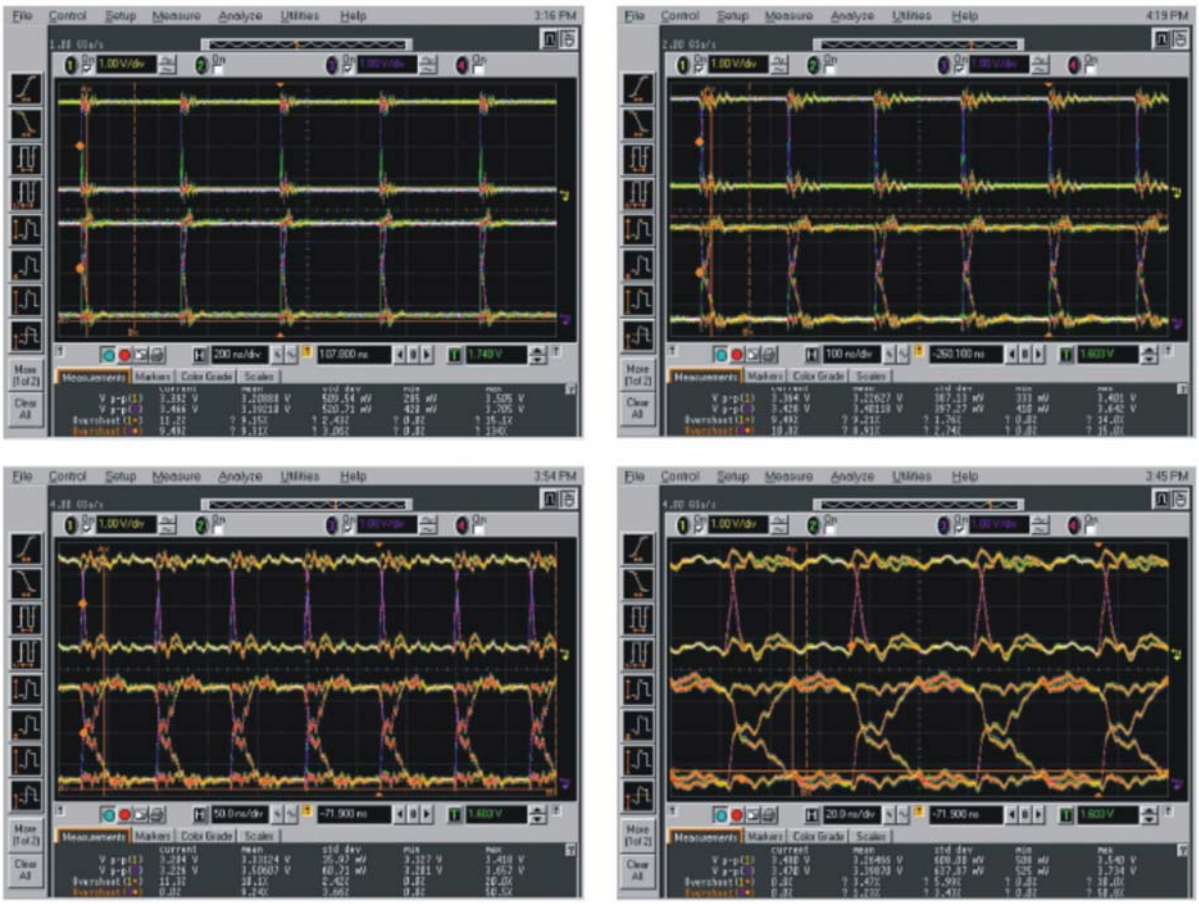

Figure 46) Eye diagrams of the driver circuit at different speeds:
(i) Upper left: 2.5MHz, (ii) Upper right: 5.7MHz, (iii) Lower left: 13.3MHz, (iv) Lower right: 20MHz.

Eye diagrams have been recorded at four different speeds, i.e. 2.5MHz, 5.7MHz, 13.3MHz and 20MHz. The signal of the FPGA is still nearly undistorted at 20MHz. This corresponds to the expected results, as the board is capable of supporting speeds up to 333MHz. At higher speeds, especially 13.3MHz and 20MHz, a clear distortion can be seen in the signal after it passes through the driver circuit. But, the eyes are still opened wide enough in order to clearly distinguish the two bit levels.

3.4.11 Results for the Full System

For the final part of this experimental work, eye diagrams of the full system were recorded using the set-up shown in Figure 44. The results for some lower transmission rates are shown in Figure 47.

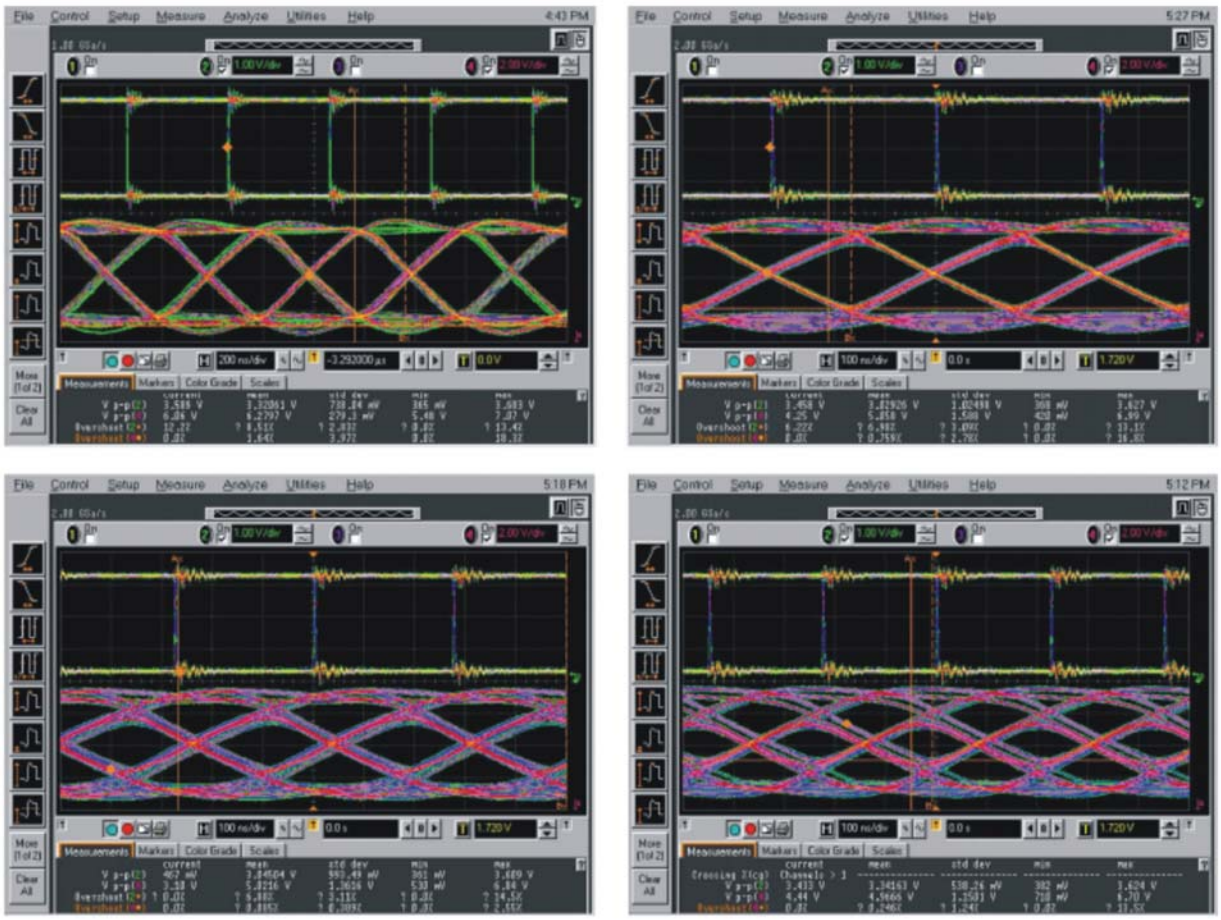

Figure 47) Eye diagrams of the Laser signal at different speeds:
(i) Upper left: 2.5MHz, (ii) Upper right: 3.07MHZ, (iii) Lower left: 3.6MHz, (iv) Lower right: 4.44MHz.

Again the eye diagrams were recorded at four different speeds, i.e. 2.5MHz, 3.07MHz, 3.6MHz, and 4.44MHz, and directly compared to the FPGA output. For the lower speeds of 2.5MHz and 3.07MHz, the eyes are still recognizable, although they were far more closed than the ones recorded for the driver circuit alone. At 3.6MHz, the eyes clearly began to close in even further. This made it extremely difficult to distinguish between the two signal levels.

At 4.4MHz, the form of the classical eye had almost completely disappeared and the differentiation between '0-level' and '1-level' was unclear, if not impossible to achieve. The result for a transmission rate of 20 MHz is shown in Figure 48.

Figure 48) Eye diagram of the Laser signal at 20 MHz

The eye pattern could not be observed and the signal had become an indistinguishable noise. As these results were not measured for the driver circuit itself, and the VCSEL was specified to work up-to $5Gbs^{-1}$, one reason for the early breakdown of the system could be related to the receiver used. This was confirmed by looking at the amplifier circuit used for the receiver. It consisted of a preamplifier with a gain bandwidth product (GBP) of 4MHz [3.24] and second amplifier with a GBP=50 MHz [3.25]. From this, it was identified that the pre-amplifier was far too slow for the desired application. A faster amplifier circuit would be required if the full potential of the system was to be investigated.

3.4.12 Summary

As a result of this experimental work, it was possible to create the system with the means available. But, there were still some points remaining to assess in order to improve system design and performance. By using a PGA with the right dimensions for the VCSEL array, it would be possible to bond up all of the VCSEL diodes. This would enable the maximum use of the data channels available, i.e. 12 outputs, and fully exploit the potential of the VCSEL array. In order to stabilize the performance of the VCSEL, it was crucial to find a way to control its operating temperature. This would enable wavelength tuning over temperature, variation of the beam divergence and other

performance degrading effects of the Laser to be minimised. This in turn would maintain good control over the operation of the Laser.

The use of another CCD camera for the Laser beam analysis would allow the full exploitation of the potential of the beam analysing software. Then, numerical results could be obtained for the examined Laser parameters. This would lead to a better system design, especially when there is more than VCSEL involved in the data transmission. A more in-depth investigation of the designed driver circuit will definitely be necessary in order to guarantee a controlled operation of the Laser diode. A final point would be that another amplifying circuit would be required in order to examine the full potential of the VCSEL, FPGA and the driver circuit. The preamplifier used would have to be replaced by another one with a higher gain bandwidth product or alternatively the construction of a completely new driver circuit is required in order to address this issue.

Although a number of improvements were necessary, the main goal of this experimental work was accomplished. It was shown that an FPGA could be provided with an optical interconnect by using a VCSEL array and developing a corresponding system solely with in-house facilities from the University. This opens numerous possibilities for further research of this exciting future technology.

3.5 Mixed Signal Chips (MSCs)

3.5.1 Introduction

This chapter describes details of the mixed signal chips (MSCs) used in this project. These devices were designed and modelled by Supélec [3.26].

Firstly an explanation of the chip layout, specifications and pin-out will be given. Then, details of the design will be explained. Finally, manufacturing and testing particulars of the component is described.

The function of this chip was to provide a test bed to assess the performances of the whole link: electrical – optical – electrical. The chips consisted of two parts: (1) an analogue section, which was devoted to driving VCSELs and to amplifying output of

photodetectors and (2) a digital one which synchronizes data to and from the processor (processor interface chip) or realizes a memory interface chip, i.e. processor and memory interfaces.

3.5.2 Chip Layout, Specifications and Pin-out

The aims of the chip were first to verify the design of the analogue photocurrent amplifiers and VCSEL drivers and second to test the technology and the design flow in a simple case. This chip needed to be versatile, so it could be used as an emitter or a receiver. In both cases, it was designed to be flip chip bonded onto multi-chip module (MCM).

The device was composed of a digital part (processor and memory interfaces), i.e. Heart, and an analogue part, i.e. VCSEL drivers and photocurrent amplifiers. This is shown in Figure 49.

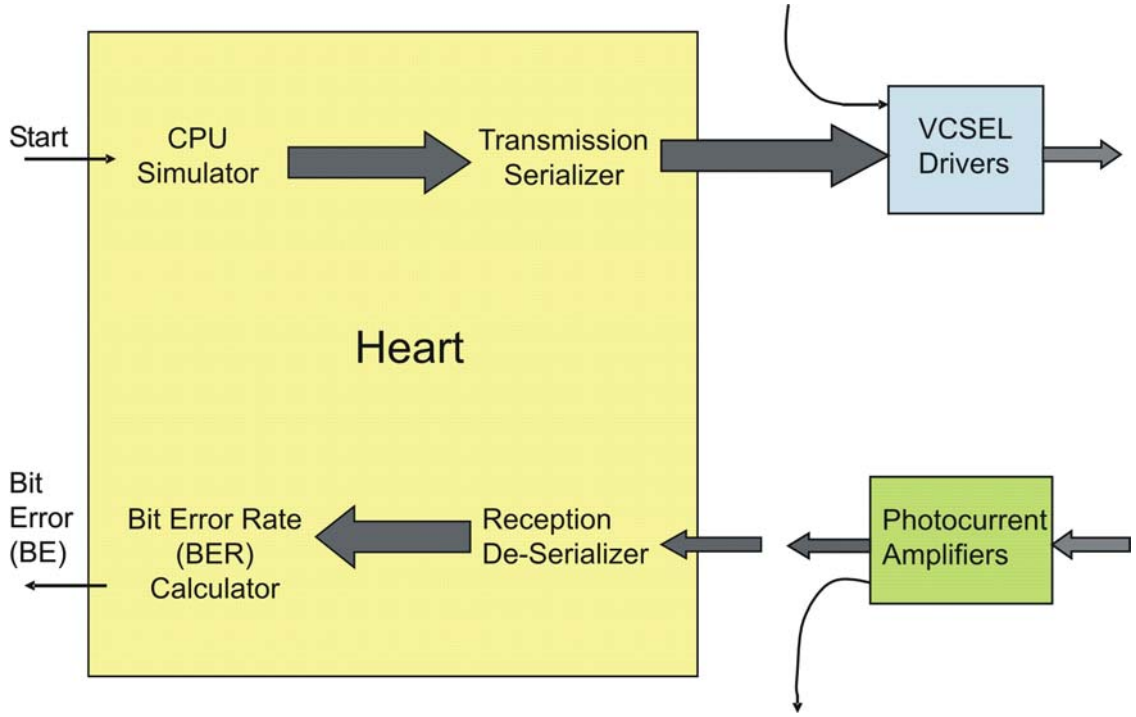

Figure 49) Schematic showing the Test chip synoptic

The chip pin-out could run as a transmitter, as a receiver or in an autonomous package, i.e. wire bonded onto a PGA. So, only one circuit was designed. This consisted of 3 pad rings, i.e. (1) Transmitter, (2) Receiver and (3) PGA bonding. This is shown in Figure 50.

The total number of transmitter (85) and receiver (83) pins on the chip were 168. Reference [3.27], pp. 16-19, provides details of the functionality of each pin for transmitter and receiver pin-out.

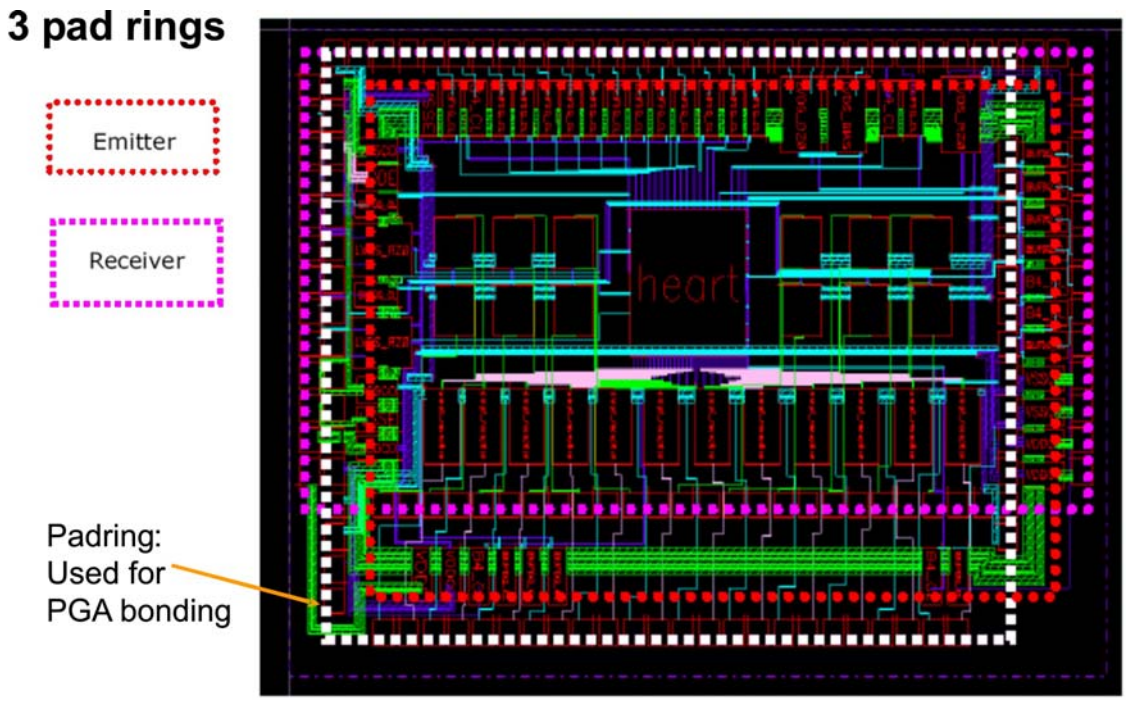

Figure 50) Chip layout

The thickness of the Test chip is 500µm and size is 3.55×2.50mm, area of 8.87mm^2. The bonding pads are made with top metal layer. Table 17 shows the specifications of the test chip bonding pads.

	Test chip bonding pad
Pad size (µm)	100
Metallization	Ti/TiN (glue layer) - 0.02-0.08µm AlCu alloy - 2µm Ti/TiN (AR coating) - 0.03µm
Number of Pads	168
Pitch	125µm (For digital and analogue pads)

Table 17) Specifications of test chip bonding pads

Full details of chip design specifications, layout, pin-out and simulations can be found in [3.27].

3.5.3 Technology Choice, Design and Modelling

Technology Choice:

The major factors which drove the technology choice were: (1) Achievable performances of analogue interfaces, i.e. VCSEL drivers and Photodetector amplifiers, (2) Power supply voltage and (3) Speed of logic.

The criteria used for choosing the technology for designing the silicon chips were: (1) required performances ~ 1Gbit/s, availability of the technology in Europractice and availability of CAD (Computer Aided Design) tools under Cadence [3.28] environment. This was compulsory because of its availability among the HOLMS consortium.

Design Kits for Photodiode Amplifier and VCSEL Driver:

As mentioned earlier, these devices, which incorporates the photodiode amplifier and VCSEL driver were designed and modelled by Supélec [3.29]. They used Austria

Microsystems 0.35um SiGe (Digital design kit) and 0.35um SiGe BiCMOS (Analogue design kit) technologies [3.30].

The analogue design kit did not provide any access to place and route tools for digital standard cell. This meant the two kits were not fully compatible since there were five routing layers in the digital CMOS kit and only four in the BiCMOS one. Consequently, the digital part was designed using the CMOS digital kit as it was too complex to be done without place and route tools. The analogue part was designed using the BiCMOS design kit with the place and route being performed manually.

The final layout of the mixed signal chip was completely manually, since no automatic place and route was available. This increased the risk of errors and was time consuming.

The uncertainty of this approach was to know if the two processes (CMOS and BiCMOS SiGe) were fully compatible and if it were possible to design a mixed signal chip using the two design kits. Europractice was consulted on this issue and they responded stating that there was no guarantee that this would work. They concluded that there was a high risk involved in doing this. Unfortunately at the time (2002), no alternative existed. So, the digital and analogue designs were completed using these processes.

3.5.4 Fabrication and testing of chips

In Mid-June 2003, the MSC design was completed and sent to IMEC, Belgium [3.30] for fabrication. They used the low cost Multi Project Wafer (MPW) run by Europractice [3.31]. This work was completed before I started my PhD research. This meant I did not have any input or involvement into the design of the chip. HWU received the fabricated devices from Supélec in December 2003. A total of 118 chips were provided.

Supélec stated that they conducted successful testing of the analogue and digital parts of the chips in November 2003. This was prior to delivery of devices to HWU. These results are documented in the reference [3.29]. To validate this data, I did not have (1) Required testing equipment and (2) The budget to purchase kit; in order to conduct these verification tests. Considering, these circumstances, which were out of my control, I was to required to rely on the validation results provided by Supélec.

3.6 Conclusion

In this chapter, a simple demonstrator was successfully constructed, which investigated reconfigurable optoelectronic systems using FPGA technology. Optoelectronic testing of the VCSEL was successfully conducted, which provided good beam profile analysis and I-V-P measurements of the VCSEL array. This was then implemented into the constructed demonstrator system, where eye diagrams examined the systems performance and characteristics of the full system and showed positive results.

The final sections of this chapter described the mixed signal chips (MSCs) used in this project.

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Chapter 4

Optoelectronic Packaging (I)

4.1 Introduction

In this chapter, an explanation of flip chip bonding techniques was given. Flip chip bonding was used in the experimental work carried out on packaging the components described in chapter 2 and chapter 3.

The outline of this chapter is as follows. In sections 4.2, 4.3 and 4.4, flip chip bonding technologies are explained. Finally, in section 4.5, the optoelectronic packaging experiments performed is discussed.

4.2 Bonding Techniques

The most common bonding technologies are wire bonding and flip chip bonding [4.1]-[4.5]. Conventional wire-bonding has been used for parallel optical data link applications, but is limited in its applicability to chips with a relatively small number of channels. Typically this would involve wire bonding both optoelectronic devices and electronic interface circuits to an intermediate substrate such as a ceramic multi-chip module.

Flip-chip bonding is a more promising technique for hybrid integration. This is a derivative of IBM's C4 (controlled-collapse chip connections) technology [4.6], [4.7] that was developed in the 1960s. Flip-chip bonding will be described in detail in the following sections. This was the main technique used for the packaging work I conducted.

4.3 Background on Flip Chip Bonding

4.3.1 Introduction

Flip chip microelectronic assembly is the direct electrical connection of face-down ("flipped") electronic components onto substrates, circuit boards, or carriers, by means

of conductive bumps on the chip bond pads or with any kind of interconnect materials and methods, e.g. fluxless solder bumps, tape-automated bonding (TAB), wire interconnects, conductive polymers, anisotropic conductive adhesives, metallurgy bumps, compliant bumps, and pressure contacts. In contrast, wire bonding, the older technology, uses face-up chips with a wire connection to each pad.

Flip chip components are predominantly semiconductor devices; however, components such as passive filters, detector arrays, and micro-electro-mechanical-devices (MEMS) are also beginning to be used in flip chip form.

The increase in flip chip packaging results both from flip chip's advantages in size, performance, flexibility, reliability, and cost over other packaging methods and from the widening availability of flip chip materials, equipment, and services.

The disadvantages of flip chip bonding are that it requires additional wafer processing to form solder bumps, which limits the available chips for processing. Also flip chip is difficult to inspect, since the devices are attached face down. In addition, this bonding process has high costs for low volume production and low I/O packaging count.

Figure 51 shows a diagram of solder bump flip chip bonding.

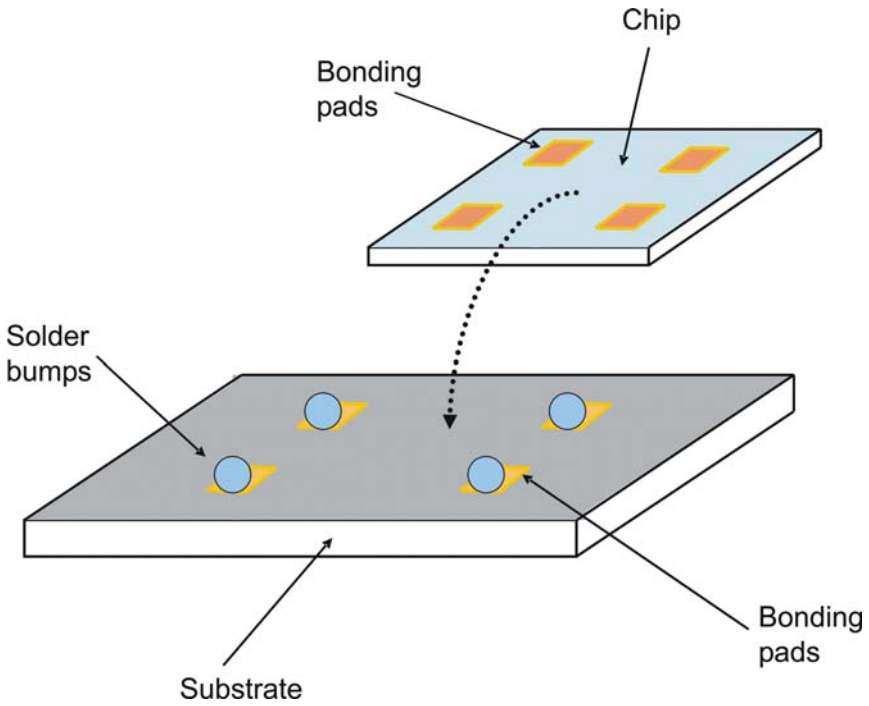

Figure 51) Example of Solder bump flip-chip bonding:
This technique requires the substrate and chip to have bonding pads of the same pitch and extent. Given a minimum pitch these bonding pads can cover the entire chip surface as an array. This will create much shorter connection than a wire bond with much less inductance and capacitance.

For high performance requirements, the electrical characteristics of a solder bump versus a wire bond packaging approach are critical. The inductance of a solder bump is less than 10% of a wire bond. This is especially significant in high speed and high frequency applications where the incorrect choice of packaging can seriously degrade signal integrity. Table 18 [4.8] illustrates best and worst case signal propagation characteristics for ICs packaged in cavity down wire-bonded pin grid arrays (PGAs) versus flip chip on ball grid array (BGA) packages.

	Worst case		Best case	
	Wire bond	Flip chip	Wire bond	Flip chip
Inductance	19.6nH	7.9nH	5.6nH	0.3nH
Capacitance	15.0pF	6.2pF	9.1pF	2.5pF
Resistance	21Ω	2.1Ω	20.1Ω	1.7Ω
Propagation delay	946psec	243psec	508psec	51psec

Table 18) Data comparing flip chip to wire bonding techniques [4.8]

4.3.2 Flip chip assembly process

The flip chip assembly process is made up of three stages:

1. Bumping the die or wafer.

2. Attaching the bumped die to the board or substrate, i.e. flip chip bonding.

3. Encapsulation or Underfill, i.e. filling the remaining space under the die with an electrically non-conductive material.

This section explains some key issues affecting assembly of solder flip chip interconnection systems.

During flip chip bonding, the bumped die is first aligned and attached to the bond pads on the substrate using a tacky flux. Then the module is heated, so that the solder melts and forms a metallurgical bond with the bond pad. The shape and geometry of the solder interconnect is determined by the process conditions.

The reflow [4.9], [4.10] is performed while the solder joint is physically deformed in its molten state. Although this process can be slow, it can produce interconnects which are more reliable. The sequence of tasks is as follows: The chip, typically at a temperature below the melting point, is aligned to the substrate and placed on the bond pad. The temperature is then raised to the peak temperature. The bumps melt and wet the substrate bond pads. The chip is then pulled away from the substrate, while the solder is

molten, and then the entire system is cooled. This enables larger stand-off gaps between the die and substrate. Such solder joints have been produced using centrifugal reflow [4.11] or self-stretching technology [4.12], and by stretching a molten solder joint in a high accuracy flip chip bonder [4.13].

Following the flip chip bonding process, the flux residues are cleaned. Then the module is underfilled [4.14]. This is shown in Figure 52. The encapsulant is used to improve reliability by reducing stress. In this step, the gap between the chip and the substrate is filled with an epoxy. Most underfills require at least a 25μm gap between the chip and the substrate. Smaller gaps can result in segregation of fillers and non-uniform chip coverage. Underfill or encapsulation provides two functions. First, it protects the chip and interconnects during subsequent processes. A second more important reason is that it improves the reliability of the interconnect system.

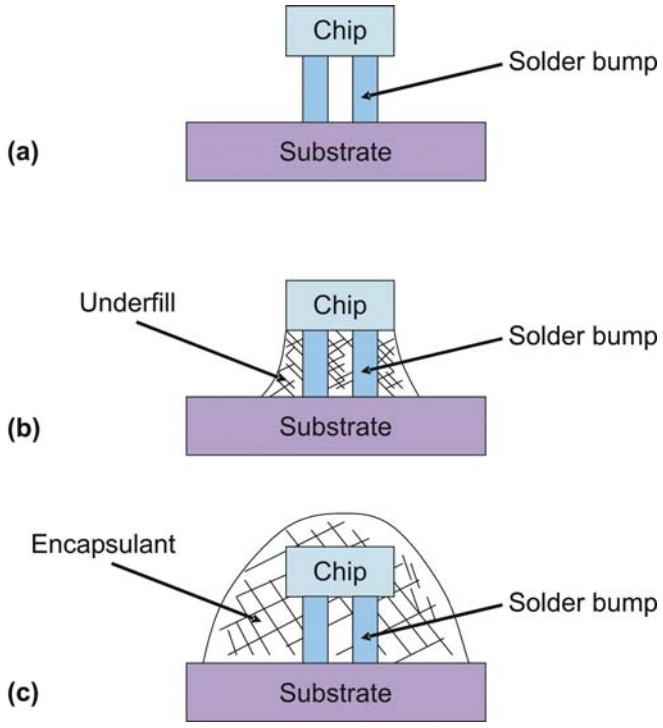

Figure 52) Schematic of a solder flip chip interconnect system: (a) Without underfill, (b) With underfill, (c) Encapsulated.

4.3.3 Under Bump Metallisation (UBM)

The most important task in wafer bumping is to put down the under bump metallurgy (UBM) on aluminium (Al) bonding pads. The UBM defines the region of terminal metallurgy on the top surface of the chip that is wetted by the solder. This is deposited

by either electroplating [4.15]-[4.17] or evaporating methods [4.2]. The UBM consists of three layers: adhesion and/or barrier layer, wetting layer and oxidation barrier layer. This is shown in Figure 53. The adhesion and/or barrier layer consists of a chromium layer (~0.15µm) and a phased 50/50 Cr/Cu layer (~0.15µm). The function of this layer is to form a strong bond with the Al pad and with the passivation layer. See Figure 53. The wetting layer is made of copper (Cu) (~1µm), which must remain at least partially intact through all the remaining reflow processes, e.g. chip level interconnect, chip carrier interconnect, PCB assembly and rework. The oxidation barrier layer (~0.15µm) is made of gold (Au), which protects the Cu from oxidation.

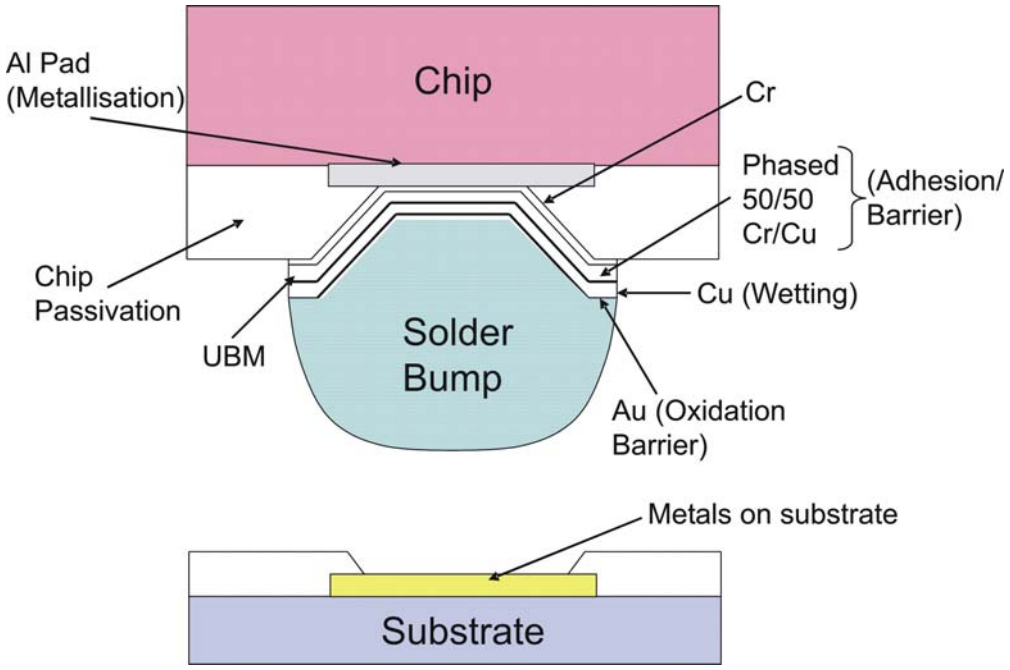

Figure 53) Schematic showing Under Bump Metallisation (UBM) structure:
Consists of three layers: adhesion/or barrier layer, wetting layer and oxidation barrier layer.

Table 19 summarises the features of each solder deposition process (apart from gold stud bumping) in terms of the UBM employed.

UBM	Evaporated	Plating (Two Processes)*	Solder paste	Electroless Nickel
Adhesion Layer	Cr	1. TiW or 2. Cr/Cu	Al	Ni

Solder Diffusion Layer	Phased Cr-Cu	1. Cu stud/mini-bump 2. Cr-Cu	Ni	Ni
Solder Wettable Layer	Cu	1. Cu 2. Cu	Cu	Au
Oxide Prevention	Au	Au	Cu	Au
Used with Probed Wafers	No	No	Yes	Mixed

**** Two plating processes are represented (1) one that uses the Cu mini-bump and (2) one that does not.***

Table 19) UBM Deposition Systems

After solder bumping, the wafer is sawn into bumped die. The bumped dies are then placed on the substrate pads, and the assembly is heated to make a solder connection.

Several varieties of flip chip assembly, including solder bump, plated bump, gold stud bump, and adhesive bump suit flip chip to a wide range of applications. In the next section each of the flip chip processes will be discussed in more detail.

4.3.4 Bump Materials

The bump serves several functions in the flip chip assembly. Electrically, the bump provides the conductive path from chip to substrate. The bump also provides a thermally conductive path to carry heat from the chip to the substrate. In addition, the bump provides part of the mechanical mounting of the die to the substrate. Finally, the bump provides a spacer, preventing electrical contact between the chip and substrate conductors, and acting as a short lead to relieve mechanical strain between board and substrate.

The melting point of the solder, the bumping process capability, manufacturability, and reliability are some of the major factors which influence the choice of a solder composition. The melting point of the solder is indicative of the maximum process temperatures encountered by the assembly elements. In order to preserve the micro-

structural and geometrical stability of the solder joint, the flip chip bonded module must be retained at temperatures well below its melting point.

Solder for flip chip applications is lead-free. Lead-free solders include those based on indium (In) and alloys with bismuth (Bi), tin (Sn) and silver (Ag). The composition of the bump materials is influenced by the bumping process compatibility. For example, plating processes can be used to deposit a variety of metals including Sn, Ag, In and Bi. However, increasing the number of elements in a plated bump increases the number of process steps. Therefore, it is more beneficial to restrict solder compositions to binary systems.

Bond pad metallization is another factor, which influences bump composition selection, i.e. In-based solders are preferred for gold bond pads because of the low dissolution rates of gold in indium.

Table 20 shows a list of some solders that have been used for optoelectronic hybridisation and some of their properties. A eutectic bond is formed in two of the cases. This is a solder in which the alloy formed has a lower melting point than either of the 2 materials on their own. This is only achieved for a certain ratio.

Solder Alloy	**Melt T [^{0}C]**	**E**	**α**	**γ**	**Relative fatigue life**	**Relative creep rate**
80 Au/20 Sn *Eutectic*	281	68	14	0.40	Poor	N/A
100 In	157	7	31	0.46	20	Soft
97 Sn/3 Cu	227	41	19	0.33	5	0.01

E: Young's Modulus [Gpa], α: CTE (ppm/^{0} C) coefficient of thermal expansion, γ: Poisson ratio

Table 20) Properties of solder materials used for optoelectronic hybridisation

Au/Sn [4.18]-[4.20] has no creep, but is brittle. Also, it is a fluxless technology. This is the solder of choice for optoelectronics and was the bumping technology used to package the VCSELs. Indium (In) [4.21], [4.22] is good for prototyping but is high cost.

It also has a large creep rate, poor corrosion resistance and a high thermo-migration rate [4.23]-[4.25]. Finally, SnCu [4.26] is a lead-free solder used in the automotive industry.

4.3.5 Gold Stud Bumping process

The gold stud bump flip chip assembly process creates conductive gold bumps on the die bond pads and connects the die to the substrate or PCB with ultrasonic assembly. Stud bumping requires no UBM and so wafer processing is not required. This means, individual die can be stud bumped as easily as they can be wire bonded.

Gold stud attach [4.27], [4.28] can give the best electrical contact. They do however require more force and higher temperature to form the bond. Gold stud bumps are placed on the die bond pads through a modification of the "ball bonding" process used in conventional wire bonding. Figure 54 shows the steps needed to form a stud bump.

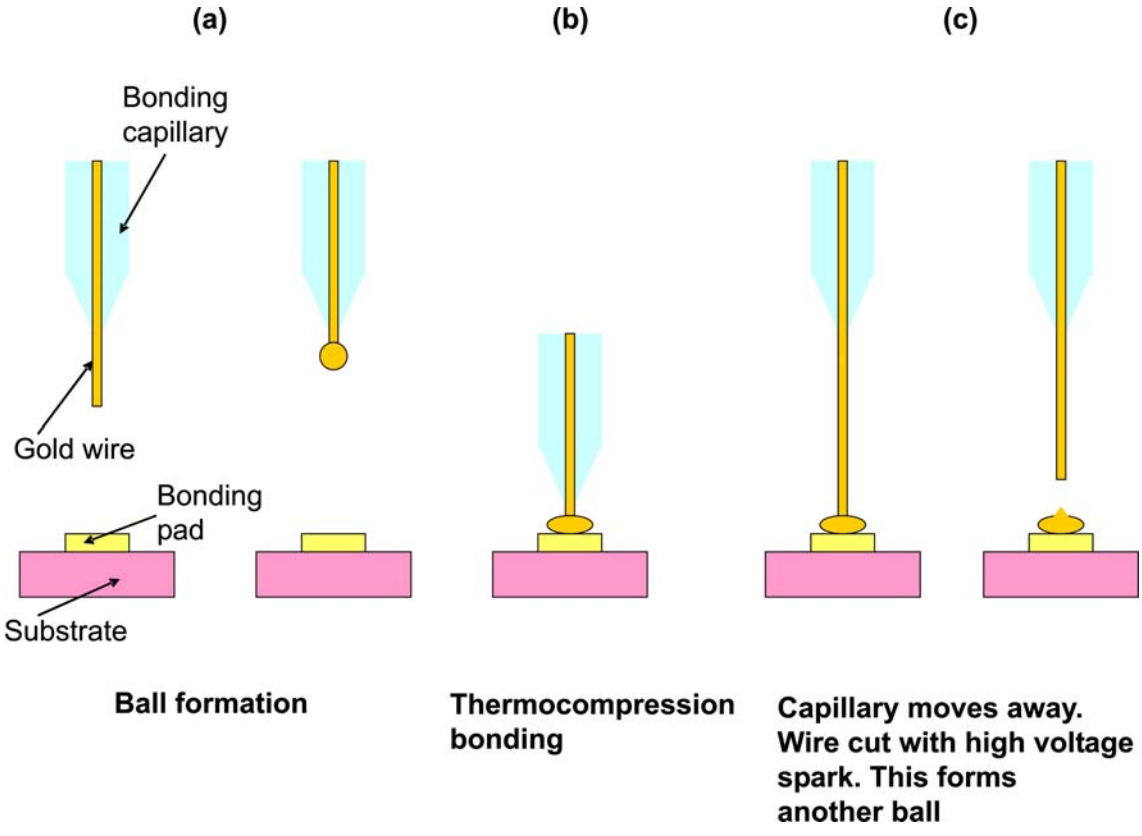

Figure 54) Gold stud bump process:
(a) Ball formation, (b) Thermocompression bonding, (c) Capillary moving away and wire cut with high voltage spark forming another ball. The stud is then 'coined' or 'flattened' to present a uniform surface to the IC to be bonded.

After placing the stud bumps on a chip, they can be "coined" by mechanical pressure to provide a flatter top surface and more uniform bump heights, while pressing any remaining wire tail into the ball. Each bump may be coined by a 'coining tool' immediately after forming, or all bumps on the die may be simultaneously coined by pressure against a flat surface in a separate operation following bumping.

4.4 Anisotropic Conductive Film (ACF)

4.4.1 Introduction

Anisotropic conductive film, commonly known as ACF, is a lead-free and environmentally-friendly epoxy system that has been used for almost 30 years in the flat panel display industry to make the electrical and mechanical connections from the drive electronics to the glass substrates of the displays. In the past decade, these Chip-On-Glass (COG) applications show an increasing focus on ever-higher signal densities and ever-smaller overall display packages. Details of interconnection using ACF and its assembly process can be found in the following references [4.29]-[4.31].

This method of attach can only be used for ICs as the conductive paste will obscure the optical window of the active III-V devices. However, its main advantage is that it can be used with a number of under bump metallisations.

4.5 Optoelectronic Packaging Experiments

4.5.1 Gold Stud Bump Experiments

Gold stud bumps were created onto a gold plated glass test substrate using the K&S 4124 manual ball bonder. A 25μm gold wire was used to form the gold stud bumps. All bonding work was conducted in a cleanroom environment. As with the wire bonding, the MISEC laboratory was used. The bumps were used to attach the Photodetectors onto the test substrate.

Bond pad coating on test substrates was Ni contact (thickness: 6μm) with Au on top (thickness: 2μm). The Au would flow and mix with the Au/ or solder contact with heating, force and temperature. This would result in good adhesion. The Ni under-layer means the contact would not be destroyed.

The gold bumps were analysed on the Zygo interferometer [4.32]. Figure 55 shows a Zygo chart of several bumps formed after coining. The Zygo interferometer uses interference to profile surfaces and can produce accurate 3D data.

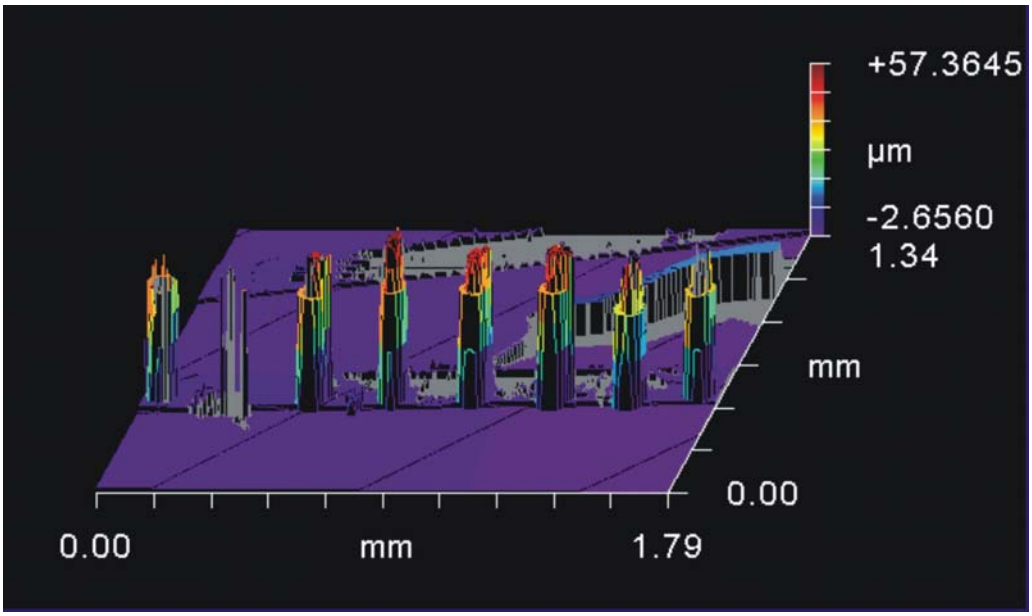

Figure 55) Picture taken using the Zygo interferometer: Several coined gold stud bumps.

The gold bumps were initially attached to the test substrate and then coined using a tool that can be attached to the ball bonder to create a uniform flat top for attachment. Figure 56 shows a single coined gold stud bump taken by the Zygo.

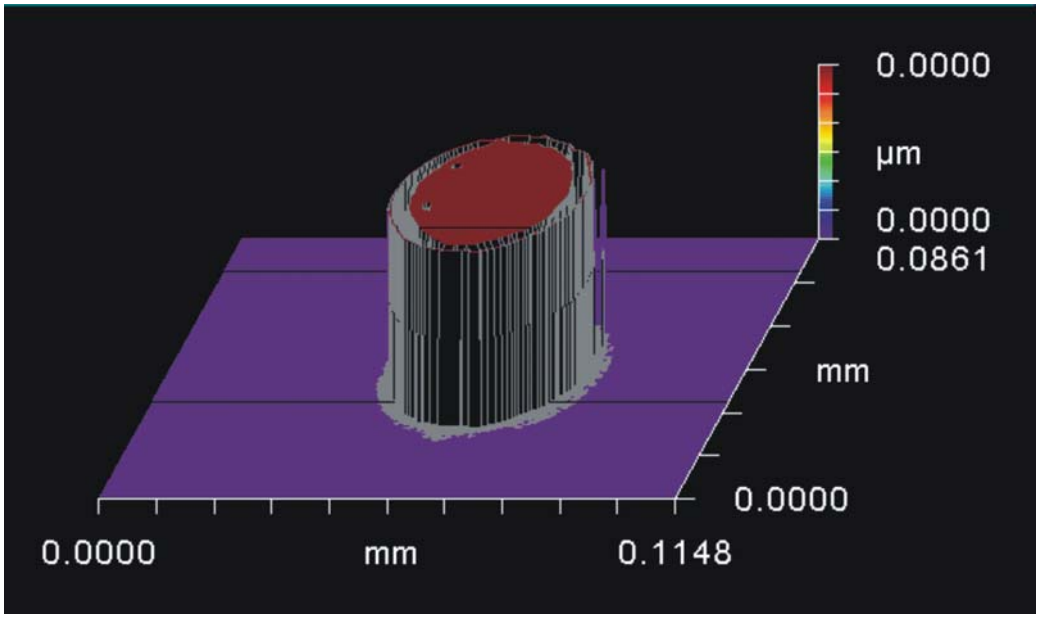

Figure 56) Picture of a coined gold stud bump taken using the Zygo interferometer

Figure 57 shows a surface profile plot of a coined stud bump taken by the Zygo. During the stud bumping process, each parameter on the ball bonder was methodically adjusted until a consistent stud bump was formed on the substrate. This gave the following final height and width measurements of the stud bump:

- Width = 27.7 ±2.5µm.
- Height = 50.3 ±2.3µm.

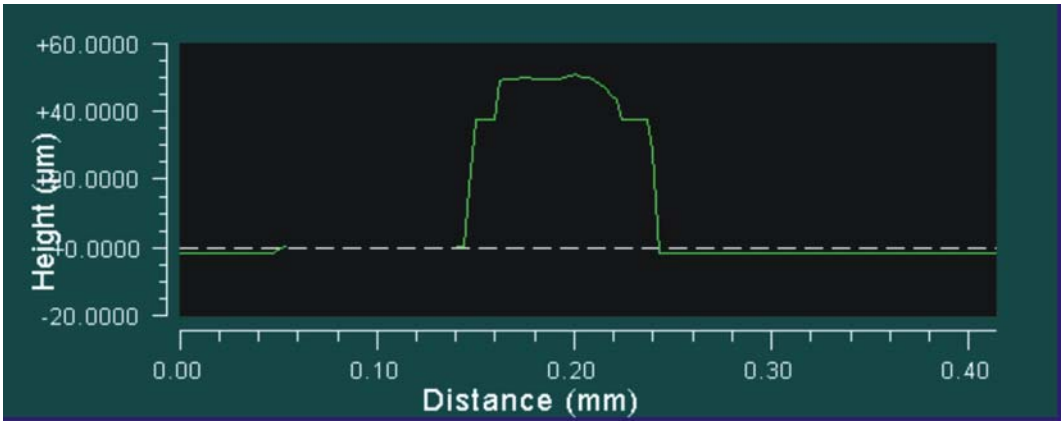

Figure 57) Picture taken by Zygo interferometer of surface profile plot of a coined gold stud bump

Table 21 gives the bonding parameters (Power, Time and Force) used.

	Wire Diameter		
Bonding Parameter	25µm	30µm	50µm
Power (W)	1-2	1.5-2.5	2-3
Time (ms)	2-5	10	5
Force	1-2 (40g)	2-3 (60g)	4-5 (80g)

Table 21) Bonding parameters used to form gold stud bumps from various sizes of gold wire

4.5.2 Flip Chip Bonding Work

Finalisation of flip chip bonding process flow for construction to ensure everything was attached in the correct order. This would prevent reflow of existing bonds.

Flip Chip Bonder:

The FC6 flip chip bonder, which is manufactured by SUSS MicroTec [4.8] was installed in the MIcroSystems Engineering Centre (MISEC) cleanroom at Heriot-Watt University. This machine was used for flip chip bonding performed in this research work.

There was also a scrubbing action available which oscillates the chip and substrate relative to each other to aid the removal of oxide films on the contact surfaces. This step can be inserted at any point in the cycle and within a range of 0 to 5000µm. SUSS MicroTec claims that the accuracy of the bonding alignment is ±5µm, which is the normal specification of the system.

Custom Designed Flip Chip Chuck:

A custom made flip chip chuck was fabricated for holding small components, i.e. VCSELs and Photodetectors. I designed and determined the specifications of the chuck, and then submitted these details to SUSS MicroTec for fabrication. The chuck was delivered in April 2004. Figure 58 shows the design and dimensions of the flip chip chuck.

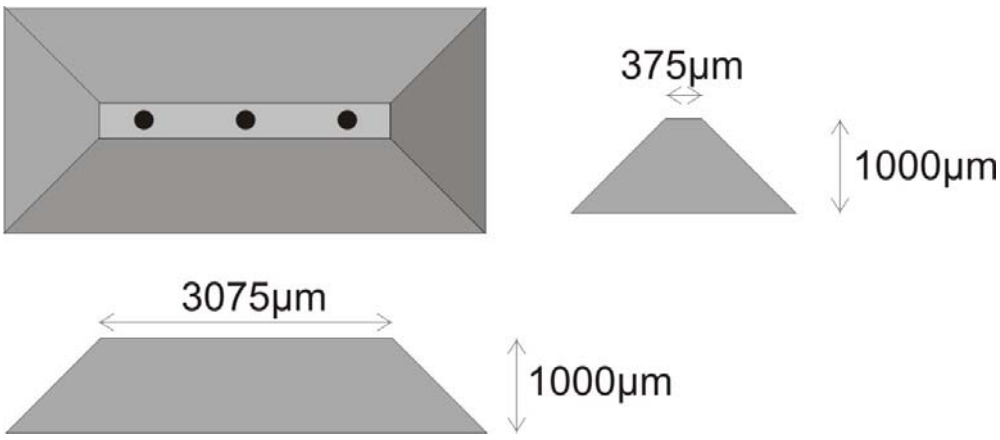

Figure 58) Schematic of Flip Chip Chuck with dimensions

4.5.3 Design of Test Substrates

I designed the mask for the test substrates. This included the footprints for VCSELs, PDs, MSCs (Driver and Amplifier). My colleague Mr Neil Ross performed the

fabrication and cleaving of the substrates using in-house facilities in the Department of Physics at HWU.

The material used for the substrate was glass. It consisted of gold tracks of width 90µm and square bonding pads of size 100µm. Thicknesses of the gold tracks and bonding pads were 0.7µm. The under bump metallisation (UBM) of the bonding pads was Chromium/Gold (Cr/Au), which is suitable for use with gold stud, AuSn solder bump and ACF attach.

Figure 59 shows the footprints on the test substrate for the VCSEL and test glass block (same dimensions as Photodetector). The pitch size = 250µm and pad size = 80µm for the dummy optoelectronic devices.

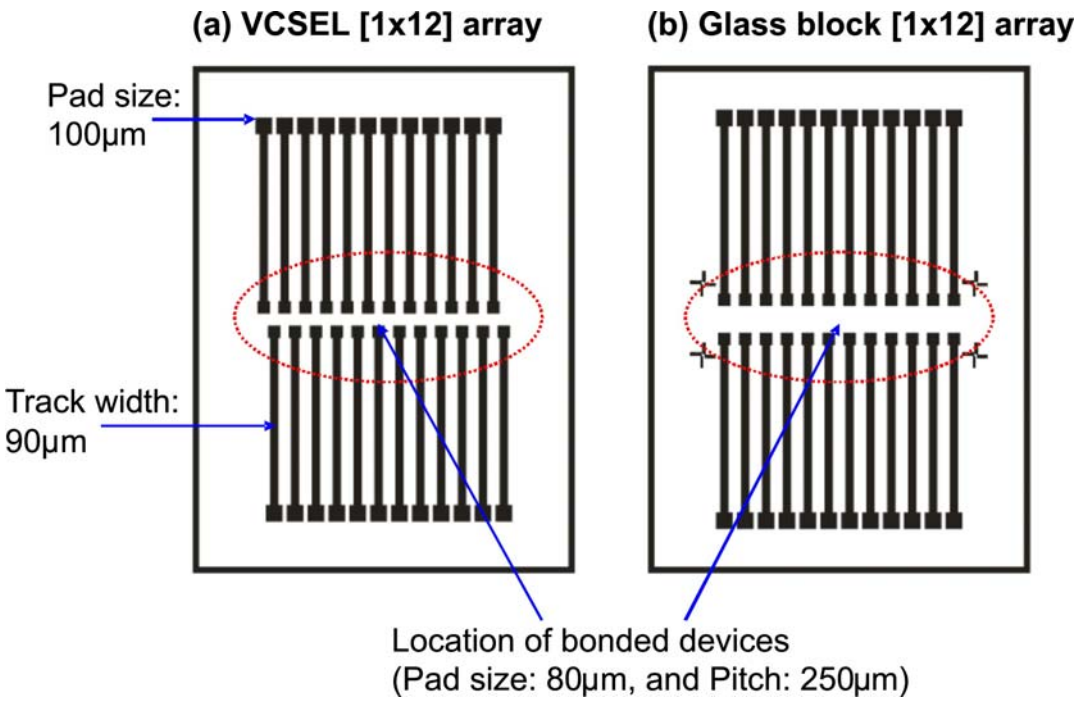

Figure 59) Test substrate footprints for: (a) VCSEL, (b) Glass block (PD).

Figure 60 shows the footprints on the test substrate for the MSC. Footprint 1 is for the driver bonding pads of the chip and footprint 2 is for the amplifier bonding pads. The pitch size = 125µm and pad size = 100µm for the dummy test chip.

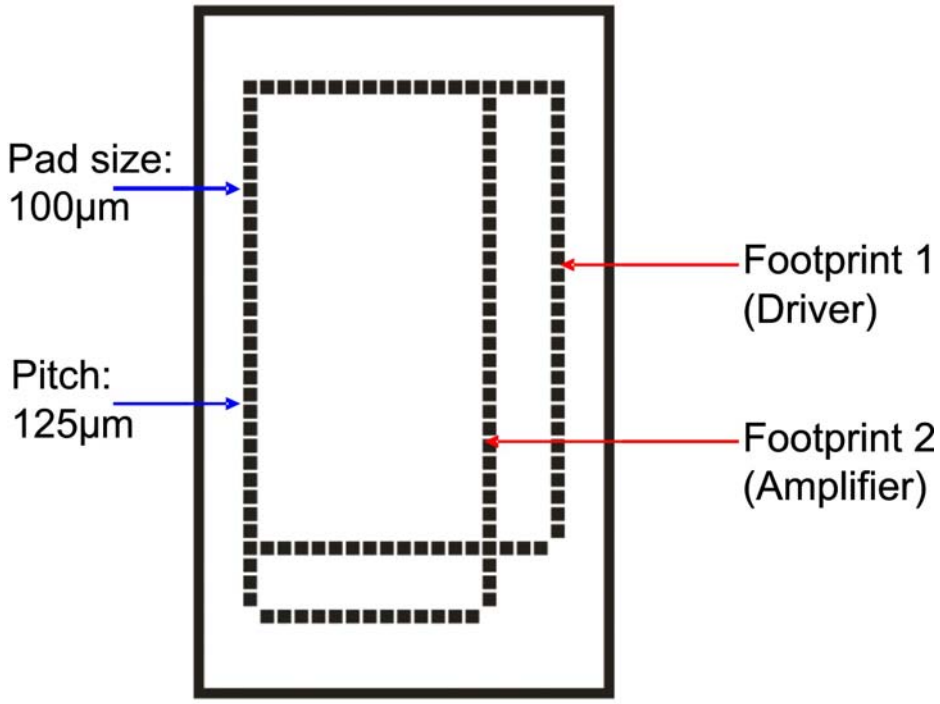

Figure 60) Test substrate footprints for MSC

4.5.4 Bonding Experiments

Flip chip experiments for each bumping technology [Au stud (PDs), AuSn solder bump (VCSELs) and ACF (MSCs)] was performed. This determined the most optimised flip chip bonding parameters applicable for each bumping technology used, which were feasible for successful attachment of devices to test substrates. This was completed in May 2004. These bonding parameters were used for flip chip packaging of working sample devices to the OE-MCMs, which is discussed in the next chapter. The flip chip bonded devices used were dummy samples. This meant no optical or electrical tests were performed on the packaged devices.

Using the FC6 bonder, the dummy components were packaged onto the test substrates in this order:

1) Test glass blocks with [1×12] array bonding pads with the same dimensions as the photodetectors. Gold stud bumps were placed onto the test substrate.

Table A-1 in Appendix A gives the parameters required to bond the [1×12] array glass test blocks to the substrate using gold stud bumps. Since gold is bonded, a high temperature and pressure is required.

Figure 61 shows photos of test glass blocks flip chip bonded using gold stud bumps onto a test substrate. A strong bond was formed between stud bump on substrate and bonding pad of glass block. Attachment was successful using these bonding parameters.

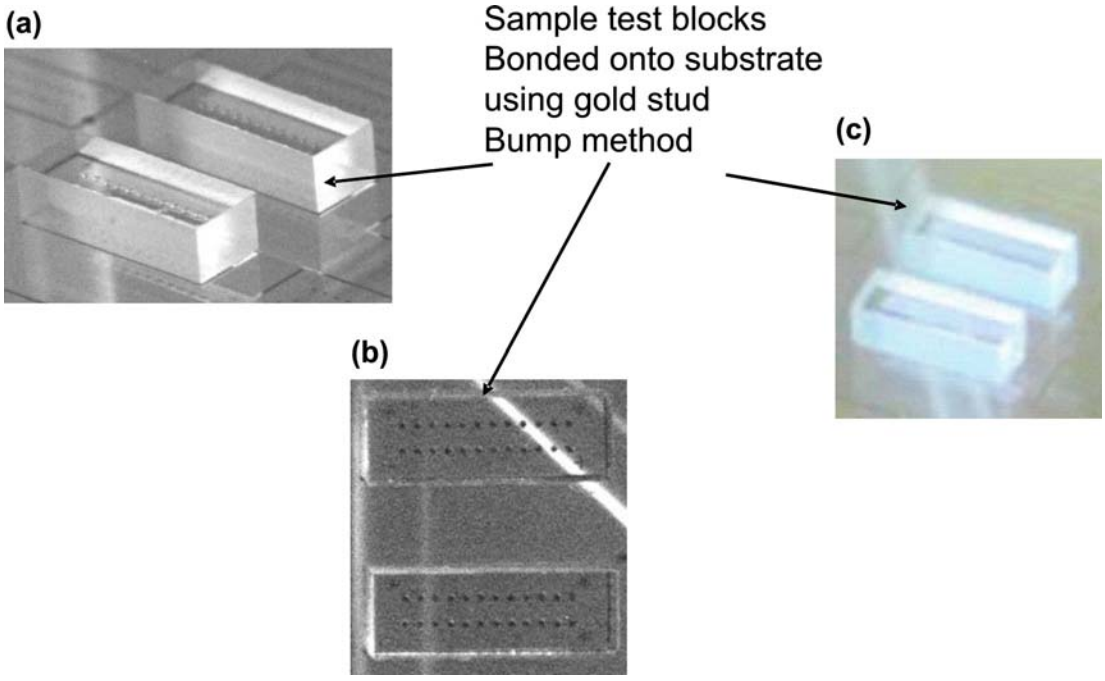

Figure 61) Photos of sample test blocks [1×12] array design flip chip bonded onto a test substrate using gold stud bumps: Photos (a) and (b) were taken with a optical microscope and photo (c) with a standard digital camera.

2) [1×12] VCSEL array devices with AuSn solder bumps.

Table A-2 in Appendix A gives the parameters required to bond the [1×12] VCSEL array devices to the test substrate using AuSn solder bumps.

Figure 62 shows a photo of VCSEL array flip chip bonded using AuSn solder bumps onto a test substrate. A strong bond was formed between solder bump on the VCSEL and bonding pad of test substrate. Attachment was successful using these bonding parameters.

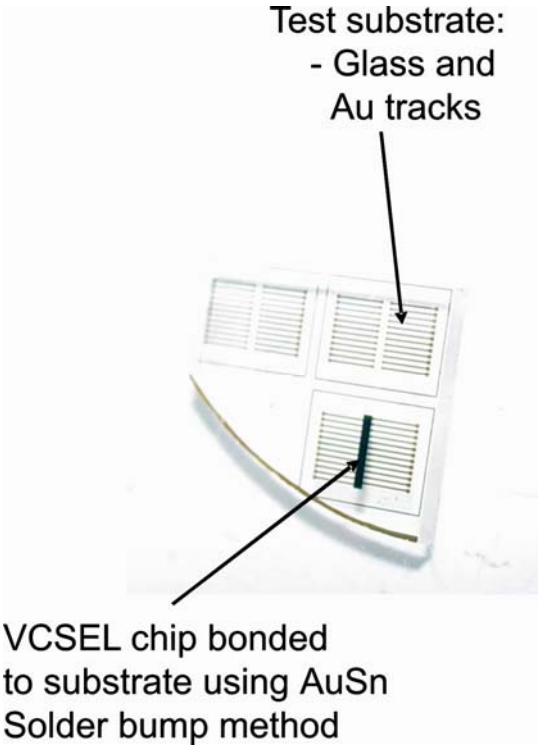

Figure 62) Photo of VCSEL (1×12) array flip chip bonded onto a test substrate using AuSn solder bumps

3) Mixed signal chip (MSC) using the Anisotropic Conductive Film (ACF) method.

Table A-3 in Appendix A gives the parameters required to bond the mixed signal chip (MSC) to the test substrate using the Anisotropic Conductive Film (ACF) method.

A sample of ACF was purchased from Ito Corporation [4.33] in Japan. This film had a shelf life of 7 months, and was required to remain frozen until use. Taking the pad size for the test chip (100μm), a force of at least 1.4kg was required.

Figure 63 shows a photo of test MSC flip chip bonded using ACF attach method onto a test substrate. A reasonable attachment was formed between test chip and test substrate with the conductive epoxy in between. Attachment was successful using these bonding parameters.

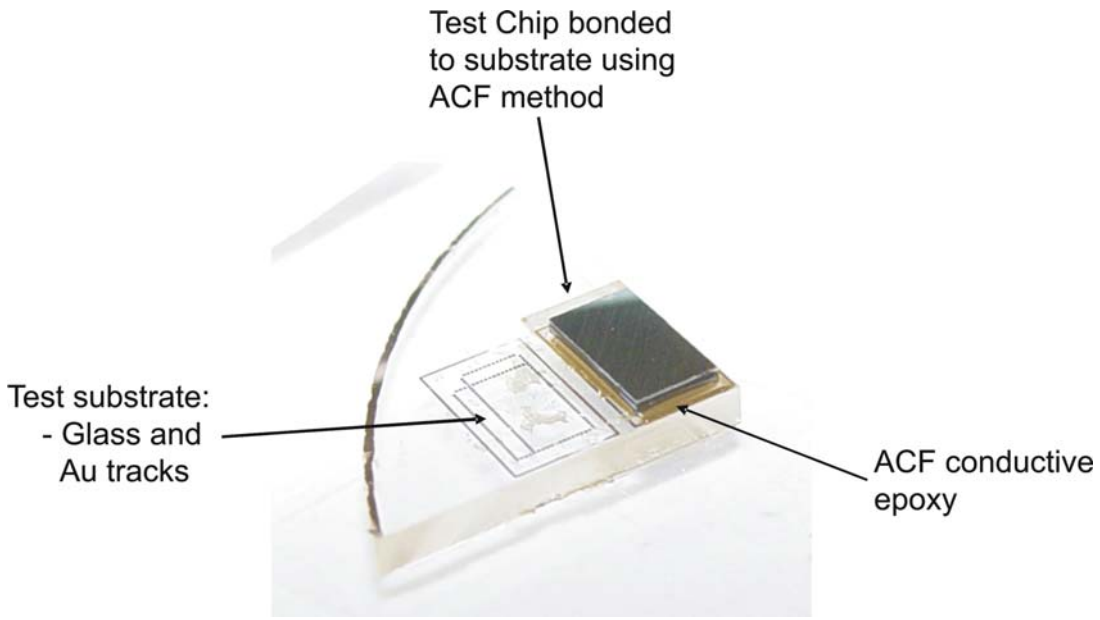

Figure 63) Photos of test mixed signal chip (MSC) flip chip bonded onto a test substrate using ACF attach

4.6 Conclusion

In this chapter, an explanation was given of the following optoelectronic bonding techniques: Wire bonding and flip chip bonding with its associated technologies, i.e. Solder, gold stud bump and ACF. Also, an overview of the optoelectronic packaging specifications and requirements of the high speed systems demonstrator was explained.

Experimental work implementing these methods on packaging the optoelectronic devices was successfully conducted and described in detail. Also, technologies such as ultrasonic flip chip bonding and gold micro-post technology were looked into and discussed.

In the following chapter, specification, assembly and preliminary testing of the optoelectronic multi chip module (OE-MCM) will be described.

4.7 References

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Chapter 5

Optoelectronic Packaging (II)

5.1 Introduction

In this chapter, the main objective was to assemble a functional optoelectronic multi-chip module (OE-MCM), which could then be implemented into the demonstrator for the HOLMS project. This was one of the main parts of the system.

Firstly an explanation of the OE-MCM is given. Next, experimental work conducted on packaging the optoelectronic devices onto the OE-MCMs will be explained. Then, electrical verification tests of bonded optoelectronic devices on test modules, is discussed. Finally, preliminary optoelectronics testing of fully populated OE-MCMs is described.

The outline of this chapter is as follows. In section 5.2, an explanation of the optoelectronic multi chip module (OE-MCM) is given. In sections 5.3, 5.4 and 5.5, optoelectronic packaging experiments on the OE-MCMs are described. In section 5.6, details of the electrical verification tests, on the assembled modules is provided. Finally, in section 5.7, preliminary optoelectronic testing of fully populated OE-MCMs is discussed.

5.2 Optoelectronic Multi-Chip Module (OE-MCM)

5.2.1 Introduction

The OE-MCM is the interface between the electronic and the optical part for this research. It consisted of elements that make the transition from optical realm to electronic realm and vice-versa, i.e. Photodetectors (PDs), VCSELs and MSCs.

The modules were designed, produced and characterised by ETHZ [1.104]. In the following sections I will provide an overview of the module. Further detailed information can be found from the following references [1.98]-[1.103].

5.2.2 Specifications and Layout of OE-MCM

The substrate chosen was transparent at the operating wavelength of 850nm. This was to ensure that optical signals could be routed through the MCM. It was made from silica glass, which had a thickness 750µm.

Four metallic layers were used. Vias were cut right through the layers down to the substrate layer in order to allow optical signals to pass through. The module was implemented using an MCM-Deposited technology [5.1]-[5.3], where thin layers were deposited on the substrate. This technology is well known and has been proven to work well in electronics.

The thickness of the electrical layers, were 2µm, with insulating Benzocyclobutene (BCB) layers in-between of 5µm [5.4], [5.5]. BCB is a material used for the insulating layers on the MCM-D. BCB has a dielectric constant of ε_r=2.6 and a thermal expansion coefficient of $52\times10^{-6}\,K^{-1}$. A passivation layer of 3µm thickness coated the top electrical layer. The plating used for the bonding pads on the module was NiAu.

The minimal feature size for line width of the electrical tracks on the module was 20µm. This had a spacing distance of 35µm.

The MCM had an area of 20mm×36mm. The module consisted of pads with metallization Ni - thickness 6 µm and Au - thickness 2 µm. For the optical elements (PDs and VCSELs), the pads had a diameter of 90µm and the mixed signal chips had a pad size of 85µm for both driver and amplifier footprints. The opening in the passivation layer was slightly smaller with a diameter of 80µm. The specifications of the module are listed in Table 22.

Specifications	Values of dimensions	Number of pads
Thickness	750µm	
Pad diameter (VCSEL and Photodetector arrays)	90µm	24
Pad diameter (MSC – driver and amplifier)	85µm	168
Passivation layer opening - diameter (for all bonding pads)	80µm	
Metallisation/Thickness of bonding pads (all)	Nickel (6µm), Gold (2µm)	

Table 22) Specifications and dimensions of test multi-chip module

The distance between Laser Diode (LD) and Photodetector (PD) was 5.6mm. A picture of the test MCM is shown in Figure 64, where the bonding pad locations for the VCSELs, Photodetectors, MSCs, passive components and connectors are illustrated.

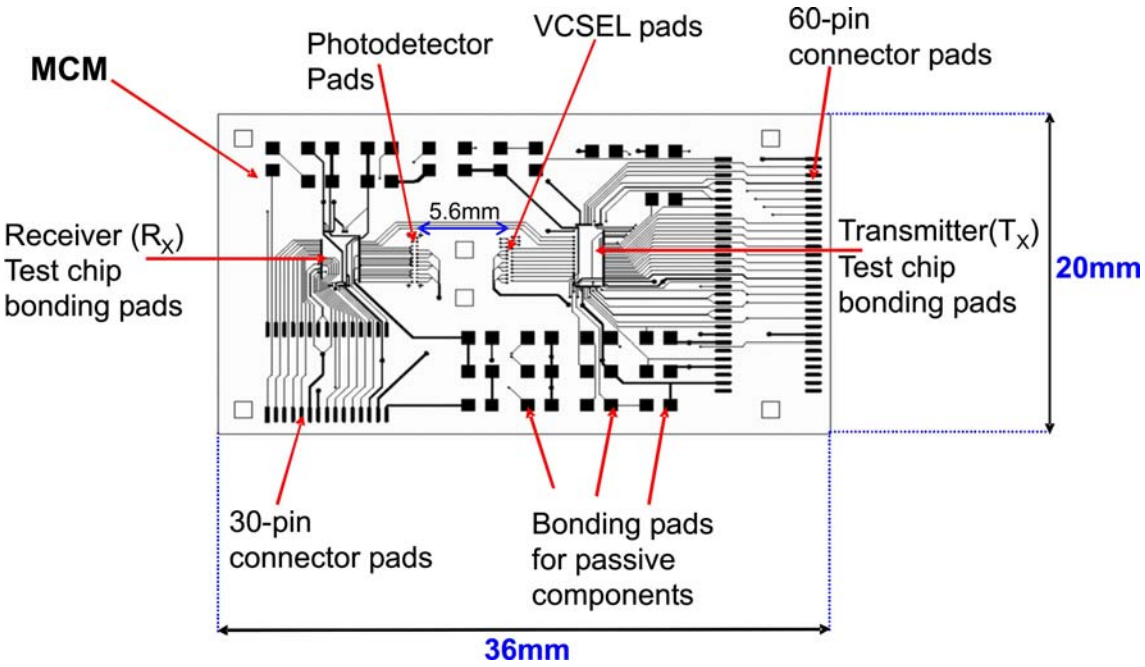


Figure 64) Schematic of MCM, showing bonding pad locations for attachment of active and passive components.

The MCM consisted of the optoelectronic interface chips (VCSEL and Photodetector [PD]), electronic driver chips (for VCSEL), and transimpedance amplifiers (for PD). Figure 65 shows the design of the OE-MCM. This will be explained in the following sections.

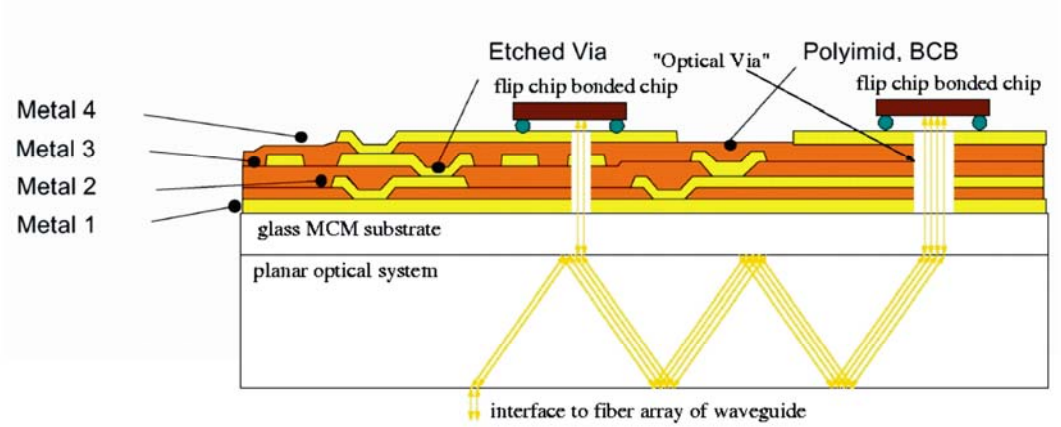


Figure 65) Schematic showing the integration of thin film MCM and planar optical systems into an optoelectronic multi-chip module (OE-MCM)

The optoelectronic components, i.e. VCSELs and photodetectors, were mounted active side facing the MCM by flip chip bonding. The devices could then illuminate (VCSELs) and receive (PDs) through the layer stack, which had an optical window.

5.3 Optoelectronic Packaging Experiments on OE-MCMs

5.3.1 Introduction

The bonding parameters determined in my earlier work in chapter 4 were used for flip chip packaging of working sample devices (PDs, VCSELs and MSCs) to the OE-MCMs.

5.3.2 Initial Experiments

Gold Stud Bumping Problems on OE-MCM:

During Au stud bumping on the OE-MCM, Au, Ni, Cu and BCB layers from the bonding pad were being pulled off. This was occurring after the bonding capillary

placed the bump and moved away from the bonding site with it pulling away the MCM layers. Figure 66 depicts this issue.

This may have been due to the smaller passivation opening of 80um (Depression). The passivation layers on the MCM were Cu/Ni/Au and Cu/BCB/Cu/BCB/Cu/Ni/Au. This problem could be overcome by increasing the thickness of the Au layer or increasing bonding pad size.

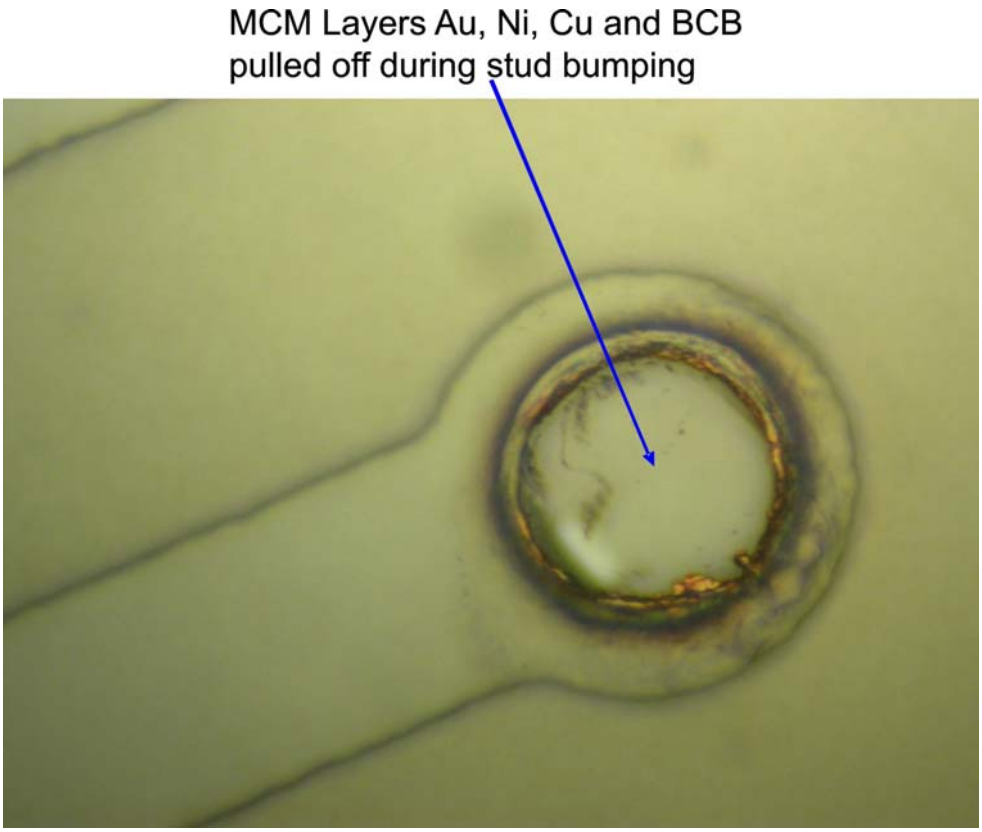


Figure 66) Photo of bonding pad on MCM: Bumps pulled off during Au stud bumping

5.3.3 Flip Chip Bonding Work on OE-MCMs

Optoelectronic bonding was performed on test multi-chip modules (MCMs), which were then used for optical testing of the OE-MCM. This was conducted on a flip chip bonder using gold (Au) stud [3.25, 3.26] and gold-tin (AuSn) bumping technologies [5.6]-[5.9] for attaching the optoelectronic devices (PDs, Test chips and VCSELs).

After the active components were attached, the passive components, i.e. Resistors, Capacitors, Inductors and Connectors, were soldered using standard solder Surface

Mount Techniques. This was conducted externally by the Electronic Manufacturing Services (EMS), Napier University, United-Kingdom [5.10].

Two runs of fully populated test modules were carried out. An explanation of the processes of both runs (1st run and 2nd run) will be given in the following sections.

5.3.4 Fully Populated Test Modules – 1st Run

In the first run, the optoelectronic devices were assembled in the following order: (1) Photodetectors were flip chip bonded using gold stud bumps, which were placed on the test modules, (2) Test chips were flip chip bonded also using stud bumps and (3) VCSELs were attached to the substrate using AuSn solder bumps, which were already placed on the device itself by the manufacturer.

(1) Photodetectors:

The shoe design of the Type B photodetector devices were used for this work. So, using the process and equipment discussed in chapter 4, gold stud bumps of height 65µm and diameter 50µm were placed on their respective bonding pads on the test modules (See Figure 64). A 25µm gold wire was used to form the gold stud bumps. All bonding work was conducted in a cleanroom environment in-house at HWU.

Initially, gold stud bumps were placed on test bonding pad in order to optimise the required parameters of bump. Figure 67 shows this in the pre-coin stage.

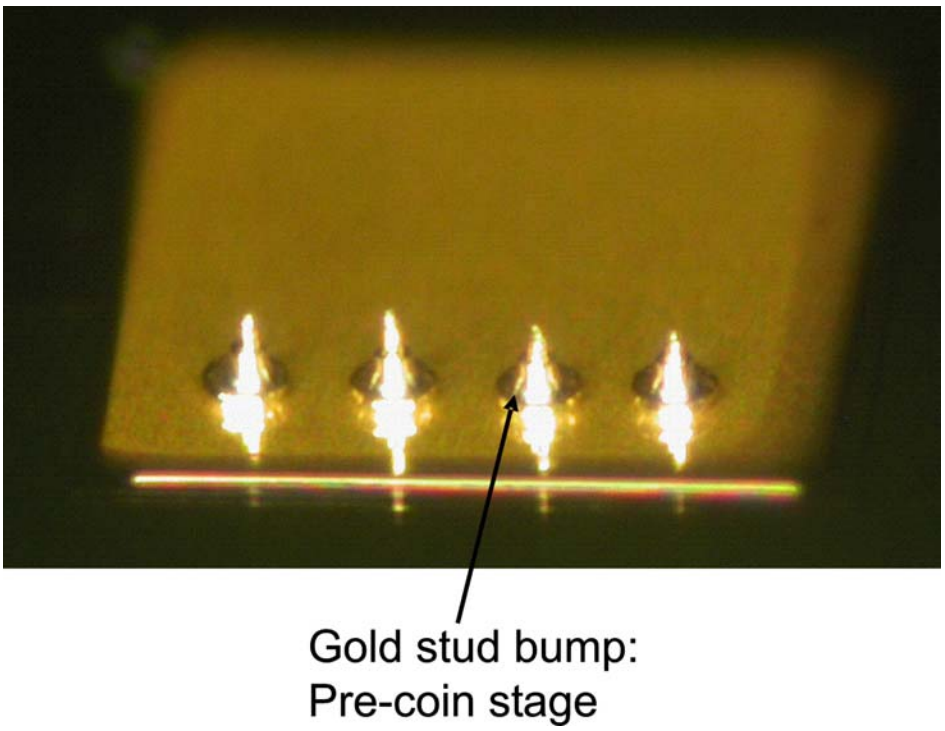


Figure 67) Photo showing gold stud bumps placed on a test pad before coining (Note: Specifications of the bump and bonding test pad are the same used on the actual components).

They were then coined using the coining tool. This process ensured consistency in the co-planarity of bump heights. Also, a Shadowgraph [5.11] was used to measure the x and y values of the bumps in pre and post-coined state.

Figure 68 shows gold stud bumps formed on a test bonding pad in the post-coin stage.

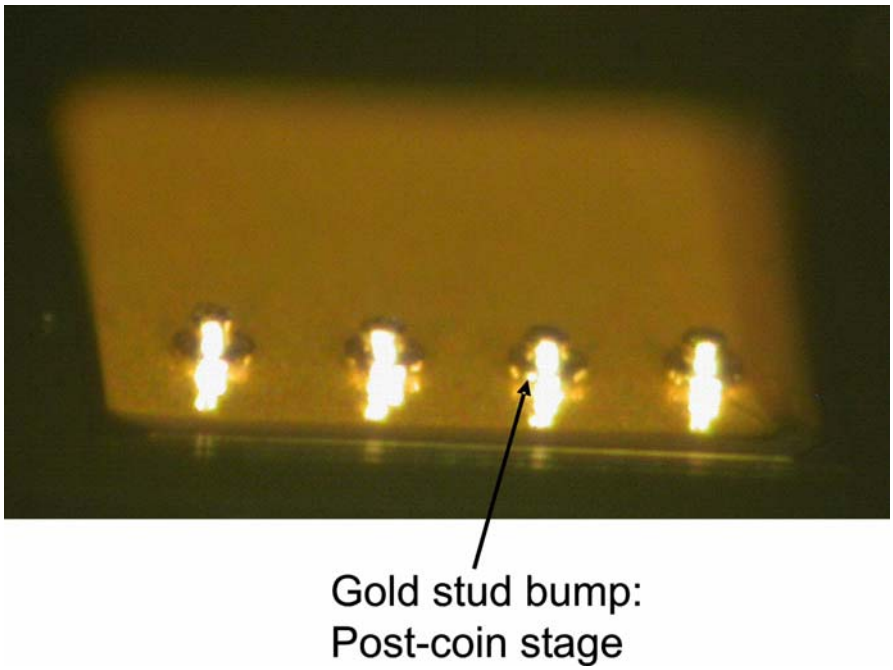


Figure 68) Photo showing gold stud bumps placed on a test pad after coining

The height of the bump formed after coining was 65µm and its diameter, 50µm. The manual ball bonder used had an accuracy of ±10µm. Table A-4 in Appendix A gives the bonding parameters (Power, Time and Force) used to produce gold stud bumps with the specifications stated. This was using the manual ball bonder – K&S 4124.

Since subsequent flip chip attachment using gold bumps required a high temperature (~300^{0}C), Force (~1000-2400g) and pressure, the photodetectors were the first devices to be assembled onto the test substrate. This was successfully conducted using the FC6 bonder in-house at HWU.

(2) Test Chips:

Initially, the test chips were successfully bonded using the ACF process. But, a decision was made by the HOLMS project coordinators to discontinue the ACF method. The reason was that a required force of ~18kg was required to bond ~700 pads on the final mixed signal chip for the HOLMS project. Details of this calculation can be found in the following reference [1.108].

This was not achievable on the FC6 bonder. The maximum force the bonder is capable of is 4kg. This was a decision, which was out of my control. Due to this, I was not able to conduct further experimental work using the ACF bonding method on the test MCMs.

So, the ACF attach method was replaced by using gold stud bumps. Stud bumps with the same specifications as those used to flip chip bond the photodetectors were placed on the respective footprints of the transmitter and receiver chips on the test modules (See Figure 64). The electronic devices were the second devices after photodetectors to be flip chip bonded onto the module.

Figure 69 shows the arrangement of the silicon test chip and MCM before flip chip bonding.

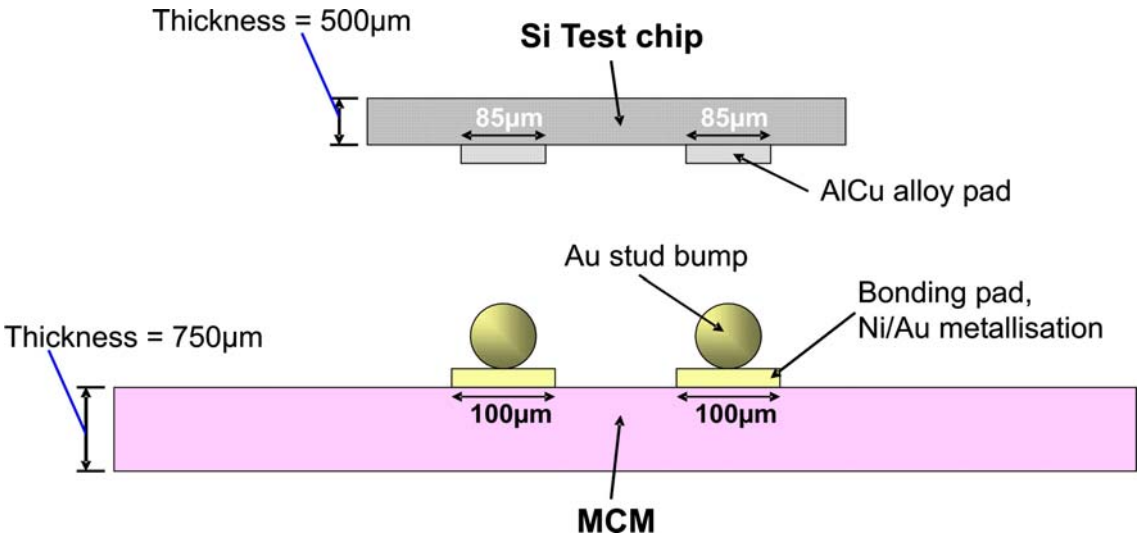


Figure 69) Picture showing pre-bonding arrangement of Silicon test chip and MCM

Problems faced with bonding the electronic devices:

After flip chip bonding the electronic chips, the following two problems occurred with the attachment: (1) The devices initially bonded onto the substrate, but after thermal cooling, they became detached from the test module or (2) The chip and substrate did not bond. The reason why these issues developed was due to the rapid oxidation of the AlCu alloy pads on the mixed signal chip. This inhibited a flip chip connection with the substrate.

I proposed the following solutions:

1. Plasma cleaning the chips would remove any contamination on the pads and then bonding the devices immediately would reduce the amount of oxidation developing on the AlCu pads. This could give an improved connection.

2. Using the scrubbing function of the FC6 bonder during pre-bonding would remove any oxidation or contamination on the bonding pads.

3. After bonding, in order to improve the stability and strengthen the connections an underfill or adhesive could be placed between chip and MCM.

4. Alternatively we could use a thermosonic flip-chip bonder, where the ultrasonic vibration in pre-bonding removes the oxidation layer from the aluminium bond pads.

Further Bonding:

For the 1st run, plasma cleaning of the test chips was conducted and then flip chip bonded onto test modules using the scrubbing function on the FC6 bonder. The scrubbing parameters were: Scrub index=5µm, Scrub Number=4. This resulted in improved connectivity between chip and substrate, but the attachment was still fragile. For the 2nd run of populated modules, the strength of attachment was improved further. Details will be discussed later in this chapter.

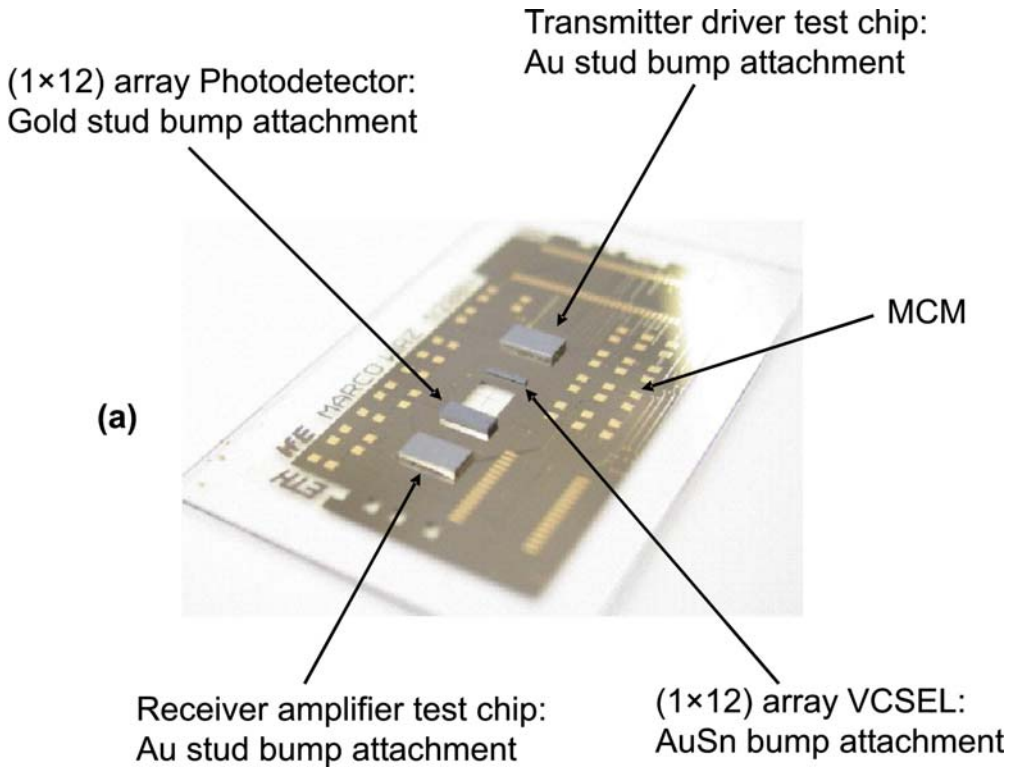
(3) VCSELs:

The VCSELs consisted of AuSn solder bumps of height 65µm and diameter 50µm. The 1mW power VCSEL devices were used for this work. Attachment using AuSn solder bumps required a lower temperature (~281^{0}C) and a considerably smaller force (~5-10g). This component was flip chip bonded after the photodetector and test chips. This was successfully performed.

Populated Test Modules:

After completing the assembly of all active components, the passive components, i.e. resistors, capacitors, inductors and connectors, were attached using standard pick and place soldering. Since this required the lowest bonding temperatures (~50-100^{0}C), the passive components were placed last. As mentioned earlier, this was performed by EMS.

Two fully assembled test MCMs were completed in December 2004. Figure 70 shows pictures of (a) Populated MCM with only active components and (b) Fully populated MCM with active and passive components attached.



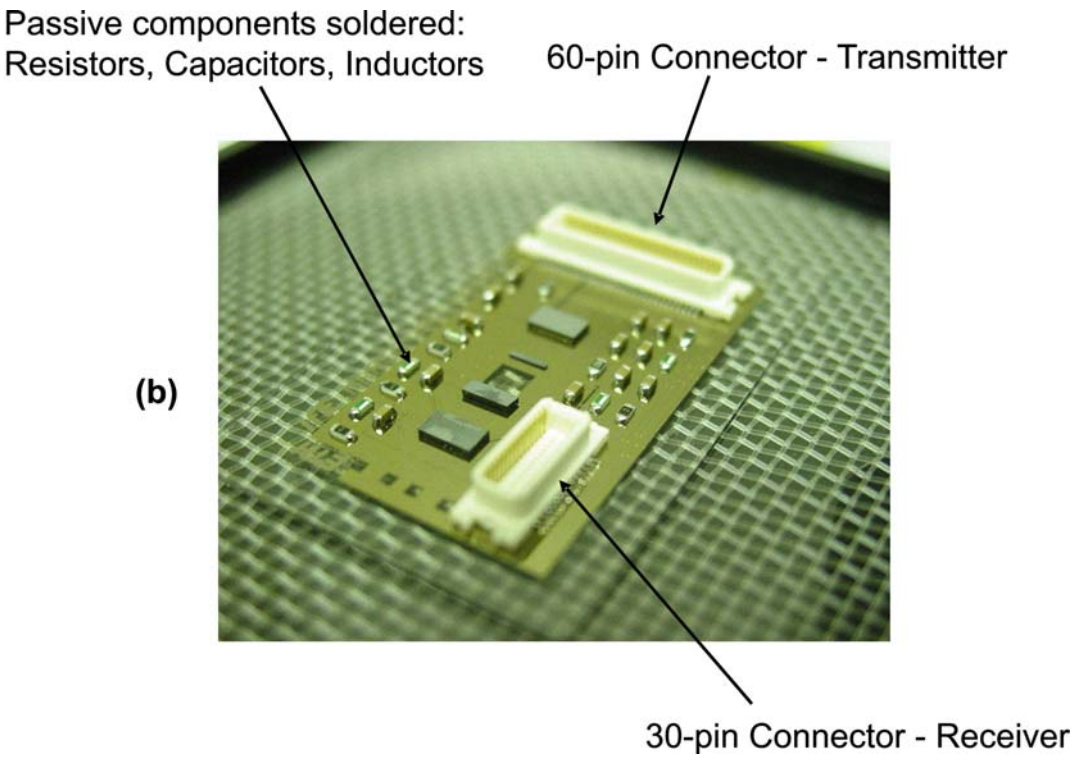


Figure 70) MCM flip chip bonded with: (a) Active devices, (Photodetectors, Test Chips and VCSELs), (b) Active devices and Passive components (Inductors, Capacitors, Resistors and Connectors attached).

5.3.5 Summary

Flip chip bonding on test chips, and photodetectors using Au stud bumps and VCSELs using AuSn solder bumps were successfully performed. Problems occurred with attaching the test chips. This was because the aluminium pads oxidised quickly, forming an oxidation layer which impeded a flip chip connection with the test modules. This was overcome by plasma cleaning the devices prior to bonding and using a scrubbing facility on the FC6 machine in the pre-bonding stage. Optoelectronic testing of the two test modules was conducted in January 2005. Details of this will be explained later in this chapter.

5.4 Further Research into Alternative Bonding Technologies

5.4.1 Lead-free Solder Bumps

I investigated into using lead-free $Sn_{0.955}Ag_{0.04}Cu_{0.005}$ (SAC405) [5.12]-[5.14] solder bump material as an alternative to using gold stud bumps for attachment of test chips. Companies such as Pac Tech [5.15] and Advanced Semiconductor Engineering Group (ASE) [5.16], [5.17] offer this bumping technology. Using a different solder technology could solve the attachment problems of the MSCs.

Lead-free solder bumps (SAC405) were a suitable technology as this is not dependent on the UBM of the bonding pad. So, aluminium pads of the test chip will not pose any risk with regard to the attachment of chip to substrate using SAC405 solder bumps.

The main issue was the cost of using this bumping technology. It was very high and exceeded the budget allocated for this project work. Budgetary quotations from Pac Tech and ASE were approximately £10,000 to have solder bumps placed on four test OE-MCMs. As the expense for this experimental work came from the HOLMS project budget, project coordinators decided not to use the SAC405 bumping technology.

Alternative bonding technologies such as gold micro-posts and Ultrasonic flip chip bonding were studied. Details are described in the following sections.

5.4.2 Gold Micro-Posts

A modification of the gold stud bump is the Micro-Post (μ post). This result preserves all of the usual advantages of gold stud bumps, while adding several new ones. The Micro-Posts are formed in a conventional thermosonic bonder, with standard stud bump gold wire. The bumps require no special UBM and can be placed directly on the bonding pads of individual dies or wafers.

Mintech Interconnect and Test [5.18] offer a μpost bumping service. I don't have information on how the process was performed by Mintech. Figure 71 shows a photo of Gold μpost bumps produced by Mintech.

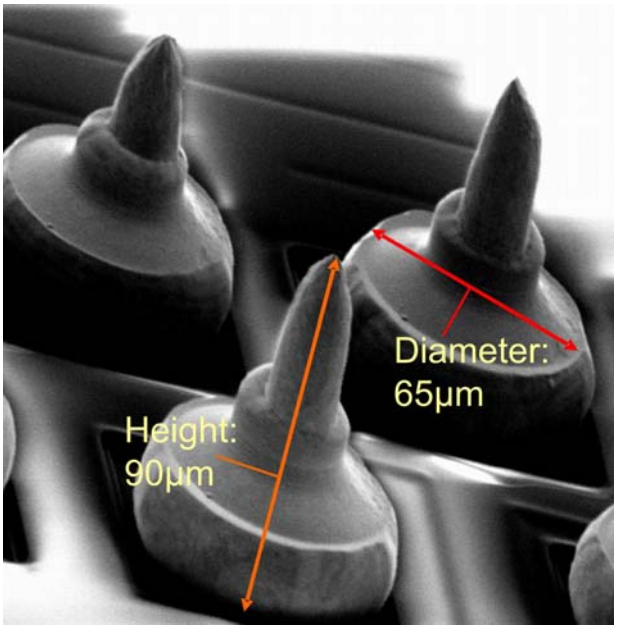


Figure 71) Gold µpost bumps produced by Mintech Interconnect and Test Division

Also, µpost bump technology is capable of a number of substrate attach methods, which include: Thermosonic, Epoxy, Ultrasonic, Solder and Thermocompression. Table 23 details the µpost capability demonstrated to date.

Pitch	80µm (Minimum)
Pad	30µm (Minimum)
Height	250µm (Maximum)
Diameter	65µm (Maximum)
Aspect Ratio	<3

Table 23) µpost capabilities demonstrated to-date

5.4.3 Ultrasonic Flip Chip Bonding

Thermosonic flip chip bonding is a solder-less technology. The thermosonic approach is used to join ICs with gold bumps to gold plated pads on the substrate. It offers a range of features superior to solder and adhesive counterparts. For example (a) simplification of the processing and assembly steps, (b) reduced levels of assembly temperature, loading pressure and bonding time, and (c) increased current carrying capacity.

Thermosonic bonding was previously applied mainly for wire bonding. This bonding method uses a combination of ultrasonic and thermocompression bonding that optimises the best qualities of each. Thermocompression bonding usually requires interfacial temperature of the order of $>300^0$C. This temperature can damage some die attach plastics, packaging materials and laminates, as well as some sensitive chips. But in thermosonic bonding the interface temperature can be significantly less, i.e. typically between 100-150^{0}C, so avoiding these problems. The ultrasonic energy helps disperse contaminants during the early part of the bonding cycle and assists in completing the bond in combination with the thermal energy.

Thermosonic bonding has the advantages of Metallurgical joining, which is more reliable than conductive particles and adhesive joining, process cycle time can be reduced from several minutes to less than 10 seconds and lower manufacturing cost per unit. Also, another advantage of such a technique is that it does not require any additional metallisation on the aluminium pads on silicon circuits.

5.5 Fully Populated Test Modules – 2nd Run

5.5.1 Test Module Production

Second run of 2 fully populated test modules were completed in October 2005. The bonding was outsourced to Optocap [5.19] for the following two reasons: (1) to make use of the automatic gold ball bonder (K&S 1488 bonder [5.20]) which improved consistency of the bump height planarity and (2) to make use of their ultrasonic flip chip bonder (Finetech Fineplacer bonder [5.21]). This alleviated the problem of the oxidation layer forming on the test chip bonding pads. Optocap are based in Livingston, Scotland, and they are a developer of packaging solutions for optoelectronics, microelectronics, nanotechnology, MEMS, biotech, micro-displays and sensors.

Optocap placed stud bumps using the automated ball bonder on the bonding pads of both electronic test chips and photodetector for each module. This time, a 17µm gold wire was used to form the bumps. The height of the bumps produced was 65µm with a tolerance of ±2.5µm. Also, the tolerance of the diameter and x/y placement of the bumps onto the pads was ±2.5µm. Table A-5 in Appendix A shows the ball bumping parameters used.

Then the optoelectronic devices, i.e. PDs, VCSELs, MSCs, were attached to the MCMs using the ultrasonic flip chip bonder. Table A-6 in Appendix A shows the ultrasonic flip chip process parameters used in this work.

For the test chips, an under-fill was added after flip chip bonding in order to increase stability and robustness. The under-fill used was Hysol FP4530, which is a low viscosity based material. This was manually dispensed, with no controlled time or pressure. The process relied on a capillary action to draw the material under the die and a 50^0C background heat was used to reduce the viscosity further. This aided the material flow under the die. After underfill was dispensed, the test modules were cured for 15 minutes at 180^0C.

5.5.2 X-ray analysis of bump attachment

Using the Micro-focus X-ray machine at Optocap, which has a resolution of <5µm, the attachment of the gold stud bumps, i.e. bump (on test chip and photodetector) to substrate (MCM) was analysed. The X-ray analysis showed good attachment of bumps to MCM and the bonds were stable over time and over temperature cycling. This is shown in Figure 72.

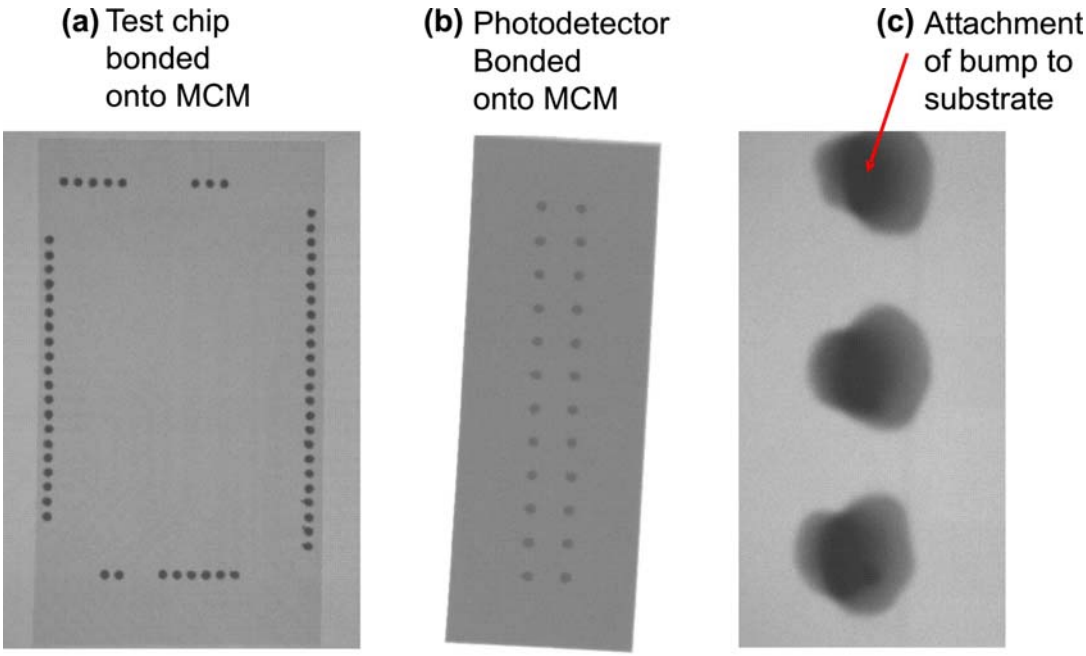


Figure 72) X-ray pictures showing attachment of gold stud bumps on test chip with MCM: (a) Test chip bonded onto MCM, (b) Photodetector bonded onto MCM, (c) Showing good attachment of gold bump to substrate.

5.5.3 Summary

After completing the assembly of all active components, the passive components, i.e. resistors, capacitors, inductors and connectors, were attached using standard pick and place soldering. As with the 1st run of populated modules, this was performed by EMS, Napier University. Optoelectronic testing of the second run of two test modules was conducted in October/November 2005.

5.6 Verification Tests of Optoelectronic Devices Packaged on Modules

Electrical tests were carried out on the flip chip bonded VCSEL and Photodetector arrays. This was in order to verify the electrical performance of the packaged devices.

These experiments were performed prior to the electronic chips and passive components being attached onto the modules.

Electrical tests were not conducted on the flip chip bonded mixed signal chips. This was because I did not have the required test instrumentation in-house at HWU. Also, I did not have the budget to purchase extra equipment or outsource the chips in order to carry out this work.

VCSEL Arrays:

The same experimental set-up as described in chapter 3 (Section 5.4.3: Characterisation of VCSELs) was used to carry out the tests on the VCSELs. Current-voltage (I-V) measurements were performed between I = 0 to +5mA. Figure 73 shows the results obtained.

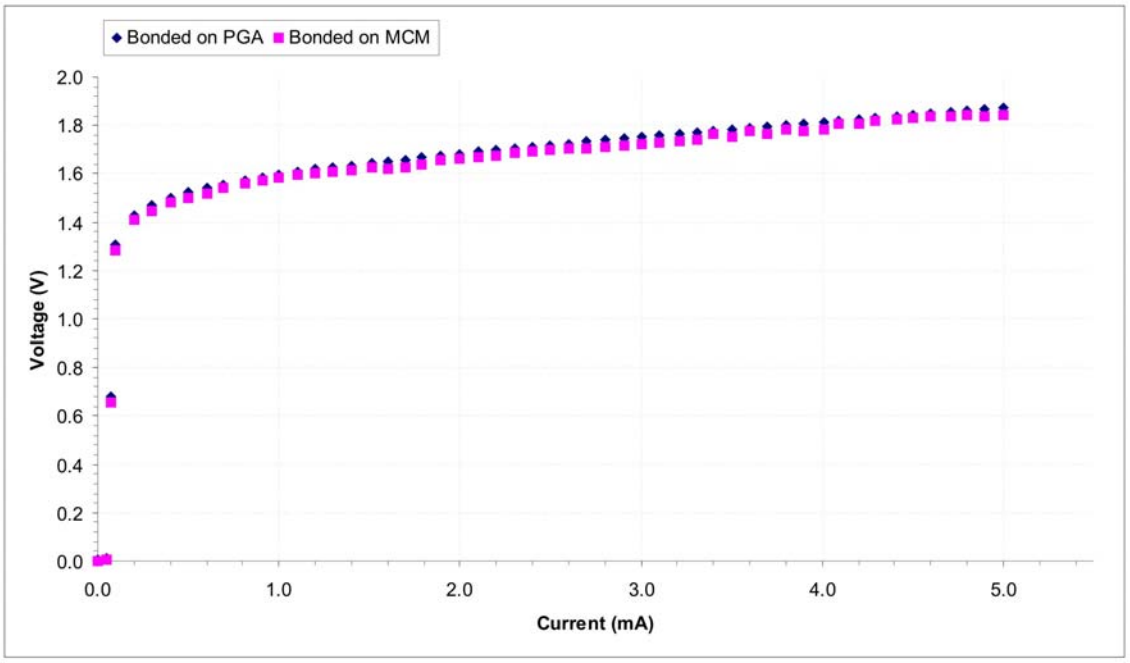


Figure 73) Current/Voltage plots of Packaged VCSEL: Bonded on PGA ◆, Bonded on MCM ■.

Also, this figure shows a comparison of the I-V plots for the VCSEL packaged on the (1) MCM and (2) PGA (work from chapter 3). Both plots closely match, which verifies that the VCSEL attached on the MCM has achieved good electrical performance and reliable bonding.

Photodetector Arrays:

The same experimental set-up as described in chapter 2 (Section 1.7: DC Characterisation of Type B Detector Arrays) was used to carry out the tests on the PDs. Dark current measurements were conducted across a voltage from –5 to +2 Volts.

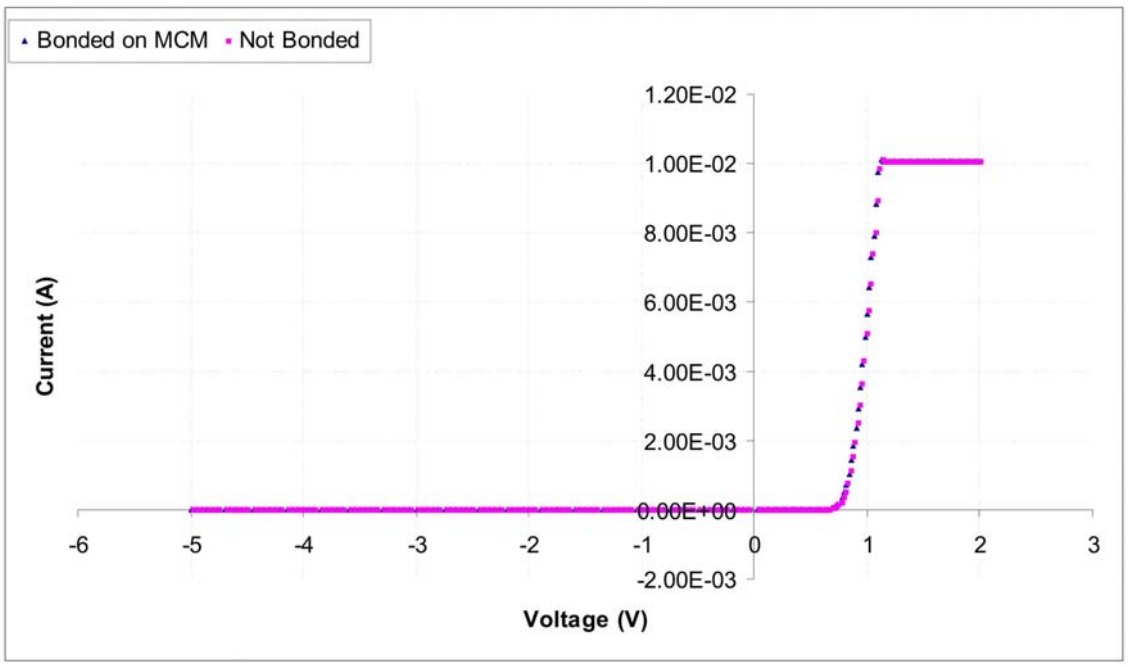


Figure 74) Current/Voltage plots: Showing comparison of dark current measurements for Shoe diode when: Bonded on MCM ▲, Not Bonded on MCM ■.

Figure 74 shows the results obtained. Also, this figure shows a comparison of the I-V plots for the Photodetector array, which is (1) Flip chip bonded on the MCM and (2) Not bonded (work from chapter 2). Both plots closely fit, which validates that the PD array attached on the MCM has achieved good electrical performance and reliable bonding.

Also, Table 24 compares dark current and series resistance values for these plots. The data shows a close match between the bonded and standalone PD arrays.

Photodetector Array	Dark Current – I[dk] (Amps)	Series Resistance (Ω)
Bonded onto MCM	5.00×10^{-10}	31.65
Not bonded	6.08×10^{-10}	29.76

Table 24) Comparison of Dark Current and Series Resistance Data for: (i) Packaged PD Array, (ii) Not-Packaged PD Array.

5.7 Preliminary Optoelectronic Testing of Fully Integrated OE-MCMs

5.7.1 Introduction

In the following sections, I will discuss the initial optoelectronic testing work carried out on the fully assembled modules. This will describe the experimental set-up, procedure and results achieved. The aim of testing was to initially power up the mixed signal chip (VCSEL driver), and then observe the VCSEL output. Due to project schedule constraints by the HOLMS Consortium, this experimental work was limited to only attaining preliminary results.

5.7.2 Experimental set-up

The main aim of testing the fully populated test modules was to generate an optical signal from the VCSEL. This would be optically transmitted on an optical test rig, where the power output of the VCSEL would be detected using the Newport 918-SL silicon detector and Newport Power Meter Model 1930-C. Figure B-1 and Figure B-2 in Appendix B shows a schematic and photo respectively of the optical test rig set-up.

The populated modules were connected to a break-out PCB with two flex boards (ribbon cables). Two connectors were used on the board, one with 30 pads and one with 60 pads. This provided the necessary flexibility to conduct the measurements. The break-out PCB was designed and manufactured by ILFA [5.22]. The dimensions of the break-out PCB were 245mm×150mm. Figure B-3 in Appendix B shows photos of these components.

5.7.3 Results

Optical testing was performed on two fully populated MCMs from the 1st run in January 2005. The Tektronix HFS 9009 Stimulus System provided pre-programmed digital signals to the PCB via SMA connectors. Figure B-4 in Appendix B shows a picture of the digital signals, which were programmed into the Tektronix stimulus system. Also, Table B-1 in Appendix B provides details of the functionalities of the pre-programmed digital signals used. A high speed digital oscilloscope (Agilent Infinium 2.25GHz 8GSa/s digital oscilloscope) was used to visualize these signals.

The VCSEL output was measured on the first module, but no power intensity was detected. The same result occurred for the second module. This failure was thought to be due to the weak attachment of the electronic chips onto the test modules. This could have inhibited electrical connectivity, and for that reason the mixed signal chip did not power up.

So, a 2nd run of two populated test modules were developed in October 2005, whereby the test chips were flip chip bonded using a ultrasonic flip chip bonder, which successfully alleviated the poor connectivity problems in the 1st run of modules.

Optical testing was performed on these modules in October/November 2005. The VCSEL output was measured on the first module, but no power intensity was detected. A similar result was obtained for the second module. I was not able to continue further experimental work in order to resolve this issue. This was because of the strict time constraints set by the European Commission reviewers.

5.8 Conclusion

I concluded that there was a problem with the functionality of the electronic mixed signal chips. These devices were not individually tested prior to attachment onto the OE-MCMs. The chips functionality was very complex and required more specialised instrumentation to perform electrical performance measurements on them. Unfortunately, my laboratory research facilities did not have this equipment in-house at HWU. Also, I did not have the financial budget from my project to purchase this equipment.

My concerns were clearly addressed at all HOLMS review meetings, project reports, and presentations. But, it was very difficult for me to progress further, because decisions were made by the HOLMS project coordinators. This meant I continued my research with the devices and equipment I had available. As a result, this determined the direction I took. Consequently, these were the results produced.

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Chapter 6

Conclusions

6.1 Introduction

Optoelectronics has already overtaken electronic interconnection over long distance and is continuing to replace electronics over shorter and shorter distances. It is strongly felt that optoelectronic interconnects have the potential to satisfy the interconnect requirements for future digital systems. The goal of the work in this thesis has been to contribute towards the development of optoelectronic devices and packaging in information photonics.

Chapter 1: Background and Thesis Overview was presented in the chapter. The aims, motivation and technological aspects of this research work, was described.

Chapter 2: Receiver Devices – Photodetector (PD) Arrays. This chapter described the background, specifications and design of photodetectors used. Also, optical characterisation experiments of two types of detectors (Type A and Type B devices) were performed. From the results, the shoe design, Type B detector was chosen.

Chapter 3: Transmitter Devices and Mixed Signal Chips (MSCs): This chapter described details of the background, specifications, and design of the transmitter devices which were used. Characterisation experiments performed on these devices were explained. Also, details of the mixed signal chips (MSCs) used to drive the transmitter devices and amplify the receiver devices were provided.

Chapter 4: Optoelectronic Packaging (I). This chapter explained the background of flip chip bonding technologies. By using these techniques, an explanation of the experiments conducted in packaging the components described in chapter 2 and chapter 3 was given.

Chapter 5: Optoelectronic Packaging (II). This chapter described the fully populated optoelectronic multi-chip module (OE-MCM) developed for my research work. Experimental work conducted on packaging and testing the OE-MCMs was explained.

6.2 Assessment of work

My research work initially tested all optoelectronic devices (Photodetectors and VCSELs). These components, including the electronic chips were then integrated onto OE-MCMs using a combination of flip chip bonding technologies. This produced mechanically stable and fully populated OE-MCMs. Electrical tests were performed on the packaged optoelectronic devices and the results verified good electrical performance.

The main failure in the project was getting the Mixed Signal Chips to work. These devices were designed and modelled by Supélec. I concluded that there was a problem with the functionality of the electronic chips because these devices were not individually tested prior to attachment onto the OE-MCMs. Supélec stated they successfully tested the chips prior to sending them to HWU. To validate this data, I did not have the required testing equipment in-house at HWU as the functionality of chips was complex. Also, I did not have the budget to purchase the kit. Considering, these conditions, which were out of my control, I was required to rely on the validation results provided by Supélec.

My concerns were clearly addressed at all HOLMS review meetings, project reports, and presentations. But, it was very difficult for me to advance further, because decisions were made by the HOLMS project coordinators. This meant I continued my research with the devices and equipment I had available. As a result, this determined the direction I took.

6.3 Future Directions

For future projects such as HOLMS, improved teamwork between consortium members is required. Using a co-design approach to develop and integrate optoelectronic and packaging technologies between project partners would enable a more compatible and better optoelectronic demonstrator to be developed.

Also, better management of funding is required in the project. This would have enabled me to purchase extra laboratory equipment for my research. For example, test instrumentation for electronic chips.

6.4 Summary

Much has been learned about the difficulties of packaging optoelectronic devices. I strongly feel that this work must be continued, albeit in another forum. The application of optics to digital systems is exciting and has potential for new architectures to which the attributes of optical interconnects are suited.

Generally, the design and layout of existing systems has been based on the properties and restrictions of electrical interconnections. The progress made in optical interconnects will give system designers an opportunity to stand back and re-evaluate system architecture in a new light.