Fifty Years of Moore's Law

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***Abstract*—The 1959 invention of the planar silicon transistor led to the development of the integrated circuit (IC) and the growth trend in IC complexity known as Moore's Law. While Moore's observation came in 1965, his original trend line showing a doubling of components per chip each year began with one component in 1959. Thus, we have now experienced 50 years of Moore's Law. This paper provides a history of Moore's Law through its many changes and reinterpretations, containing possibly a few new ones as well.**

***Index Terms*—History, learning curve, Moore's Law.**

I. Introduction

THE IMPACT of the semiconductor integrated circuit (IC) on modern life has been so profound that it is now often taken for granted; consumers have come to expect increasingly sophisticated electronics products at ever lower prices, just as the business world has come to expect greater productivity through improved information technology. And on a macroeconomic scale, electronics have grown to become a U.S. $2 trillion industry as well as an enabler for productivity and growth in virtually all areas of economic activity.

Underlying the electronics revolution has been a remarkable evolutionary trend called Moore's Law. Begun as a simple observation that the number of components integrated into a semiconductor circuit doubled each year for the first few years of the industry, Moore's Law has come to represent the amazing and seemingly inexhaustible capacity for exponential growth in electronics. In the past 50 years, this observation that we call Moore's Law has expanded far beyond its original intentions, with the very real danger of losing its meaning, and possibly its usefulness. As G. Moore has recently said, "The definition of Moore's Law has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line" [1].

What is Moore's Law, how did it come about, and how is it useful? How can its predictive power be explained? What is its relevance to semiconductor trends today? When will Moore's Law end? This paper will attempt to answer these questions, extending previous work on this topic [2], [3].

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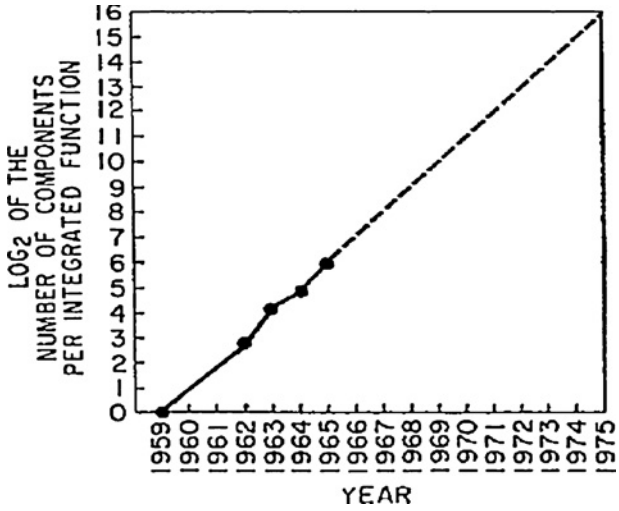

Fig. 1. Moore's 1965 prediction of the doubling of the number of "minimum cost" components on a chip each year, based on historical data and extrapolated to 1975 [4].

II. History of Moore's Law

The remarkable evolution of semiconductor technology from crude single transistors to multi-billion-transistor microprocessors and memory chips is a fascinating story. One of the first "reviews" of progress in the semiconductor industry was written by G. Moore, a founder of Fairchild Semiconductor (and later Intel), for the 35th anniversary issue of *Electronics* magazine in 1965 [4]. After only six years since the introduction of the first commercial planar transistor in 1959, Moore observed an astounding trend: the number of components per chip was "roughly" doubling every year, reaching about 64 components in 1965 (Fig. 1). Extrapolating this trend for a decade, Moore predicted that chips with 65 000 components would be available by 1975. This observation of exponential growth in circuit density has proven to be one of the greatest examples of prescience (or least trend spotting) in modern times.

Some important details of Moore's remarkable 1965 paper have become lost in the lore of Moore's Law. First, Moore described the number of components per IC, which included resistors and capacitors, not just transistors. Later, as the digital age reduced the predominance of analog circuitry, transistor count became a more useful measure of IC complexity. Further, Moore clearly defined the meaning of the "number of components per chip" as the number which minimized the cost of a given circuit (equivalent to minimizing the cost per component of the circuit). This "minimum cost per component" concept is in fact the foundation of the economics of Moore's Law. Note that this curve in Fig. 1 represents the

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maximum economically viable complexity of an IC, since less complex chips are frequently commercially viable as well.

In 1975, Moore revisited his 1965 prediction and provided some critical insights into the technological drivers of the observed trends [5]. Checking the progress of component growth, the most advanced memory chip in the works at Intel in 1975 (a charge-coupled device (CCD) memory that in fact was never commercialized) had about 32 000 components (but only 16 000 transistors). Thus, Moore's extrapolation by three orders of magnitude was off by only a factor of 2. Even more importantly, Moore divided the advances in circuit complexity among its three principle technical drivers: increasing chip area, decreasing feature size, and improved device and circuit designs. Minimum feature sizes were decreasing by about 10% per year (resulting in transistors that were about 21% smaller in area, and an increase in transistors per area of 25% each year). Chip area was increasing by about 20% each year. These two factors alone resulted in a 50% increase in the number of transistors per chip each year. Design cleverness (eliminating nonfunctional chip area) made up the rest of the improvement (33%). In other words, the 2X improvement = (1.25)(1.20)(1.33).

Again, there are important details in Moore's second observation that are often lost in the retelling of Moore's Law. How is "minimum feature size" defined? Moore explained that his density-representing feature size was an average of the minimum line-width and the minimum space-width found on the chip. Today, we use a roughly equivalent metric, the minimum pitch divided by 2 (called the minimum half-pitch).

By breaking the density improvement into its three technology drivers, Moore was able to extrapolate each trend into the future and predict a change in the slope of his observation. Moore saw the progress in lithography allowing continued feature size shrinks to "one micrometer or less." Continued reductions in defect density and increases in wafer size would allow the die area trend to continue. But in looking at "device and circuit cleverness," Moore saw a limit. Although improvements in device isolation and the development of the metal-oxide-semiconductor transistor had contributed to greater packing density, Moore saw the latest circuits as approaching their design limits. Seeing an end to the design cleverness trend in four or five years, Moore predicted a change in the slope of his trend from doubling every year, to doubling every two years.

Moore's prediction of a slowdown was both too pessimistic and too generous. The slowdown from doubling each year had already begun by 1975–Intel's 16 kb CCD memory chip was never commercialized due to its sensitivity to radiation. The 64 kb dynamic random access memory (DRAM) chip, which should have been introduced in 1976 according to the original trend, was not available commercially until 1979 [6].

However, Moore's prediction of a slowdown to doubling components every two years instead of every year was too pessimistic. The 50% improvement in circuit density each year due to feature size and die size was really closer to 60% (according to Moore's 1995 retelling of the story [7]), resulting in a doubling of transistor counts per chip every 18 mo or so. Offsetting the curve to switch from component counts to transistor counts and beginning with the 64 kb DRAM in 1979, the industry followed the "new" Moore's Law trend throughout the 1980s and early-1990s. Although Moore never predicted an 18 mo doubling time for chip complexity, actual DRAM density trends closely followed this slope and industry "common knowledge" soon claimed the 18-mo doubling time as the accepted meaning of Moore's Law.

By the late-1970s, another interesting trend emerged: the bifurcation of Moore's Law into memory and logic trend lines. While memory chips continued to advance at the Moore's Law "complexity limit," logic chips (such as microprocessors) advanced at a slower pace [8]. In essence, the ability to put more transistors on a chip outstripped the ability to design chips with that many transistors for a market need. This split of Moore's Law in two persisted for the next two decades, where by the year 2000 memory chips used 1 billion transistors, but advanced microprocessors had only 20–40 million transistors. While memory chips increased their transistors per chip by 1.58X per year, microprocessors saw only a 1.38X per year increase [9].

Over the years, predictions of future industry performance reached such a level of acceptance that they have been codified in industry-sanctioned "roadmaps" of the future. The National Technology Roadmap for Semiconductors (NTRS) was first developed by the Semiconductor Industry Association (SIA) in 1994 to serve as an industry standard Moore's Law [10]. It extrapolated then-current trends to the year 2010, where 70 nm minimum feature sizes were predicted to enable 64 Gb DRAM chip production. This official industry roadmap has been updated many times, going international in 1999 to become the International Technology Roadmap for Semiconductors (ITRS). These roadmaps described the lockstep industry progression along technology "nodes," provided common terminology to suppliers and customers of the semiconductor industry, and attempted to describe the major challenges to continued progress along Moore's Law.

Throughout the 1980s and early 1990s, DRAM manufacturing was used a bellwether for industry innovation. The industry even named its technology nodes based on the equivalent DRAM generation, e.g., the 16 Mb node of 1992. But over the last ten years, DRAM size has not kept pace with historical trends (we are nowhere near producing the 64 Gb DRAM that the original NTRS predicted for 2010). It seems that 1–2 Gb is about the most bits needed in a DRAM chip for high volume products. That does not mean that DRAM production has stopped advancing. These 1 Gb DRAM chips continue to get better, smaller, and cheaper. But the packing of more bits onto a single chip has now moved to the realm of Flash memory, where 64 Gb Flash chips are entering production (right on schedule).

Thus, as the growth of overall DRAM size slowed, the roadmaps simply labeled the nodes by their lithographic feature size (the 130 nm node, e.g., going into mass production in 2001). This subtle change, however, offered an important insight; the greatest value of Moore's Law came from improved circuit density and transistor performance, not increased functions per chip. Moore's Law was no longer about scaling up, it was about scaling down. It was the shrinking transistor that

created the compelling economic advantages of Moore's Law. While Flash memory can still use every transistor that can be made (as long as they are cheap enough), essentially all other chips do not need anywhere near the maximum number of transistors that can be economically fabricated.

An alternate way of explaining this change in Moore's Law was a change in importance from transistors per chip to transistors per unit area of silicon. This can be seen in the industry trend for chip size, one of Moore's original three technology drivers for Moore's Law. Through the 1970s, chip area grew by about 20% per year, but by the mid-1990s it had slowed closer to 10% per year. But by the end of the 1990s, chip area had leveled off. Today, it is rare to find a chip bigger than about $2\,\mathrm{cm}^2$, the same as ten years ago. By contrast, the 1997 SIA roadmap predicted a DRAM chip size of greater than $11\,\mathrm{cm}^2$ in 2009. Without increasing chip size as a driver for complexity increase, one would expect another change in the Moore's Law slope. Instead, feature size reduction accelerated, allowing the Moore's Law slope to stay roughly on track.

III. Why Does Moore's Law Work?

Through a period of 50 years, the miraculous-seeming exponential growth of Moore's Law has continued, though with several bumps and turns along the way. This unprecedented technological evolution begs for an explanation. Some have argued that industry momentum simply pushes semiconductor technology forward. Others describe semiconductor technology development as "fashionable" engineering, attracting the brightest minds. Most people regard Moore's Law as a self-fulfilling prophecy [11]. We all understand the economic benefits of continuing down the roadmap, and the economic consequences of falling behind our competitors. We make Moore's Law happen because we want it to be true.

Ultimately, the drivers for technology development fall into two categories: push and pull. Push drivers are technology enablers, those things that make it possible to achieve the technical improvements. Moore described the three push drivers as increasing chip area, decreasing feature size, and design cleverness. Pull drivers are the economic drivers, those things that make it worth while to pursue the technical innovations. Although, as we shall see, the two drivers are not independent, it is the economic drivers that always dominate. As R. Noyce, co-inventor of the IC and co-founder of Intel, wrote in 1977, "...further miniaturization is less likely to be limited by the laws of physics than by the laws of economics" [12].

The economic drivers for Moore's Law have been extraordinarily compelling. As the dimensions of a transistor shrank, the transistor became smaller, lighter, faster, consumed less power, and in most cases was more reliable. All of these factors make the transistor more desirable for virtually every possible application. But there is more. Historically, the semiconductor industry has been able to manufacture silicon devices at an essentially constant cost per area of processed silicon. Thus, as the devices shrank they enjoyed a shrinking cost per transistor. As many have observed, it has often been a life without tradeoffs (unless, of course, you consider the stress on the engineers trying to make all of this happen year after year). Each step along the roadmap of Moore's Law virtually guaranteed economic success.

It is interesting to note that the most compelling benefits of Moore's Law, a better transistor at a lower cost, does not fundamentally rely on increasing the number of transistors per chip. Certainly, the increased memory capacity and/or functional abilities of more complex chips enable new applications that increase the demand for chips. But this high-end driver does not account for the majority of chips produced. The ability to produce moderate functionality at incredibly low prices enables new mass markets (like the microprocessor running Linux in my microwave oven, or that fact that my dishwasher has more compute power than existed in the world in 1950). For these applications, increased functions per chip are not important. Increased circuit density at near-constant cost per unit area is an enabler for all applications.

Unfortunately, the "no tradeoff" life of the shrinking transistor is over. The always faster and lower power transistor relied on voltages scaling with feature size. But since thermal voltage fluctuations (noise) do not scale, voltage scaling ran into this noise limit in the early part of the previous decade. Without the ability to scale voltage lower, shrinking the transistor might make it lower power or faster, but not both, and often neither. Just to keep the transistor from getting worse as it shrinks requires novel materials and designs (e.g., metal gates and high-k dielectrics). Chip speed (clock frequency) has reached a limit, and increasing chip power consumption has became a major limitation to further increases in chip complexity and density. It seems that the cost benefit of Moore's Law, reducing the cost per function by cramming more components into a fixed-cost area of silicon, is about the only benefit of shrinking left.

But while the economic drivers for Moore's Law explain why Moore's Law exists, they do not explain how. One possible explanation comes from learning curve theory [2], [3]. The basic tenet of learning curve theory is that a consistent improvement in the performance of some task is possible through increasing practice. To be specific, the "learning curve" expresses a constant percent improvement in some performance metric each time the cumulative number of trials, or practice attempts, is doubled. By plotting the performance metric of interest as a function of the cumulative output of a person, factory, or industry, learning curve theory predicts a straight line on a loglog scale.

How can learning curves be applied to the semiconductor industry? The logical metrics of interest are memory size (first DRAM, then Flash) and the transistor's representative feature size (such as minimum half-pitch). But what is the measure of "practice," the cumulative output of the industry? One obvious output measure is cumulative area of silicon produced by the industry [2], [3], but cumulative industry revenue is also appropriate. Since the manufacturing cost of a square centimeter of finished silicon chip has remained roughly constant throughout the history of the industry, cumulative silicon area produced and cumulative industry revenue are roughly proportional. Fig. 2 shows the result, using industry roadmaps for both the historical and projected feature size data, and SIA data for industry revenue [13].

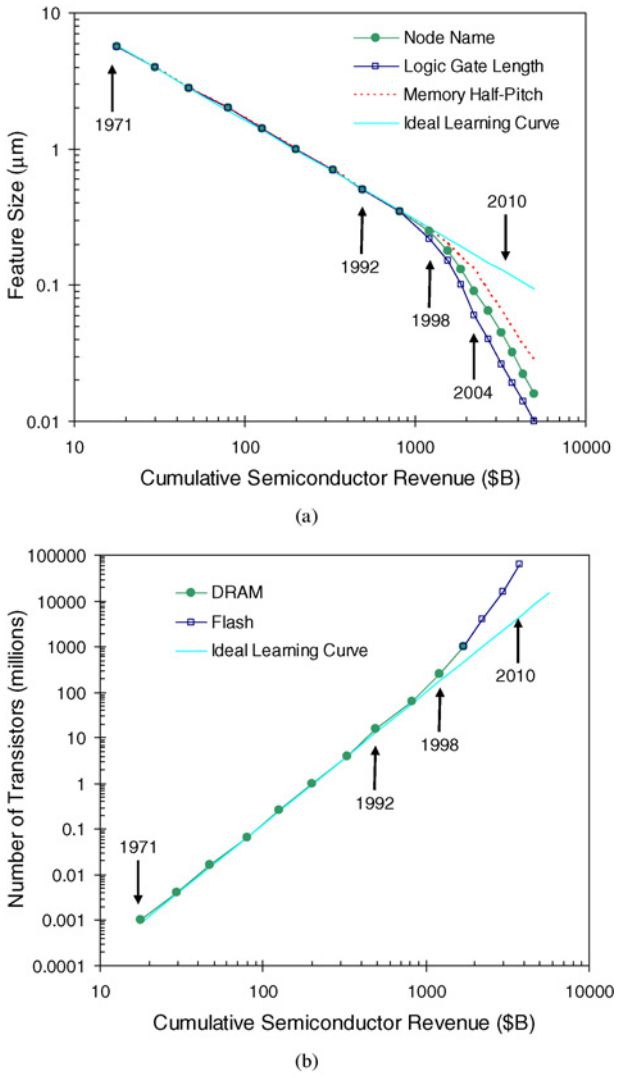

Fig. 2. Expressing Moore's Law as a learning curve. (a) Minimum feature size. (b) DRAM and Flash product introductions. Projections for 2009 and beyond assume 5% revenue growth and ITRS projections.

Looking at the historical trend shown in Fig. 2, there is a roughly linear progression (on the log-log scale, of course) of minimum feature size and memory size as a function of cumulative industry revenue until about 10 years ago. In the 1998–2000 time frame, accelerated shrinking of feature size, to make up for the loss of chip area increases, caused a marked deviation from the linear learning curve trend. But memory size also accelerated relative to the learning curve trend. It seems that the industry has broken free from the learning curve "constraint" and beaten the pace of development that our accumulating revenues could justify. This is quite a remarkable achievement for semiconductor manufacturers.

An explanation of sorts comes from looking at the trends in semiconductor revenue (Fig. 3). Until about 1997, semiconductor revenue grew at a compound annual growth rate (CAGR) of 16.2% since 1960. Since 1997, the CAGR has been 4.9%. To help appreciate the dramatic difference between these revenue growth rates, if the 16.2% growth rate had continued through 2008, the industry revenue that year would have been three times larger than it actually was. The

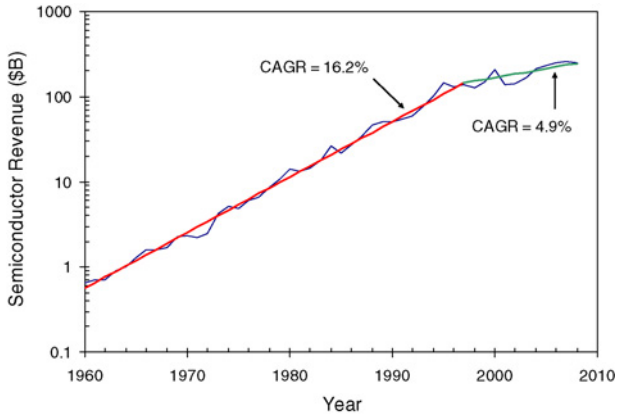

Fig. 3. Semiconductor revenue [12] and a piecewise continuous exponential growth model with a break set in 1997.

incredibly high rate of growth for the industry for 40 years fueled the investments needed to develop improved design and manufacturing technology and to stay on Moore's Law. But as the growth rate of the industry fell by a factor of three, investments in technology development have tried to keep pace with prior spending trends, enabling the continuation of the historical Moore's Law slope. Over the last decade, research and development spending has grown at twice the rate of chip revenues. But is this research and development spending sustainable? According to recent studies [14], [15], there is a growing research and development funding gap for semiconductor manufacturing technology, a gap that will only widen if revenue growth remains near 5%.

IV. Coupling Technology to Economics

The discussion above emphasizes the important role of economics in Moore's Law. But surely continuation of the IC evolution to allow smaller and smaller features is dependent on technology development, not just economics? Of course. There is a critical technology/economy cycle that rolls down the slope of Moore's Law. A technological development that enables the cost-effective manufacture of smaller transistors allows the manufacturer to offer a new, desirable product to the market place (faster, smaller, cheaper). This new capability (either due to an increase in performance or a decrease in cost, or both) creates a new market for the product, which increases the volume of sales. Higher sales volumes allow a percentage of those sales to be reinvested in the development of the next technology evolution (the cause and effect relationship of an industry learning curve). Even though each technology generation requires an increasing investment for development, the higher sales volume driven by the newly enabled markets justifies the investment. Technology development feeds economic growth which allows investment in further technology development.

But, as G. Moore himself has said many times, no exponential is forever. There are both economic limits and technology limits (no amount of money can be used to overcome the laws of physics). The economic limits are defined by the growing demand for more silicon. If demand growth slows, so

will Moore's Law. On the technology side, increasingly costly manufacturing processes required by the smaller transistors may cause an increase in the historical manufacturing cost per area of silicon. Higher cost per function limits the potential for growth of new markets, which lowers the growth of cumulative silicon area and revenue, which slows the learning.

Each generation of process technology developed to enable one more node on the ITRS roadmap requires a host of new and expensive equipment and materials. In what has sometimes been called Moore's second law, the cost of new fabrication facilities has risen exponentially over time. And yet the economic driver of Moore's Law requires significant reductions in the cost per transistor over time. In fact, the amazing economic reality of the semiconductor industry is that the cost of producing one square centimeter of finished silicon has remained approximately constant (or has risen only slowly) throughout the entire history of the semiconductor industry. How has this been accomplished?

There have been three main avenues to control manufacturing costs per area of silicon in the presence of dramatically rising equipment and material costs: increasing wafer sizes, increasing yields, and improved equipment effectiveness. From the one inch wafers used 40 years ago to the 300 mm (12 inch) wafers popular today, the increase in wafer size takes advantage of the fact that some processing costs are essentially per wafer rather than per unit area. Thus, an increase in wafer size can actually reduce the processing costs per unit area of silicon. As the slow transition of the industry to 300 mm wafers has shown, however, there is no guarantee that larger wafers will be more cost effective and significant development effort is required to provide improved process quality over larger wafer sizes at reduced cost per unit area. Further, each increase in wafer size requires a commensurate increase in total shipped silicon area (and thus revenue): volume drives the need for larger wafers. It is unlikely that wafers larger than 300 mm will prove cost effective, despite fitful industry efforts at developing a 450 mm wafer processing capability.

The second method for improving device costs is to improve the yield of the devices. In essence, it costs about the same to build a non-working device as it does to build a working device. Thus, all other things being equal, a process with 50% yield will have twice the cost per finished, saleable device than a process with 100% yield. In the 1970s, yields of 20–40% for leading edge products were not uncommon. By the 1980s, 50–70% yields were the norm. By the 1990s, chip makers came to expect 80–90% yields during volume production. While this trend has resulted in considerable cost improvements for the industry, there is little upside left with respect to yield. The emphasis today is on increasing the ramp to high yield, i.e., decreasing the time from first silicon to 90%+ yield so that the average fab throughput of good devices is nearer its theoretical maximum.

Overall equipment effectiveness is the final, and possibly most significant, enabler for low cost semiconductor manufacturing. By far the most important component of equipment effectiveness is throughput. Taking lithography exposure tools as an example, a stepper in 1980 costs $500 K, while a scanner today may run over $30 M. However, that 1980 stepper had a maximum throughput of 40 four-inch wafers per hour (actual throughputs were usually much less), while today's scanner is capable of processing more than 150 300-mm wafers in an hour—a greater than 33X increase of silicon area throughput. The result is a roughly constant equipment cost per square centimeter of processed silicon. Note, however, that using this much higher equipment productivity requires a need for producing large amounts of chips. Productivity improvements are volume driven. Thus, in the face of growing process complexity, there have been three historical enablers of nearly constant manufacturing cost per unit area of silicon: growing wafer size, increasing yield, and improved manufacturing productivity through improved equipment effectiveness (throughput). Of these three, only improved equipment productivity remains today as a significant factor.

V. Conclusion: The Limits of Moore's Law

Moore's Law is a direct consequence of the incredible and unique scaling heuristics of semiconductor manufacturing: by holding the cost per unit area of manufacturing constant, increasing transistor density gives lower cost per function. But smaller transistors are more difficult to make, and that means manufacturing at a constant cost per unit area is a result of a concerted engineering effort to make it so. Moore's Law is not a law, it is an act of will. Considerable effort is devoted to its continuation because there is a strong economic incentive to do so.

The economic benefits of Moore's Law come from the shrinking of the transistor. That is why Moore's Law has drifted from its historical origins as describing the number of transistors per chip to the more important metric of minimum lithographic feature size. While the popular press has failed to notice this shift, in the semiconductor industry there is no doubt today that the technology nodes of Moore's Law are governed by the historical 0.7X shrink in minimum feature size per generation.

It is my opinion that Moore's Law is an example of an industry-wide learning curve. There is a constant fractional improvement in technical capability (e.g., as judged by the minimum feature size) for every constant fractional increase in cumulative investment of effort. Since investment effort is generally proportional to output, Moore's Law can be formulated as a learning curve by plotting minimum feature size as a function of cumulative revenue or area of silicon produced by the industry on a log-log scale. As presented here, Moore's Law has kept on a relatively constant learning curve until about 1998–2000. The acceleration of this Moore's learning curve over the last decade is likely an unsustainable, momentum-driven attempt to recapture past revenue growth rates.

The economics drivers of Moore's Law can be divided into push drivers and pull drivers. Push drivers are the technology innovations that enable low cost manufacturing of smaller transistors. Pull drivers are the new applications that these smaller, faster, cheaper, or more powerful devices enable. As the discussion of Moore's Law as a learning curve should indicate, the importance of pull drivers is in the creation of

increasing demand and thus increasing volume of silicon area and revenue. These two drivers, push and pull, are inexorably linked due to the relationship between capability and cost for the technology push, and the relationship between cost and demand for the volume pull. Any reduction in the force of the push or the pull drivers will result in a slowdown in Moore's Law.

It appears that the semiconductor industry and Moore's Law are in the midst of a perfect storm. Semiconductors as a percentage of electronic devices are probably near or at saturation, so that semiconductor growth is now limited by overall electronics growth. A decade of lower industry revenue growth makes funding chipmaking research and development at the level required by the historic Moore's Law pace unlikely. The end of chip voltage scaling means that smaller transistors are no longer better transistors—the only reason for shrinking them is to make them cheaper. And the near-term evolution of manufacturing technology, especially lithography, does not look good for keeping manufacturing costs low as device dimensions shrink. Innovations in semiconductor manufacturing will surely continue, but the traditional scaling of feature size is reaching its limits. The industry, and the world, has enjoyed 50 remarkable years of Moore's Law. There are unlikely to be many more years left.

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